3D-integration for machine learning accelerators

master thesis / research project

Reserach field

The everlasting demand for higher computing power for neural networks (NNs) drives the development of parallel computing architectures. Monolithic 3D integration, in which chips are integrated and connected vertically, can further increase performance because it introduces another level of spatial parallelism.

Research topic

In this work, the possibilities for monolithic 3D integration for DNN accelerators will be evaluated. In a preliminary work, we showed that 3D integration allows for up to magnitude of performance increase. Monolithic 3D integration allows to add different partition schemes for computation and memories. These are evaluated here. An analog work was done for CPUs by Gopireddy and Torrellas in 2019 *"Designing Vertical Processors in Monolithic 3D"* (see QR). Please read this reference to get a flavor for this work.

Work topics

- Monolithic 3D integration of compute cores.
- Evaluation of partition schemes for on-chip memory.
- Implement testbenches, evaluation etc.
- Evaluate power, performance, area.

Required skills

- Python, C++, VHDL.
- Interest in synthesis for standard cell libs.

Contact

Jan Moritz Joseph
jan.joseph@ovgu.de
G09 R427
Date: February 13, 2020