File: c:\My_Designs\design4\design4\src\TestBench.v

```
1   `timescale 1 ns / 10 ps
2
3   module TestBench;
4
5       reg clk, reset, d;
6       wire q;
7
8       parity UUT(clk, reset, d, q);
9
10      // Initial conditions for clk, reset, and d
11      initial
12          begin
13              clk = 1; reset = 0; d = 0;
14          end
15
16      always #5 clk = ~clk;
17
18      // Computational tests of the dff
19      initial
20          begin
21              #2 reset = 1;
22              #10 reset = 0; d = 1;
23              #10 d = 0;
24              #20 d = 1;
25              #20 d = 0;
26              #10 d = 1;
27              #10 d = 0;
28              #10 d = 1;
29              #30 d = 0;
30          end
31
32      // Monitor the console and save simulation data
33      initial
34          begin
35              $dumpfile("dff.vcd");
36              $dumpvars(1, clk, reset, d, q);
37              $dumpflush;
38          end
39
40      // Set test to finish after 80ms
41      initial
42          #142 $finish;
43
44  endmodule
```