File: c:\My_Designs\Design2\Design2\src\adder.v

```
1   // Jonathan Monreal
2
3   // Implements a complete adder
4   module adder(a, b, ci, s, co);
5
6       input a, b, ci;
7       output s, co;
8       wire aORb, aANDb_, aANDb, d1, d2;
9
10      OAO U1(ci, a, b, a, aORb, aANDb_, co);   // Finds the carry out
11      OAO U2(co_, aORb, ci, aANDb, d1, d2, s); // Finds the sum
12      not U3(co_, co);       // Inverts the carry out for use in U2
13      not U4(aANDb, aANDb_); // Inverts aANDb_ for use in U2
14
15  endmodule
16
17  // Implements an or-and-or arrangement
18  module OAO(d, e, f, g, y1, y3_, y4);
19
20      input d, e, f, g;
21      output y1, y3_, y4;
22      wire e_, f_, y2_;
23
24      not u5(e_, e);
25      not u6(f_, f);
26      nand u1(y1, e_, f_);
27      nand u2(y2_, d, y1);
28      nand u3(y3_, f, g);
29      nand u4(y4, y2_, y3_);
30
31  endmodule
```