File: c:\My_Designs\design3\design3\src\TestBench.v

```
1   `timescale 1 ns / 10 ps
2
3   module TestBench;
4
5       reg [3:0] A, B;
6       reg [1:0] S;
7       wire [3:0] F;
8
9       alu4 UUT(A, B, S, F);
10
11      // Initial conditions for A, B, and S
12      initial
13          begin
14              A = 4; B = 1; S[1] = 1; S[0] = 0;
15          end
16
17      // Computational tests of the ALU
18      initial
19          begin
20              #10 A = 7; B = -8;
21              #10 A = -1; B = 5; S[0] = 1;
22              #10 A = 3; B = 2;
23              #10 A = 'b1111; B = 'b0101; S[1] = 0; S[0] = 0;
24              #10 A = 'b1010; B = 'b0000;
25              #10 A = 'b1111; B = 'b0101; S[0] = 1;
26              #10 A = 'b1010; B = 'b1111;
27          end
28
29      // Display the truth table
30      initial
31          begin
32              $display("                TIME | A | B | S0 | S1 | F");
33              $monitor($time, "    %d  %d    %b    %b  %d", A, B, S[0], S[1
    ], F);
34          end
35
36      // Monitor the console and saves simulation data
37      initial
38          begin
39              $dumpfile("alu.vcd");
40              $dumpvars(1, A, B, S, F);
41              $dumpflush;
42          end
43
44      // Set test to finish after 80ms
45      initial
46          #80 $finish;
47
48  endmodule
```