File: c:\My_Designs\Design1\Design1\src\TestBench.v

```
1   // Jonathan Monreal
2
3   module TestBench;
4
5       reg a, b;        // Two registers for inputs
6       wire y1, y2, y3; // Three wires for outputs for and, or, and xor
    gates
7
8       partD UUT(a, b, y1, y2, y3); // The current unit under test
9
10      // Initial conditions for a and b
11      initial
12          begin
13              a = 0; b = 0;
14          end
15
16      // Changes values of a and/or b every 10ms
17      always
18          begin
19              #10 b = 1;
20              #10 a = 1; b = 0;
21              #10 b = 1;
22          end
23
24      // Displays values of a and b
25      initial
26          begin
27              $display("                TIME | a | b | y1 | y2 | y3");
28              $monitor($time, "    %b   %b   %b    %b    %b", a, b, y1, y2
    , y3);
29          end
30
31      // Sets test to finish after 40ms
32      initial
33          #40 $finish;
34
35  endmodule
36
```