File: c:\My_Designs\design3\design3\src\alu.v

```
1   module alu(A, B, CI, S0, S1, F, CO);
2
3       input A, B, CI, S0, S1;
4       output F, CO;
5
6       adder U1(A, B ^ S0, CI & S1, F, CO);
7
8   endmodule
9
10  module alu4(A, B, S, F);
11
12      input [3:0] A, B;
13      input [1:0] S;
14      output [3:0] F;
15      wire CO0, CO1, CO2, CO3;
16
17      alu B0(A[0], B[0], S[0], S[0], S[1], F[0], CO0);
18      alu B1(A[1], B[1], CO0, S[0], S[1], F[1], CO1);
19      alu B2(A[2], B[2], CO1, S[0], S[1], F[2], CO2);
20      alu B3(A[3], B[3], CO2, S[0], S[1], F[3], CO3);
21
22  endmodule
```