File: c:\My_Designs\design3\design3\src\cpu.v

```
1   module cpu4(clk, reset, s, b, a);
2
3       input clk, reset;
4       input [3:0] b;
5       input [1:0] s;
6       output [3:0] a;
7       wire [3:0] f;
8
9       alu4 U1(a, b, s, f);
10      dff4 U2(clk, reset, f, a);
11
12  endmodule
```