File: c:\My_Designs\design3\design3\src\TestBench.v

```
1   `timescale 1 ns / 10 ps
2
3   module TestBench;
4
5       reg clk, reset;
6       reg [1:0] s;
7       reg [3:0] b;
8       wire [3:0] a;
9
10      cpu4 UUT(clk, reset, s, b, a);
11
12      // Initial conditions for clk, reset, b, and s
13      initial
14          begin
15              clk = 1; reset = 0; b = 'h0; s = 'h0;
16          end
17
18      always #5 clk = ~clk;
19
20      // Computational tests of the cpu
21      initial
22          begin
23              #2 reset = 1;
24              #10 reset = 0; s = 'h2; b = 'h1;
25              #100 s = 'h3; b = 'h3;
26              #40 s = 'h1; b = 'hE;
27          end
28
29          // Monitor the console and save simulation data
30      initial
31          begin
32              $dumpfile("cpu.vcd");
33              $dumpvars(1, clk, reset, b, s, a);
34              $dumpflush;
35          end
36
37      // Set test to finish after 80ms
38      initial
39          #170 $finish;
40
41  endmodule
```