File: c:\My_Designs\Design2\Design2\src\TestBench.v *

```
1   `timescale 1 ns / 10 ps
2
3   module testbench();
4       reg a, b, ci; // Three registers for inputs
5       wire s, co;   // Three wires for outputs for and, or, and xor gates
6
7       adder UUT(a, b, ci, s, co);
8
9       // Initial conditions for a, b, and ci
10      initial
11          begin
12              a = 0; b = 0; ci = 0;
13          end
14
15      // Change values of a, b, and ci at appropriate intervals
16      always #40 a = ~a;
17      always #20 b = ~b;
18      always #10 ci = ~ci;
19
20      // Display the truth table
21      initial
22          begin
23              $display("                  TIME | a | b | ci | s | co");
24              $monitor($time, "    %b   %b   %b    %b   %b", a, b, ci, s,
    co);
25          end
26
27      // Monitor the console and saves simulation data
28      initial
29          begin
30              $dumpfile("adder.vcd");
31              $dumpvars(1, a, b, ci, s, co);
32              $dumpflush;
33          end
34
35      // Set test to finish after 80ms
36      initial
37          #80 $finish;
38
39  endmodule
```