File: c:\My_Designs\Design2\Design2\src\adder.v (/UUT)

```
1   `timescale 1 ns / 10 ps
2
3   // Jonathan Monreal
4
5   // Implements a complete adder
6   module adder(a, b, ci, s, co);
7
8       input a, b, ci;
9       output s, co;
10      wire aORb, aANDb_, aANDb, d1, d2;
11
12      OAO U1(ci, a, b, a, aORb, aANDb_, co);   // Finds the carry out
13      OAO U2(co_, aORb, ci, aANDb, d1, d2, s); // Finds the sum
14      not #0.5 U3(co_, co);       // Inverts the carry out for use in U2
15      not #0.5 U4(aANDb, aANDb_); // Inverts aANDb_ for use in U2
16
17  endmodule
18
19  // Implements an or-and-or arrangement
20  module OAO(d, e, f, g, y1, y3_, y4);
21
22      input d, e, f, g;
23      output y1, y3_, y4;
24      wire e_, f_, y2_;
25
26      not #0.5 u5(e_, e);
27      not #0.5 u6(f_, f);
28      nand #1 u1(y1, e_, f_);
29      nand #1 u2(y2_, d, y1);
30      nand #1 u3(y3_, f, g);
31      nand #1 u4(y4, y2_, y3_);
32
33  endmodule
```