Project Nautilus — Power Testbed MVP Spec
(Generator-Mode Evaluation Platform)

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February 1, 2026

Abstract

This document defines the engineering specification for the **Nautilus Power Testbed MVP**, a remote-operated, fully instrumented platform designed to validate generator-mode operation of rotating-field devices. Unlike ad-hoc experiments, this testbed is designed as a *metrology instrument* first and a power source second. It enforces strict energy accounting, automatic null-hypothesis testing, and layered safety protocols to produce auditable, uncertainty-bounded evidence of non-trivial energy gain. The specification targets a **10 kW continuous / 25 kW peak** envelope at up to **600 VDC**, optimizing for high-Q resonant operation, rapid iteration, and undeniable signal-to-noise ratios.

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1　Introduction and Strategic Intent

Project Nautilus aims to transition Recognition Science (RS) from theoretical physics to engineered reality. The critical path to this transition lies in demonstrating *Metric Engineering*—specifically, the ability to extract energy from the vacuum by ordering it via a resonant rotating field (the "Vacuum Pump" hypothesis).

Historical attempts (Searl, Podkletnov) relied on spinning physical matter (magnets, superconductors), which introduces vibration, thermal noise, and material defects that destroy the phase coherence required for the effect. To maximize the probability of success, Nautilus explicitly favors a **Solid-State Virtual Rotor (SSVR)** architecture. By replacing moving parts with precise, computer-controlled electromagnetic fields, we maximize coherence, tunability, and safety.

To avoid the trap of ambiguous results, the Nautilus Power Testbed is designed not merely to "make power," but to **manufacture credible evidence**.

The strategic intent of this MVP is to build a single, golden-standard test cell that can:

1. **Safely Drive** solid-state virtual rotors to their resonant limits.

2. **Rigorously Measure** energy balance with a closed accounting loop.

3. **Automatically Reject** artifacts via pre-registered null tests.

4. **Scale** the technology from milliwatt curiosities to kilowatt industrial relevance.

2　MVP Deliverable: The "Precision 10kW" Standard

The MVP is defined as a single, integrated rack system and test cell. The choice of a **10 kW continuous / 25 kW peak** envelope is deliberate and strategic.

2.1　Primary DUT: The Solid-State Virtual Rotor (SSVR)

The reference Device Under Test (DUT) is not a mechanical rotor, but a **multi-layer PCB stack** (approx. 200–300mm diameter) containing precise ϕ-spiral coil geometries.

- **Why Solid State?** Matter is noisy; fields are clean. A virtual rotor has zero friction, zero vibration, and can "spin" at relativistic speeds simply by changing the commutation frequency.

- **Why PCB?** Lithographic etching allows for micron-level geometric precision that machining cannot match.

- **Why Tunable?** A software-defined rotor allows sweeping millions of configuration parameters (pole count, speed, phase) in a single day to find the resonance, rather than machining a new rotor for every guess.

2.2　Why 10 kW?

- **Undeniable Signal**: At 10 kW, thermal drift, sensor noise, and RF interference are negligible errors relative to the signal. If the system consumes 8 kW and outputs 10 kW, the 2 kW delta is physically massive—it cannot be explained away as measurement error.

- **Iteration Speed**: Systems larger than 25 kW typically require liquid cooling, arc-flash suits, and dedicated substations. A 10 kW air-cooled system fits in a standard server rack, runs on standard lab power, and allows hardware iterations in days rather than months.

- **Safety Management**: While 10 kW is lethal if mishandled, the energy release during a catastrophic failure is containable within a standard blast enclosure, unlike megawatt-class systems.

2.3   System Capabilities

The delivered system will be capable of:

- Driving a solid-state phased array (SSVR) with arbitrary 8-tick commutation schedules.

- Extracting output power into a controlled load, regulating the "back-action" on the core.

- Measuring E_{in}, E_{out}, and ΔE with a real-time uncertainty budget.

- Failing safely (without destroying the prototype) upon loss-of-load or thermal runaway.

- Producing a cryptographically signed "Run Bundle" for every experiment, ensuring data provenance.

3   Requirements Matrix and Verification Plan

This section translates the MVP intent into **testable requirements**. Each requirement has a verification method: *Inspection* (I), *Analysis* (A), *Test* (T), or *Demonstration* (D).

3.1   MVP requirements (non-exhaustive, high-signal)

3.2   IP alignment (internal)

The above requirements map directly to the docket families: metrology and artifact rejection (NTL-PROV-010/011), provenance (NTL-PROV-012), generator pickup and load shaping (NTL-PROV-013/014), strict accounting (NTL-PROV-015), thermal diagnostics (NTL-PROV-016), detuning governor (NTL-PROV-017), and watchdog/dump-load safety (NTL-PROV-018).

4   Electrical Envelope and Architecture

The electrical architecture is optimized for high-Q resonant operation, which often favors higher voltages and lower currents to minimize $I^2 R$ losses in the drive coils.

4.1   Input Supply (Drive Side)

The input stage provides the energy to establish and maintain the rotating field.

- **Bus Architecture**: High-voltage DC bus (HVDC) with active precharge and contactor isolation.

- **Voltage Range**: **0–600 VDC**. Higher voltage reduces current for a given power level and improves efficiency in high-Q inductive loads.

- **Current Range**: envelope-dependent; design for **0–50 A** continuous at high bus voltages, with peak capability up to **200 A** at lower voltages for short bursts. Define a configurable hardware current limit I_{max} used by safety interlocks.

- **Driver Technology**: **GaN or SiC FETs** are preferred to achieve high switching frequency, tight phase control, and low timing jitter. The driver must support programmable dead-time and edge shaping to balance coherence, efficiency, and EMI.

- **Power Capacity**: 10 kW continuous, with a **25 kW peak** capability for transient pulses.

4.2 Output Path (Extraction Side)

The output stage is the critical interface for harvesting energy. It must handle the complex, potentially high-frequency AC waveforms induced in the pickup coils.

- **Topology**: Pickup → Rectification → DC Buffer → Load Interface.

- **Dump Load**: A dedicated, fast-switching resistive load bank rated for $\geq$ **25 kW**. This is crucial for safety: if the external load disconnects, the dump load must instantly absorb the energy to prevent voltage spikes.

- **Crowbar/Clamp**: A hardware-level voltage clamp (thyristor/IGBT) to short the bus if voltage exceeds safe limits, protecting the expensive drive electronics.

4.3 Grounding and EMI Strategy

Given the high-frequency pulsed nature of the drive, EMI management is paramount.

- **Star Ground**: A single central ground point to prevent ground loops.

- **Isolation**: All measurement front-ends (voltage probes, current shunts) must be galvanically isolated from the DAQ system.

- **Shielding**: All power cabling runs in shielded conduit; the DUT is housed in a Faraday cage.

5 Metrology and Instrumentation

The "product" of this testbed is data. Therefore, the instrumentation stack is non-negotiable.

5.1 Measurement Boundaries

To prevent ambiguity, we define explicit boundaries:

- **Input Boundary**: The terminals where DC power enters the driver inverter. We do not measure "at the wall" (which includes power supply inefficiencies), nor do we measure "at the coil" (which ignores driver losses). We measure the *total electrical energy invested* to create the field.

- **Output Boundary**: The terminals where DC power leaves the rectification stage to the load.

- **The Golden Rule**: Voltage and current must be measured **simultaneously** on the **same time base** for both input and output. Power is integrated sample-by-sample ($p(t) = v(t) \cdot i(t)$) to capture harmonic power flow correctly.

5.2 Data Acquisition (DAQ) Specs

- **Timebase**: A single master clock distributes synchronization pulses to all digitizers. Inter-channel alignment must be calibrated to better than **1 μs** (Tier-0 minimum); for high-frequency SSVR runs, target < 100 **ns**.

- **Sample Rate**: Minimum **100 kS/s** per channel (Tier-0 minimum). For SSVR operation where significant power-flow content exists above 10 kHz, ≥ 1 **MS/s** is recommended. The effective bandwidth must be justified by measured spectra and matched anti-alias filtering.

- **Sensors**:
  - **Current**: Precision coaxial shunts are preferred over Hall sensors for their bandwidth and lack of drift.
  - **Voltage**: High-voltage differential probes with documented frequency response.

5.3 Artifact Rejection Sensors

To prove that an effect is real, we must prove it is *not* an artifact.

- **Thermal**: Fast thermocouples on coils, switches, and bus bars. We compute dT/dt in real-time to detect thermal runaway.

- **EMI**: Near-field probes monitor radiated noise. If a "power anomaly" correlates perfectly with an EMI burst, the run is flagged as suspect.

- **Vibration**: An accelerometer on the DUT fixture ensures that mechanical resonance isn't mistaken for electrical effects (e.g., via microphonics).

6 Energy Accounting and Uncertainty (Data-Gated)

This MVP is designed so that any claim of "generator mode" is defined in terms of **measurable energy balance** with an explicit uncertainty bound. The testbed never assumes an effect exists; it computes an accounting result and then applies quality gates and matched controls to decide whether the result is credible.

6.1 Power and energy definitions

At the input and output boundaries (Section 5.1), define:

$$P_{\text{in}}(t) = V_{\text{in}}(t)\, I_{\text{in}}(t), \tag{1}$$

$$P_{\text{out}}(t) = V_{\text{out}}(t)\, I_{\text{out}}(t). \tag{2}$$

Energy over an accounting window $[t_1, t_2]$ is computed by integration:

$$E_{\text{in}} = \int_{t_1}^{t_2} P_{\text{in}}(t)\, dt, \tag{3}$$

$$E_{\text{out}} = \int_{t_1}^{t_2} P_{\text{out}}(t)\, dt. \tag{4}$$

Define the net energy balance:

$$\Delta E := E_{\text{out}} - E_{\text{in}}. \tag{5}$$

Stored energy correction (minimum viable). If the system includes appreciable stored energy (DC bus capacitance, inductors, buffers), the accounting window must include a correction term:

$$\Delta E_{\text{stored}} := E_{\text{stored}}(t_2) - E_{\text{stored}}(t_1), \tag{6}$$

so that the corrected balance is $\Delta E_{\text{corr}} = E_{\text{out}} - E_{\text{in}} - \Delta E_{\text{stored}}$. In MVP, ΔE_{stored} should be computed from measured bus voltages (and known capacitances) and included in the uncertainty budget.

6.2 Accounting windows (how we avoid self-deception)

The runbook defines accounting windows explicitly. Minimum recommended windows:

- **Baseline window**: device unpowered, sensors running (offset and drift characterization).

- **Ramp window**: drive ramp and load soft-connect ramp (excluded from main accounting unless explicitly modeled).

- **Steady window**: resonance lock held, load stable (primary accounting window).

- **Cooldown window**: post-run drift/offset check.

The report must state which window(s) were used for ΔE and why.

6.3 Uncertainty budget (required output)

Every reported ΔE must include an uncertainty estimate $u(\Delta E)$ and a list of contributing terms. The budget is not a formality: it is the mechanism that makes results defensible.

Reporting metric. The report should include a normalized score (illustrative):

$$z := \frac{\Delta E_{\text{corr}}}{u(\Delta E_{\text{corr}})}.$$

This is not a claim of statistical significance by itself; it is a compact way to track whether the observed balance is large relative to the known uncertainty.

6.4 Traceability to IP

This section is aligned with NTL-PROV-015 (strict accounting) and supports credibility claims for the entire power product line.

7 Commissioning and Calibration Procedures (MVP)

The MVP is only as credible as its calibration. Commissioning is therefore treated as a first-class deliverable: the testbed is not considered operational until calibration artifacts exist and pass acceptance criteria.

7.1 Commissioning sequence (high-level)

1. **Mechanical and wiring inspection**: torque checks, connector keying, labeling, strain relief, ground bonding.

2. **Interlock verification**: door/E-stop/coolant-flow/smoke/overtemp interlocks trip as designed.

3. **Precharge and contactor test**: verify controlled precharge ramp and safe discharge behavior.

4. **DAQ integrity test**: verify sampling, channel mapping, timestamp monotonicity, and storage throughput.

5. **Accounting calibration**: calibrate V/I channels, timing alignment, and compute an uncertainty budget.

6. **Fault injection tests**: intentionally trigger representative faults (loss-of-load, overvoltage) and record mitigation response.

7.2 Time alignment calibration (required)

Because real power uses $V(t)I(t)$, timing skew between voltage and current channels can create systematic bias. The MVP must implement and document a timing calibration that produces per-channel delay corrections.

Minimum viable procedure (illustrative):

1. Inject a reference waveform (edge-rich square wave or pulse train) that is simultaneously visible on all relevant channels.

2. Estimate relative delays via cross-correlation and/or edge timestamping.

3. Store delay corrections in `calibration.json` and apply them prior to computing $p(t)$.

4. Re-run the procedure at the start and end of a measurement day to bound drift.

7.3 Electrical sensor calibration (required)

- **Voltage**: calibrate differential probes/dividers against a traceable reference at multiple points (e.g., 50 V, 200 V, 400 V, 600 V). Record gain/offset and uncertainty.

- **Current**: calibrate shunts (or transducers) using a traceable current source or a calibrated shunt standard. Record gain/offset, temperature coefficient, and uncertainty.

- **Bandwidth/phase**: characterize the frequency response of the measurement chain sufficiently to justify the sampling and filtering choices used in accounting.

7.4 Thermal sensor calibration (minimum viable)

Thermal channels are used both for safety and for artifact rejection. At minimum:

- verify each sensor is physically attached and responds plausibly to controlled heating/cooling;

- record baseline noise and drift over a fixed interval;

- set conservative dT/dt thresholds for runaway detection and validate the trip path.

7.5 Accounting sanity check (required acceptance test)

Before any DUT experiment is considered meaningful, the platform must demonstrate that on a purely resistive dummy load and/or a simulated pickup source, the measured balance satisfies:

$$\Delta E_{\text{corr}} \approx 0 \quad \text{within} \quad u(\Delta E_{\text{corr}})$$

across repeated runs and across the primary operating envelope. This is the minimum credibility bar.

8 Control and Safety Architecture

The system is divided into two independent planes: the **Control Plane** (which tries to make the system work) and the **Safety Plane** (which tries to stop it from exploding).

8.1 Control Plane (Primary Controller)

This is the "brain" of the experiment. It runs the runbook.

- Generates the complex 8-tick commutation schedules.

- Performs frequency/phase sweeps to find resonance.

- Manages the "Soft Connect" load ramp, gradually increasing power extraction to stabilize the core without stalling it.

8.2 Safety Plane (Independent Watchdog)

This is the "nervous system"—a hardware-based watchdog that does not rely on the primary controller's software state.

- **Independence**: It has its own power supply, its own clock, and its own sensors.

- **Hard Thresholds**: It monitors for Bus Overvoltage, Overcurrent, Thermal Runaway ($dT/dt >$ limit), and the specific "Loss-of-Load" signature (Voltage $\uparrow$, Current $\downarrow$).

- **Mitigation Ladder**: Upon detecting a fault, it executes a prioritized sequence:

  1. **Detune**: Inject phase noise to kill the resonance (De-Q).
  2. **Dump**: Fire the dump load to drain the bus.
  3. **Clamp**: Fire the crowbar if voltage is still rising.
  4. **Kill**: Open the main contactors.

- **Latched State**: Once tripped, the system locks down until a human operator manually resets it.

8.2.1 Recommended safety thresholds (initial defaults)

The specific numerical thresholds are platform-dependent and must be tuned during commissioning; however, the MVP must include explicit defaults and test evidence that each threshold triggers the intended mitigation. Let $V_{\text{bus,max}}$ denote the configured maximum bus voltage for the selected envelope (e.g., 600 V for Precision 10kW, 200 V for Tier-0, 60 V for Tier-0 Lite).

8.2.2 Fault handling timing budget (guidance)

Where feasible, the highest-severity protections (overvoltage/overcurrent) should be implemented with *hardware-fast paths* (comparators and hardwired kill lines) so response does not depend on firmware scheduling under EMI.

- **Comparator trip to driver disable**: target < 10 μs.

- **Dump load engagement**: target < 100 μs from loss-of-load detect.

- **Crowbar clamp**: target < 100 μs after crowbar threshold.

- **Contactor open**: target < 50 ms (mechanical constraint) after hard fault.

8.2.3 Reset and recovery procedure (minimum viable)

1. Verify V_{bus} is below a safe threshold (e.g., < 50 V) and that precharge resistors have discharged the bus.

2. Verify temperatures are within safe limits and dT/dt is near baseline.

3. Capture and archive the fault run bundle (raw + derived + gate outcomes).

4. Perform a scripted interlock test (door/E-stop/coolant flow) and watchdog self-test.

5. Explicitly re-arm the watchdog, then re-enable contactors and proceed with a conservative bring-up run.

9 Software and Operations

9.1 Run Orchestration

Experiments are not run ad-hoc. They are defined as declarative **Run Plans** (JSON/YAML) that specify the geometry, schedule, load profile, and pass/fail criteria. The software engine executes these plans automatically.

9.2 Null Tests and Matched Controls

To ensure scientific rigor, the runbook engine automatically interleaves **Control Runs** with **Active Runs**. The MVP must support:

- **Detuned Control**: Running the exact same power profile but at an off-resonant frequency.

- **Load-Only Control**: Driving the load using a standard power supply (simulating the pickup) to characterize the extraction efficiency baseline.

- **Geometry-Neutral Control**: Running the drive electronics into a dummy load (no coil) to quantify switching losses.

9.3 Provenance and Auditability

Every single run produces a **Signed Run Bundle**. This is a zip archive containing the raw data, the config snapshot, the firmware hash, and a cryptographic signature. This ensures that data cannot be cherry-picked or modified after the fact. If the hash doesn't match the chosen anchor (e.g., internal notarization or a distributed ledger), the data is invalid.

10 Run Bundle and Deterministic Replay (Minimum Schema)

The MVP must treat every run as a first-class artifact: a bundle that can be re-analyzed, audited, and replayed. This section specifies the minimum bundle contents and the canonicalization rules required to prevent "configuration drift" from invalidating results.

10.1 Run bundle structure (required files)

At minimum, each run bundle contains:

- **manifest**: a machine-readable manifest (e.g., `manifest.json`) listing every file and its digest;

- **config snapshots**: `config.json`, `schedule.json`, `calibration.json`, `safety.json`;

- **raw streams**: synchronized binary or CSV logs for V/I accounting channels and auxiliary channels (thermal/EMI/vibration);

- **derived outputs**: computed $p(t)$, E_{in}, E_{out}, ΔE, $u(\Delta E)$, plots, and summaries;

- **gate outcomes**: pass/fail for every quality gate and matched-control label for the run;

- **signature**: a signature file and public key identifier (implementation-defined).

10.2 Canonical configuration snapshot (what must be captured)

The canonical snapshot must include enough information that another team can reproduce the *intent* and the *waveform realization*:

- DUT identifiers (device ID, revision, serials) and fixture identifiers;

- geometry ID and parameters relevant to the run;

- schedule ID and schedule parameters (intent layer);

- waveform realization parameters (dead-time, edge shaping, current limits, protections);

- clock/timing calibration (per-channel latency corrections, jitter bounds);

- sensor metadata (placement, sampling rate, filters, channel mapping);

- calibration constants and their uncertainties;

- safety envelope parameters (thresholds, stop criteria, governor settings);

- software identifiers (firmware hashes, analysis version hashes).

10.3 Integrity and signatures (minimum viable)

The bundle must include:

- a digest per file (e.g., SHA-256);

- a manifest digest;

- a signature over the manifest digest (e.g., Ed25519 or ECDSA).

Optional enhancements include Merkle trees for efficient partial disclosure and external timestamping/anchoring.

10.4   Example run plan (illustrative)

Below is a non-normative example of a minimal Run Plan structure:

```
{
  "run_id": "2026-02-01T12:34:56Z__A17",
  "dut": { "device_id": "DUT-001", "rev": "A", "serial": "0007" },
  "geometry_id": "GEO-PHI-SPIRAL-275MM-K1",
  "schedule_id": "SCHED-8TICK-V1",
  "drive": { "v_bus": 420, "limit_a": 40, "sweep_hz": [1000, 5000] },
  "load_profile": { "mode": "soft_connect", "target_kw": 5.0, "ramp_s": 10.0 },
  "controls": { "ab_label": "DETUNED_CONTROL", "random_seed": 1337 },
  "gates": { "clip": true, "time_align_us_max": 1.0, "dvdt_max": 50.0 }
}
```

10.5   Deterministic replay

Deterministic replay means: given the signed config snapshots (including timing calibration), a future run can re-execute the same schedule intent and achieve waveform realization within specified tolerances. Replays must produce their own signed run bundles and a diff report against the original.

11   Budgetary Cost Estimate (Prototype Validation Testbed)

This section provides an *order-of-magnitude* estimate to build a single prototype validation cell matching this specification. Costs vary widely based on (i) how much is purchased as COTS (commercial off-the-shelf) vs custom power electronics, (ii) the metrology rigor required ("nice" vs "audit-grade"), and (iii) facility constraints (test cell, ventilation, fire containment, EMI shielding).

11.1   What is included (and excluded)

Included: one test cell/rack, HV bus and protections, dump load/crowbar/contactor stack, DAQ + probes + sensors sufficient to satisfy the accounting requirements, primary control + watchdog hardware, runbook + signed run bundles, and commissioning/calibration labor.

Excluded by default: dedicated building upgrades (new service transformers/substation work), utility interconnect hardware for grid export, and large-scale manufacturing tooling. One or more DUT prototypes may be required for meaningful validation; those are estimated separately.

11.2   Cost drivers

- **Metrology stack**: high-end power analyzers / digitizers, isolated front ends, calibrated shunts/probes, and timing infrastructure.

- **Safety hardening**: fast protection hardware (crowbar/dump load switches), independent watchdog, interlock system, and containment enclosure.

- **Engineering labor**: integration, calibration, software (runbook + analysis + provenance), and test/commissioning.

11.3   Line-item estimate (prototype cell, one-off build)

11.4   DUT prototype allowance (separate)

The testbed is infrastructure. For an initial validation campaign, also budget:

- **SSVR Prototypes (PCB-based)**: $5k–$25k (PCB fabrication, high-copper heavy oz boards, assembly). This is significantly cheaper than machined mechanical rotors.

- **Fixturing**: $5k–$15k (non-conductive, thermal-managed mounting).

11.5   Practical budget bands (recommended)

- **COTS-heavy "credible" MVP**: $250k–$750k (fastest path; uses more commercial instruments).

- **Audit-grade credibility build**: $1M–$3M (more redundancy, calibrated standards, stronger containment).

- **Facility-grade / pre-product cell**: $5M+ (multiple cells, higher power, extensive shielding and operations).

11.6   Smaller-scale option (bench validation cell)

Yes: you can run an earlier validation campaign at materially smaller scale *without changing the scientific rules.* The key is to keep the same accounting discipline (boundaries, synchronized V/I, uncertainty budget, matched controls, signed run bundles) while reducing stored energy, fault energy, and facility demands.

Recommended bench envelope (Tier-0).

- **Power**: 0.5–2 kW continuous (5 kW peak bursts $\leq$ 2 s).

- **Bus voltage**: 0–200 VDC (simplifies safety and COTS sourcing).

- **Dump load**: 2–5 kW with fast switching.

- **Watchdog/crowbar**: still required, but sized for lower fault energy.

Ultra-lean bench envelope (Tier-0 Lite).   If your primary goal is "Searl-scale replication" and signature discovery (cooling, anomalous electrical pickup, self-acceleration signatures) rather than immediate 10 kW throughput, you can start even smaller *while preserving the metrology rules.*

- **Power**: 0.1–1 kW continuous (2 kW peak bursts $\leq$ 1 s).

- **Bus voltage**: 0–60 VDC (materially reduces shock/arc risk and COTS cost).

- **Dump load**: 1–2 kW fast-switched load (still required for loss-of-load regimes).

- **Watchdog**: still required (OV/OC/thermal/loss-of-load), but can be simpler due to lower fault energy.

What you learn at Tier-0.   Tier-0 is primarily for: proving the measurement pipeline, proving the runbook + A/B controls, characterizing EMI/thermal confounds, and validating that any apparent gain persists under artifact rejection. It also allows rapid iteration on geometry/schedules at low risk.

What Tier-0 cannot fully answer.   If the effect (if real) turns on only above certain field strengths, frequencies, or coupled energy scales, Tier-0 may fail to reach the regime. In that case, Tier-0 still de-risks the metrology and safety stack before scaling to 10 kW.

Tier-0 budget band.   For a bench-scale build, the all-in prototype cost typically compresses to:

- **Ultra-lean Tier-0 Lite (incremental)**: $25k–$100k (assumes you already own meaningful metrology assets such as a power analyzer / digitizer, probes, and calibration aids; focuses spend on safety and integration).

- **COTS-heavy Tier-0**: $75k–$250k (single bench cell, minimal containment).

- **Higher-credibility Tier-0**: $250k–$750k (better DAQ, more redundancy, more containment).

The main costs that do *not* scale down are software, calibration discipline, and engineering integration time.

12   Conclusion and Build Order

The Nautilus Power Testbed MVP is a machine for generating truth. By constraining the scope to a 10 kW envelope and focusing heavily on metrology and safety, we create a platform that can rapidly iterate on the core physics while providing the extraordinary evidence required for extraordinary claims.

Recommended Build Sequence:

1. **Bench Validation**: Build the DAQ and timebase first. Prove you can measure DC and AC power accurately on dummy loads.

2. **Safety Integration**: Build the Watchdog, Dump Load, and Contactor board. Verify it trips correctly on simulated faults.

3. **Drive Integration**: Connect the primary inverter and drive a dummy inductive load. Verify 600V operation and thermal management.

4. **Full Loop**: Install the first **SSVR PCB Prototype**. Run the "Soft Connect" sequence.

5. **Automation**: Enable the A/B runbook engine and signed reporting.

ID	Requirement	Level	Verify
REQ-001	Operation is remote-first: no human presence in the test cell is required during energized runs.	**MUST**	D/T
REQ-002	Input and output boundaries are explicitly defined and measured using simultaneous $V(t)$ and $I(t)$ on a shared time base.	**MUST**	I/T
REQ-003	Energy is computed by samplewise real-power integration (no RMS-only substitutions): $p(t) = V(t)I(t)$, $E = \int p(t)\,dt$.	**MUST**	A/T
REQ-004	Inter-channel time alignment after calibration is better than 1 μs for all accounting channels.	**MUST**	T
REQ-005	Accounting channels sample at $\geq$100 kS/s and use documented anti-alias filtering matched to the sampling plan.	**MUST**	I/T
REQ-006	Electrical envelope supports 0–600 VDC, 10 kW continuous, and 25 kW peak bursts ($\leq$ 10 s).	**MUST**	T
REQ-007	HV bus includes controlled precharge and contactor isolation with explicit safe-state behavior.	**MUST**	T
REQ-008	Output path includes a fast dump load ($\geq$25 kW) and a hardware clamp/crowbar for overvoltage protection.	**MUST**	T
REQ-009	Independent watchdog (separate power/clock where feasible) executes a mitigation ladder on overvoltage/overcurrent/thermal runaway/loss-of-load.	**MUST**	T
REQ-010	A runbook engine executes declarative Run Plans and supports matched-control A/B sequencing and gating.	**MUST**	D/T
REQ-011	Each run produces a Signed Run Bundle containing config snapshot, raw streams, derived outputs, and gate outcomes.	**MUST**	I/D
REQ-012	MVP includes at least four matched controls: detuned, load-only, geometry-neutral, and cable/ground shuffle.	**MUST**	D
REQ-013	Every report includes an uncertainty estimate $u(\Delta E)$ and discloses assumptions used to compute it.	**MUST**	A
REQ-014	The system enters a latched safe state on fault and requires an explicit reset/re-arm procedure.	**MUST**	T
REQ-015	Optional: external timestamping/anchoring of run digests (not required for MVP).	**SHOULD**	D
REQ-016	Optional: redundant sensing (e.g., secondary current sensor) to detect sensor faults.	**SHOULD**	I/T

Table 1: MVP requirements and verification methods.

Contribution	What it captures	Type
Current measurement gain/offset	Shunt calibration error, amplifier gain/offset, temperature coefficient	A/T
Voltage measurement gain/offset	HV probe calibration error, divider drift, common-mode limitations	A/T
Time skew / latency mismatch	Residual timing error between V and I channels affecting $V \cdot I$	T
Bandwidth and phase response	Phase error and attenuation at switching/harmonic frequencies	A
Aliasing and filtering mismatch	Under-sampling or insufficient anti-alias causing power bias	A/T
Numerical integration error	Discretization of $\int p(t)\, dt$ under finite sampling	A

Table 2: Representative uncertainty components (MVP).

Hazard	Initial default	Action
Bus overvoltage (warn)	$V_{\text{bus}} > 1.02\, V_{\text{bus,max}}$	Detune + engage dump load (soft)
Bus overvoltage (trip)	$V_{\text{bus}} > 1.05\, V_{\text{bus,max}}$	Dump load + driver disable (hard)
Bus overvoltage (crowbar)	$V_{\text{bus}} > 1.08\, V_{\text{bus,max}}$	Crowbar clamp + contactor open
Bus overcurrent	$I_{\text{bus}} > I_{\text{max}}$ (configurable by envelope)	Driver disable + contactor open
Thermal runaway	$dT/dt > \gamma$ (e.g., 1–2°C/s)	Detune + power derate; if persistent, shutdown
Loss-of-load signature	$I_{\text{load}} \downarrow$ and $dV_{\text{bus}}/dt \uparrow$	Immediate dump load + detune
Heartbeat timeout	$\tau_{\text{hb}} > 50$ ms	Hardware kill + dump load

Table 3: Illustrative initial safety thresholds. Values are starting points; engineering tuning required.

Category	Budget (USD)	Notes
HV power + energy handling	$50k–$200k	0–600V programmable supply, bus caps, precharge, contactors, wiring, enclosures
Driver / inverter stage	$25k–$250k	COTS inverter (motor-drive-class acceptable) vs custom GaN/SiC inverter + controls
Dump load + crowbar/clamp	$15k–$150k	Fast dump switching and hardware clamp; tuned to transient energy
Instrumentation (V/I)	$25k–$250k	Shunts, HV probes, isolation, calibration standards
DAQ + timing	$20k–$250k	Simultaneous sampling, time alignment, storage throughput
Thermal/EMI/vibration sensors	$5k–$100k	Thermocouples/RTDs, IR camera (optional), EMI probes, accelerometers
Test cell + safety interlocks	$25k–$300k	Fire containment, remote ops, E-stops, door interlocks, ventilation
Compute + software infra	$10k–$100k	Industrial PC, storage, runbook/analysis/provenance plumbing
Integration + commissioning labor	$250k–$2.0M	2–6 engineers for 2–6 months (fully loaded)
Subtotal (testbed cell)	**$425k–$3.35M**	Order-of-magnitude; overlaps between categories possible

Table 4: Order-of-magnitude prototype cost estimate for one validation cell.