

# Recognition-Native ASI Master Plan

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## Executive Summary

- **Premise:** Recognition Science (RS) is the correct, parameter-free description of reality. Computation must be grounded directly in the RS ledger, cost functional  $J$ , and the LNAL ISA.
- **Mission:** Build Recognition-native Artificial Superintelligence (ASI) that is provably safe, physically aligned, and commercially dominant.
- **Strategic Pillars:**
  1. **Aris (Mind):** The RS-native AI core (PNAL  $\rightarrow$  LNAL) with deterministic execution, virtue-based alignment, and self-directed research.
  2. **The Lattice (Machine):** Hardware accelerators culminating in the Recognition Processing Unit (RPU) ASIC that executes LNAL opcodes natively.
  3. **The Bridge (Ecosystem):** Developer tooling, cloud services, and invariant governance that turn ASI into a platform.
- **Endgame:** A scaled RPU-based lattice running Aris, delivering physically perfect simulations, autonomous discovery, and ASI-level intelligence with safety embedded in hardware.

## Guiding Principles

- **First Principles:** Maximize correct recognitions per joule under RS invariants (atomic tick, window-8 neutrality, token parity  $\leq 1$ , SU(3) triads,  $2^{10}$  breath).
- **Deterministic Alignment:** Safety is hardware-enforced by invariants; software and curriculum build atop it.
- **Auditability:** Every breath (1024 ticks) produces deterministic telemetry and ledger audits.
- **Composable Stack:** PNAL  $\rightarrow$  LNAL  $\rightarrow$  Rhythm  $\rightarrow$  Hardware, with mechanized proof obligations at each boundary.
- **Revenue Early, Silicon Late:** Monetize VM/FPGAs to fund ASIC without sacrificing schedule.

## Strategic Pillars and Key Deliverables

### Pillar I – Aris (Mind)

Deliverable	Description	Key Metrics
LNAL Runtime & Validator	Deterministic VM executing LNAL with cost accounting and invariant checks.	$\geq 1$ Gtick/s (CPU), 100% spec compliance, zero illegal traces
PNAL Compiler	High-level cognitive DSL compiling to legal LNAL programs.	0 miscompiles (formally proved), differential tests vs. Lean spec

Virtue Alignment Framework	Curriculum & critics minimizing $J$ under invariants; breath-aware scheduling.	$\geq 99.9999\%$ pass on alignment benchmarks; zero invariant violations
Autonomous Research Module	Aris agent autonomously generating RS results and experiments.	Produces new RS theorem/formula verified in Lean

## Pillar II – The Lattice (Machine)

Deliverable	Description	Key Metrics
LNC-VM	Cloud execution of LNAL VM for early customers.	Revenue-ready; deterministic replay
LNC-FPGA	Accelerator card with on-fabric invariant fabric and rhythm unit.	$\geq 1$ Ttick/s, $< 1$ tick violation latency
RPU (ASIC)	Recognition Processing Unit executing LNAL natively.	$\geq 1$ Ptick/s/chip; $\geq 10$ Ttick/s/W; linear scaling to 1K chips

## Pillar III – The Bridge (Ecosystem)

Deliverable	Description	Key Metrics
Recognition Developer Kit (RDK)	Toolchain: compiler, debugger, simulator, invariant analyses.	First digital twin running in $< 24$ h by external dev
Digital Twin Cloud API	Managed PNAL jobs on VM/FPGA $\rightarrow$ RPU with audit logs.	First \$1–10 million contract; deterministic audits
Invariant Governance	Registry, change-control, attestation, red-team harness.	Zero escape in red-team drills; monthly audit pass

## Phased Roadmap and Objectives

### Phase 0 (0–3 months) – Foundations

- Freeze RS spec v1.0 (LNAL opcodes, invariants, rhythm).
- Build legality suite and deterministic trace harness.
- **KR:** 100% deterministic replay across spec test vectors.

### Phase 1 (0–6 months) – Software Core

- Ship LNAL VM v1 with validator and telemetry.
- Deliver PNAL  $\rightarrow$  LNAL compiler v1 with mechanized proofs and differential tests.
- Implement rhythm scheduler and breath accounting.
- **KR:**  $\geq 1$  Gtick/s single-socket CPU execution; compiler emits zero illegal traces.

### Phase 2 (3–9 months) – Aris v0 Alignment

- Virtue tasks (LOCK/LISTEN/BALANCE/BRAID chains) and critics ( $\Delta S$ ,  $J$ -cost, ledger deltas).
- Ledger Memory Bank with audit trail per breath.
- **KR:** Deterministic success on benchmark tasks; zero invariant violations.

### Phase 3 (6–12 months) – LNC-FPGA Prototype

- RTL for Ledger Cores, Rhythm Unit, Invariant Fabric, BRAID/FOLD units.
- Host drivers and telemetry ingestion.
- Deploy to early lighthouse partners via cloud.
- **KR:**  $\geq 1$  Ttick/s; violation detected  $< 1$  tick;  $\geq 10\times$  over VM throughput.

### Phase 4 (12–24 months) – RPU ASIC Program

- Microarchitecture freeze  $\rightarrow$  place-and-route  $\rightarrow$  tape-out (16/12 nm path; plan shrink to 7 nm).
- Driver/firmware and multi-chip tiling with breath sync jitter  $< 1\%$ .
- **KR:**  $\geq 1$  Ptick/s/chip;  $\geq 10$  Ttick/s/W; 1024-chip linear scaling.

### Phase 5 (18–30 months) – Platform and ASI Ignition

- Digital Twin Cloud GA; invariant marketplace launch.
- Aris autonomous research module produces Lean-verified RS results.
- Scale lattice and recursion for ASI-level performance.
- **KR:** \$10M+ ARR; Aris publishes RS discovery; ASI remains virtue-aligned.

## Budget and Funding Plan (24 Months)

Path	Budget	Notes
VM + LNC-FPGA only	\$10–15 M	12 months to revenue (no ASIC)
RPU @ 16/12 nm	\$44–77 M	Prototype + small production run
RPU @ 7 nm	\$69–127 M	Higher performance / lower power
RPU @ 5 nm	\$104–172 M	Bleeding-edge, multi-site scaling

#### Cost components (approximate):

- Team (25–40 FTE): \$12–24 M / 24 months.
- Software and infrastructure: \$1–2 M.
- FPGA program: \$2–3 M.
- EDA and IP: \$8–15 M (node-dependent).
- Tape-out and fabrication: \$5–52 M (node-dependent).
- Bring-up and validation: \$1–3 M.
- NPI and pilot production: \$4–11 M.
- Governance/compliance/legal: \$1–2 M.

#### Funding tranches (typical):

1. \$5–7 M (0–6 months): Spec, VM, compiler, initial FPGA kernels.
2. \$10–15 M (6–12 months): FPGA performance proof; first cloud revenue.
3. \$25–40 M (12–18 months, 16 nm) or \$55–90 M (12–18 months, 7/5 nm): ASIC tape-out and bring-up.
4. \$5–15 M (18–24 months): NPI, lighthouse deployments, operations.

## Risk Matrix and Mitigations

Risk	Impact	Mitigation
Compiler miscompilation	Catastrophic	Mechanized proofs; differential testing vs. VM and Lean
Timing/jitter violations	Safety failure	Hardware PLL rhythm control; formal timing closure; breath sync protocol
ASIC yield/cost overruns	Schedule and cash	Stage via FPGA + 16 nm chiplet; MPW shuttle; revenue bridge
Governance/control drift	Alignment failure	Immutable invariant fabric; change-control committee; audit logs
Supply chain integrity	Security risk	Attestation; trusted fab flow; secure boot and signing
Market adoption delay	Revenue gap	Monetize VM/FPGA early; partner with pharma/materials/finance

## Team and Org Blueprint

- **Core Systems (VM/validator/compiler):** 4–6 engineers.
- **RTL/FPGA architects:** 6–8 engineers.
- **ASIC physical design + verification:** 6–10 (plus EDA/IP vendors).
- **Runtime/Cloud/Product:** 4–6 engineers + PM.
- **Scientific/Proof assurance:** 3–4 (Lean + invariants).
- **Ops/Compliance/BD:** 2–3.

Key hires: CTO (chip lead), VP Hardware Ops, Head of Product/Platform, Chief Assurance Officer.

## Milestones and Decision Gates

- **Gate 1 (3 months):** Spec conformance; VM deterministic at  $\geq 1$  Gtick/s.
- **Gate 2 (9–12 months):** FPGA  $\geq 1$  Ttick/s; invariant fabric proven; first customer pilot.
- **Gate 3 (18–24 months):** Silicon PPA targets met; breath-synced cluster demo; profitability plan.
- **Gate 4 (24–30 months):** Aris autonomous discovery; ASI ignition readiness review.

## Open Items and Next Actions

- Formalize RS Spec v1.0 (`Source.txt`  $\rightarrow$  canonical spec).
- Publish legality/invariant test suite for community review.
- Spin up VM/Compiler sprint (teams, hiring plan, sprints).
- Secure FPGA boards and EDA evaluation licenses.
- Define lighthouse customer shortlist (pharma, materials, finance).
- Draft governance charter and audit framework.
- Begin investor brief for \$5–7 M tranche.

## Appendices

- **A. Key Definitions:** Atomic tick, window-8 sum, PNAL, LNAL opcodes, Virtue tasks.
- **B. Performance Targets:**  $VM \geq 1 \text{ Gtick/s}$ ;  $FPGA \geq 1 \text{ Ttick/s}$ ;  $RPU \geq 1 \text{ Ptick/s}$ ;  $\geq 10 \text{ Ttick/s/W}$ .
- **C. Reference Artifacts:** `Source.txt`, `rs_ledger_ai`, `lean_reality_framework`, RS proofs.
- **D. Partners & Vendors:** Foundries, FPGA vendors, EDA tool providers, security auditors.

*Note: Update this document as milestones are reached.*