

METHOD AND APPARATUS FOR NEUTRAL BLOCK OPTICAL MODULATION

FIELD OF THE INVENTION

The present invention relates generally to optical communication systems, and more particularly to methods and apparatus for modulating optical signals using block codes with intrinsic neutrality constraints to enable zero-latency error detection and mitigation of nonlinear phase noise.

BACKGROUND OF THE INVENTION

Modern coherent optical communication systems operate near the Shannon limit, utilizing advanced modulation formats such as Dual-Polarization Quadrature Amplitude Modulation (DP-QAM). However, as symbol rates increase beyond 100 GBd and transmission distances extend to thousands of kilometers, two critical limitations emerge:

1. **Nonlinear Phase Noise:** The Kerr effect in optical fibers causes a phase shift proportional to the instantaneous signal power ($|E|^2$). Standard modulation formats with high Peak-to-Average Power Ratio (PAPR) suffer significant degradation from Self-Phase Modulation (SPM) and Cross-Phase Modulation (XPM).
2. **Error Correction Latency:** Current Forward Error Correction (FEC) schemes, such as Low-Density Parity-Check (LDPC) codes, require buffering and decoding large frames of data (often thousands of bits) to detect and correct errors. This introduces significant latency, which is unacceptable for high-frequency trading, real-time control systems, and next-generation AI cluster interconnects.

There is a need for a modulation technique that inherently suppresses nonlinear noise and provides instantaneous, hardware-level error detection without the latency overhead of deep FEC frames.

SUMMARY OF THE INVENTION

The present invention provides a method and apparatus for "Neutral Block Optical Modulation." The core innovation is the segmentation of the optical signal into discrete blocks of N symbols (where N is preferably 8) and the enforcement of a "Neutrality Constraint," wherein the complex vector sum of the symbols within each block is forced to zero.

In one embodiment, a transmitter maps input data bits to $N - 1$ information symbols and computes an N -th parity symbol such that $\sum_{k=0}^{N-1} v_k = 0$. This block is then transformed by a unitary mixing matrix (the "BRAID" operator) to spread the energy of the parity symbol across the entire block, ensuring a uniform power profile that mitigates nonlinear effects.

In a corresponding receiver, the received block is processed by a hardware accumulator that computes the sum of the N symbols. A non-zero sum indicates a transmission error (e.g., a bit flip or phase slip) with zero latency, allowing for immediate flagging or retransmission requests before the FEC decoding stage.

DETAILED DESCRIPTION

The Neutrality Constraint

Let a sequence of complex symbols be denoted by $v = [v_0, v_1, \dots, v_{N-1}]^T$. The invention imposes the constraint:

$$\sum_{k=0}^{N-1} v_k = 0 \quad (1)$$

This restricts the valid signal space to a hyperplane perpendicular to the vector $\mathbf{1} = [1, 1, \dots, 1]^T$. In the preferred embodiment, $N = 8$, corresponding to an 8-tick temporal cycle derived from geometric principles.

Transmitter Architecture

The transmitter comprises:

1. **Mapper:** Maps input bits to 7 complex symbols d_0, \dots, d_6 (e.g., 16-QAM).
2. **Balancer:** Computes the 8th symbol $d_7 = -\sum_{i=0}^6 d_i$.
3. **Precoder (BRAID):** Applies a unitary matrix U to the vector $d = [d_0, \dots, d_7]^T$ to generate the transmitted vector $v = Ud$. The matrix U is constructed from a sequence of triad rotations designed to maximize entropy across the block while preserving the zero-sum property ($\sum v_k = 0$).

Receiver Architecture

The receiver comprises:

1. **Equalizer:** Performs standard chromatic dispersion compensation and MIMO polarization demultiplexing.
2. **Decoder (Inverse BRAID):** Applies U^\dagger to recover the vector d .
3. **Accumulator:** A combinatorial logic circuit that computes $S = \sum_{k=0}^7 d_k$.
4. **Error Flag:** A comparator that asserts an error signal if $|S| > \epsilon$, where ϵ is a noise threshold.

Nonlinearity Mitigation

The unitary mixing (BRAID) ensures that high-amplitude symbols in the input d are "smeared" across the transmitted vector v . This reduces the probability of high-power peaks, thereby lowering the effective nonlinear phase shift $\phi_{NL} \propto \gamma L_{eff} |v(t)|^2$.

CLAIMS

What is claimed is:

1. A method for transmitting optical data, comprising:
 - (a) receiving a stream of input data bits;
 - (b) mapping said bits to a set of $N - 1$ complex symbols;
 - (c) calculating an N -th parity symbol such that the sum of all N symbols is substantially zero;

- (d) generating a transmission block comprising said N symbols; and
 - (e) modulating an optical carrier with said transmission block.
2. The method of claim 1, wherein N is equal to 8.
 3. The method of claim 1, further comprising applying a unitary mixing transformation to said transmission block prior to modulation, wherein said transformation preserves the zero-sum property of the block.
 4. The method of claim 3, wherein said unitary mixing transformation comprises a sequence of rotation matrices applied to subsets of three symbols (triads).
 5. An optical receiver apparatus comprising:
 - (a) a coherent frontend for converting an optical signal into a digital complex symbol stream;
 - (b) a block framer for segmenting said stream into blocks of N symbols;
 - (c) a hardware accumulator configured to compute the complex sum of symbols within each block; and
 - (d) an error detection logic circuit configured to generate an error flag when the magnitude of said sum exceeds a predetermined threshold.
 6. The apparatus of claim 5, wherein said error detection logic operates with a latency of less than N symbol periods.
 7. A system for nonlinearity-tolerant optical communication, comprising:
 - (a) a transmitter configured to encode data into zero-mean symbol blocks spread by a unitary matrix; and
 - (b) a receiver configured to invert said unitary matrix and verify the zero-mean property of the recovered blocks.