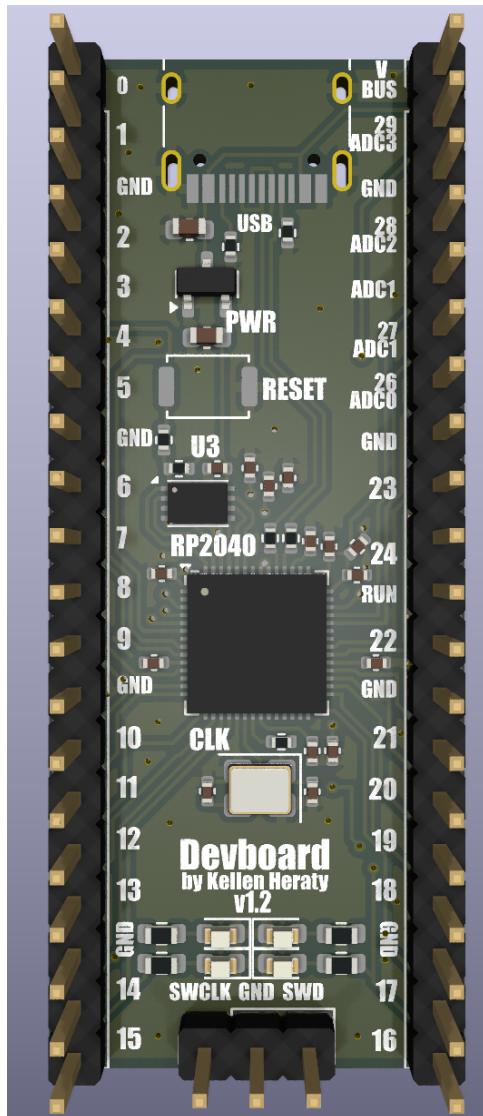


# Devboard v1.2

RP2040 Development Platform



Designed by Kellen Heraty

<https://github.com/kaileh57/devboard>

Date: December 9, 2025

## Product Overview

The **Devboard v1.2** is a compact, high-performance microcontroller board powered by the Raspberry Pi RP2040. It combines the power of dual Cortex-M0+ cores with a modern USB-C interface and a simplified GPIO layout.

### 1.1 Technical Specifications

- **MCU:** RP2040 (Dual-core ARM Cortex-M0+ @ 133MHz)
- **Flash Storage:** 2MB QSPI (Winbond W25Q16JV)
- **SRAM:** 264kB on-chip
- **Power Input:** 5V via USB-C
- **Operating Voltage:** 3.3V (Onboard MCP1700 LDO, 250mA Max)
- **GPIO:** 20x user-accessible pins (plus 4x LED pins)
- **Dimensions:** 40-pin DIP form factor (Standard 2.54mm pitch)

## Pinout & Interfaces

The board features a 40-pin header layout designed for breadboard compatibility.

Left Function	GP	Pin	Pin	GP	Right Function
UART0 TX / I2C0 SDA	<b>0</b>	1	40	<b>VBUS</b>	5V Input
UART0 RX / I2C0 SCL	<b>1</b>	2	39	<b>29</b>	ADC3
Ground	GND	3	38	GND	Analog GND
I2C1 SDA	<b>2</b>	4	37	<b>28</b>	ADC2
I2C1 SCL	<b>3</b>	5	36	<b>27</b>	ADC1
SPI0 RX	<b>4</b>	6	35	<b>26</b>	ADC0
SPI0 CSn	<b>5</b>	7	34	GND	Ground
Ground	GND	8	33	<b>23</b>	User IO
SPI0 SCK	<b>6</b>	9	32	<b>24</b>	User IO
SPI0 TX	<b>7</b>	10	31	<b>RUN</b>	Reset/Enable
SPI1 RX	<b>8</b>	11	30	<b>22</b>	User IO
SPI1 CSn	<b>9</b>	12	29	GND	Ground
Ground	GND	13	28	<b>21</b>	I2C0 SCL
SPI1 SCK	<b>10</b>	14	27	<b>20</b>	I2C0 SDA
SPI1 TX	<b>11</b>	15	26	<b>19</b>	SPI0 TX
UART0 TX	<b>12</b>	16	25	<b>18</b>	SPI0 SCK
UART0 RX	<b>13</b>	17	24	GND	Ground
Ground	GND	18	23	<b>17</b>	<b>LED D4</b>
<b>LED D1</b>	<b>14</b>	19	22	<b>16</b>	<b>LED D3</b>
<b>LED D2</b>	<b>15</b>	20	21	-	(No Pin)

Table 1: Devboard v1.2 Pin Map

### 2.1 Status LEDs

Four red LEDs are connected to the lower GPIO pins. Writing HIGH to these pins turns the LED ON.

LED D1	LED D2	LED D3	LED D4
GPIO 14	GPIO 15	GPIO 16	GPIO 17

## Schematic Diagram

The following schematic details the core RP2040 connections, USB-C interface, and power regulation circuit.

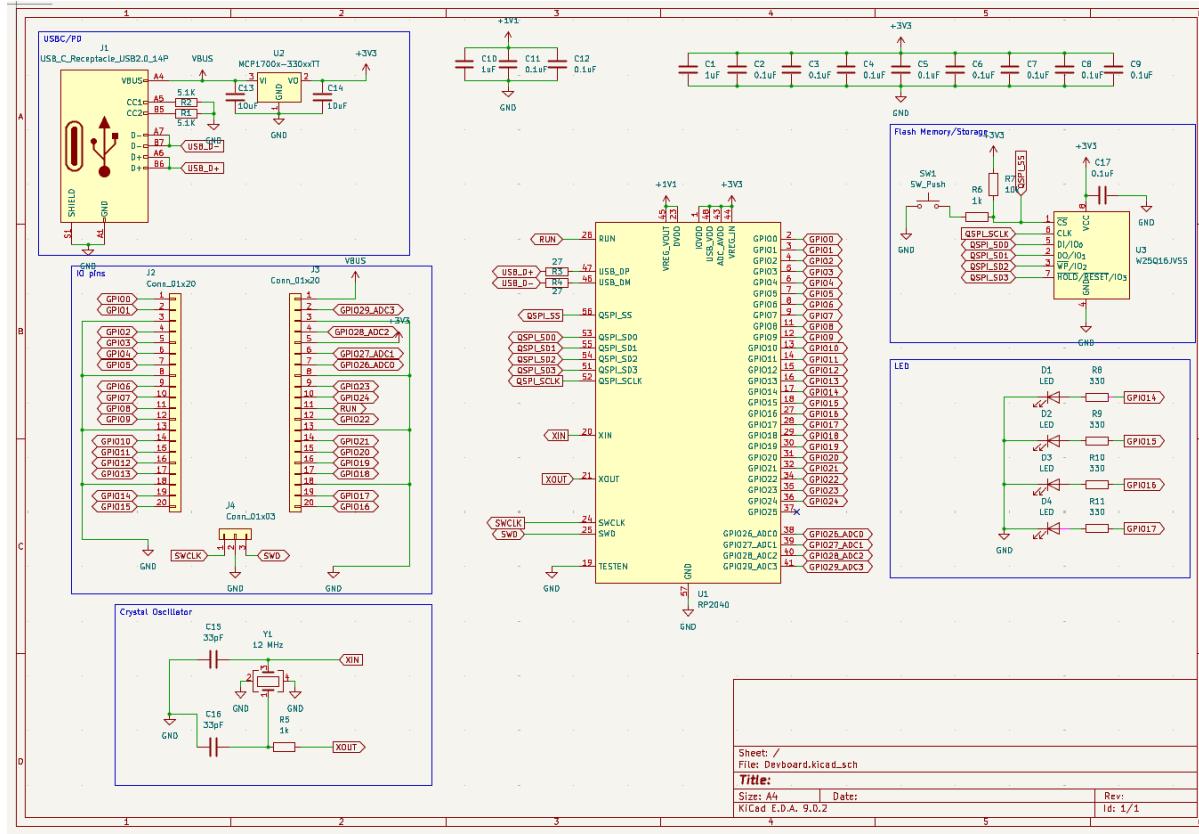


Figure 1: Full System Schematic

### 3.1 Design Notes

- **Crystal Oscillator:** 12MHz external crystal (Y1) with 33pF load capacitors.
- **USB Termination:** 27Ω series resistors on D+ and D- lines.
- **Flash Memory:** W25Q16JV connected via QSPI interface.
- **Bootloader:** Pulls CSn low via SW1 to enter USB Mass Storage mode.