The CPU09GPP provides:

* local HD63C09 CPU at 4MHz clocks
* 1Kx8 dual port RAM between host CPU and local CPU with interrupt flags and arbitration system
* up to 32KB(31KB) of local RAM
* up to 32KB(31KB) of (E)EPROM
* up to 1K Bytes of dedicated IO space (A0...A9)
* (optional) periodic timer interrupt circuitry (3.3, 6.6, 13.2 mS)
* LED's which signal host CPU access and local CPU access
* local CPU can be individually reset from assigned bus pin (A3)
* the CPU09GPP has it own, full address, decoding for the system bus.
  - (Page select for F8,F9,FA,FB or FE (default))
  - Cardselect 0...3 (x000..0x3FF, x400...x7FF, x800...xBFF, xC00...xFFF)
* 40 pin IO expansion connector with local: Data, Address and Control signals.

Functional description:

The card contains it’s own CPU with 64k addressing capacity.
There’s 8K (default) of program space in the (E)Prom accessible for the processor.
(Changing the GAL can increase this space to 32K)

The logic in the GAL’s take care of all device addressing decoding.
A 1Kx8 dual port ram for exchange of data between the GPP and the host CPU.
An bi-directional interrupt for data present on either side of the dual port ram.

System bus decoder:

The GAL G1 (U2) takes care of the decoding of the page and card selection.
Placing the correct jumpers on J3 and J4 selects the page and card.

No jumpers defaults to page FE and card select 3, because of the pull-up array RA2.
FEC00-FEFFF for the host CPU.

Data exchange:

The host CPU can only see the 1K dual-port RAM page and has no direct access to other area's in the GPP memory map. By writing to the dual-port ram address $3FF, the IRQ line to the GPP-CPU is set, signaling that data is available from the host side.
If an identical ram location is accessed simultaneously by both the host CPU and the GPP-CPU, the busy flag is asserted on one side. If this is the host CPU side, the signal B-MRDY (C24) is asserted, provided that link L2 is connected.

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CPU LED:

Active if the host CPU accesses the dual-port ram.

GPP address decoder:

The GAL G2 (U10) takes care of all address decoding. It also processes the reset signals. Either the system bus reset (A21) or the GPP-card reset (A3) will reset the GPP processor.

The dual-port ram is mapped to $0000-$03FF. Like on the system-bus side, the GPP can signal data present by writing to a special address in the ram. This is $3FE and a write operation to this address sets an IRQ to the system-bus.

Similar to the system-bus, the GPP side has a busy fline. If L1 has a jumper, the MRDY input of the processor is asserted by this.

RAM:

Location U4 is intended for the system ram. The layout is a narrow 28 pin, intended for a 32k ram. This is mapped to $0400-$7FFF. (1KB is taken by the dual-port RAM)

(E)PROM:

Location U5 is intended for system rom. The layout is a 28 pin, intended for a maximum of 32K Rom. The current GAL decoding is set for $E000-$FFFF. This is a 8 K area that can be expanded by changing the content of GAL2. However the lowest 1K will always be taken by the IO space.

SEL1 and SEL2:

These signals select the access to devices connected to the 40 pin header J5.
SEL1 = $8000-$80F7
SEL2 = $8080-$80FF

NB: A8 and A9 are not used in the decoding. This means the same physical locations will be accessed multiple time in the area $8000-$83FF

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LCLIO:

Interrupt handling register. Address $8400-$847F. Also multiple locations in $8400-$87FF.
$8400 timstat read, interrupt time and status
%00000001 IRQENB
%01000000 IRQFLG
%10000000 IRQTIM

$8400 timctl write, enable timer interrupt
%00000001 IRQENB

$8401 timrst write, reset IRQ from timer
%xxxxxxxx ANY value

The whole timer circuitry may be ommitted if the application has no requirements for it.
U8, U6, U9 and U7 .

IO LED:

Active when CPU addresses area $8000-$83FF

Interrupt timer (optional, see LCLIO):

The divider U9 processes the SIG30 clock signal 1.2288Mhz (4.9142/4) into pulses of 3.3mS, 6,6mS of 13,3mS. Placing only ONE of R7, R4 or R5 selects an interrupt timing signal.

The input to U9 is actually protected by R6, C11, D3 and D4. This makes sure that the input will not be damaged if a supply voltage is accidentally fed to this bus signal (e.g. +/-12V , in case the busline is carrying high voltages)

Connector J5:

This connector carries Data Bus D0...D7, Address Lines A0...A9, SEL1/2, and the control signals R/W, E, Q, BS, AB, HALT, IRQ and FIRQ.

A buffered 1.2288Mhz signal is also available if U9 is present on the board.

Still some spare pins available.

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