

## Modification to run CPU09CMI on 4.5MHz bus.

Now we need the Q clock on the 09FLP

Replace xtal into 18MHz.

Replace C1 and C2 by 15pF.

Place 10M smd between crystal pins.

Replace GAL CMI\_1 by CMI-4\_1

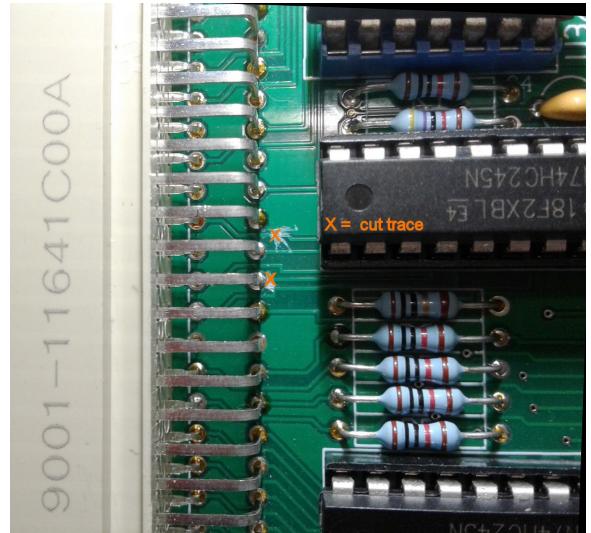
Only use the HD63C09.

**Skip next if already on 16Mhz modification!**

*On top side:*

Cut trace between U4-14 and J1 C-21 (B\_VMA-)

For REV:0.9 print only cut trace from J1 A23 to R15



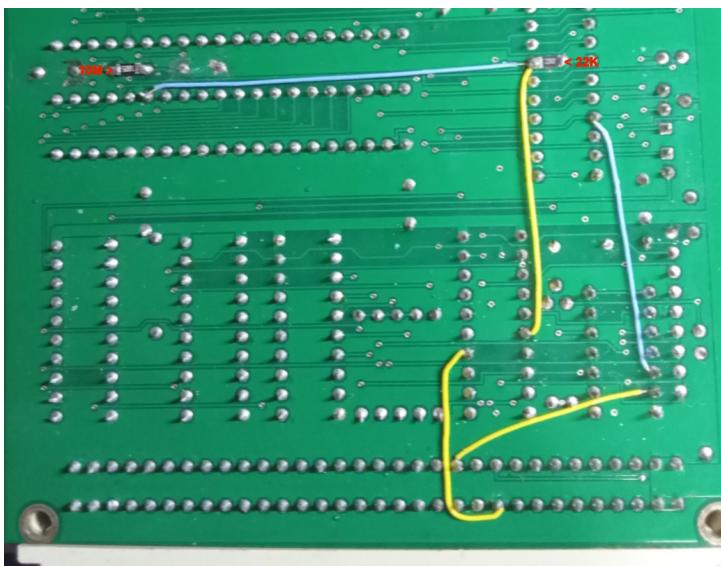
*On solder side:*

Cut trace between U13-19 and via (OVMA-)

Place 22K resistor between U13-19 and Gnd

Place wire from U6-35 to U13-19 (blue) and U4-6 (Q) (yellow)

Place wire from U4-14 to J1 A-23 (B\_Q) (yellow)



Place wire from U3-7 to J1 C-21 (B\_VMA-) , Or:

**To keep CPU09CMI 68x02 compatible  
or need VMA- signal with 68x02 on the bus  
for CPU09GPP or CPU09RAM card.**

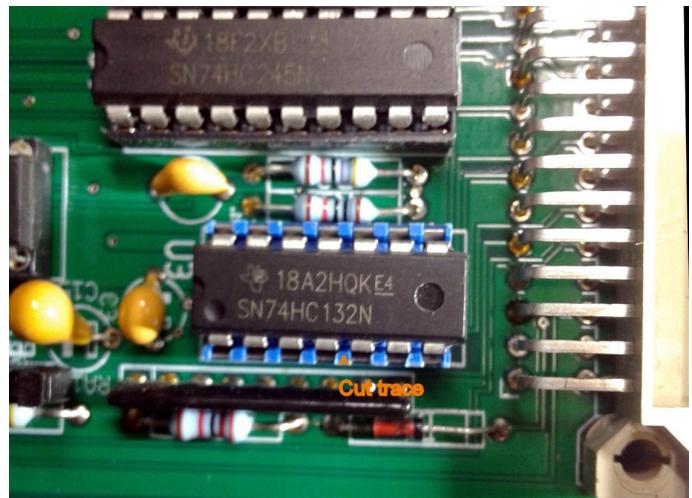
*On top side:*

Cut trace between U3-4 and U3-5

*On solder side:*

Place wire from U3-5 to U13-9 (VMA) (blue)

Place wire from U3-6 to J1 C-21 (B\_VMA-) (yellow)



Remarks:

Only tested ACIA with HD63B50 chip.

CPU09RAM, CPU09IDE still work fine. FLXMIN + 09FLP read FLP\_MRDY.

Should work on REV:0.9 and REV:1.1 print

With xtal up to 12 MHz and correct GAL's the S6802, MC68B02 still works on this board.