RF Technologies for Low Power Wireless Communications
Edited by Tatsuo Itoh, George Haddad, James Harvey

ISBNs: 0-471-38267-1 (Hardback); 0-471-22164-3 (Electronic)

6

POWER AMPLIFIER APPROACHES FOR HIGH EFFICIENCY AND LINEARITY

PETER M. ASBECK AND LARRY LARSON
Department of Electrical and Computer Engineering, University of California—San Diego
ZOYA POPOVIC
Department of Electrical Engineering, University of Colorado, Boulder
TATSUO ITOH
Department of Electrical Engineering, University of California—Los Angeles

6.1 INTRODUCTION

To reduce the power consumption of a wireless transceiver, greatest leverage is often provided by the output power amplifier of the transmitter. This chapter describes a series of novel concepts to increase microwave power amplifier efficiency. Within modern wireless systems, power amplifiers must meet exacting linearity specifications, which tend to be at odds with the need for high efficiency. To characterize these specifications and associated trade-offs, we first review the linearity requirements and dynamic range requirements of representative high performance communication systems. We then demonstrate concepts for power amplifier improvement that can meet the system requirements.

Output power levels and demands on efficiency and linearity are typically somewhat different for handsets (which rely on battery energy sources and have relatively modest demands on power and linearity) and base stations (which have

higher output power and more stringent linearity requirements, although their efficiency concerns are not as overriding as for handsets). The approaches outlined here can be applied to both handsets and base stations. They have particular relevance to the scenario of peer-to-peer communication, where there are no unique base stations. This scenario characterizes many communications networks for military applications.

One of the approaches discussed in this chapter is based on amplifiers operating in Class AB, used in conjunction with an efficient, rapidly modulated dc–dc converter that is capable of providing a supply voltage optimized in accordance with the instantaneous output power. It is shown that this system can provide dramatic increases in efficiency, particularly if the power amplifier is required to operate over a wide range of output power levels.

Other approaches described in this chapter are based on the operation of transistors in switching mode. By ensuring that the transistor current is zero when its output voltage is high, and conversely, that the transistor voltage is minimum when its current is high, the amplifier efficiency can in principle be increased dramatically over Class A or AB operation. Class E and F switching-mode amplifiers are also discussed, which achieve efficiency above 80% at frequencies above 5 GHz. Typically the switching-mode amplifiers have relatively poor linearity; thus they are not adequate for wireless communications applications. Here we show that a great deal of the efficiency of the Class E and F amplifier is preserved if the output is ''backed off'' to the level needed in representative handset applications. Also discussed are several approaches that can achieve in principle very high linearity without sacrificing the efficiency of switching-mode applications. These include the LINC (linear amplification with nonlinear components) and the bandpass Class S approaches.

An additional approach for transmitter improvement is based on a synergistic design of the power amplifier and the output antenna. By removing the typical constraint of matching each component to 50 Ω, it is possible to simplify the system, while improving its characteristics. For maximization of efficiency, the antenna design must take into account the requirements of the power amplifier impedances at various harmonic frequencies, as well as the fundamental.

6.2 LINEARITY AND EFFICIENCY REQUIREMENTS IN WIRELESS COMMUNICATIONS

Although the output signal for FM-modulated analog transmission systems (e.g., AMPS) has a constant envelope, the majority of the spectrally efficient wireless systems use modulation formats that have a variable signal envelope. For example, the output signal for filtered quaternary phase shift keying (QPSK) is shown in Figure 6.1, in both the time domain and frequency domain (for a raised-cosine filter characterized by $\alpha = 0.5$). The spectrum is well confined to a narrow frequency channel, which allows multiple users within an allocated frequency band, but it has variations in instantaneous power with a peak-to-average power ratio of 5.2 dB. If

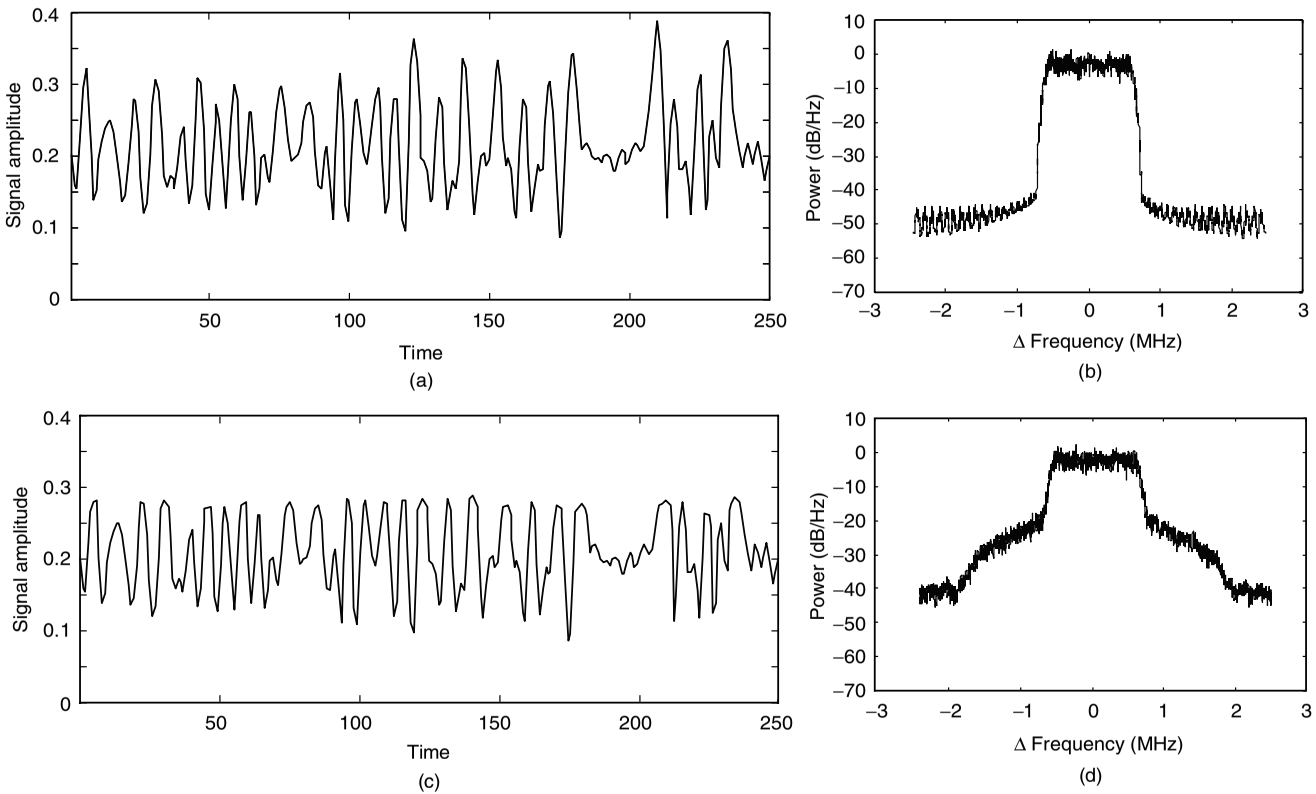


Figure 6.1. (a) Representative output envelope for a filtered QPSK signal in time domain (time units on the horizontal axis correspond to one-quarter of the bit interval); (b) same signal in frequency domain; (c) signal passed through clipping amplifier; (d) resulting output spectrum, showing adjacent channel power.

such a signal is passed through an amplifier that saturates (and thus clips the high-amplitude signals) then a distorted output waveform will be obtained (such as that shown in Fig. 6.1(c)), and correspondingly an output spectrum is obtained that is spread over a wide range of frequencies (as shown in Fig. 6.1(d)). The nonlinear action of the amplifier leads to the generation of power in adjacent channels. This power, measured with the adjacent channel power ratio (ACPR) must be kept within tight bounds (as specified by the FCC for commercial air interface standards) to prevent interference to neighboring users. The clipping also leads to a loss of modulation accuracy within the transmitted channel itself, which degrades the signal-to-noise ratio. As a result, for filtered QPSK and similar signals, the power amplifier must be operated in a mode where the clipping of large amplitude signals is kept to a minimum. This, in turn, dictates that the average output power of the amplifier must be substantially lower than its maximum (or ''saturated'') output power.

The signals that must be transmitted from base stations typically have even higher peak-to-average power ratios than those from handsets (and thus they require greater ''output power backoff'' in order to preserve linearity). A base station serving multiple users typically transmits signals at different carrier frequencies at the same time. The different carriers add with random phases, and at some instances constructively interfere in a way that considerably enhances the instantaneous peak power. This leads to high values of peak-to-average power ratio. In code division multiple access (CDMA) systems, multiple signals that have the same carrier frequency but are spread with different sequences are added together at the base station for transmission (with, in general, different power levels). This leads to a base station output signal that also has high peak power relative to the mean. To preserve the signal fidelity through the power amplifier, a relatively high value of the saturated power relative to the average power must be maintained (typically >10 dB).

Table 6.1 summarizes the peak-to-average power ratio for representative wireless communications signals. Signals for the handsets have differing values of peak-to-average power, as a result of differences in modulation format. Signals from base stations tend to behave similarly for all formats and have an output power distribution that resembles that of white Gaussian noise modulation. The variation of the

TABLE 6.1. Peak-to-Average Power Ratio for Signals Used in a Variety of Wireless Communications Systems

System	Modulation	Peak-to-Average Power Ratio
AMPS (handset)	FM	0 dB
GSM (handset)	GMSK	0 dB
NADC (handset)	$\pi/4$ DQPSK	3.2 dB
CDMA IS-95 (handset)	OQPSK	5.1 dB
Multicarrier CDMA		>13 dB
Sum of eight sinusoids		9 dB
White Gaussian noise		10 dB

signal occurs on a rapid time scale, on the order of the inverse of the signal bandwidth.

Amplifiers also need to function with a wide range of average output power levels, as a result of changing characteristics of the wireless channel. The power output is varied in accordance with the changing degrees of fading and varying mobile-to-base-station distances on a time scale of milliseconds or longer [1]. Figure 6.2 shows a representative probability distribution for the transmitted power of a CDMA handset. Although the peak output power is over 600 mW, the amplifier is seldom used in this condition; the average output power is below 10 mW. Within the CDMA network, accurate control over the output power of each user is critical, since if a user employs greater power than is optimal, he/she will create interference at the base station for other users (as a result of the nonorthogonality of the signals used). Base station average power also changes significantly over time as the number of users in a given sector changes over time.

Efficiency of power amplifiers for wireless handsets is one of the most critical concerns for prolonging battery life. In base stations, power efficiency is also important, since it impacts both prime power usage and cooling requirements. While power-added efficiency (PAE) of microwave power amplifiers above 80% has been reported, in practice, the efficiencies attained in wireless networks is much lower, typically near 5–10%. A key issue limiting power efficiency in wireless communications power amplifiers is the variation in signal level that must be accommodated, as just described. Power amplifier efficiency typically drops rapidly as the amplifier output is reduced below its saturated power level, leading to low overall system

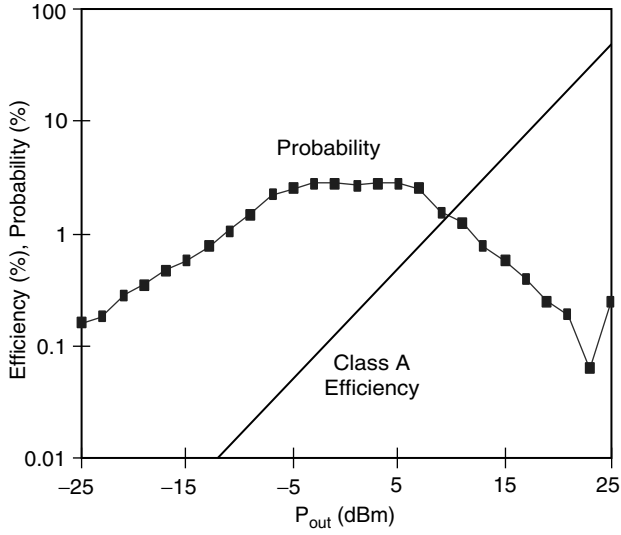


Figure 6.2. Probability distribution of the transmitted power level for a representative CDMA handset. Also shown is the efficiency of an ideal Class A amplifier at the given output power level.

efficiency. For example, Class A amplifiers have efficiency that depends linearly on the output power. Figure 6.2 shows the drain (or collector) efficiency of an ideal Class A amplifier as a function of the output power, *P*. The proportionality of efficiency to output power stems from the fact that the dc current and voltage used to bias the output transistor are both independent of output power—and must be selected to accommodate the maximum output power. To improve the situation, the dc current and dc voltage supplied to the amplifier (or both) must be allowed to vary as output power changes. Figure 6.3 schematically illustrates how the dc bias point of an amplifier can be varied as the power is reduced from its maximum (saturated) value, in relation to the current–voltage characteristics of the output transistor and its associated load line.

The most straightforward manner to vary the bias conditions is to alter the dc drain (or collector) current of the output transistor. In Class AB mode the current waveform is not symmetric about the quiescent bias point. As a result, the dc average current varies as the output swing is increased (as thus automatically changes with output power level). In the limit of Class B operation, the dc bias varies according to the square root of output power. As a result, power efficiency varies as $P^{0.5}$ over a narrow range (albeit at some cost in linearity). Dynamic gate biasing (changing bias conditions as a function of input power by using an input signal envelope sensitive biasing network) is an additional technique that can be used to change output current for different output powers. The number of gate (or emitter) fingers in a composite large power transistor can also be varied to optimize the current consumption (while also changing input and output impedance). The limit on dc bias current reduction is set by the trade-off of linearity and efficiency. This technique is used in many presently available power amplifiers. Figure 6.4 shows, for example, the bias current and efficiency as a function of output power for a commercial heterojunction bipolar transistor (HBT)-based power amplifier. The $P^{0.5}$ regime is clearly visible. This provides for a significantly higher efficiency when the amplifier is operated at low average power levels (which are encountered much of the time in actual handset usage).

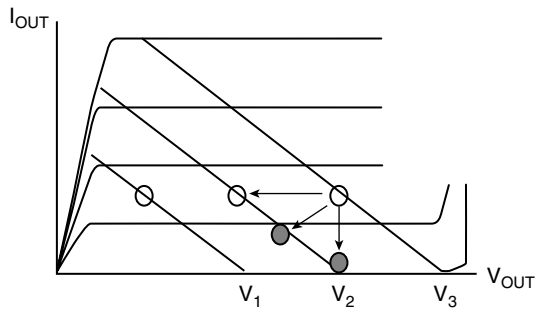


Figure 6.3. Schematic representation of output transistor characteristics and load line. The dc bias conditions at maximum power are shown, as well as desirable directions in which to vary the bias at lower output power levels.

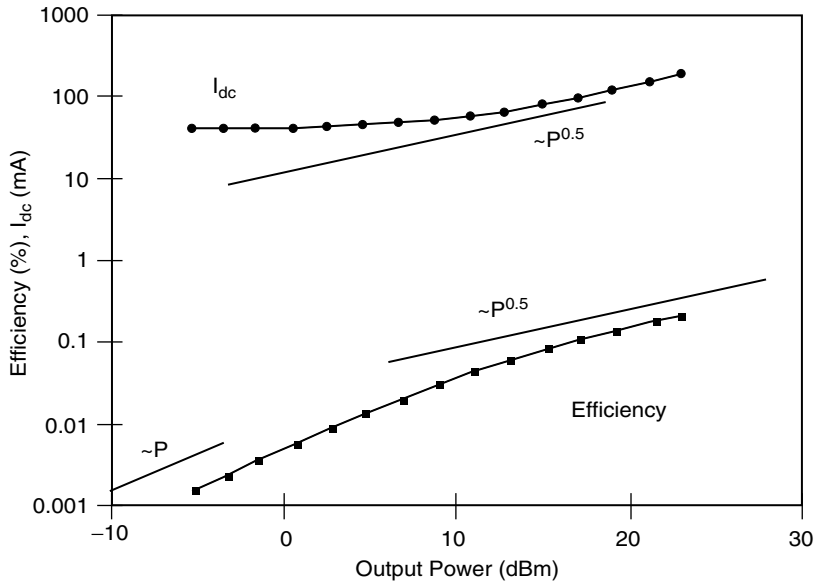


Figure 6.4. Measured dc input current and efficiency versus output power for a commercial CDMA power amplifier.

It is also possible to vary the dc supply voltage in accordance with the output power level [2–4], in order to provide additional increases in efficiency at low output power levels. The most desirable solution is to vary simultaneously dc bias current and supply voltage. In principle, efficiency that is constant over a wide range of output powers can thereby be obtained. This architecture is termed here *dynamic supply voltage (DSV) amplifier*; the term *envelope tracking amplifier* has also been applied. In the following, research results for the dynamic supply voltage amplifier are described in detail.

6.3 DYNAMIC SUPPLY VOLTAGE AMPLIFIER

The DSV amplifier structure is shown in Figure 6.5. The structure comprises a basic Class AB power amplifier and a dc–dc converter, which transforms the battery voltage to a level that is optimized for the amplifier in accordance with the instantaneous output power level. The input signal power is sensed with an envelope detector, which controls the value of V_{DD} for the power amplifier stage. The relationship between the value of V_{DD} and the output power is shown in Figure 6.6. The value of V_{DD} is chosen to be somewhat larger than the amplitude of the radio frequency (RF) signal at the drain of the device. This avoids clipping of the large voltage excursions, which would cause unacceptable signal distortion. At the same time, V_{DD} is kept as small as possible to achieve optimal efficiency.

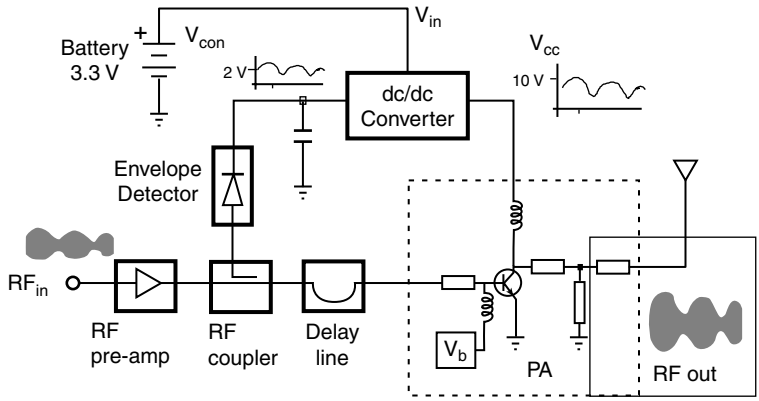


Figure 6.5. Block diagram of the dynamic supply voltage power amplifier.

It should be noted that the power amplifier remains in Class AB operation, and the overall output amplitude is governed primarily by the input signal amplitude, rather than by the value of V_{DD} (which would apply for an "envelope restoration" amplifier). Thus it is not crucial for overall system linearity that the V_{DD} value exactly replicate the input signal—only that it remain in a regime suitable to avoid clipping and increase efficiency.

Figure 6.7 shows the measured efficiency of the combined system as a function of output power. The value shown incorporates the inefficiency of the dc–dc converter as well as that of the amplifier. At the highest output power levels, the amplifier alone (without the dc–dc converter) is more efficient, since there is no loss associated with the voltage converter. At lower power levels, the system with the dc–dc converter is superior, because of its ability to tailor the power supply voltage optimally. By using the dc–dc converter with the power amplifier, a significant improvement of overall

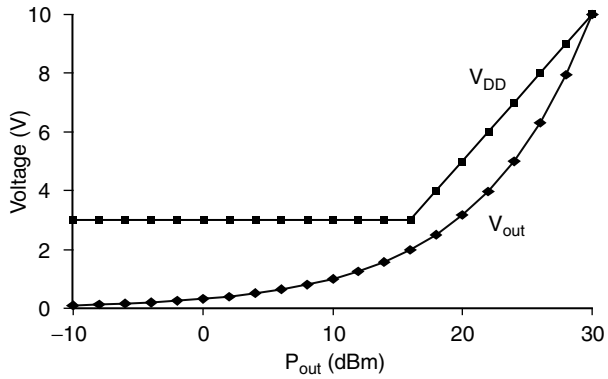


Figure 6.6. The dc–dc converter output voltage (V_{DD}) and calculated RF output voltage amplitude, as a function of output power.

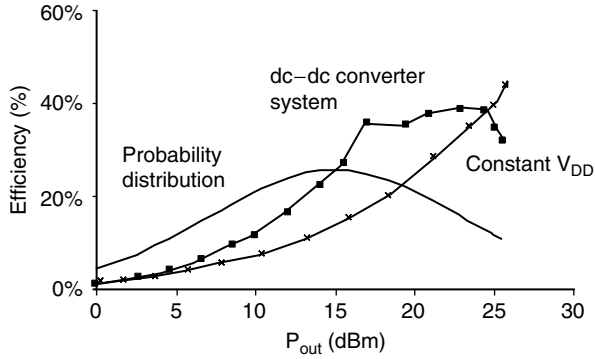


Figure 6.7. Measured efficiency of the amplifier operated at constant V_{DD} value and with dc–dc converter (to provide V_{DD} variable with input power). Also shown is a representative profile of power usage probability.

efficiency results—because the net energy consumption of the system is dominated by the low power regime, where the amplifier alone is highly inefficient. After averaging the energy consumption weighted by probability of usage, the amplifier overall efficiency was increased by 40%. Further increases should be possible, by increasing the ratio of the maximum to minimum voltage obtainable from the dc–dc converter, as discussed below. For example, by providing a power supply voltage lower than the battery voltage (as well as higher), a better average efficiency should result.

The observed improvement in efficiency is in good agreement with the result expected from simple analysis. For a Class A amplifier $\eta = \eta_{0A}(P/P_{max})$; for a Class B amplifier $\eta = \eta_{0B}(P/P_{max})^{1/2}$; and for the DSV amplifier, $\eta = \eta_{0D}$ (constant), for $P_m < P < P_{max}$, while $\eta = \eta_{0D}(P/P_{max})^{1/2}$ for $P > P_m$. Here η is the amplifier efficiency, η_0 is the maximum efficiency for the Class A, B and DSV amplifiers (achieved at the limiting power P_{max}), and P_m is the minimum power at which the supply voltage can still be effectively controlled in the DSV amplifier. The overall efficiency, averaged over the conditions of usage, is given by

$$\langle \eta \rangle = \frac{\int P_p(P)\,dP}{\int P_p(P)/\eta(P)\,dP}. \tag{6.1}$$

Here $p(P)$ is the probability that the system will have an output power P. The average efficiency depends on the characteristics of the signal. In many present applications, the average power is very much lower than P_{max}. If the average power is also much lower than P_m, then the improvement in efficiency becomes approximately $(P_{max}/P_m)^{0.5} \approx V_{max}/V_{min}$, where V_{max} and V_{min} are the maximum and minimum values of power supply voltage that can be provided by the converter. This result illustrates the importance of achieving a large V_{max}/V_{min} ratio.

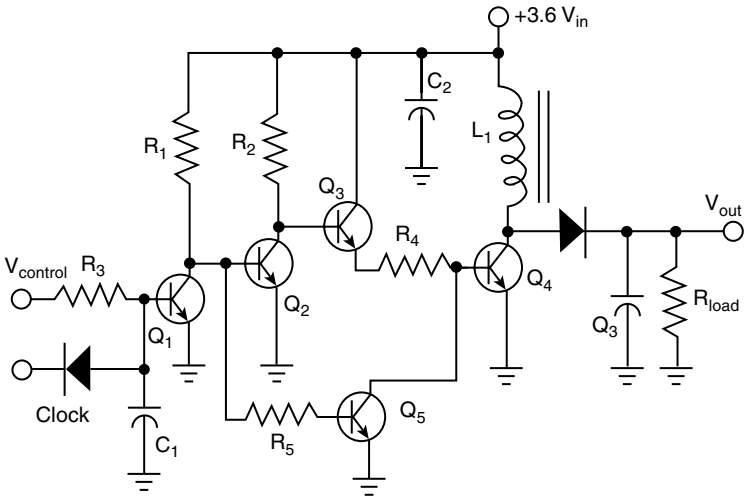


Figure 6.8. Circuit schematic of the dc–dc converter.

To enable a changing voltage supply with output power, we implemented dc–dc converters of small size, in a technology (GaAs HBT) that can be integrated monolithically with the power amplifier itself [5]. The circuit schematic for the dc–dc converter is shown in Figure 6.8. A boost topology is used, providing an output voltage in the range 3–10 V, for an input voltage of 3.3 V. The converter employs a power HBT, capable of handling up to 1 A of current. The inductor, Si Schottky rectifier, and output capacitor are external elements. The circuit incorporates a pulse-width modulator in order to allow a dc input control voltage to regulate the output voltage.

The dc–dc converter employs a high switching frequency (10–20 MHz). Typical waveforms in cellular handsets have envelope variations in the 50 KHz to 2 MHz range, according to different standards. By operating at a switching frequency of 10 MHz or above, several advantages are obtained. The output filter components may be reduced in value and size: inductors may be implemented with relatively few turns, thus reducing skin effect and dc power loss, and capacitors may be simple ceramic surface mount devices, easily located on the power circuit layout. A second benefit is that the dynamic response of the power supply has greater bandwidth. A switching frequency of 10 MHz allows for transient response time less than 1 μm. A third advantage is that the electromagnetic interference sent back on the input line (which could interfere with other circuitry powered from the same point) is much easier to remove by filtering.

The power HBT utilized in this converter exhibited a current gain of 60. Breakdown voltage exceeded 20 V. Figure 6.9 shows a microphotograph of the fabricated power switch HBT integrated circuit (IC). Emitter area for this device was over 5700 μm^2. The overall area of the converter IC was 750 μm by 900 μm. It is noteworthy that the converter was fabricated with the same process that is used to

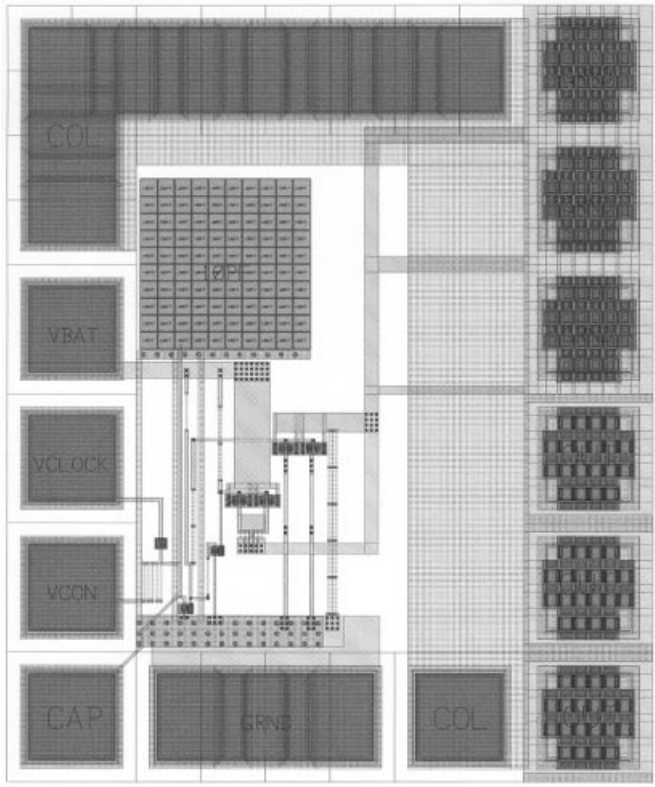


Figure 6.9. Layout of high speed dc–dc converter implemented with GaAs HBTs.

manufacture microwave (1–2 GHz) power amplifiers, which may facilitate the cointegration of these converters with microwave power circuits.

Measured efficiency of the integrated HBT-based converter was nearly flat over an output power range of 0.3–1.65 W, as shown in Figure 6.10. In the region to the left of the data point shown in the figure, the converter is off and no boost occurs.

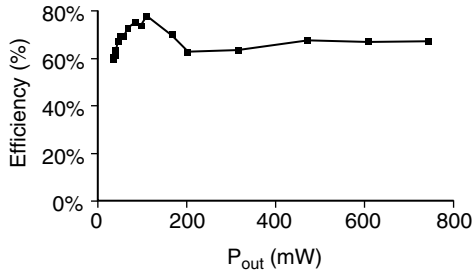


Figure 6.10. Measured efficiency of the dc–dc converter under various load conditions.

The highest efficiency measured was 80.3% at a load resistance of 20 Ω. Output ripple was less than 0.3 Vpp. Efficiency of the converter is limited principally by dissipation in the switching HBT, both on a transient and dc basis. We estimate that the switching loss, P_{0v}, due to simultaneous current and voltage overlap is 0.15 W at peak output power and 10 MHz clock frequency. Since, at full load, the converter was operated in the discontinuous mode, that is, the inductor current at switch turn-on was zero, overlap losses only occur during the switch turn-off. The dc (or resistive [4]) HBT loss is due to the large V_{CE} saturation voltage of the HBT and its series resistance. The HBT had a measured offset voltage, V_{OFFSET}, of 0.25 V, as a result of the difference in band structure between the AlGaAs emitter and the GaAs collector. The use of HBTs with wide bandgap collectors or other structural modifications could greatly reduce this value, as described elsewhere in this book. Series resistance in the power switch path due to the inductor, conductor traces, contact resistance, and the internal resistance of the HBT was estimated to be less than 0.4 Ω. The overall loss from these contributions is estimated to be 0.15 W for a duty cycle ($t_{ON} f$) of 40%. The small 0.3 V forward drop of the Schottky diode in the output path limits the loss of this device to only 50 mW. Input power for the PWM and driver was measured to be 30 mW. The overall power efficiency was thus estimated to be about 80%, which compares well with the experimentally observed value.

The DSV amplifier has significant benefit in increased efficiency. It also has a few potential problems for widespread application in wireless communications systems. One concern involves the ripple output of the 10 MHz converter. In order to increase response time, the output capacitor was reduced in size, increasing the output ripple to over 10%. However, it was found that very little conversion of V_{DD} amplitude variation (at 10 MHz) to gain variation resulted. This is evident in the spectral response of the amplifier output with a single sinusoidal tone input; there are sidebands in the output spaced at 10 MHz from the fundamental output, whose amplitude is lower by -60 dBc (an acceptably low value).

Another issue for the DSV amplifier concerns linearity. There is an inherent source of nonlinearity for this amplifier that is not present in conventional amplifiers, which must be kept within tolerable bounds. The new mechanism for nonlinearity arises because as the input power is varied and as the drain voltage of the RF output transistor correspondingly changes, in general the RF gain also varies [6]. The signal-dependent gain constitutes a mechanism for AM to AM conversion, which can cause intermodulation distortion, or exacerbate the adjacent channel power ratio (ACPR).

To avoid introducing distortion by the power supply time dependence, we explored two techniques. In one technique, in addition to varying the drain supply voltage V_{DD}, we also controlled the gate bias voltage V_{gg} in accordance with the signal level, in such a way to compensate for the variation in gain brought about by V_{DD}. This required implementing a circuit in which the gate bias voltage was generated with an operational amplifier, one of whose inputs was derived from the (signal-dependent) V_{DD}. This technique allowed improvement of the linearity to the level required for IS-95 CDMA signals; that is, the ACPR was measured to be better than -42 dBc.

An alternative, potentially very powerful, approach to overcome the inherent nonlinearity in DSV amplifiers is to use digital control of the dc–dc converter, coupled with digital predistortion of the amplifier input signal. In fact, the digital control can also be used to control V_{DD} to maximize the efficiency at the same time as it corrects the linearity problems. Application of DSP thus allows flexibility in the algorithm for power supply selection, ability to equalize the delay and the frequency response of the dc–dc converter, and ability to predistort the RF signal to overcome the associated AM–AM conversion [7, 8]. The resulting amplifier architecture, shown in Figure 6.11, is a significant step towards realization of a ''smart'' power amplifier, in which amplifier parameters are dynamically varied in accordance with the signal requirements to maximize performance.

The digital signal processor (DSP) computes an appropriate control voltage for the dc–dc converter according to the signal envelope, taking into account the dc and ac response of the converter. It also computes a predistorted input signal for both the I and the Q channel, to feed into the amplifier. The DSP computations are carried out at baseband. The I and Q signals must then be upconverted and amplified to provide the inputs to the power amplifier. In a cellular phone realization the computations can be performed in the same DSP that generates the conventional signal. In our experiments, the signals were precomputed using MATLAB in a conventional PC and then stored in the memory of arbitrary waveform generators (high speed digital-to-analog converters). They were subsequently read out and upconverted to feed into the power amplifier.

Figure 6.12(a) shows the power amplifier gain as a function of input power at various power supply voltages, for the uncorrected metal semiconductor field effect transistor (MESFET)-based power amplifier. No particular design optimization of the MESFET-based amplifier was done to minimize the gain variations. From these data, substantial changes in gain as a function of output power could be inferred, leading to objectionable AM–AM conversion. The DSP predistortion function was

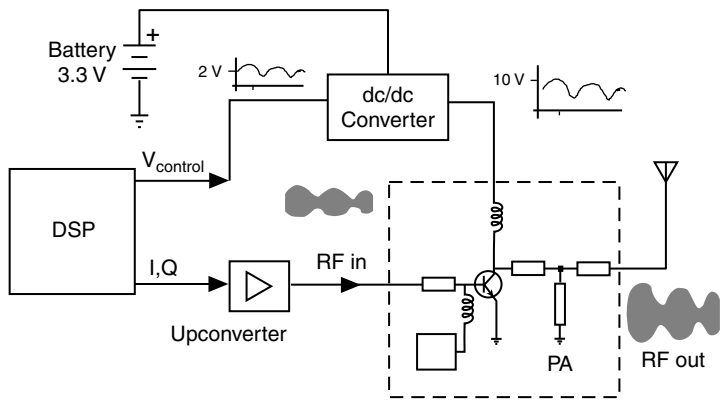


Figure 6.11. Amplifier architecture using a digital processor for dynamic supply voltage control and equalization, as well as input signal predistortion.

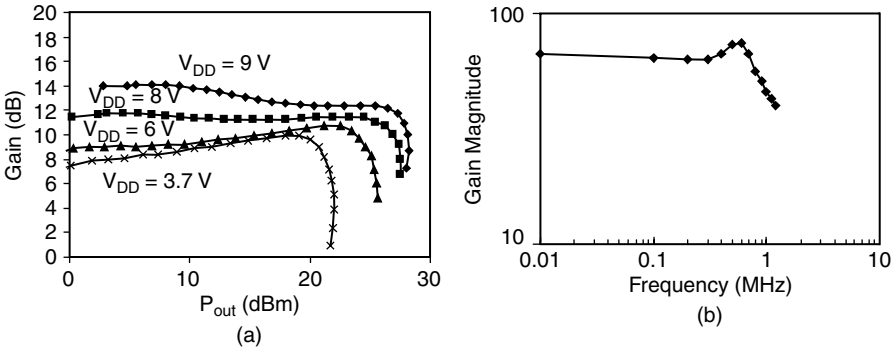


Figure 6.12. (a) Measured variation of the power amplifier gain with V_{DD}; (b) measured frequency response of the dc–dc converter.

computed to compensate for this variation (as well as for the corresponding phase variation). The frequency response of the dc–dc converter is shown in Figure 6.12(b). The equalization employed in the DSP was computed to compensate for this response (together with the nonlinear dc response and the delay of the dc–dc converter).

With the use of the DSP, the output frequency spectrum for an IS-95 CDMA input signal was considerably improved. A representative output spectrum is shown in Figure 6.13 (together with the spectrum obtained without predistortion for comparison). An improvement of 8 dB in ACPR was observed. The value of the ACPR with predistortion is -44 dBc (which exceeds the IS-95 minimum specification of -42 dBc) at the largest output power (and is better at lower output power). The linearization by DSP allows increasing the output power by about 4 dBm (and thus improving efficiency) while staying within the specifications of the IS-95 signals.

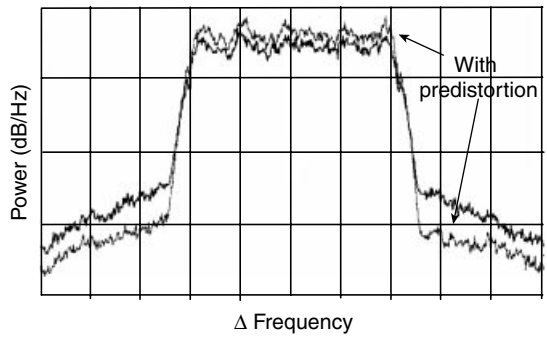


Figure 6.13. Measured output power spectra for an IS-95 CDMA signal with and without predistortion and equalization (10 dB/div, 30 kHz resolution bandwidth, 3 MHz span). The corresponding ACPR values are -44dB and -36dB.

The digitally controlled DSV architecture has considerable promise for future development. It uses DSP control over amplifier input signal as well as power supply voltage. The system can flexibly implement a variety of algorithms for system optimization. Application of DSP to amplifier control is becoming increasingly cost effective [7]. This approach requires integrated design of the overall transmitter, however, since the DSP function and the power amplifier must be closely coupled.

6.4 SWITCHING-MODE AMPLIFIERS

The power dissipation within the output transistor can be minimized by operating it as a switch, that is, by ensuring zero current when the voltage is high, and developing near-zero voltage (limited typically by on-resistance) when the current is nonzero. Nominally, with ideal, lossless passive elements, all the power delivered by the power supply reaches the load, and the efficiency is 100%. At lower RF values, transistors can be operated efficiently as switches driven by square waveforms, leading to amplifiers that have measured efficiencies over 90% when their operating load line consists of the I and V axes of the I to V curves [9]. At higher microwave frequencies, however, the output capacitance and resistance of the transistor, when driven into saturation, limit the switch performance: microwave transistors are not good switches. Switched-mode amplifiers can still be implemented at microwave frequencies, but the designer needs to keep the switch limitations in mind. If the large signal output capacitance is known, it can be used as part of the output tuning circuit. Knowing the on-resistance allows the designer to predict the maximum obtainable efficiency. An important issue for microwave PA designers is the highest frequency at which a given device can operate efficiently. A rule of thumb is that for switched-mode operation (i.e., when output power is not sacrificed at the expense of efficiency), the device can operate at high efficiency at about one-third of the cutoff (small signal unity gain) frequency. More details are given in the next section, specifically for Classes E and F, for which an interesting conclusion can be reached about the degradation of efficiency as one operates the device above the optimal efficiency frequency. The efficiency is found to decrease slowly as frequency increases, degrading first to ''suboptimal'' switched-mode operation [10], and then into the familiar Class AB mode.

6.4.1 Class E and F Microwave Amplifiers

In this section, we describe briefly the main properties and experimental results obtained with Class E and F microwave amplifiers, ranging in frequency from 0.5 to 10 GHz. The differentiation between E and F classes can be made in several different ways. We choose to define them with respect to output harmonic termination: in Class E, all harmonics are presented with an open circuit (or high impedance), while in Class F all even harmonics are shorted and odd harmonics open at the output.

Equations governing the design of Class E amplifiers can be derived from an approximation based on high-Q output tuned circuits. These equations include

expressions for Z_{out}, the output impedance required for Class E operation; f_{opt}, the maximum frequency at which the device can operate in "optimal" class E mode; and η_d, the drain efficiency (ratio of RF output power to dc input power) [11]:

$$Z_{out} = \frac{0.28015}{\omega C} e^{j49.0524^\circ} \tag{6.2}$$

$$f_{opt} = \frac{I_{max}}{56.5\,CV_d} \tag{6.3}$$

$$\eta_d = \frac{1 + (\pi/2 + \omega CR)^2}{1 + \pi^2/4(1 + \pi\omega CR)^2} \tag{6.4}$$

In the above approximate formulas, C is the output capacitance of the device, L is the output inductance (usually due to the package), R is the on-resistance, ω is the operating (switching) frequency, I_{max} is the maximum current the device can handle, and V_d is the bias voltage. These formulas are derived from a high-Q approximation of the tuned output circuit, in which the current through the load is assumed to be purely sinusoidal. Even though this assumption is not strictly valid in many microwave amplifiers, it is a very useful starting point in the design. When designing a Class E amplifier at a microwave frequency, C and L need to be incorporated in the output circuit impedance Z_{out}, as well as in any harmonic tuning impedance. As an example, the approximate Class E circuit schematic with no on-resistance is shown in Figure 6.14(a); the hybrid implementation is shown in Figure 6.14(b). Here, the output circuit meets the Class E conditions at the fundamental and second harmonic, while it is assumed that the transistor has low or no gain at the higher harmonics. Transmission line l_2 is a quarter-wavelength long at the second harmonic so that an open is transformed to a short at plane AA'; l_1 along with L and C is designed to be also a quarter-wavelength effectively, to translate the short to an open at the transistor (switch) output. Lines l_1 to l_4 provide Z_{out} at the fundamental. However, it is commonly the case that a single-stub match is sufficient to provide Z_{out} at the fundamental while simultaneously providing a high enough impedance at the second harmonic, eliminating the need for an extra stub and reducing a portion of the losses associated with the transmission line sections.

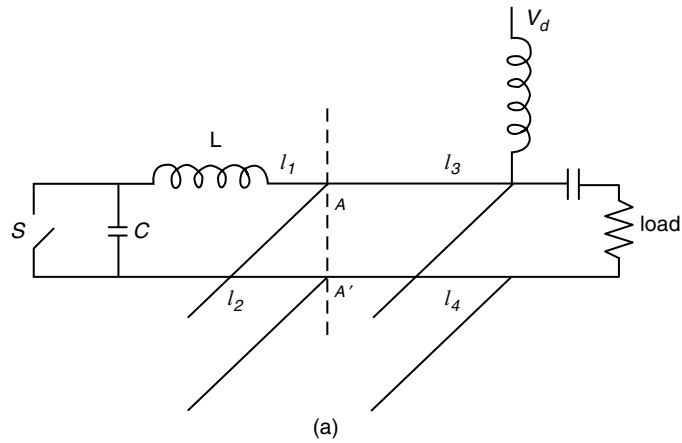
In Class F amplifiers, since the even harmonics are shorted and the odd open-circuited, the voltage waveform at the drain is ideally a square wave and in practice contains a limited number of odd harmonics that approximate a square wave. At the fundamental, the device should be matched for maximum saturated power transfer to the load, which can be shown to be the same as the maximum linear power match, $R_{opt} = 2V_d/I_{dss}$, where I_{dss} is the maximum allowable drain current.

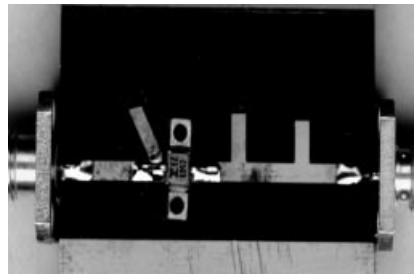
To date, several amplifiers have been implemented at microwave frequencies. They are described in detail in Refs. 11–17 and are summarized in this chapter. Experimental results are tabulated in Table 6.2, followed by a discussion of their salient features.

The first three Class E amplifiers were designed around a Siemens CLY5 MESFET, for which a modified Materka–Kacprzak nonlinear model was available.

TABLE 6.2. Summary of Experimental Switched Mode Microwave Amplifiers

f (GHz)	Device	P_{out} (mW)	G_{sat} (dB)	PAE (drain eff.)%	Reference	Comments
0.5	CLY5	550	15.3	80 (83)	12	
1.0	CLY5	940	14.7	73 (75)	12	
2.0	CLY5	530	9.1	56 (62)	12	$f_{opt} = 1.4$ GHz
2.5	FLK052	100		70	13	$V_d = 1$ V
4.5	FLK052	150	15	75 (80)	14	$V_d = 3$ V, gate biased on
4.5	FLK052	100	10	86 (95)	14	$V_d = 3$V, gate pinched off
5.0	FLK052	610	9.8	72 (81)	15	
5.0	FLK202	1800	7.6	60 (73)	15	Four times larger device
8.4	FLK052	685	7.4	60 (72)	16	Class F ($f_{opt} = 1.5$ GHz)
8.35	FLK202	1700	5.3	48 (69)	16	Four times larger device
10.0	AFM042	100	10	62 (74)	17	Active nonresonant antenna





(b)

Figure 6.14. (a) Approximate Class E power amplifier circuit in which the transistor is represented as an ideal switch, and transmission line sections are used for the output match and harmonic tuning. (b) Hybrid implementation with single stub.

Harmonic balance simulations at these low frequencies are in good agreement with the measurements: the simulated PAE is within 2%, and the simulated power within about 1 dB [15]. Details on the nonlinear simulations are given in Markovic et al. [18]. At the higher microwave frequencies, we found that better nonlinear models are needed for switched-mode operation, especially for higher saturation levels. The design in these cases is done starting from a linearized device model, and then the essential large signal parameters are de-embedded from measurements, giving the final design in the next iteration.

The harmonic balance simulations also predict time-domain waveforms that correspond to the definition of Class E operation, as shown in Figure 6.15(a). At 0.5 GHz, one can measure the drain waveform using a large valued resistor probe [11], but at higher frequencies this is not possible. In order to confirm the class of operation of the X-band amplifiers, a very high impedance photoconductive sampling probe was used, which enables almost noninvasive waveform measurements at any point in the circuit that can be contacted by the probe [19]. An example of such a measurement is shown in Figure 6.15(b).

It is clear that the X-band amplifiers operate in suboptimal switched mode. The Fujitsu FLK052 MESFETs are intended to operate in the Ku band with 30% PAE, so even the 5 GHz amplifiers using these devices operate beyond the optimal theoretical frequency for Class E operation. However, they still have enough gain at the harmonics to allow for waveshaping. In the lower frequency amplifiers using the CLY5 device, the optimal frequency for Class E operation is 1.4 GHz. It can be seen from Table 6.2 that the 2 GHz amplifier has considerably lower power and efficiency, due to the fact that a higher peak drain current is required than the device can provide.

In Mader et al. [15], Class E, F, and saturated A(AB) amplifiers are experimentally compared at 0.5 GHz. The conclusions are: (1) AB and F have essentially the same saturated output power, with Class F having 15% higher efficiency; (2)

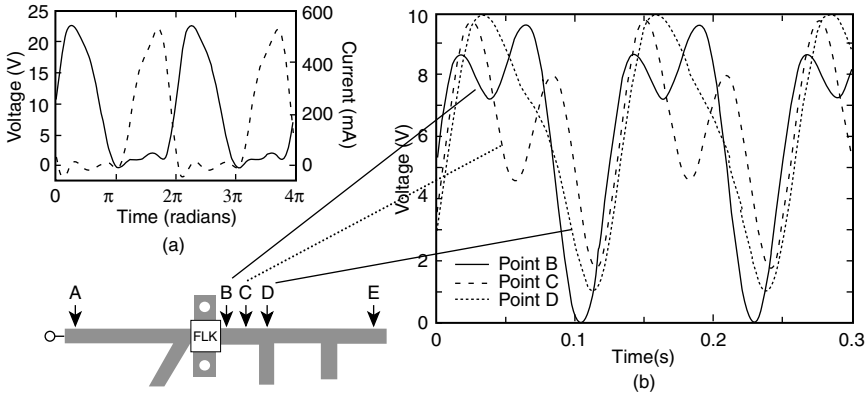


Figure 6.15. (a) Simulated Class E waveforms for the 0.5 GHz amplifier using a modified Materka–Kacprzak device model and harmonic balance show salient features of the Class E mode. (b) Measured Class F waveforms at three points at the output of an X-band amplifier using a photoconductive sampling probe.

Class E has the highest efficiency; (3) the gain of the Class E amplifier compresses at a lower input power level than the Class F gain (since the second harmonic short in the Class F amplifier flattens the switch voltage waveform, reducing the peak stress on the device); (4) for a given high efficiency, the Class F amplifier produces more power; and (5) for the same maximum output power, the third-order intermodulation products are 10 dB lower for Class F than for Class E, while the extrapolated intercept point occurs at the same power level.

If greater power is needed than available from a given device, power combining of several amplifiers is usually the solution. Some interesting conclusions can be made about types of power combining appropriate under different conditions. One can accomplish power combining at the chip level (increasing the gate periphery); by using circuit combiners; by using spatial combining; or with any combination of the three. As seen in Table 6.2, two amplifiers of different power levels were demonstrated at both 5 and 8.4 GHz, one using a device with four times larger gate periphery than the other in each case. At 5 GHz, the two amplifiers were both designed to operate in Class E mode, while at the X-band, one was Class E and the other was Class F (which corresponded to the design that gives for each the highest efficiency and power of which they were capable).

At 5 GHz, although the larger device delivers a three times higher output power, it requires five times the input power to operate in Class E mode. The on-chip power-combining efficiency is about 65% [11], while a four-element spatial combiner with the smaller device yielded a combining efficiency of 84%.

The measured frequency and power sweeps of the two X-band amplifiers are shown in Figure 6.16. In these plots, overall efficiency, defined as $P_{\text{out}}/(P_{\text{dc}} + P_{\text{in}})$, is plotted, since it was felt that this was a better indicator of low power dissipation than the conventional PAE. The chip-level combining efficiency in this case is 89%, but the bandwidth is much narrower for the larger device. The larger device yields a $2.5\times$ higher output power, but about $3.5\times$ higher heat power than the smaller device, with a 12% lower PAE and 2 dB lower gain. Even though on-chip combining is high, this approach is limited by propagation delays as the device size increases and by the reduced input impedance resulting from an increased number of gate fingers. From a more detailed combining efficiency comparison based on these two demonstrated amplifiers [16], the following general conclusions can be drawn: (1) in circuit combiners, a small number of larger devices is more efficient and takes up less real estate; (2) in spatial combiners, assuming the combining efficiency does not significantly drop with the number of devices combined, it is more efficient to use a large number of smaller devices; and (3) in applications that require an antenna array at the transmitter output, distributed amplification (spatial combining) is more efficient with respect to the total EIRP and thermal management as compared to circuit combiners.

As discussed below, integration of antennas with amplifiers, particularly switched-mode amplifiers, has several advantages. The antenna can be used effectively as the output tuned circuit, thereby eliminating the need for a matching network, which in turn reduces the losses and the volume taken up by the antenna and PA. This was first demonstrated by Mader et al. [15], where a second resonant slot antenna

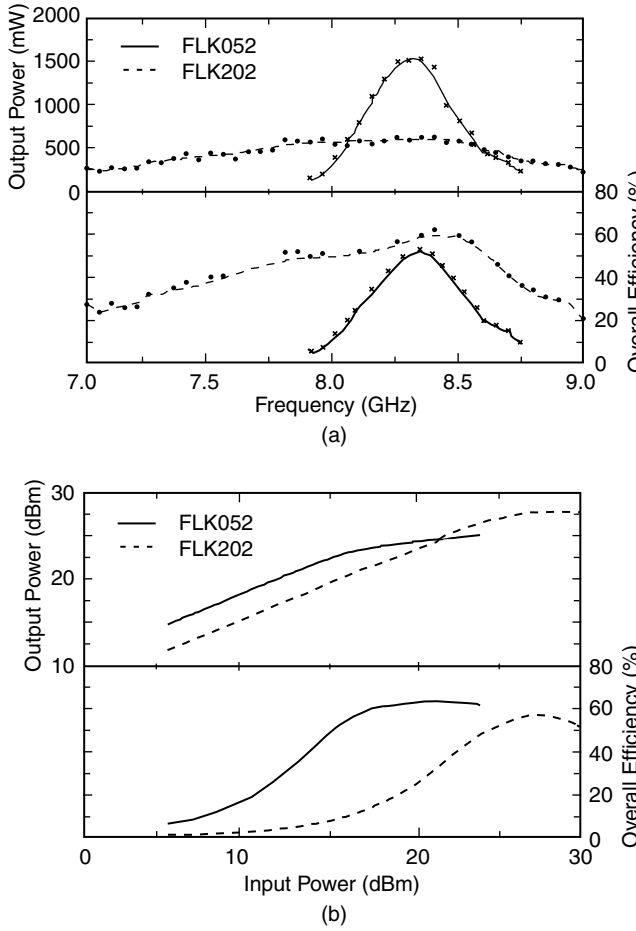


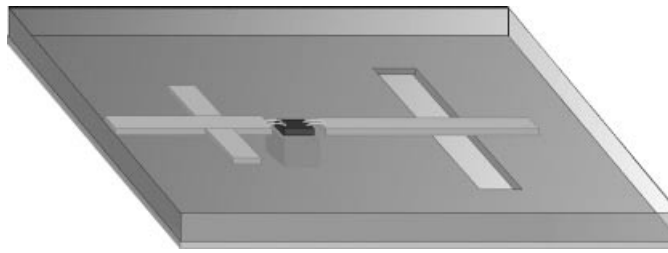
Figure 6.16. (a) Measured output power and overall efficiency versus frequency for two X-band switched-mode amplifiers. Input power levels were 20 and 26 dBm for the smaller and larger devices, respectively, and the drain and gate bias voltages in both cases were 7 and −0.9 V, respectively. (b) Measured output power and efficiency versus input power around 8.4 GHz for the two amplifiers under equal bias conditions.

provided the correct harmonic termination (high impedance at the second harmonic) to the Class E amplifier. This active antenna radiates 0.67 W with a drain efficiency of 80%, PAE of 71%, and a compressed gain of 9.3 dB at 5 GHz, which is almost identical to the microstrip circuit with no antenna. A four-element two-dimensional array of such active antennas all biased in parallel radiates 2.4 W with 74% drain efficiency estimated from the measured EIRP and radiation pattern. Based on the Class E and F X-band amplifiers described by Figure 6.16, several active patch antenna arrays were demonstrated with EIRPs up to 2.6 kW from 36 elements [13].

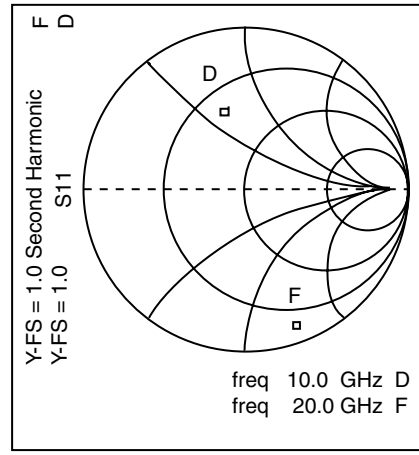
A 10-GHz Class E integrated antenna with an overall area of 0.4 free-space wavelengths squared is discussed in detail in Weiss and Popovic [17]. The antenna is a nonresonant microstrip-fed slot designed to have an impedance at the 10 GHz fundamental frequency equal to the Class E optimal load impedance given by Eq. (6.1), and a large capacitive impedance at the 20 GHz second harmonic. As seen in Table 6.2, this active antenna had a record drain efficiency of 74% and a PAE of 65% at 10 GHz while sacrificing only 1 dB of the manufacturer specified maximum output power of 21 dBm. A sketch of this active antenna and the passive antenna impedance at 10 and 20 GHz is shown in Figure 6.17.

6.4.2 Future Trends of Switched-Mode Power Amplifiers

The switched-mode circuit approach has also been applied at microwave frequencies to oscillators, frequency multipliers, and dc–dc power converters with switching rates in the gigahertz range. The oscillator [20] was based on the 5 GHz Class E



(a)



(b)

Figure 6.17. (a) Sketch of 10 GHz Class E active antenna with chip device, and (b) fundamental and second harmonic impedance of passive antenna designed to act as the optimal Class E load.

amplifier with added feedback for optimal conversion efficiency (equal in theory to the amplifier PAE) and exhibited a maximum conversion efficiency of 59% (with 300 mW power) and a maximum power of 600 mW (with 48% conversion efficiency). Several multipliers with conversion gain were demonstrated by designing the output circuit to be a Class E match at the second harmonic. For example, 5.2 dB conversion gain with 30% PAE and 330 mW of power was produced at 5 GHz with a 100 mW, 2.5 GHz input signal. It was found using photoconductive sampling [19] that a substantial harmonic power was reflected back at the input of this circuit, pointing to harmonic tuning at both input and output for improved efficiency and conversion gain.

An interesting direct application of a Class E amplifier is the dc–ac conversion stage of a dc–dc switching power converter [21], which is followed by a rectifier (ac–dc) stage. The converter switching speed was 4.5 GHz, and the overall dc–dc demonstrated conversion efficiency was 64%. This switching rate is orders of magnitude higher than other existing high speed converters. The advantages of this feature are a completely planar (low-volume) structure amenable to monolithic integration, the absence of magnetic components, and excellent dc to dc isolation provided by electromagnetic (capacitive) coupling between the dc–ac and ac–dc stages. The amplifier performance is given in Table 6.1 for two different gate biases. In this application, it is appropriate to bias the gate of the transistor in pinch-off, so that the device is off when no input switching signal is present. The diode rectifier efficiency in this circuit was 98% (defined as the ratio of the dc output power to the RF input power), and its conversion efficiency, which takes into account the reflected RF input power, is 83%. In this design, 6% is lost in total dc–dc conversion efficiency when integrating the Class E amplifier and diode rectifier.

There are a number of important and interesting issues that remain to be understood for switched-mode high efficiency microwave circuits: how to push the frequency into the millimeter-wave range (which will require devices with cutoff frequencies above 60 GHz); characterization of switched-mode linearity for different transmitter modulation schemes; efficient dynamic bias and drive control associated with signals with varying envelopes; use of devices with lower bias voltages; and combining strategies for high power transmitters.

6.5 LINC AMPLIFIER

While switching-mode amplifiers offer attractive improvements in efficiency, their output linearity is inherently reduced from that of Class A operation. There are several amplifier architectural approaches than can in principle achieve ideal linearity while providing the efficiency of switching-mode circuits. These are the out-phased (or LINC) approach and the bandpass Class S approach.

The out-phased power amplifier concept dates back to the early 1930s as an approach for the simultaneous realization of high efficiency *and* high linearity amplification [23]. It has been revived recently for wireless communication applications under the rubric of LINC (linear amplification with nonlinear components)

and many recent papers have developed the concept further [24, 25]. The LINC concept takes an envelope modulated bandpass waveform and resolves it into *two* out-phased constant envelope signals, which are applied to highly efficient—and highly nonlinear—power amplifiers, whose outputs are summed. The advantage of this approach is that each amplifier can be operated in a very efficient ''switching'' mode, and yet the final output can be highly linear—a key consideration for bandwidth efficient wireless communications. This is shown schematically in Figure 6.18. In theory, the efficiency of this scheme can approach 100% without any degradation of linearity.

The out-phased amplifier of Figure 6.18 takes a general baseband representation of an RF signal,

$$s(t) = a(t)e^{j\phi(t)},$$

where $a(t)$ is the instantaneous amplitude and $\phi(t)$ is the instantaneous phase of the input signal, and resolves it into two *constant envelope* vectors $s_1(t)$ and $s_2(t)$ through what is known as a signal component separator (SCS), such that

$$s_1(t) = s(t) + x_1(t),$$
$$s_2(t) = s(t) - x_1(t),$$

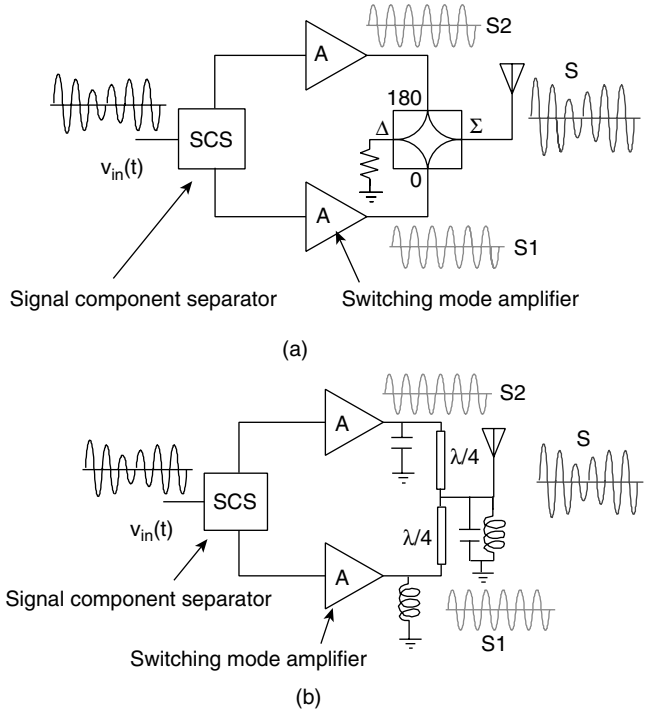


Figure 6.18. (a) Schematic diagram of LINC amplifier with hybrid output power combiner; (b) similar schematic of LINC with Chereix output power-combining technique.

and

$$x_1(t) = ja(t)\sqrt{\frac{a_{\max}^2}{|a^2(t)| - 1}},$$

where $a_{\max}$ is the maximum value of the signal a. These signals $s_1(t)$ and $s_2(t)$ can then be upconverted in the traditional manner and sent to highly efficient *constant envelope* power amplifiers, whose outputs are summed in a hybrid combiner. After summing, the $x_1(t)$ components of the signals cancel, and the desired $s(t)$ is recovered.

Despite its apparent attractiveness, the LINC approach has several disadvantages that have limited its applicability. The first is that the power is typically summed with a hybrid power-combining network, as shown in Figure 6.18(a). That portion of the power delivered to the hybrid that is not delivered to the antenna is dissipated in the 50 Ω terminating resistor. As a result, the amplifier only achieves its peak operating efficiency at maximum output power, and its efficiency decreases linearly as the output power decreases. This efficiency behavior is comparable to a Class A amplifier, which is known to have a very poor overall efficiency. Of course, the *peak* efficiency of this LINC approach is much higher than the Class A amplifier, but it would be desirable to do even better.

The power-combining approach of Figure 6.18(a) allows power to be wasted in the power-combining network. It is possible, however, to derive some benefit from the power dissipated in the 50 Ω load of Figure 6.18(a). By introducing a rectifier in the circuit, we have shown that significant power can be recycled, returning the ''waste'' power to the battery [26]. This can improve the LINC amplifier efficiency by 1.5 times over a range of output powers.

Another approach to improved power combining relies on replacing the hybrid combiner with the so-called Chireix power combiner, illustrated in Figure 6.18(b) [23]. In this case, two quarter-wave transmission line impedance transformers and a shunt susceptance are added in order to improve the efficiency. The analysis of the Chireix system is complicated, but it has been studied extensively by Raab [24] and the benefit is substantial. The added shunt susceptance (which is inductive in one branch and capacitive in the other branch) cancels out the varying susceptance seen by each amplifier at one particular output power.

A second problem associated with the LINC approach is that gain and phase mismatch lead to severe intermodulation and distortion [27]. Typical requirements for CDMA applications are on the order of 0.3 degree phase matching and 0.5 dB gain matching, a near impossibility in most practical cases. As a result, several compensation or calibration schemes have been proposed. These techniques have not achieved wide application due to their inherent complexity and lack of flexibility. For the future, the application of digital signal processing techniques to LINC calibration is promising.

6.6 DELTA–SIGMA AMPLIFIERS

An alternative technique to achieve high linearity with a switching-mode amplifier is the Class S technique. With a Class S amplifier, output signals with excellent

linearity can be produced by using an appropriate pulse-width modulation of the input switch control voltage, followed by filtering after the switching-mode amplifier. For example, Figure 6.19 illustrates the schematic structure and waveforms used in a representative Class S amplifier for audio frequencies. The output voltage is binary in nature (switched between output levels V_{DD} or 0), but the current is constrained to the desired low frequency output as a result of the output lowpass filter. Consequently, there is no power dissipated at the high switching frequency, only at the desired output frequency; thus, in principle, the Class S amplifier can have an efficiency of 100%. The application of this approach in the microwave region is complicated by the need for extremely high switching speed. We have investigated novel Class S amplifiers appropriate for microwave signals, in which the input control signals have a bandpass delta–sigma modulation, and the overall switching rate is not much greater than the frequency to be amplified [28].

The structure of a bandpass delta–sigma Class S amplifier is shown in Figure 6.19(b). The control voltage for the amplifier switch is a binary (digital) signal derived from the input signal through the use of a bandpass delta–sigma (BPDS) A/D converter, whose structure is shown schematically in Figure 6.20. Within an approximate, linearized analysis framework, the signal input to the BPDS system is found to be filtered by the passband of a resonant filter within the converter, while the quantization noise is spectrally shaped by a function that effectively eliminates it from the band of interest. The digital clock rate of the converter is typically four times the signal frequency. Practical implementations of BPDS converters operating in the microwave regime have recently been demonstrated [29].

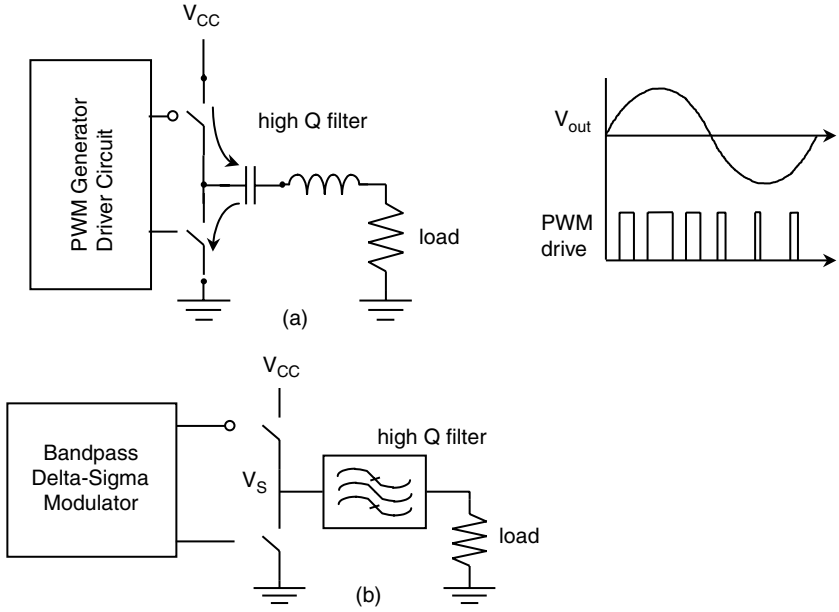


Figure 6.19. (a) Block diagram and representative waveforms in a conventional Class S amplifier for audio signals; (b) corresponding diagrams for the bandpass Class S amplifier for microwave signals.

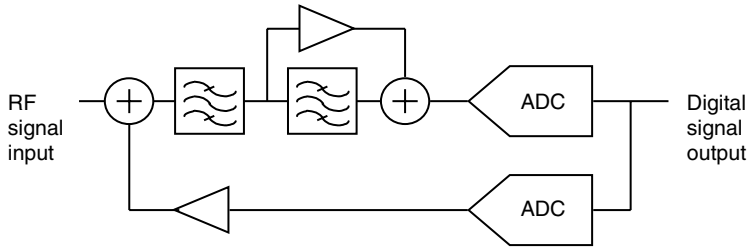


Figure 6.20. Block diagram of a bandpass delta–sigma modulator, and representative frequency response of the modulator for the signal and the quantization noise.

To demonstrate experimentally the operation of the bandpass delta–sigma Class S amplifier, we have constructed a ''scaled model amplifier'' operating at a low frequency (10 MHz) at which it is easy to obtain appropriate delta–sigma digital signals (from an appropriately programmed logic analyzer) and complementary switching FETs can be used. Figure 6.21 illustrates representative signals measured with this amplifier, in the frequency domain. Figure 6.22 contains the output spectrum recorded for a two tone input, illustrating the relatively low value of third order intermodulation products (-40 dB below the fundamental). The efficiency of the output amplifier under this condition was 51% (which is dramatically higher than attained for a Class AB amplifier at this level of linearity).

Amplifier efficiency is affected by voltage drop across the switches (R_{on}), dissipation during on–off transients, and discharge of input and output capacitances per cycle. To increase efficiency, it is important to use large switching devices for low R_{on}, to minimize the drain capacitance of the switching transistors, and to appropriately time the signals through the two switching transistors to avoid periods where both devices are simultaneously on. An additional factor is dissipation within the filter associated with signal components outside the frequency band of interest. To prevent current flow in the filter, the output impedance must be high at all frequencies other than the desired band. In conventional filters, the reflection coefficient is high everywhere outside the passband, but this is achieved by combinations of low impedance and high impedance. Insertion of extra series resonance elements can optimize the filter impedance profile.

Results suggest delta–sigma Class S power amplifiers are promising for high, efficiency, high linearity applications. It is envisioned that, in the future, DSP techniques can be used to generate the switch control voltages starting with baseband signals. Such an approach will allow considerable flexibility and software control over the output.

6.7 ACTIVE INTEGRATED ANTENNA APPROACH FOR POWER AMPLIFIERS

Most of this chapter has focused on increased transmitter efficiency by using various techniques to increase the performance of the power amplifier itself, which

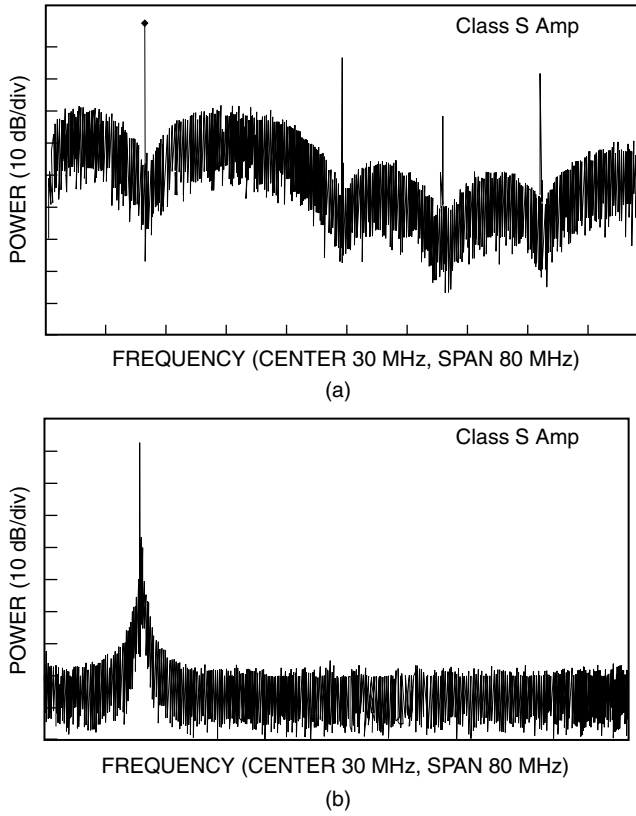


Figure 6.21. Representative measured spectra of a bandpass delta–sigma amplifier: (a) after the switching amplifier and (b) at the output.

consumes the majority of dc power in a typical handset. Another possibility for improving the efficiency of the *overall* transmitter is to focus on the insertion loss of the components between the power amplifier output and free space, including matching circuits for the antenna and power amplifier, isolator, harmonic filter, and antenna. The losses associated with each of these components will directly increase the required amplifier power output for a given radiated transmitter power. Therefore a logical technique for increasing the overall transmitter front-end efficiency is the elimination of as many components as possible between the PA output and the antenna without sacrificing system performance. The extreme of this technique, elimination of all components (except for possibly direct matching between the PA output and antenna), is known as the *active integrated antenna* (AIA) approach for power amplifiers. In order to keep transmitter performance from being sacrificed, it is necessary that the antenna take on new functionality in addition

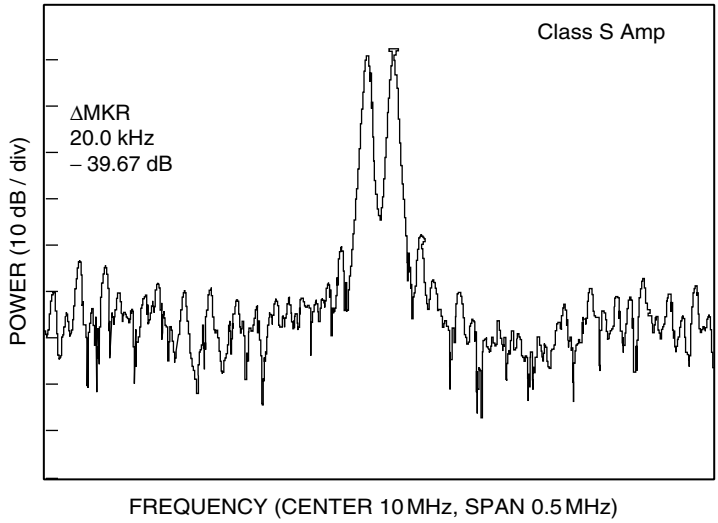


Figure 6.22. Output spectrum of bandpass delta–sigma amplifier, for input of two tones separated by 20 kHz.

to its original role as radiator. If designed properly, the resulting topology yields high transmitter efficiencies, compact size, and reduced component count. By using a planar antenna, the transmitter and antenna can be integrated onto a single printed circuit board (PCB). Therefore, the AIA approach delivers a transmitter front-end with maximum possible efficiency at minimum cost. More about the AIA approach, including more detailed design methodology and measurement techniques, is presented in Chapter 11.

Several classes of planar antennas have recently been developed for the AIA approach [30]. These antennas were designed with the goal of eliminating harmonic radiation and increasing the PAE of the transmitter through harmonic tuning. For high efficiency operation, the load impedance should provide a reactive termination at higher harmonics to reflect the power back to the MESFET with proper phase. Ideally, an open or short-circuit should be placed at the drain of the device for proper harmonic termination. However, at microwave frequencies, due to device parasitics, the higher harmonics are should be reflected back to the FET with appropriate phasing to resonate the drain-to-source capacitance. Therefore the output circuit should have a reflection coefficient of magnitude 1.0 at undesired harmonic frequencies and appropriate phase chosen to maximize efficiency. Traditionally, adding a short-circuited stub that is one-quarter wavelength at the fundamental frequency is done for this purpose, where the stub is added at the output (most often at the drain bias line) [31,32]. At low operating frequencies, this stub may be quite large. Alternatively, chip capacitors can be used for reflection of the second harmonic if they have a self-resonance near this frequency [33]. However, the AIA approach uses specifically designed antennas to achieve harmonic tuning.

In this section, the concept of AIA harmonic tuning is illustrated by two design examples. Specific emphasis is placed on the engineering of specific antennas to enhance the high efficiency performance of these front ends. Typically, when considering an antenna, the antenna designer is interested in the antenna characteristics only at the system operating frequency. However, when the antenna is used for harmonic tuning, antenna characteristics over a broad frequency span must be considered. These characteristics fall into two categories. The first characteristic, input impedance at operating frequency and higher harmonics, must be chosen to maximize amplifier performance. This means that the input impedance at the fundamental frequency should be close to the optimum output impedance of the amplifier for maximum PAE or P_{out}. Additionally, the antenna should present a reactive termination at undesired harmonics. As will be seen, this second constraint is contrary to practice in many planar antennas. The second of category characteristics covers the radiation properties of the antenna; these properties are chosen for optimal wireless performance and will depend on the application at hand.

Harmonic radiation is another important issue in wireless systems. Harmonic radiation is caused when the power amplifier generates significant harmonics, which may radiate through the antenna and consequently degrade system performance. One example of this is co-site interference, which may occur when a number of antennas operating at different frequencies are mounted in close proximity. Employing an additional filter to solve the resulting EMI problem is not only expensive but decreases the transmitter efficiency and may degrade the receiver noise figure. The harmonic tuning techniques presented in the following examples not only improve efficiency but also reduce unwanted harmonic radiation.

6.7.1 AIA with Modified Patch Antenna

One of the most commonly used planar antennas at microwave frequencies is the microstrip patch antenna. The patch antenna is a resonant-type antenna formed by a wide open-circuited microstrip conductor that is $\lambda/2$ in length at the first resonance. This causes standing waves in the cavity, which will radiate at the edges. Figure 6.23 shows the geometry of a standard rectangular patch antenna and the mode profile for the first three radiating modes: $TM_{1,0}$, $TM_{2,0}$, and $TM_{3,0}$. The operating frequency is chosen slightly away from resonance of the $TM_{1,0}$ mode to avoid overly large input impedance. When integrated with an amplifier, the second harmonic would therefore fall near the resonance of the $TM_{2,0}$ mode, where an appreciable radiation resistance exists. Therefore undesired harmonic radiation will effectively radiate from this structure and the structure in its current state is unsuitable for harmonic tuning.

Figure 6.24 shows the geometry of a rectangular patch antenna modified to eliminate the $TM_{2,0}$ mode. Referring to the mode profiles of the standard patch in Figure 6.23, the $TM_{2,0}$-mode electric field peaks at the center of the antenna. At this point, the electric field of the $TM_{1,0}$ mode is at a null. Therefore the $TM_{2,0}$ mode can be eliminated by properly modifying the boundary conditions along the centerline of the patch without affecting the $TM_{1,0}$ mode. This has been done by inserting a row of shorting pins along the centerline [34]. It was found that nine evenly placed pins

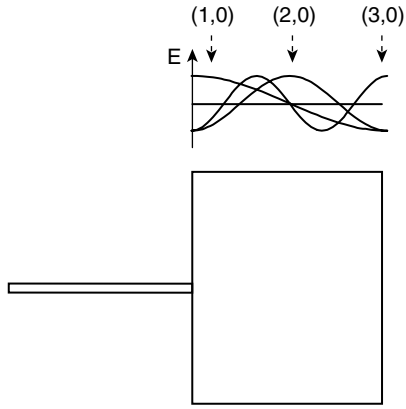


Figure 6.23. Geometry of standard microstrip patch antenna and corresponding mode profile of the first three modes.

effectively suppress the $TM_{2,0}$ mode without significantly perturbing the $TM_{1,0}$, as seen in the plot of the input impedance of the modified structure shown in Figure 6.25. From this, the resonance of the $TM_{2,0}$ mode has been eliminated, and the real part of the input impedance is almost zero where the $TM_{2,0}$ resonance should occur. Therefore this modified structure is suitable for harmonic tuning. Additionally, the characteristics of the $TM_{1,0}$ mode of the patch are virtually unchanged. This has been verified by measuring the normalized copolarization levels for both *E* and *H* planes, as shown in Figure 6.26. The cross-polarization was measured to be below -17 dB in all directions. The measured gain was 7.9 dB. These results are consistent with a conventional patch of the same dimensions operating near the $TM_{1,0}$ resonance.

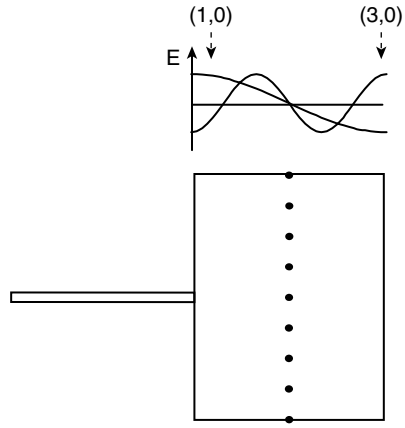


Figure 6.24. Geometry of patch antenna modified to eliminate the $TM_{2,0}$ radiation mode. Note line of vias down centerline of geometry.

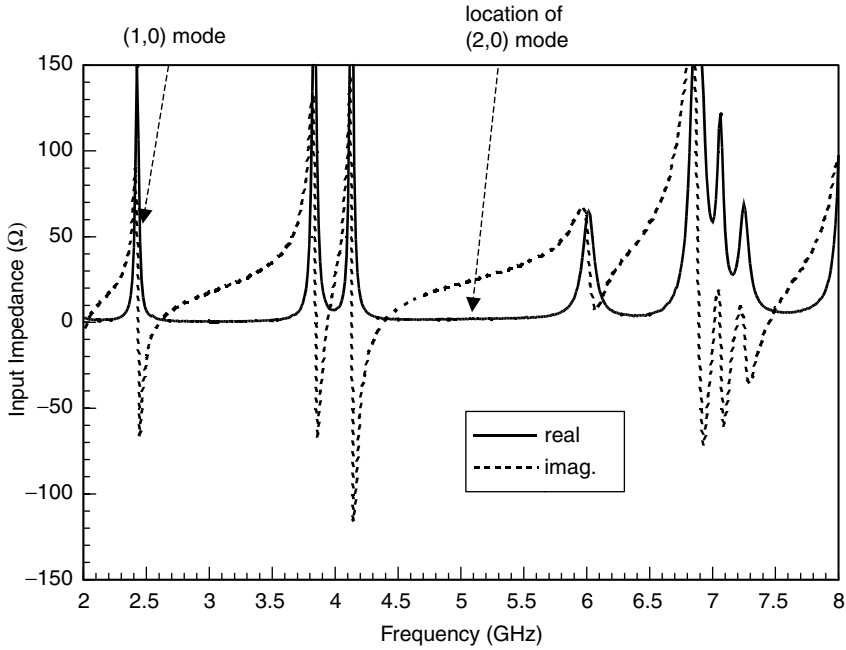


Figure 6.25. Input impedance of modified patch antenna. Elimination of $TM_{2,0}$ radiation mode is evident by negligible radiation resistance at twice the fundamental resonant frequency.

Next, two Class B AIA amplifiers were designed using a Fujitsu FLL351ME GaAs FET. The first reference amplifier used the standard patch antenna while the second used the modified patch with shorting pins for second harmonic suppression. The amplifiers are designed by incorporating the patch antenna *S* parameters directly into a circuit simulator (in this case, Hewlett-Packard Microwave Design System). The patch is modeled as a one-port network and data from a broad span (0.13–10 GHz) are incorporated to include effects of the first three harmonics. Then, harmonic balance is used to design the amplifier.

Both AIA amplifiers were then measured in an anechoic chamber using the Friis transmission equation to determine the radiated power. Note that the antenna gain has been calibrated out of the amplifier gain calculations for a fair comparison. It was found that the tuned AIA amplifier gave 0.5 dB higher output power when compared to the nontuned AIA with standard patch antenna, resulting in a 7% improvement in PAE [34]. This is illustrated in Figure 6.27, which shows measured PAE versus input power for both AIA modules. Maximum measured PAE is 55%. From this, we see that a very simple modification of the antenna can result in significant gains in efficiency.

6.7.2 AIA with Circular Segment Patch Antenna for Harmonic Tuning

One disadvantage to the previous structure is radiation of higher odd harmonics. The shorting pins will eliminate all even modes and therefore suppress even harmonic

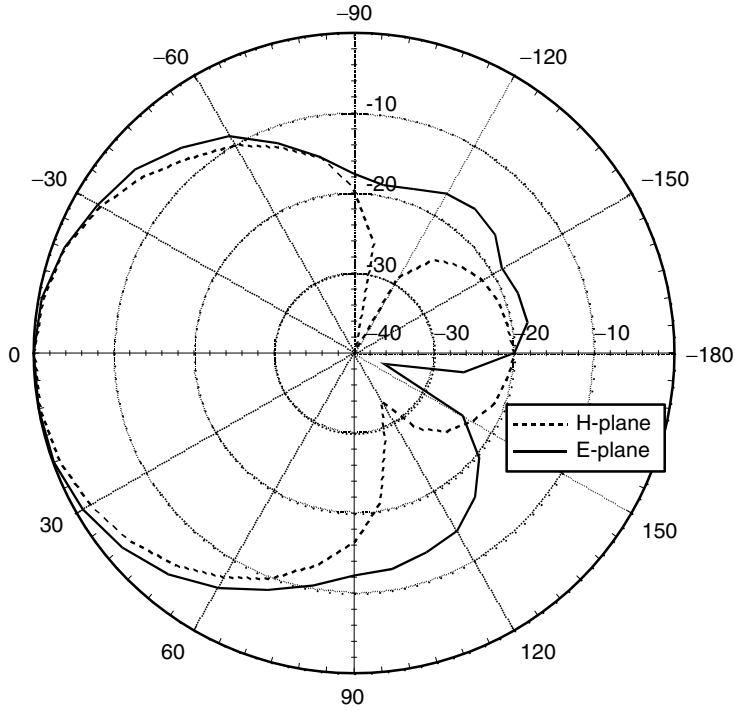


Figure 6.26. Radiation patterns of modified patch antenna.

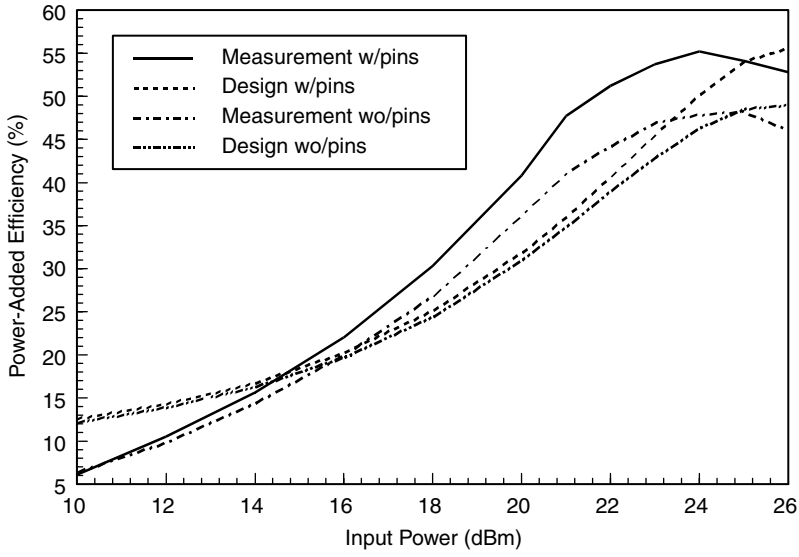


Figure 6.27. PAE of AIA PA using modified patch antenna.

radiation. However, odd modes remain unaffected, which can result in undesired radiation at these frequencies, depending on the nonlinearity of the amplifier. Designing an antenna where the higher radiation modes do not correspond to harmonic frequencies of the transmitter can eliminate this and is therefore highly desired.

Figure 6.28 shows a circular sector patch antenna used for this purpose along with its input impedance characteristics. For a circular geometry, the resonances of this antenna will be given by circular harmonics, which are not multiples of the fundamental frequency. By carefully optimizing the geometry, radiation at the second and third harmonics of the amplifier can be almost entirely eliminated. The optimized antenna consists of a circular patch of radius 740 mils. Note that the antenna is fabricated on a standard RT/Duroid of permittivity 2.33 and a thickness of 31 mils, as was the antenna of the previous example. A 120° sector of the antenna has been removed for optimal impedance. A microstrip feed is placed 30° from the edge of the voided sector. Referring to the input plot of the input impedance in Figure 6.28 resonances of the antenna structure occur where an appreciable resistance exists and the imaginary part of the input impedance crosses through zero. If the operating frequency is chosen slightly off the fundamental resonance, radiation resistance at second and third harmonics is negligible. Therefore harmonic radiation will be suppressed at these frequencies and harmonic power will be reflected back to the amplifier to add to the PAE of the transmitter [35]. It should also be noted that the circular geometry antennas feature a broad radiation pattern similar to the more

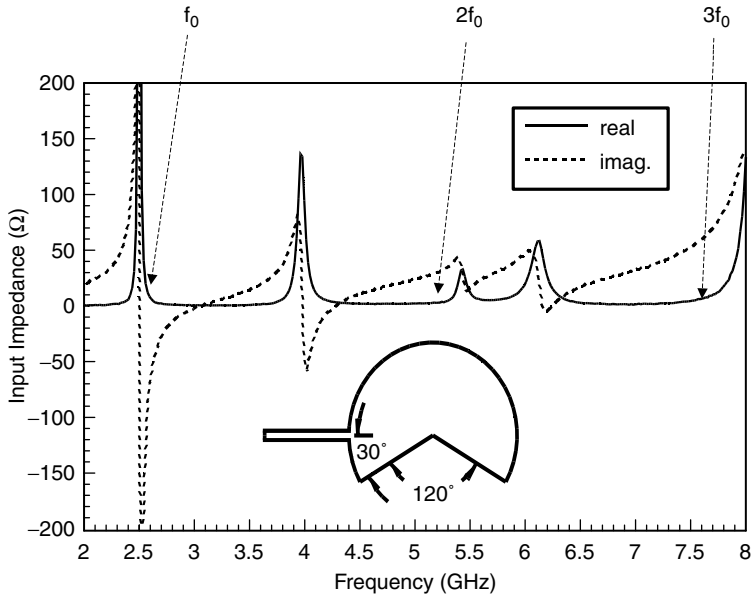


Figure 6.28. Input impedance and geometry of circular segment patch antenna.

standard rectangular patch antennas. The measured radiation characteristics of this particular antenna include 5.8 dB gain and -16 dB cross-polarization.

Using the same design procedure as with the patch antenna based AIA amplifier, one-port S parameters of the circular segment patch antenna are incorporated directly into a harmonic balance simulation. This time, a Class F AIA is designed for. A simple matching circuit between the device drain and antenna brings the antenna impedance to an optimal value at the fundamental and first two harmonics required for the Class F design. A microwave technology MT-8HP power GaAs FET biased at 10% I_{DSS} is used as the active device. Maximum measured PAE at 2.55 GHz is 63% at an output power of 24 dBm, as shown in Figure 6.29. We can also see that this hybrid-simulation method shows excellent agreement with measurements at both small-signal and large-signal operation. Additionally, this amplifier satisfies the IS95/98 ACPR linearity requirement for OQPSK (ACPR < -42 dBc at 1.25 MHz offset) even when operated at a high PAE of 43%.

Harmonic suppression has also been examined for this particular AIA power amplifier. This is observed by measuring the second and third harmonics frequency radiation. Since the shape of the pattern is typically different at harmonic frequencies, it is necessary to measure the entire pattern to get an idea of the harmonic suppression level. Measured E and H plane cuts of the circular segment patch antenna AIA amplifier are shown in Figure 6.30. The input power is set for maximum PAE. From the figure it is apparent that the second and third harmonics

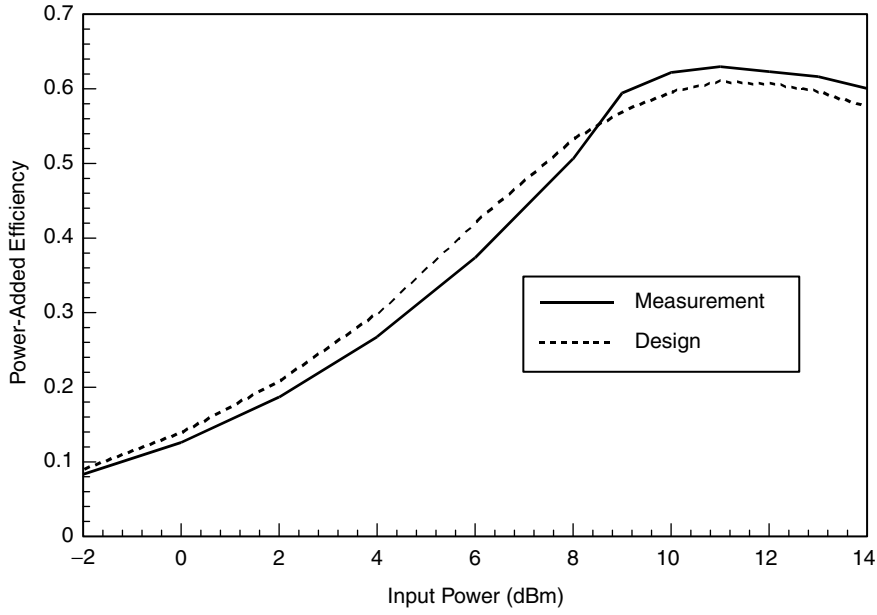


Figure 6.29. PAE of AIA PA using circular segment patch antenna at an operating frequency of 2.55 GHz.

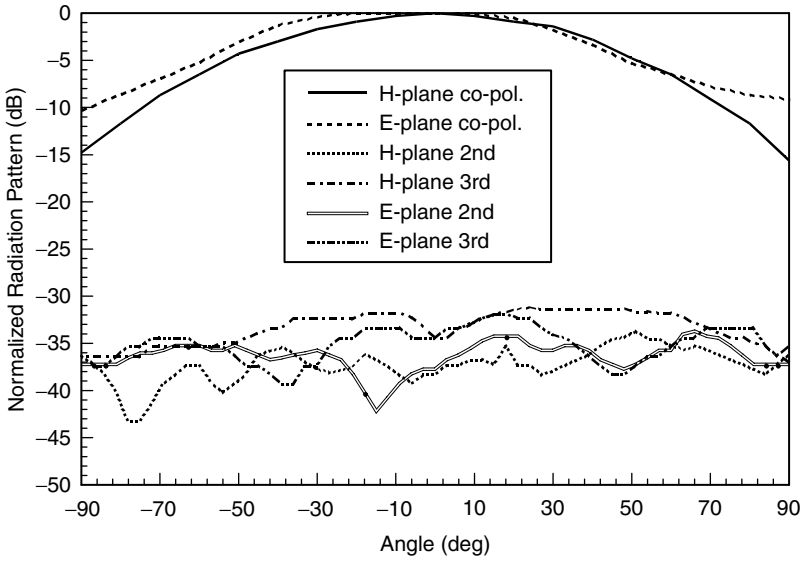


Figure 6.30. Normalized *E* and *H* plane copolarization radiation pattern of fundamental, second, and third harmonics for the Class F amplifier integrated with circular segment antenna.

are 33.8 dB and 31.4 dB below peak measured fundamental power, respectively, for all angles. Note that it would be necessary to integrate the power in the entire radiation pattern for each of the harmonics to determine the absolute harmonic suppression value. The output power has been calibrated using the receiving antenna gain and the Friis transmission formula at corresponding frequencies. Therefore the fundamental and harmonic power levels are referenced at the output of the antenna integrated with the amplifier.

6.7.3 Trends for Active Integrated Antennas

In both of the preceding examples, an antenna was developed that was nonradiating at one or more higher harmonics, the benefit being harmonic tuning via the reflected harmonic power and increased harmonic suppression. Therefore, in the AIA approach for power amplifiers, the job of the antenna designer is to develop an antenna with an input impedance characteristic that can be used as a tuned load at the operating and harmonic frequencies. Additionally, the antenna must maintain sufficient radiation characteristics for the application at hand. The result is a compact transmitter front end with extremely high realized efficiency.

In many cases, the AIA technique can be combined with other techniques presented in this book for even greater gains in efficiency or linearity. One example is an AIA integrated with a novel harmonic tuning structure. The novel tuning structure is based on a simple form of the periodic structure referred to as photonic

bandgap (PBG) in Chapter 8 [36,37]. The structure consists of periodically etched holes in the microstrip ground planes. At the resonant frequency of the period (spacing equal to one-half a guided wavelength), a deep stopband effect is observed in the insertion loss characteristic of the structure. In particular, this structure has been used to implement third harmonic tuning in a new version of the patch with pins AIA power amplifier presented in the first example of this section. Since the PBG structure is designed for third harmonic tuning, it is relatively compact at the fundamental frequency where the spacing would correspond to one-sixth of a guided wavelength. A total of four periods were used. It was found that the peak PAE for this AIA reached 61% at an input power of 14 dBm [33]. The operating frequency was 2.45 GHz. Additionally, the measured second and third harmonics are 33.8 dB and 31.4 dB below peak measured fundamental power, respectively, for all angles, indicating that third harmonic tuning has successfully been implemented. Therefore this technique is a simple and effective method of tuning additional harmonics that results in increased efficiency and low harmonic radiation levels.

6.8 SUMMARY AND OUTLOOK

The power amplifier is the most critical individual circuit for overall communications system efficiency. However, to obtain significant performance improvements, it is beneficial to optimize the power amplifier together with other parts of the wireless system. This chapter has focused on improvement approaches that have resulted from an interdisciplinary study carried out as a multiuniversity research program. The interdisciplinary themes critical for amplifier improvement include the following:

1. The amplifier efficiency is strongly related to system requirements for transmitted power variability and linearity (which in turn stem from the modulation format).
2. To optimize the system in an environment of large power variations (resulting from variations of transmission distance, fading, or envelope variations caused by the modulation), it is highly advantageous to implement a variable power supply voltage.
3. For even higher efficiency, switching-mode power amplifiers offer many benefits. The success of these circuits relies, however, on improving the high frequency characteristics of the transistors used, since the switching transitions must be very fast relative to the period of the transmitted signal.
4. Switching-mode amplifiers with high linearity require novel signal processing concepts. To achieve these, and for a variety of other benefits, it is worthwhile to employ digital signal processing.
5. Finally, to optimize the overall transmitter system, it is useful to integrate the design of the power amplifier and the transmitting antenna.

We expect that, in the future, the themes outlined here will be pursued further with continued success. There are other, related, themes that have not adequately

been described in this chapter. These themes include the improvement of amplifier linearity by specific architectures such as adaptive predistortion and Cartesian feedback and feed-forward. Such techniques can allow trading off linearity for efficiency in a bare amplifier, and subsequently recovering the linearity through the auxiliary circuitry. Another approach that is promising for the future is based on using switching-mode amplifiers together with low frequency amplifiers that control the envelope of the output signal (the envelope elimination and restoration technique, or Kahn amplifier approach). These advanced architectures, as well as the ones described in this chapter, rely on the continuing advance of transistor technology that will enable cost-effective manufacturing of increasingly complex and powerful signal processing circuits to accompany the basic output power transistors.

ACKNOWLEDGMENTS

The work reported here has been carried out under the sponsorship of the U.S. Office of the Secretary of Defense and the Army Research Office under the ''Low Power, Low Noise Electronics Technologies for Mobile Wireless Communication'' MURI, monitored by Dr. J. Harvey, Dr. R.Trew, Dr. J. Mink, and Dr. D. Woolard. The authors are grateful to them, and to their MURI team colleagues, for numerous discussions of the issues presented. This chapter describes the work of many graduate students and researchers. The authors are additionally grateful to G. Hanington, M. Iwamoto, C. Fallesen, A. Metzger, W. Deal, V. Radisic, J. Sevic, K. Gard, M. F. Chang, W. Hooper, and H. Finlay for numerous helpful conversations during the course of this work. HBTs that were used in the dc–dc converter were provided by HRL Laboratories and Conexant Systems Corporation.

REFERENCES

1. J. Sevic, ''Statistical characterization of RF power amplifier efficiency for IS-95 CDMA digital wireless communication systems,'' in *Proceedings 2nd Annual Wireless Communications Conference*, 1997.
2. T. Nojima, S. Nishiki, and K. Chiba, ''High efficiency transmitting power amplifiers for portable radio units,'' *IEICE Transactions*, Vol. E74, 1563 (1991).
3. C. Buoli, A. Abbiati, and D. Riccardi, ''Microwave power amplifier with envelope controlled drain power supply,'' in *25th European Microwave Conference*, 1995.
4. G. Hanington, P. F. Chen, V. Radisic, T. Itoh, and P. M. Asbeck, ''Microwave power amplifier efficiency improvement with a 10 MHz HBT dc–dc converter,'' *1998 IEEE MTT-S International Microwave Symposium Digest*, Vol. 2, 589–592 (1998).
5. G. Hanington, A. Metzger, P. Asbeck, and H. Finlay, ''Integrated dc–dc converter using GaAs HBT technology,'' to be published.
6. S. Bouthillette and A. Platzker, ''High efficiency L-band variable output power amplifiers for use in communication systems,'' *1996 IEEE MTT-S International Microwave Symposium Digest*, Vol. 2, 563–566 (1996).

7. F. Zavosh, M. Thomas, C. Thron, T. Hall, D. Artusi, D. Anderson, D. Ngo, and D. Runton, ''Digital predistortion techniques for RF power amplifiers with CDMA applications,'' *Microwave Journal*, Oct. 1999.
8. C. Fallesen, G. Hanington, and P. Asbeck, ''Improved linearity of a dynamic supply voltage power amplifier using digital predistortion,'' in *1999 IEEE Topical Workshop on Power Amplifiers for Wireless Communications*.
9. N. A. Sokal and A. D. Sokal, ''Class E—a new class of high-efficiency single-ended switched power amplifiers,'' *IEEE Journal of Solid State Circuits,* Vol. SC-10, 168–176 (June 1975).
10. F. H. Raab, ''Suboptimum operation of class-E power amplifiers,'' in *Proceedings RF Technology Exposition,* Santa Clara, CA, pp. 85–98, Feb. 1989.
11. T. B. Mader,'' Quasi-optical class E power amplifiers,'' Ph.D. dissertation, Department of Electrical and Computer Engineering, University of Colorado, Boulder, Aug. 1995.
12. T. B. Mader and Z. Popovic, ''The transmission-line high-efficiency class-E amplifier,'' *IEEE Microwave and Guided Wave Letters,* Vol. 5, No. 9, 290–292 (Sept. 1995).
13. E. Bryerton, ''High-efficiency switched-mode microwave circuits,'' Ph.D. dissertation, Department of Electrical and Computer Engineering, University of Colorado, Boulder, June 1999.
14. S. Djukic, D. Maksimovic, and Z. Popovic, ''A planar 4.5-GHz dc–dc power converter,'' *IEEE Transactions on Microwave Theory and Techniques*, Vol. 47, No. 8, 1457–1460 (Aug. 1999).
15. T. B. Mader, E. W. Bryerton, M. Markovic, M. Forman, and Z. Popovic, ''Switched-mode high-efficiency microwave power amplifiers in a free-space power-combiner array,'' *IEEE Transactions on Microwave Theory and Techniques*, Vol. 46, No. 10, 1391–1398 (Oct. 1998).
16. E. Bryerton, M. Weiss, and Z. Popovic, ''Efficiency of chip-level versus external power combining,'' *Special Issue on Low-Power/Low-Noise Circuits of the IEEE Transactions on Microwave Theory and Techniques*, 1482–1485 (July 1999).
17. M. Weiss and Z. Popovic, ''A 10-GHz high-efficiency active antenna,'' in *1999 IEEE IMS Symposium Digest*, Anaheim, CA, pp. 663–666, June 1999.
18. M. Markovic, A. Kain, and Z. Popovic, ''Nonlinear modeling of Class-E microwave power amplifiers,'' *Journal of the RF and Microwave Computer-Aided Engineering*, Vol. 9, Issue 2 (Mar./Apr. 1999).
19. M. Weiss, M. Crites, E. Bryerton, J. Whitacker, and Z. Popovic, ''Time domain optical sampling of nonlinear microwave amplifiers and multipliers,'' *IEEE Transactions on Microwave Theory and Techniques*, Vol. 47, No. 12, 2599–2604 (Dec. 1999).
20. E. Bryerton, W. Shiroma, and Z. Popovic, ''A 5-GHz high-efficiency class-E oscillator,'' *IEEE Microwave and Guided Wave Letters*, Vol. 8, No. 12, 441–443 (Dec. 1996).
21. S. Djukic, D. Maksimovic, and Z. Popovic, ''A planar 4.5-GHz dc to dc power converter,'' *Special Issue on Low-Power/Low-Noise Circuits of the IEEE Transactions on Microwave Theory and Techniques*, 1457–1460 (July 1999).
22. M. Weiss, Z. Popovic, and F. H. Raab, ''Linearity characteristics of X-band power amplifiers in high-efficiency transmitters'' (unpublished work).
23. H. Chireix, ''High power outphasing modulation,'' *Proceedings of the IRE*, Vol. 23, No. 11, 1370–1392 (Nov. 1935).

24. F. H. Raab, ''Efficiency of outphasing RF power-amplifier systems,'' *IEEE Transactions on Communications*, Vol. COM-33, No. 10, 1094–1099 (Oct. 1985).

25. F. Casadevall and J. Olmos, ''On the behavior of the LINC transmitter,'' in *Proceedings IEEE Vehicular Technology Conference*, pp. 29–34, 1990.

26. R. Langridge, T. Thornton, P. M. Asbeck, and L. E. Larson, ''A power re-use technique for improved efficiency of outphasing microwave power amplifiers,'' *IEEE Transactions on Microwave Theory and Techniques*, Vol. 47, 1467–1470 (Aug. 1999).

27. L. Sundstrom, ''The effect of quantization in a digital signal-component separator for LINC tranmsitters,'' *IEEE Transactions on Vehicular Technology*, Vol. 45, No. 2, 346–352 (May, 1996).

28. A. Jayaraman, P. F. Chen, G. Hanington, L. Larson, and P. Asbeck, ''Linear high-efficiency microwave power amplifiers using bandpass delta-sigma modulators,'' *IEEE Microwave and Guided Letters*, Vol. 8, No. 3, 121–123 (1998).

29. A. Jayaraman, P. Asbeck, K. Nary, S. Beccue, and K.-C. Wang, ''Bandpass delta–sigma modulator with 800 MHz center frequency,'' in *IEEE Gallium Arsenide Integrated Circuit Symposium, 19th Annual Technical Digest*, pp. 95–98, 1997.

30. V. Radisic, Y. Qian, and T. Itoh, ''Novel architectures for high-efficiency amplifiers for wireless applications,'' *IEEE Transactions on Microwave Theory and Techiques*, Vol. 46, 1901–1909 (Nov. 1998).

31. J. R. Lane, R. G. Freitag, H.-K. Hahn, J. E. Degenford, and M. Cohn, ''High-efficency 1-,2- and 4-W class-B FET power amplifiers,'' *IEEE Transactions on Microwave Theory and Techniques*, Vol. 34, 1318–1325 (Dec. 1986).

32. C. Duvanaud, S. Dietsche, G. Patanut, and J. Obregon, ''High-efficiency class F GaAs FET amplifier operating with very low bias voltage for use in mobile telephones at 1.75 GHz,'' *IEEE Microwave Guided Wave Letters*, Vol. 3, 268–270 (Aug. 1993).

33. E. Camargo and R. M. Steinberg, ''A compact high power amplifier for handy phones,'' *IEEE MTT-S International Microwave Digest*, 565–568 (June 1994).

34. V. Radisic, S. T. Chew, Y. Qian, and T. Itoh, ''High efficiency power amplifier integrated with antenna,'' *IEEE Microwave Guided Wave Letters*, Vol. 7, 39–41 (Feb. 1997).

35. V. Radisic, Y. Qian, and T. Itoh, ''Class F power amplifier integrated with circular sector microstrip antenna,'' *IEEE MTT-S International Microwave Digest*, Vol. 2, 687–690 (June 1997).

36. V. Radisic and T. Itoh, ''Active antenna power amplifier with PBG,'' in *28th European Microwave Conference Digest*, Vol. 1, Amsterdam, The Netherlands, pp. 156–160, Oct. 1998.

37. V. Radisic, Y. Qian, and T. Itoh, ''Broad-band power amplifier integrated with slot antenna and novel harmonic tuning structure,'' *IEEE MTT-S International Microwave Digest*, Vol. 3, 1895–1898 (June 1998).