

Single Channel 10A High Speed Low-Side MOSFET Driver

NCP81074A, NCP81074B

The NCP81074 is a single channel, low-side MOSFET driver. It is capable of providing large peak currents into capacitive loads. This driver can deliver a 7 A peak current at the Miller plateau region to help reduce the Miller effect during MOSFETs switching transitions. It exhibits a split output configuration allowing the user to control the turn on and turn off slew rates. This part is available in SOIC-8 and DFN8 2x2 mm packages.

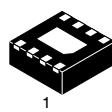
Features

- High Current Drive Capability ± 10 A
- TTL/CMOS Compatible Inputs Independent of Supply Voltage
- High Reverse Current Capability (10 A) Peak
- 4 ns Typical Rise and 4 ns Typical Fall Times with 1.8 nF Load
- Fast Propagation Delay Times of 15 ns with Input Falling and 15 ns with Input Rising
- Input Voltage Range from 4.5 V to 20 V
- Split Output Configuration
- Dual Input Design Offering Drive Flexibility
- These Devices are Pb-Free, Halogen Free/BFR Free and are RoHS Compliant

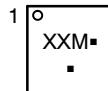
Applications

- Server Power
- Telecommunication, Datacenter Power
- Synchronous Rectifier
- Switch Mode Power Supply
- DC/DC Converter
- Power Factor Correction
- Motor Drive
- Renewable Energy, Solar Inverter

MARKING DIAGRAMS



DFN8
MN SUFFIX
CASE 506AA

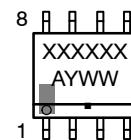


XX = Specific Device Code
M = Date Code
■ = Pb-Free Device

(Note: Microdot may be in either location)



SOIC-8
CASE 751



XXXXXX = Specific Device Code
A = Assembly Location
Y = Year
WW = Work Week
■ = Pb-Free Package

ORDERING INFORMATION

See detailed ordering, marking and shipping information on page 2 of this data sheet.

NCP81074A, NCP81074B

ORDERING INFORMATION

| Device | Temperature Range (°C) | Marking | Input Type | Package Type | Shipping [†] |
|----------------|------------------------|-----------|-------------------------|--------------------|-----------------------|
| NCP81074AMNTBG | -40 to +140 | CL | Fixed Digital Threshold | DFN8 2x2 (Pb-Free) | 3000 / Tape & Reel |
| NCP81074BMNTBG | -40 to +140 | CM | VDD Based Threshold | DFN8 2x2 (Pb-Free) | 3000 / Tape & Reel |
| NCP81074ADR2G | -40 to +140 | NCP81074A | Fixed Digital Threshold | SOIC-8 (Pb-Free) | 2500 / Tape & Reel |
| NCP81074BDR2G | -40 to +140 | NCP81074B | VDD Based Threshold | SOIC-8 (Pb-Free) | 2500 / Tape & Reel |

[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

BLOCK DIAGRAM

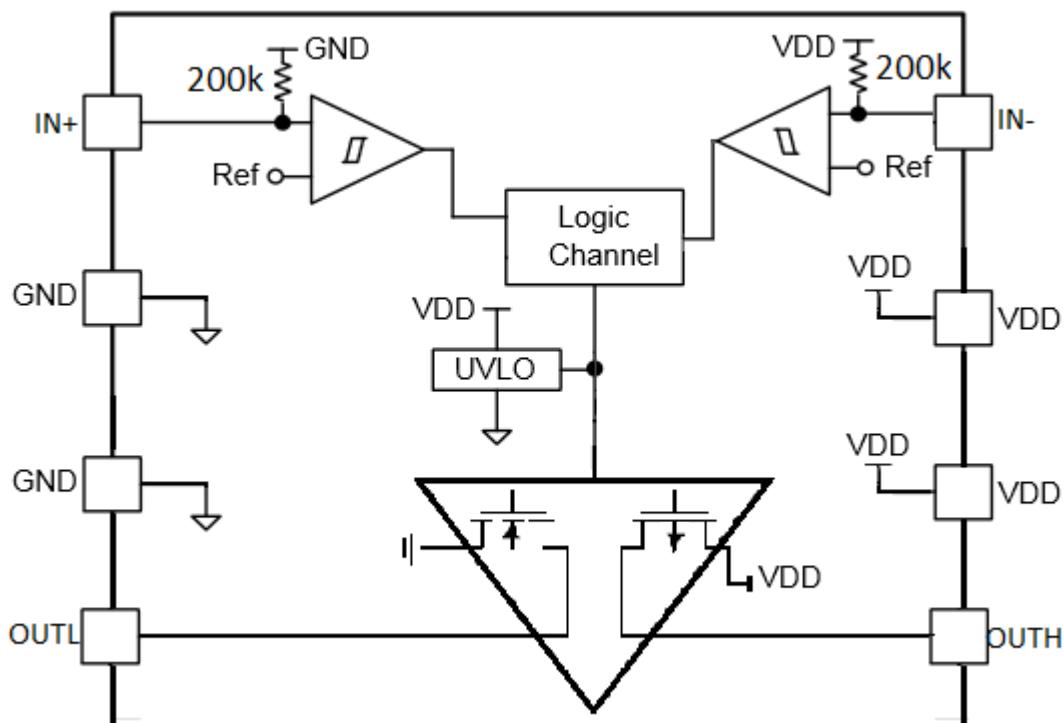


Figure 1. NCP81074 Block Diagram

NCP81074A, NCP81074B

PIN DESCRIPTION

| Pin No. | Symbol | Description |
|---------|--------|---|
| 1 | IN+ | Non-Inverting Input which has logic compatible threshold and hysteresis. If not used, this pin should be connected to VDD. It should not be left unconnected. |
| 2 | GND | Common ground. This ground should be connected very closely to the source of the power MOSFET. |
| 3 | GND | Common ground. This ground should be connected very closely to the source of the power MOSFET. |
| 4 | OUTL | Sink pin. Connect to Gate of MOSFET. |
| 5 | OUTH | Source Pin. Connect to Gate of MOSFET. |
| 6 | VDD | Power Supply Input Pin. |
| 7 | VDD | Power supply Input Pin. |
| 8 | IN- | Inverting Input which has logic compatible threshold and hysteresis. If not used, this pin should be connected to GND. It should not be left unconnected. |

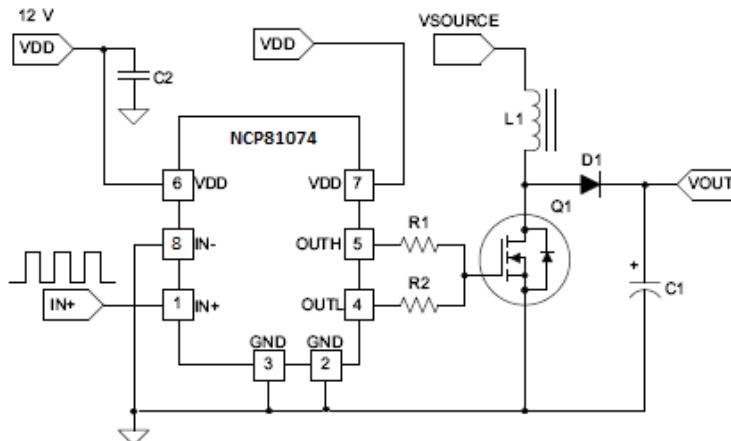


Figure 2. TYPICAL APPLICATION CIRCUIT

ABSOLUTE MAXIMUM RATINGS

| Parameter | | Value | | Unit |
|----------------------------------|--------------------------|-------|-----------|------|
| | | Min | Max | |
| Supply Voltage | VDD | -0.3 | 24 | V |
| Output Current (DC) | Iout_dc | 0.6 | | A |
| Reverse Current (Pulse<1 μs) | | | 10 | A |
| Output Current (Pulse<0.5 μs) | Iout_pulse | 10 | | A |
| Input Voltage | IN+, IN- | -6 | 24 | V |
| Output Voltages | OUTH, OUTL | -0.3 | VDD + 0.3 | V |
| Output Voltages (Pulse<0.5 μs) | OUTH, OUTL | -3.0 | VDD + 3.0 | V |
| Junction Operation Temperature | T _J | -40 | 150 | °C |
| Storage Temperature | T _{stg} | -65 | 160 | |
| Electrostatic Discharge | Human body model, HBM | 4000 | | V |
| | Charge device model, CDM | 1000 | | |
| OUT Latch-up Protection | | 500 | | mA |
| Moisture Sensitivity Level (MSL) | | MSL1 | | |

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

NCP81074A, NCP81074B

RECOMMENDED OPERATING CONDITIONS

| Parameter | Rating | Unit |
|----------------------------|-------------|------|
| VDD supply Voltage | 4.5 to 20 | V |
| IN+, IN- input voltages | -5 to 20 | V |
| Junction Temperature Range | -40 to +140 | °C |

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

Table 1. THERMAL INFORMATION

| Package | Theta JA (°C/W) | Theta JC (°C/W) |
|-----------|-----------------|-----------------|
| DFN-8 2x2 | 80.3 | 11.9 |
| SOIC-8 | 115 | 50 |

Table 2. ELECTRICAL CHARACTERISTICS (Note 1) (Typical values: V_{DD} = 12V, 1uF from VDD to GND, TA = TJ = -40°C to 140°C, typical at T_{AMB} = 25°C, unless otherwise specified)

| Parameter | SYMBOL | Test Conditions | MIN | TYP | MAX | Unit |
|--|-------------------------|---|----------|----------|----------|------|
| SUPPLY VOLTAGE | | | | | | |
| VDD Under Voltage Lockout (rising) | V _{CCR} | VDD rising | 3.7 | 3.9 | 4.1 | V |
| VDD Under Voltage Lockout (Falling) | V _{CCF} | VDD falling | 3.4 | 3.6 | 3.8 | V |
| VDD Under Voltage Lockout (hysteresis) | V _{CCH} | | | 300 | | mV |
| Operating Current (no switching) | I _{DD} | | | 1.2 | 2 | mA |
| VDD Under Voltage Lockout to Output Delay (Note 1) | | VDD rising | | 10 | | μs |
| INPUTS | | | | | | |
| NCP81074A High Threshold | V _{thH} | Input rising from logic low | 1.9 | 2.1 | 2.3 | V |
| NCP81074A Low Threshold | V _{thL} | Input falling from logic high | 1.1 | 1.3 | 1.5 | V |
| VIN_HYS | Input Signal Hysteresis | | | 0.8 | | V |
| NCP81074B High Threshold | V _{thH} | Input rising from logic low (VDD = 8 V to 12 V) | VDD -3.5 | VDD -3.1 | VDD -2.7 | V |
| NCP81074B Low Threshold | V _{thL} | Input falling from logic high (VDD = 8 V to 12 V) | GND +2.6 | GND +2.9 | GND +3.2 | V |
| IN- Pull-up Resistor | R _{in-} | | | 200 | | kΩ |
| IN+ Pull-Down Resistor | R _{in+} | | | 200 | | kΩ |
| OUTPUTS | | | | | | |
| Output Resistance High | R _{OH} | I _{OUT} = -10 mA | | 0.4 | 0.8 | Ω |
| Output Resistance Low | R _{OL} | I _{OUT} = +10 mA | | 0.4 | 0.8 | Ω |
| Peak Source Current ⁽²⁾ | I _{Source} | OUT = GND 200 ns Pulse | | 10 | | A |
| Miller Plateau Source Current ⁽²⁾ | I _{Source} | OUT = 5.0 V 200 ns Pulse | | 7 | | A |
| Peak Sink Current ⁽²⁾ | I _{Sink} | OUT = VDD 200 ns Pulse | | 10 | | A |
| Miller Plateau Sink Current ⁽²⁾ | I _{Sink} | OUT = 5.0 V 200 ns Pulse | | 7 | | A |
| SWITCHING CHARACTERISTICS | | | | | | |
| Propagation Delay Time Low to High, IN Rising (IN to OUT) (Note 2) | t _{d1} | C _{Load} = 1.8 nF | | 15 | 27 | ns |

NCP81074A, NCP81074B

Table 2. ELECTRICAL CHARACTERISTICS (Note 1) (Typical values: $V_{DD} = 12V$, $1\mu F$ from VDD to GND, $TA = TJ = -40^{\circ}C$ to $140^{\circ}C$, typical at $T_{AMB} = 25^{\circ}C$, unless otherwise specified)

| Parameter | Symbol | Test Conditions | MIN | TYP | MAX | Unit |
|---|----------|-----------------------------|-----|-----|-----|------|
| SWITCHING CHARACTERISTICS | | | | | | |
| Propagation Delay Time High to Low, IN Falling (IN to OUT) (Note 2) | t_{d2} | $C_{Load} = 1.8 \text{ nF}$ | | 15 | 27 | ns |
| Rise Time (Note 2) | t_r | $C_{Load} = 1.8 \text{ nF}$ | | 4 | 7 | ns |
| Fall Time (Note 2) | t_f | $C_{Load} = 1.8 \text{ nF}$ | | 4 | 7 | ns |

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

- All Limits are 100% tested at $T_{AMB} = 25^{\circ}C$ and guaranteed across temperature by design and statistical analysis.
- Guaranteed by characterization. *See timing Waveforms.

Table 3. LOGIC TRUTH TABLE

| IN+ | IN- | OUTH | OUTL | OUT (OUTH & OUTL CONNECTED TOGETHER) |
|-----|-----|--------|--------|--|
| L | L | HIGH-Z | L | L |
| L | H | HIGH-Z | L | L |
| H | L | H | HIGH-Z | H |
| H | H | HIGH-Z | L | L |

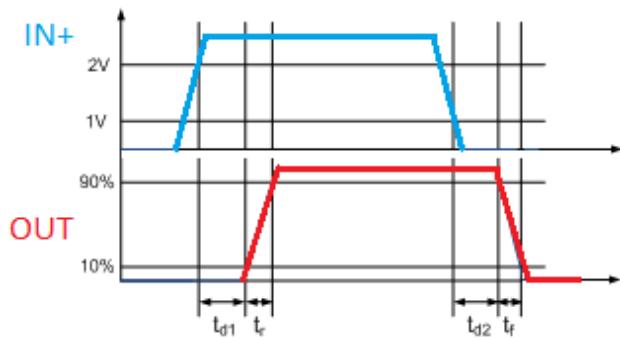


Figure 3. Non-inverting Input Driver Operation

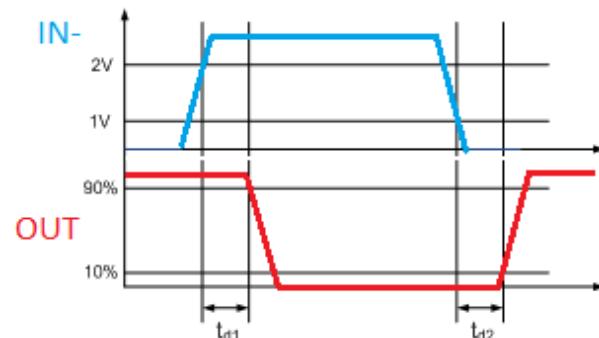


Figure 4. Inverting Input Driver Operation

NCP81074A, NCP81074B

TYPICAL CHARACTERISTICS

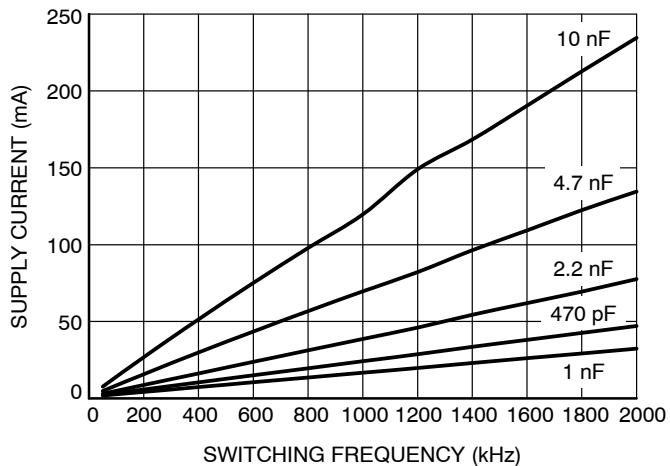


Figure 5. Supply Current vs. Switching Frequency, $V_{DD} = 12\text{ V}$

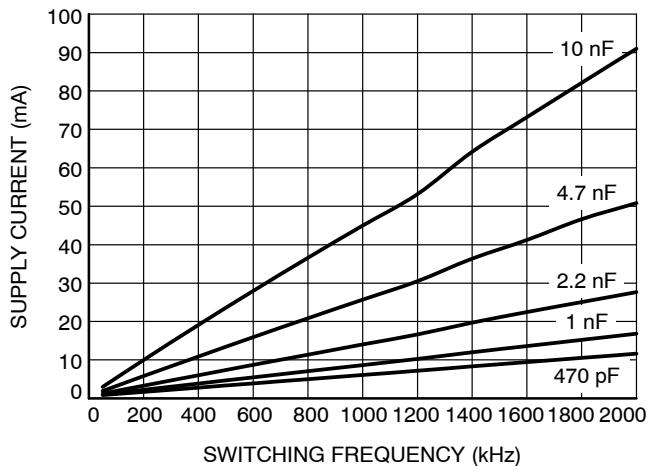
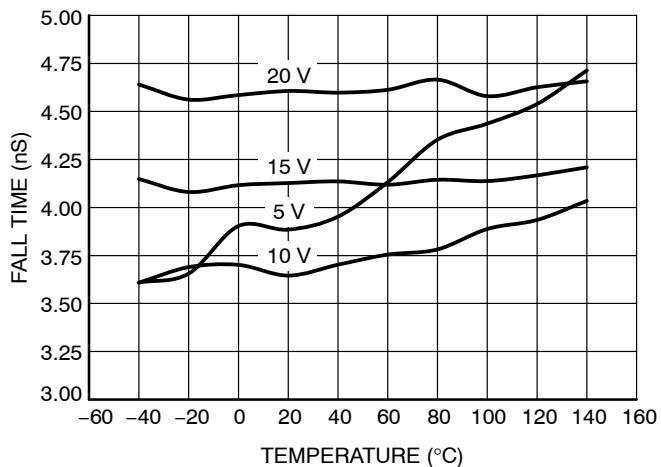
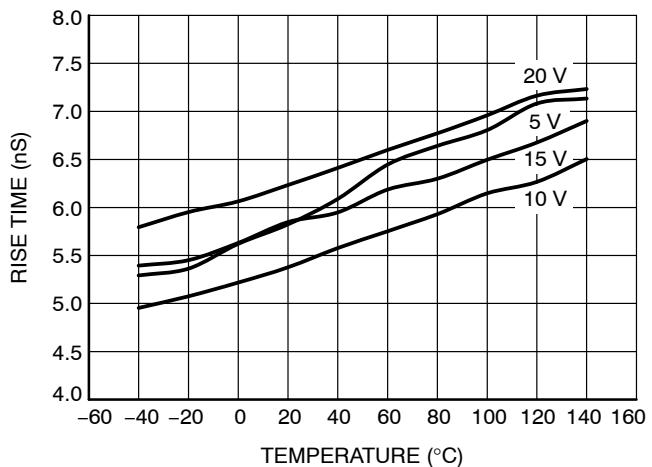


Figure 6. Supply Current vs. Switching Frequency, $V_{DD} = 4.5\text{ V}$



**Figure 7. Fall Time vs. Temperature
 $C_{LOAD} = 1.8\text{ nF}$**



**Figure 8. Rise Time vs. Temperature
 $C_{load} = 1.8\text{ nF}$**

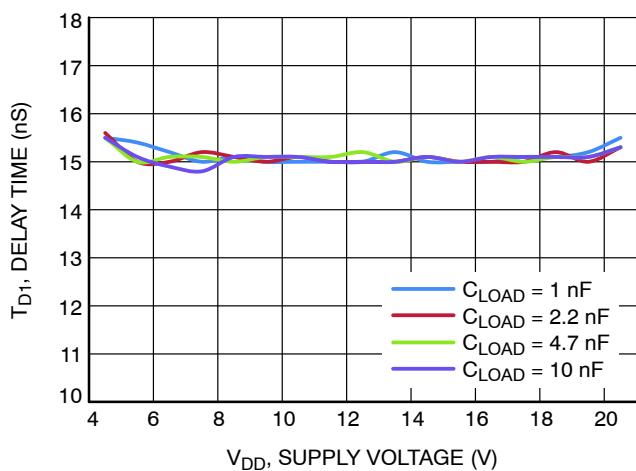


Figure 9. Propagation Delay T_{D1} vs. Supply Voltage

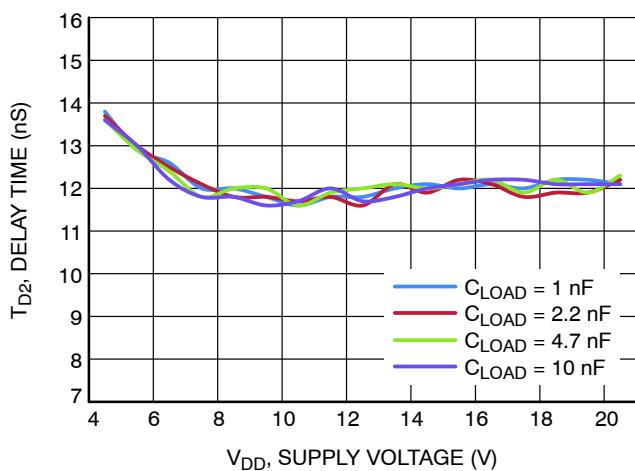


Figure 10. Propagation Delay T_{D2} vs. Supply Voltage

NCP81074A, NCP81074B

TYPICAL CHARACTERISTICS

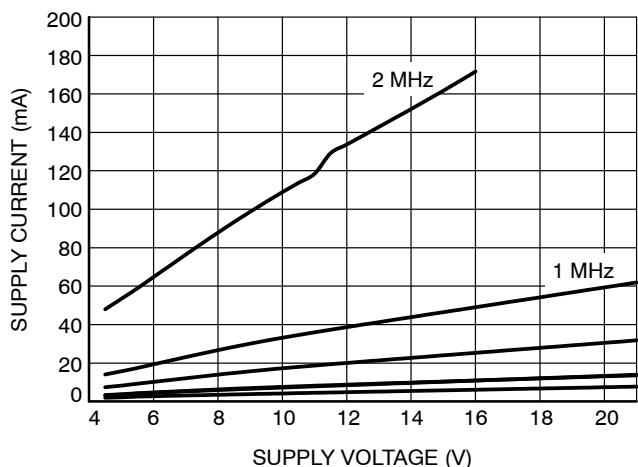


Figure 11. Supply Current vs. Supply Voltage
 $C_{LOAD} = 2.2 \text{ nF}$

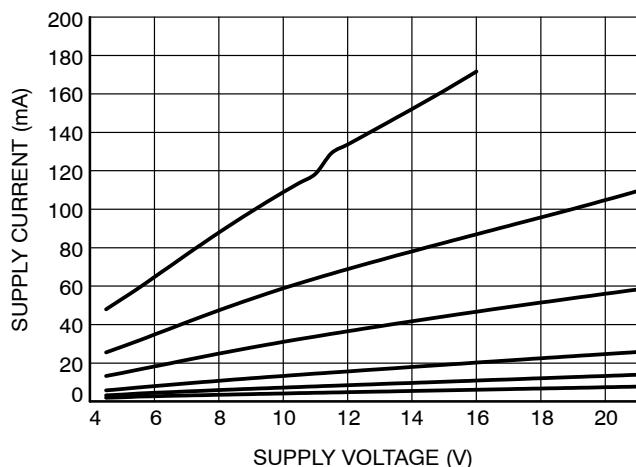


Figure 12. Supply Current vs. Supply Voltage
 $C_{LOAD} = 4.7 \text{ nF}$

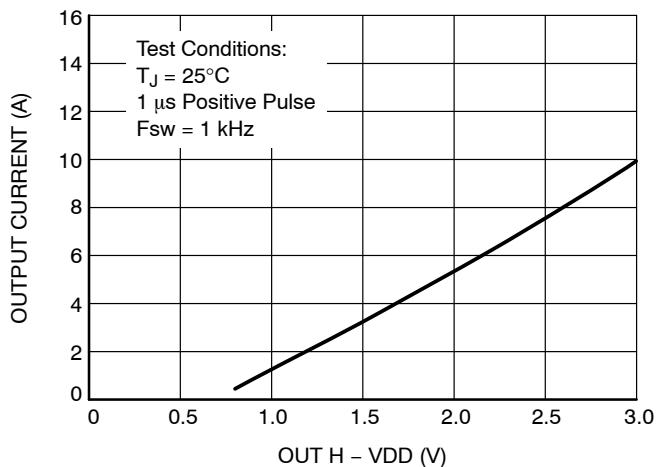


Figure 13. Reverse Current, $P_{\text{MOS}(\text{on})}$, $P_{\text{MOS}(\text{off})}$

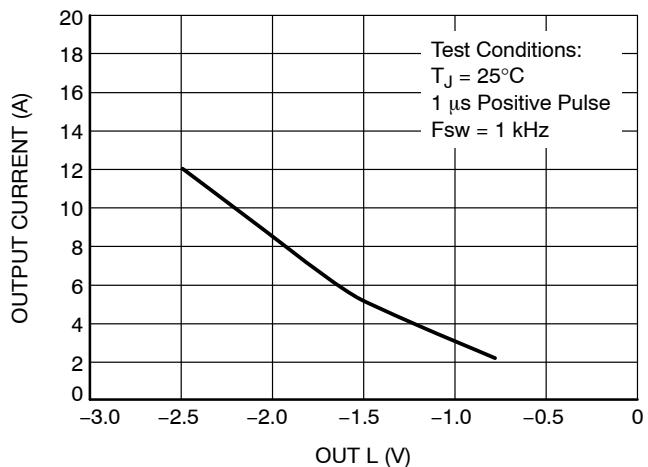


Figure 14. Reverse Current, $P_{\text{MOS}(\text{off})}$, $P_{\text{MOS}(\text{on})}$

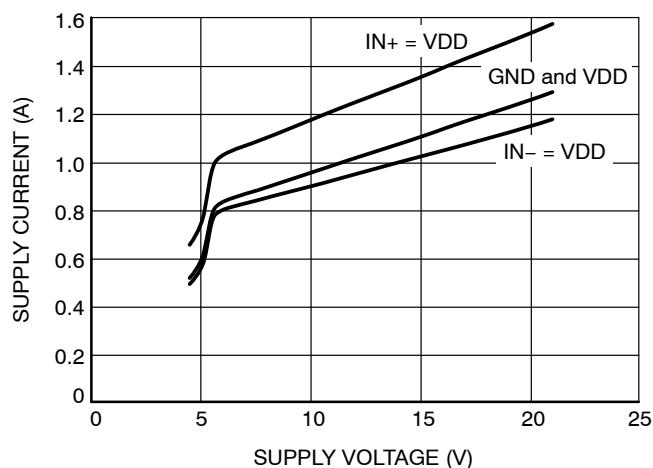
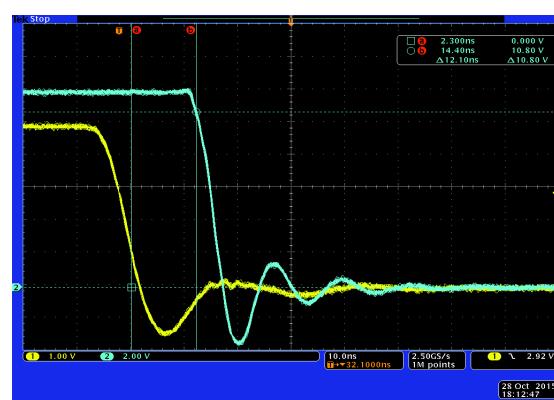
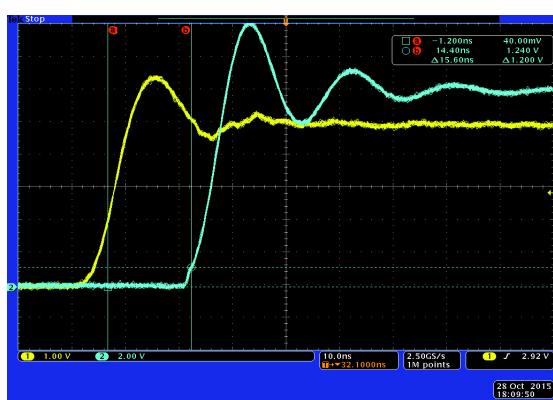
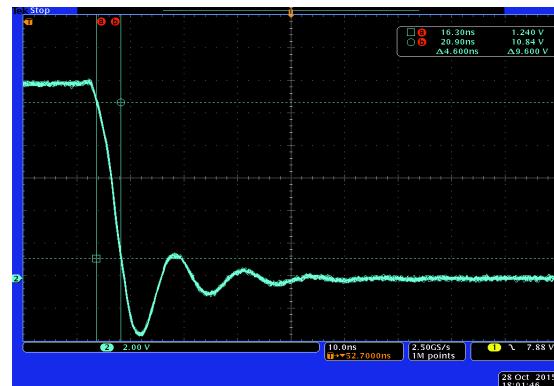
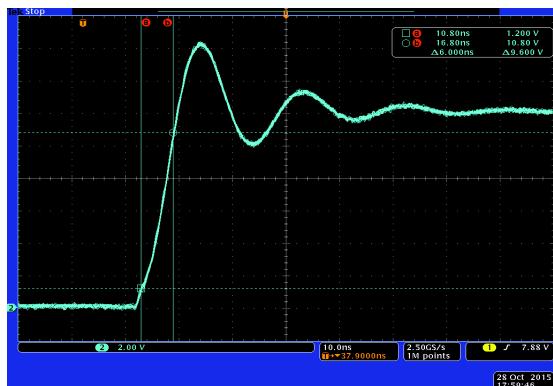


Figure 15. Supply Current vs. Supply Voltage

NCP81074A, NCP81074B

BENCH WAVEFORMS – NON-INVERTING INPUT



NCP81074A, NCP81074B

BENCH WAVEFORMS – INVERTING INPUT

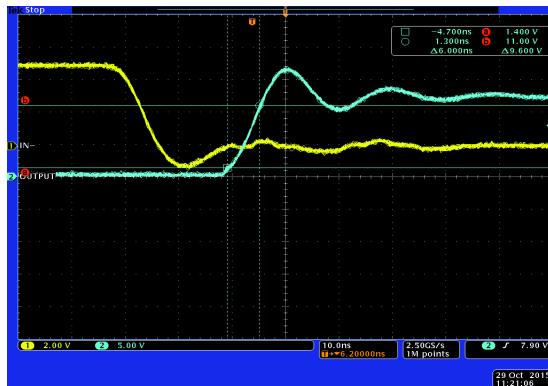


Figure 20. Rise Time with 1.8 nF Load

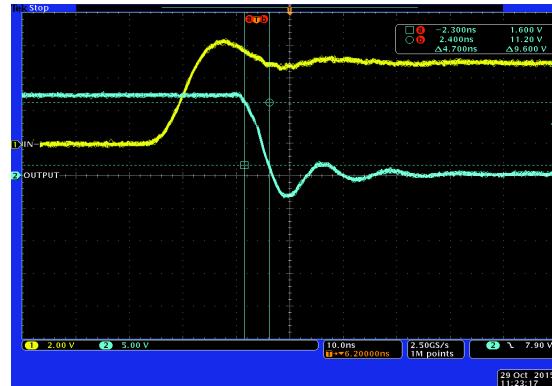


Figure 21. Fall Time with 1.8 nF Load

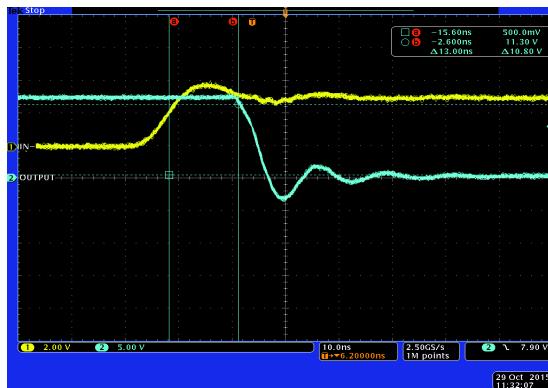


Figure 22. Propagation Delays with 1.8 nF Load

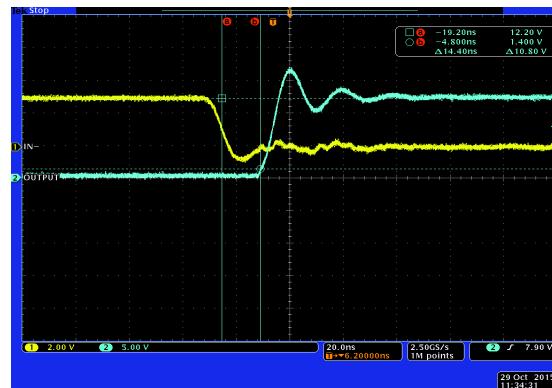


Figure 23. Propagation Delays with 1.8 nF Load

NCP81074A, NCP81074B

PCB LAYOUT RECOMMENDATION

Proper component placement is extremely important in high current, fast switching applications to provide appropriate device operation and design robustness. The NCP81074 gate driver exhibits a powerful output stage enabling large peak currents with fast rise and fall times. Eventhough the NCP81074 provides a split output configuration for slew rate control, a proper PCB layout is crucial to ensure maximum performance. The following circuit layout guidelines are strongly recommended when designing with the NCP81074.

- Place the driver close to the power MOSFET in order to have a low impedance path between the output pins and the gate. Keep the traces short and wide to minimize the parasitic inductance and accommodate for high peak currents.
- Place the decoupling capacitor close to the gate drive IC. Placing the VDD capacitor close to the pin and ground improves noise filtering. This capacitor supplies

high peak currents during the turn-on transition of the MOSFET. Using a low ESL chip capacitor is highly recommended.

- Keep a tight turn-on turn-off current loop paths to minimize parasitic inductance. High di/dt will induce voltage spikes on the output pin and the MOSFET gate. Parallel the source and return signals taking advantage of flux cancellation.
- Since the NCP81074 is a 2x2mm package driving high peak currents into capacitive loads, adding a shielding ground plane helps in power dissipation and noise blocking. The ground plane should not be a current carrying path to any of the current loops.
- Any unused pin, should be pulled to either rail depending on the functionality of the pin to avoid any malfunction on the output. Please refer to the pin description table for more information.

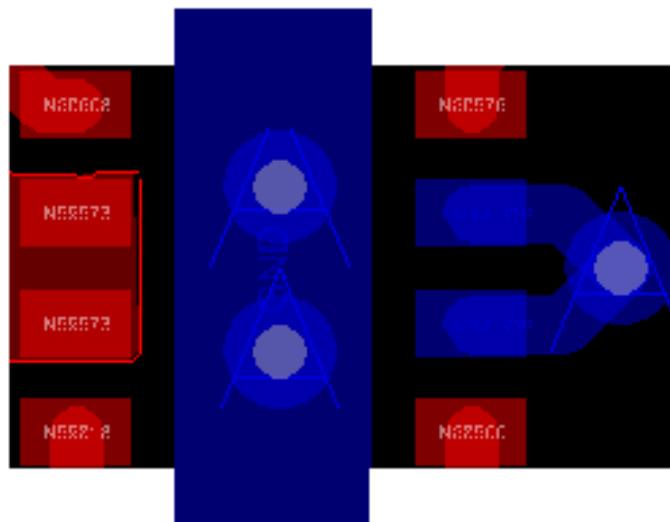
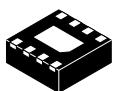
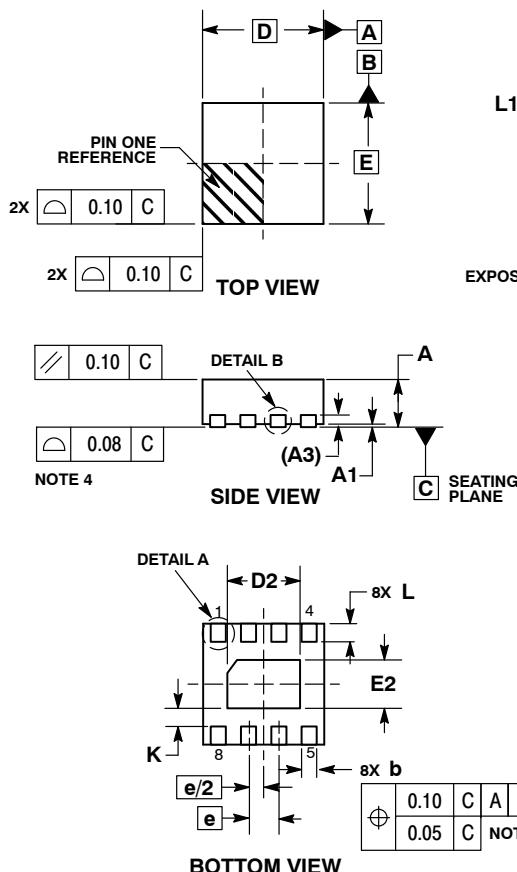


Figure 24.



SCALE 4:1

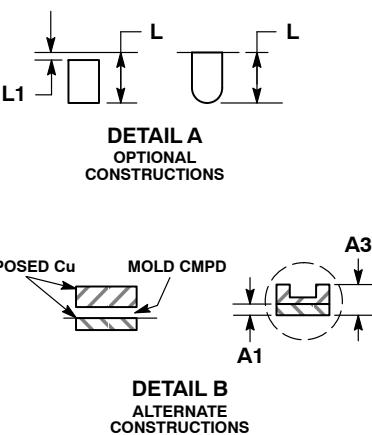
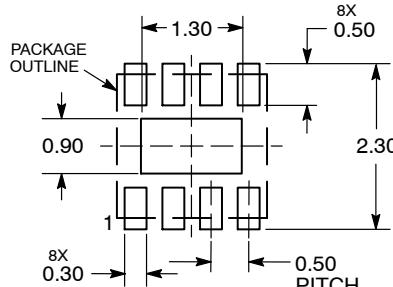
DFN8 2x2, 0.5P
CASE 506AA
ISSUE F

DATE 04 MAY 2016

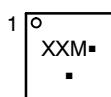
NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION *b* APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.20 MM FROM TERMINAL TIP.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

| MILLIMETERS | | |
|-------------|----------|------|
| DIM | MIN | MAX |
| A | 0.80 | 1.00 |
| A1 | 0.00 | 0.05 |
| A3 | 0.20 REF | |
| b | 0.20 | 0.30 |
| D | 2.00 BSC | |
| D2 | 1.10 | 1.30 |
| E | 2.00 BSC | |
| E2 | 0.70 | 0.90 |
| e | 0.50 BSC | |
| K | 0.30 REF | |
| L | 0.25 | 0.35 |
| L1 | --- | 0.10 |

RECOMMENDED
SOLDERING FOOTPRINT*

*For additional information on our Pb-Free strategy and soldering details, please download the **onsemi** Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC
MARKING DIAGRAM*

XX = Specific Device Code
M = Date Code
▪ = Pb-Free Device

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

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| DESCRIPTION: | DFN8, 2.0X2.0, 0.5MM PITCH | PAGE 1 OF 1 |

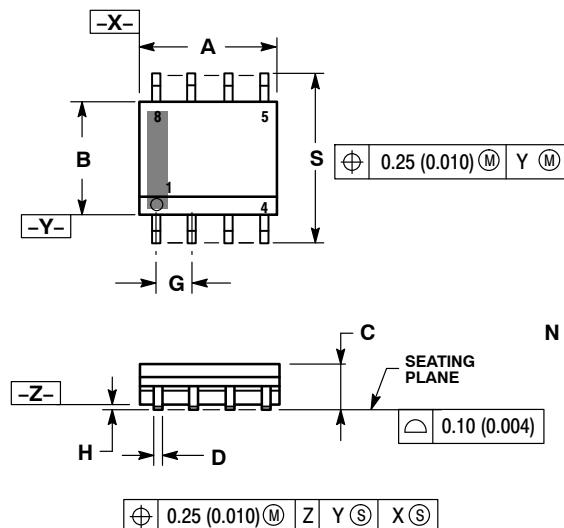
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SCALE 1:1

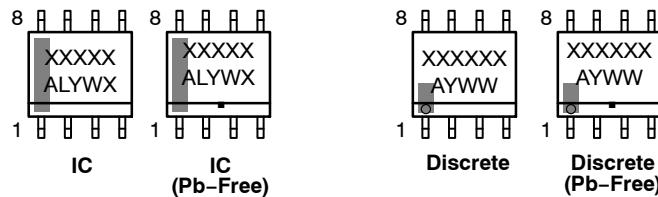
SOIC-8 NB
CASE 751-07
ISSUE AK

DATE 16 FEB 2011



- NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
 2. CONTROLLING DIMENSION: MILLIMETER.
 3. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
 4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
 5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.
 6. 751-01 THRU 751-06 ARE OBSOLETE. NEW STANDARD IS 751-07.

| DIM | MILLIMETERS | | INCHES | |
|-----|-------------|-----------|--------|-------|
| | MIN | MAX | MIN | MAX |
| A | 4.80 | 5.00 | 0.189 | 0.197 |
| B | 3.80 | 4.00 | 0.150 | 0.157 |
| C | 1.35 | 1.75 | 0.053 | 0.069 |
| D | 0.33 | 0.51 | 0.013 | 0.020 |
| G | 1.27 BSC | 0.050 BSC | | |
| H | 0.10 | 0.25 | 0.004 | 0.010 |
| J | 0.19 | 0.25 | 0.007 | 0.010 |
| K | 0.40 | 1.27 | 0.016 | 0.050 |
| M | 0 ° | 8 ° | 0 ° | 8 ° |
| N | 0.25 | 0.50 | 0.010 | 0.020 |
| S | 5.80 | 6.20 | 0.228 | 0.244 |

GENERIC
MARKING DIAGRAM*

XXXXX = Specific Device Code
A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb-Free Package

XXXXXX = Specific Device Code
A = Assembly Location
Y = Year
WW = Work Week
▪ = Pb-Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

*For additional information on our Pb-Free strategy and soldering details, please download the **onsemi** Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

STYLES ON PAGE 2

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| DESCRIPTION: | SOIC-8 NB | PAGE 1 OF 2 |

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SOIC-8 NB
CASE 751-07
ISSUE AK

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|--|---|---|---|
| STYLE 1: PIN 1. Emitter 2. Collector 3. Collector 4. Emitter 5. Emitter 6. Base 7. Base 8. Emitter | STYLE 2: PIN 1. Collector, Die #1 2. Collector, #1 3. Collector, #2 4. Collector, #2 5. Base, #2 6. Emitter, #2 7. Base, #1 8. Emitter, #1 | STYLE 3: PIN 1. Drain, Die #1 2. Drain, #1 3. Drain, #2 4. Drain, #2 5. Gate, #2 6. Source, #2 7. Gate, #1 8. Source, #1 | STYLE 4: PIN 1. Anode 2. Anode 3. Anode 4. Anode 5. Anode 6. Anode 7. Anode 8. Common Cathode |
| STYLE 5: PIN 1. Drain 2. Drain 3. Drain 4. Drain 5. Gate 6. Gate 7. Source 8. Source | STYLE 6: PIN 1. Source 2. Drain 3. Drain 4. Source 5. Source 6. Gate 7. Gate 8. Source | STYLE 7: PIN 1. Input 2. External bypass 3. Third stage source 4. Ground 5. Drain 6. Gate 3 7. Second stage Vd 8. First stage Vd | STYLE 8: PIN 1. Collector, Die #1 2. Base, #1 3. Base, #2 4. Collector, #2 5. Collector, #2 6. Emitter, #2 7. Emitter, #1 8. Collector, #1 |
| STYLE 9: PIN 1. Emitter, Common 2. Collector, Die #1 3. Collector, Die #2 4. Emitter, Common 5. Emitter, Common 6. Base, Die #2 7. Base, Die #1 8. Emitter, Common | STYLE 10: PIN 1. Ground 2. Bias 1 3. Output 4. Ground 5. Ground 6. Bias 2 7. Input 8. Ground | STYLE 11: PIN 1. Source 1 2. Gate 1 3. Source 2 4. Gate 2 5. Drain 2 6. Drain 2 7. Drain 1 8. Drain 1 | STYLE 12: PIN 1. Source 2. Source 3. Source 4. Gate 5. Drain 6. Drain 7. Drain 8. Drain |
| STYLE 13: PIN 1. N.C. 2. Source 3. Source 4. Gate 5. Drain 6. Drain 7. Drain 8. Drain | STYLE 14: PIN 1. N-Source 2. N-Gate 3. P-Source 4. P-Gate 5. P-Drain 6. P-Drain 7. N-Drain 8. N-Drain | STYLE 15: PIN 1. Anode 1 2. Anode 1 3. Anode 1 4. Anode 1 5. Cathode, Common 6. Cathode, Common 7. Cathode, Common 8. Cathode, Common | STYLE 16: PIN 1. Emitter, Die #1 2. Base, Die #1 3. Emitter, Die #2 4. Base, Die #2 5. Collector, Die #2 6. Collector, Die #2 7. Collector, Die #1 8. Collector, Die #1 |
| STYLE 17: PIN 1. VCC 2. V2OUT 3. V1OUT 4. TXE 5. RXE 6. VEE 7. GND 8. ACC | STYLE 18: PIN 1. ANODE 2. ANODE 3. SOURCE 4. GATE 5. DRAIN 6. DRAIN 7. CATHODE 8. CATHODE | STYLE 19: PIN 1. SOURCE 1 2. GATE 1 3. SOURCE 2 4. GATE 2 5. DRAIN 2 6. MIRROR 2 7. DRAIN 1 8. MIRROR 1 | STYLE 20: PIN 1. SOURCE (N) 2. GATE (N) 3. SOURCE (P) 4. GATE (P) 5. DRAIN 6. DRAIN 7. DRAIN 8. DRAIN |
| STYLE 21: PIN 1. Cathode 1 2. Cathode 2 3. Cathode 3 4. Cathode 4 5. Cathode 5 6. Common Anode 7. Common Anode 8. Cathode 6 | STYLE 22: PIN 1. I/O LINE 1 2. COMMON CATHODE/VCC 3. COMMON CATHODE/VCC 4. I/O LINE 3 5. COMMON ANODE/GND 6. I/O LINE 4 7. I/O LINE 5 8. COMMON ANODE/GND | STYLE 23: PIN 1. LINE 1 IN 2. COMMON ANODE/GND 3. COMMON ANODE/GND 4. LINE 2 IN 5. LINE 2 OUT 6. COMMON ANODE/GND 7. COMMON ANODE/GND 8. LINE 1 OUT | STYLE 24: PIN 1. BASE 2. Emitter 3. Collector/Anode 4. Collector/Anode 5. Cathode 6. Cathode 7. Collector/Anode 8. Collector/Anode |
| STYLE 25: PIN 1. VIN 2. N/C 3. REXT 4. GND 5. IOUT 6. IOUT 7. IOUT 8. IOUT | STYLE 26: PIN 1. GND 2. dv/dt 3. ENABLE 4. ILIMIT 5. SOURCE 6. SOURCE 7. SOURCE 8. VCC | STYLE 27: PIN 1. ILIMIT 2. OVLO 3. UVLO 4. INPUT+ 5. SOURCE 6. SOURCE 7. SOURCE 8. DRAIN | STYLE 28: PIN 1. SW_TO_GND 2. DASIC_OFF 3. DASIC_SW_DET 4. GND 5. V_MON 6. VBUCK 7. VBUCK 8. VIN |
| STYLE 29: PIN 1. BASE, Die #1 2. Emitter, #1 3. BASE, #2 4. Emitter, #2 5. Collector, #2 6. Collector, #2 7. Collector, #1 8. Collector, #1 | STYLE 30: PIN 1. DRAIN 1 2. DRAIN 1 3. GATE 2 4. SOURCE 2 5. SOURCE 1/DRAIN 2 6. SOURCE 1/DRAIN 2 7. SOURCE 1/DRAIN 2 8. GATE 1 | | |

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