Job Posting:173406 - Position: W26 FPGA Development Intern (Winter 2026) 173406

Co-op Work Term Posted:	2026 - Winter
App Deadline	09/23/2025 09:00 AM
Application Method:	Through Employer Website
Posting Goes Live:	09/16/2025 03:31 PM
Job Posting Status:	Approved

ORGANIZATION INFORMATION

Organization	Ciena Canada
Country	Canada

JOB POSTING INFORMATION

Placement Term	2026 - Winter
<b> Job Title <b>	W26 FPGA Development Intern (Winter 2026) 173406
Position Type	Co-op Position
Job Location	Ottawa, ON
Country	Canada
Duration	4 or 8 months
Salary Currency	CAD
Salary	Salary Not Available, 0 Major List
Salary Range $	$25.00 - $34.00/hour

Job Description

FPGA Development Intern (Winter 2026)

R028891

As the global leader in high-speed connectivity, Ciena is committed to a people-first approach. Our teams enjoy a culture focused on prioritizing a flexible work environment that empowers individual growth, well-being, and belonging. We're a technology company that leads with our humanity-driving our business priorities alongside meaningful social, community, and societal impact.

The Opportunity:

4-12 month co-op

How You Will Contribute:

The FPGA development team is seeking eligible co-op candidates to participate in the design, test, and support of optical networking products. You will be introduced to FPGA design and verification methodologies where we place a significant emphasis on early in career development through our FPGA curriculum and mentorship programs.

You will learn and contribute to:

• FPGA design using SystemVerilog for AMD, Intel, and Lattice FPGAs.

•FPGA verification using Universal Verification Methodology (UVM).

•Technical documentation writing and datasheet analysis.

•The life cycle of an FPGA design from concept to release.

Pay Range: The hourly pay range for this position is $25.00 - $34.00

Pay ranges at Ciena are designed to accommodate variations in knowledge, skills, experience, market conditions, and locations, reflecting our diverse products, industries, and lines of business. Please note that the pay range information provided in this posting pertains specifically to the primary location, which is the top location listed in case multiple locations are available.

In addition to competitive compensation, Ciena offers students access to the Employee Assistance Program (EAP), company-paid holidays, paid sick leave, and vacation pay as required by applicable laws.
Not ready to apply? Join our Talent Community to get relevant job alerts straight to your inbox.

At Ciena, we are committed to building and fostering an environment in which our employees feel respected, valued, and heard. Ciena values the diversity of its workforce and respects its employees as individuals. We do not tolerate any form of discrimination. Ciena is an Equal Opportunity Employer, including disability and protected veteran status.
If contacted in relation to a job opportunity, please advise Ciena of any accommodation measures you may

Job Requirements

The Must Haves:
• Working towards completion of a Bachelor's degree in Electrical Engineering, Computer Engineering or equivalent.
•Foundational knowledge of circuit design and digital logic.
•Excellent verbal and written communication skills.
Assets:
Familiarity with the following:
• Hardware description languages such as Verilog or SystemVerilog.
•Scripting and command languages such as Python, TCL, or Bash.
•FPGA development tools such as Questa, VCS, Quartus, or Vivado.

Citizenship Requirement N/A

APPLICATION INFORMATION

Application Procedure Through Employer Website
Cover Letter Required? Optional

Special Application Instructions

Application Link:

https://ciena.wd5.myworkdayjobs.com/Careers/job/Ottawa/FPGA-Development-Intern--Winter-2026-_R028891
Please click the "I intend to apply to this position" button on SCOPE and also submit your application via the employer's website.
Applications are accepted on a rolling basis and the posting may be expired at any time by the employer as submissions are received. Students should submit their applications as soon as they are ready.