

## **Job Posting: 176521 - Position: S26 DCS Validation Engineer Co-op 176521**

<b>Co-op Work Term Posted:</b>	2026 - Summer
<b>App Deadline</b>	01/14/2026 09:00 AM
<b>Application Method:</b>	Through UBC Science Co-op
<b>Posting Goes Live:</b>	01/06/2026 03:52 PM
<b>Job Posting Status:</b>	Approved

### **ORGANIZATION INFORMATION**

<b>Organization</b>	Microchip Technology Inc.
<b>Address Line 1</b>	8555 Baxter Pl
<b>Address Line 2</b>	105
<b>City</b>	Burnaby
<b>Postal Code / Zip Code</b>	V5A 4V7
<b>Province / State</b>	BC
<b>Country</b>	Canada

### **JOB POSTING INFORMATION**

<b>Placement Term</b>	2026 - Summer
<b>&lt;b&gt; Job Title &lt;b&gt;</b>	S26 DCS Validation Engineer Co-op 176521
<b>Position Type</b>	Co-op Position
<b>Job Location</b>	Burnaby, BC
<b>Country</b>	Canada
<b>Duration</b>	4 or 8 months
<b>Work Mode</b>	In-Person
<b>Salary Currency</b>	CAD
<b>Salary</b>	22.75 per hour for 40 Major List
<b>Salary Range \$</b>	22.75-34.5
<b>Job Description</b>	

#### **DCS Validation Engineer Co-op**

##### **Division:** DCS Arch & Validation

The System Engineering group in collaboration with Product Development, is responsible for ensuring that the end products operate fully in their intended applications. This involves the planning, design, integration, test and documentation of a complete system level platform used to test the prototype SoC's and associated Firmware/Software. The System Validation Design Engineer works in parallel with the IC and FW/SW designers to design an entire validation test systems, which could involve custom firmware development, digital/analog board designs, test script coding, and System-on-Chip integration.

Using these systems, together with the latest communication analyzers and test equipment, the System Validation Design Engineer will work as part of a team to develop and execute a Feature Test Plan that fully validates all features of the prototype IC and associated FW/SW. Working at the system level, the System Validation Design Engineer will be gain knowledge in relevant industry standards could include PCIe, NAND, DDR and other standards commonly used in computer & data center solutions.

### **Responsibilities**

As a VALIDATION ENGINEER CO-OP, you will work as part of a team to develop, execute and document a series of Feature Tests that will fully validate the operation of the prototype SOC as part of the overall system. These feature tests will exercise the various functional blocks of a prototype IC, associated FW/SW and tests the system level circuitry to performance criteria and to industry standards. Work will involve designing, building and debugging system level HW, SW and FW to test leading edge prototype SOC's in their intended applications. Specific tasks could include:

- Executing & managing system test suites to validate firmware feature enhancements & fixes.
- Building test setups & fixtures required to support validation testing
- Application level scripting for automated control of the test systems using Python or Tcl/Tk.
- Troubleshoot and resolve problems that may arise in complex PCIe system topologies.
- C/C++ test FW development
- Presenting technical information to small teams of engineers.

### **Job Requirements**

#### **Qualifications**

- Electrical or Computer Engineering co-op student
- Experience/Knowledge of basic software engineering & programming concepts
- Basic knowledge of microprocessor architectures & computer systems
- Basic knowledge of Computer related protocols such as USB, PCIe, UART, etc
- Experience in a lab or testing environment, especially using test & measurement equipment

- Ability to read & understand basic electronic schematics involving digital and analog circuitry

- Experience/knowledge of Linux & Windows is an asset

**Citizenship Requirement** N/A

**Position Start Date** May 04, 2026 12:00 AM

**Position End Date** August 28, 2026 12:00 AM

## **APPLICATION INFORMATION**

**Application Procedure** Through UBC Science Co-op

**Cover Letter Required?** Yes

**Address Cover Letter to** Isaac Leung