Job Posting:173735 - Position: W26 ASIC Engineer Intern 173735

Co-op Work Term Posted:	2026 - Winter
App Deadline	10/03/2025 09:00 AM
Application Method:	Through Employer Website
Posting Goes Live:	09/22/2025 03:58 PM
Job Posting Status:	Approved

ORGANIZATION INFORMATION

Organization	Ciena Canada
Country	Canada

JOB POSTING INFORMATION

Placement Term	2026 - Winter
<b> Job Title <b>	W26 ASIC Engineer Intern 173735
Position Type	Co-op Position
Job Location	Ottawa, ON
Country	Canada
Duration	4 or 8 months
Salary Currency	CAD
Salary	25.0 per hour for 0 Major List
Salary Range $	$25.00-34.00

Job Description

Job Title: ASIC Engineer Intern (Winter 2026)

Job ID: R029030

As the global leader in high-speed connectivity, Ciena is committed to a people-first approach. Our teams enjoy a culture focused on prioritizing a flexible work environment that empowers individual growth, well-being, and belonging. We're a technology company that leads with our humanity-driving our business priorities alongside meaningful social, community, and societal impact.

The Opportunity:

4-month work terms, extendable to 8 months

How You Will Contribute:

Ciena Corporation is a global networking leader holding the #1 market position in our field.?The R&D headquarters in Ottawa is home to our world leading Digital Signal Processing (DSP) WaveLogic ASIC chipsets, forming the core of Ciena's Optical Communications Systems.

We are looking for a passionate and enthusiastic student to help develop?and evolve the automation infrastructure used for?our next generation ASIC devices.?As a member of the team, you will contribute to the infrastructure, design and integration of Ciena's intellectual property into our next generation of ASICs. We are looking for students who have an interest in ASIC and Hardware Design with an interest in design, verification, and scripting. The position will be catered to a student's previous experience, strengths, and expertise.

You will enjoy working in a team environment, with mentors who want to help you throughout the work term.

In this role, you will…

- Work with a fast-paced team developing large-scale DSP ASICs for optical communications. There are multiple jobs we are hiring for. Students will be trained and will have access to key engineers while working on these projects. Some projects can be extended to 8 months.
- Interact daily with other developers and team-leads for guidance and support
- ASIC Design Tasks

• Develop small design blocks
•Assist designers on analysing the design for correctness and speed
•Assist with implementation and verification of designs
•ASIC Layout Tasks
• Work with layout engineers to implement netlists into a silicon-realiseable form
•Assist with automating the placement and extraction of key building blocks
•ASIC Integration Tasks
• Working with the integration team to create constraints to implement the design
•Assist with analysing reports to find deficiencies
•Assist with automating the integration of designs and IP to build the ASIC
•ASIC Verification Tasks
• Develop reusable System Verilog/UVM verification classes.
•Develop and enhance Python scripts to improve developers' productivity and product quality, examples include the following:
• simulation reporting and analysis (collating data and reporting using Python).
•optimizing our build, simulation and debug workflow.
In this role you will gain…
• Experience building complex scripts and applications using Excel, Python, TCL
•A deeper understanding of ASIC and Hardware design and verification techniques and languages
•First-hand exposure to real world class ASIC developments using the latest ASIC technologies
•A strong sense of responsibility for quality and completion of assigned tasks
Pay Range: The hourly pay range for this position is $25.00 - $34.00
• Good Communication Skills
Pay ranges at Ciena are designed to accommodate variations in knowledge, skills, experience, market conditions, and locations, reflecting our diverse products, industries, and lines of business. Please note that the pay range information provided in this posting pertains specifically to the primary location, which is the top location listed in case multiple locations are available.
In addition to competitive compensation, Ciena offers students access to the Employee Assistance Program (EAP), company-paid holidays, paid sick leave, and vacation pay as required by applicable laws.
Not ready to apply? Join our Talent Community to get relevant job alerts straight to your inbox.
At Ciena, we are committed to building and fostering an environment in which our employees feel respected, valued, and heard. Ciena values the diversity of its workforce and respects its employees as individuals. We do not tolerate any form of discrimination. Ciena is an Equal Opportunity Employer, including disability and protected veteran status.
If contacted in relation to a job opportunity, please advise Ciena of any accommodation measures you may require

Job Requirements

The Must Haves:
• Programming experience (ideally using at least one of Java, Python, TCL, Skill/Ocean, and System Verilog)
•Familiarity with Linux based development environments
Assets:
• Previous experience ASIC or FPGA development programs
•Strong analytical and debugging skills
•Familiarity with Agile JIRA, Confluence, GIT

Citizenship Requirement N/A

APPLICATION INFORMATION

Application Procedure Through Employer Website
Cover Letter Required? Optional
Special Application Instructions

Application Link:

https://ciena.wd5.myworkdayjobs.com/en-US/Careers/job/Ottawa/ASIC-Engineer-Intern--Winter-2026-_R029030
Please click the "I intend to apply to this position" button on SCOPE and also submit your application via the employer's

website. Applications are accepted on a rolling basis and the posting may be expired at any time by the employer as submissions are received. Students should submit their applications as soon as they are ready.