Luis E. P.

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Overview

I seek to work on a state-of-the-art systems project where I can apply my performance analysis, hardware/software codesign and distributed systems skills.

Professional Experience

Arm

Austin, TX

Systems Research Engineer, Arm Research — Jan 2016 – Present

Three-Chains & Two-Chains

- *Three-Chains* is a framework for injecting code and data between heterogeneous devices on distributed systems
- *Three-Chains* leverages the UCX framework and RDMA to accelerate code and data delivery
- *Three-Chains* leverages LLVM to work on a variety of systems, including Arm and x86 CPUs, DPUs and CSDs
- Actively developing the next generation of *Three-Chains*, where the framework is decoupled from UCX
- Designed and implemented benchmarks to highlight the benefits of using *Three-Chains* over Active Messages and RDMA gets
- Defined and improved the API used by *Three-Chains* to prepare, send and execute injected functions (*ifuncs*)
- Identified and fixed instruction-cache misconfiguration affecting performance of high-level software
- Developed new microbenchmarks to analyze the impact of last-level cache stashing on Active Messages
- Tested and analyzed the impact of the wait-for-event (WFE) instruction on cache-stashed Active Messages
- Co-authored 9 reports for funded Department of Energy projects
- Published 3 papers to peer-reviewed conferences (see publications 1, 2 & 3)
- Three-chains source code: https://github.com/openucx/three-chains
- Two-Chains source code: https://github.com/openucx/ucx-two-chains

EdgeFaaS

- Designed, developed and tested FaaS system optimized for the edge
- EdgeFaaS was adopted by a large telecom operator as part of their edge computing solution
- Only function source code is shipped and installed, reducing overhead of function deployment by 100x
- EdgeFaaS is based on OpenFaaS
- Source code: https://gitlab.com/arm-research/smarter/edgefaas/edgefaas
- Blogpost: https://community.arm.com/arm-research/b/articles/posts/faas-runtimes-on-edge-devices

Serverless Framework Performance Gaps

- Identified bottlenecks of serverless frameworks: container networking, secure computing mode, Arm GoLang performance
- Used a combination of benchmarks and tools (Perf, Memcached, FlameGraphs, OLDIsim) to uncover areas of improvement
- Experimented with user-space networking to reduce the tail-latency of the applications under test

Datacenter Workload Effects on TLBs

- Simulated TLB performance for Cortex A55 and A75 CPUs when running distributed applications
- Validated design decisions and provided CPU team with areas to improve TLB performance
- Modified the Gem5 simulator to accurately represent the memory subsystems of the processors under test

Miscellaneous

- Bring up and benchmark state-of-the-art Arm-based systems, including Nvidia BlueField-2 data processing units, NGD computational storage drives and Arm Neoverse N1 SDPs.
- Led 6 successful internships, 3 of them leading to post-internship collaboration and papers
- Generated 3 patents (2 being drafted & 1 filed)

VMware

Palo Alto, CA

Open vSwitch Research Engineer, Network & Security Business Unit — Jun 2015 – Aug 2015

- Explored the capabilities of next-generation NICs with on-board flow processing
- Adapted Intel DPDK and Open vSwitch to work with these new NICs
- Helped integrate the hardware and software flow-handling capabilities
- Used the Intel Ethernet Switch API to configure network flows on the NICs

The Boeing Company

Seattle, WA

Embedded Systems Student Engineer, Boeing Research & Technology — May 2014 – Aug 2014

- Explored and developed Verilog of airborne deterministic Ethernet controllers on FPGAs
- Integrated µC/OS-II Real-Time OS into an FPGA development board

The Boeing Company Seattle, WA

Embedded Systems Student Engineer, Boeing Research & Technology Jun 2013 – Aug 2013

- Designed and implemented an embedded C SNMP agent to manage airborne network systems
- Wrote a custom CSV to MIB parser for the SNMP agent and for off-the-shelf MIB browsers
- Saved the group 15K dollars with the software I developed

Selected Publications

1. Lu, W., **Peña, L.E.**, Shamis, P., Churavy, V., Chapman, B. and Poole, S., 2022, September. **Bring the BitCode – Moving Compute and Data in Distributed Heterogeneous Systems**. In *2022 IEEE International Conference on Cluster Computing (CLUSTER)*
2. **Peña, L.E.**, Lu, W., Shamis, P. and Poole, S., 2021, September. **UCX Programming Interface for Remote Function Injection and Invocation**. In *2021 OpenSHMEM and Related Technologies Workshop (OpenSHMEM 2021)*
3. Grodowitz, M., **Peña, L.E.**, Dunham, C., Zhong, D., Shamis, P. and Poole, S., 2021, September. **Two-Chains: High Performance Framework for Function Injection and Execution**. In *2021 IEEE International Conference on Cluster Computing (CLUSTER)*
4. Ferreira, A., Van Hensbergen, E., Adeniyi-Jones, C., Grimely-Evans, E., Minor, J., Nutter, M., **Peña, L.E.**, Agarwal, K. and Hermes, J., 2020. **{SMARTER}: Experiences with Cloud Native on the Edge**. In *3rd USENIX Workshop on Hot Topics in Edge Computing (HotEdge 20)*

Education

The University of Texas at Austin Austin, TX

Partial PhD in Computer Architecture and Embedded Processors Sept 2013 – Dec 2015

Advisor: Derek Chiou

Columbia University New York, NY

Bachelor of Science in Computer Engineering, *cum laude* May 2013

Skills

Programming Languages:	C, Python, Java, VHDL, Verilog, C++, CUDA, Assembly
Software:	Docker, Kubernetes, UCX, RDMA, Gitlab CI, LLVM, Git, Wireshark
Research & Development:	FPGA Development, Certified Scrum Master, OpenFlow, DPDK, Software-Defined Networking
Languages:	Fluent in written and spoken Spanish