UCSD 237C: Project 4 OFDM

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1. Introduction

This report details the optimizations performed on a hardware implementation of the OFDM in HLS. One optimal design was explored: 1. FFT using dataflow for each stage.

2. OFDM Design

2.1. Throughput

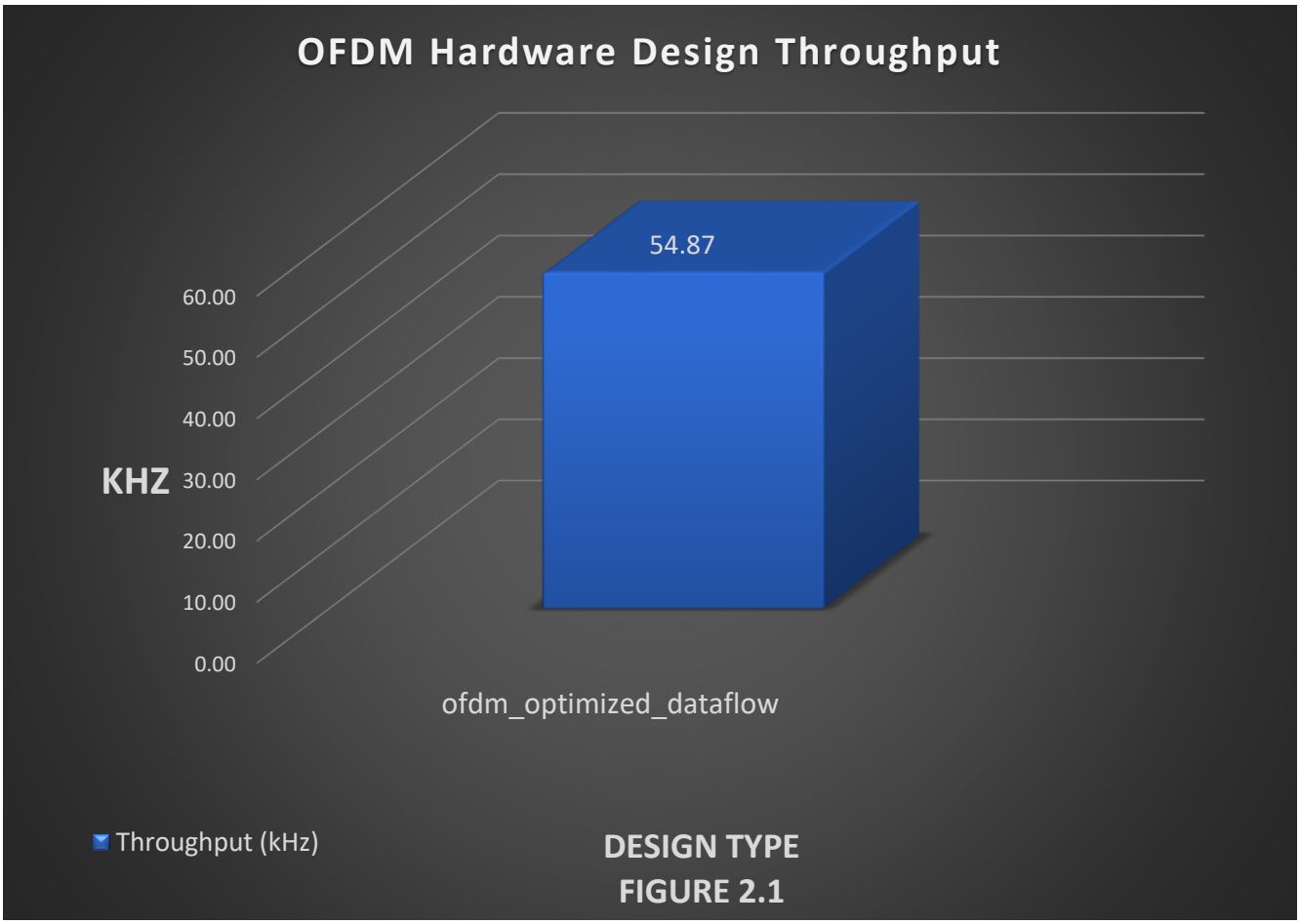

FIGURE 2.1

2.2. Implementation

```
void qpsk_decode(DTYPE R[SIZE], DTYPE I[SIZE], int D[SIZE]) {

    int quadrature;
    int in_phase;
    unsigned int i;
    qpsk_loop:
    for (i = 0; i < SIZE; i++)
    {
#pragma HLS UNROLL
        in_phase   = R[i] < 0;
        quadrature = I[i] < 0;

        //takes a complex number and translates it into an integer
        D[i] = (quadrature << 1) | in_phase;
    }
}
```

2.3. Resources

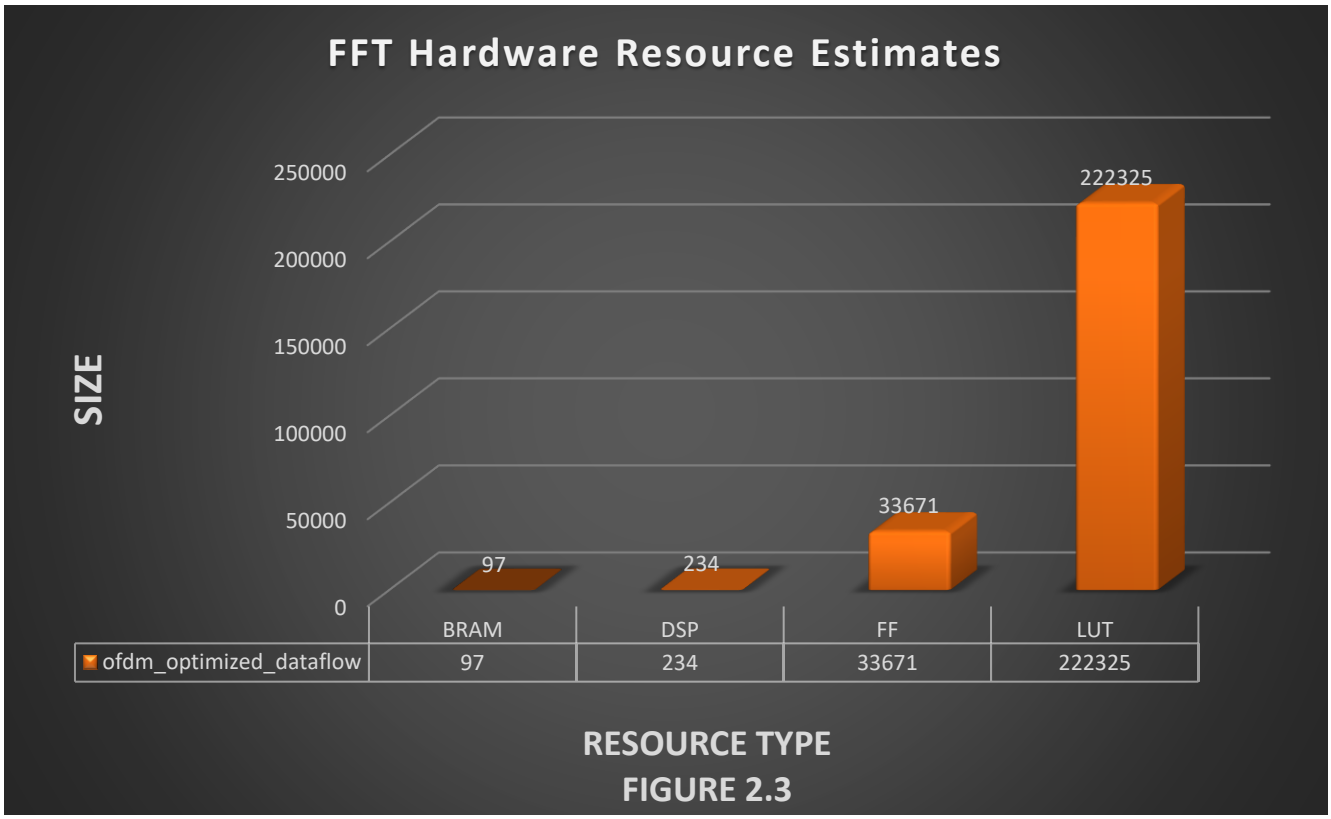

FIGURE 2.3

2.4. Optimizations

- Added dataflow to top level FFT function.
- Unrolled qpsk decode loop.

2.5. Analysis

This design provides an optimized version of an OFDM receiver and achieves near target performance of 54Khz of throughput. The dataflow pragma was used to ensure that the FFT stages overlap thereby making use of task pipelining. Additional performance gains were achieved by completely partitioning the precomputed twiddle factors used in the inner loop of the FFT algorithm and unrolling the qpsk demodulation function. The primary tradeoffs of this design were in the usage of hardware resources where a large amount of DSP's and Flip Flops

were used. The main drawback of this design is the high DSP usage. This architecture exceeds the number of DSP available on the PYNQ-Z2 and is not a good design choice.