UCSD 237C: Project 4 FFT

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December 2, 2023

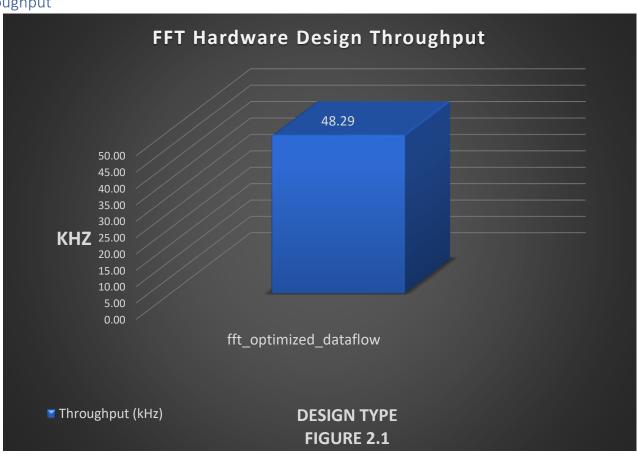
1. Introduction

This report details the optimizations performed on a hardware implementation of the Fast Fourier Transform in HLS. One optimal design was explored:

1. FFT using dataflow for each stage.

2. FFT Design

2.1. Throughput



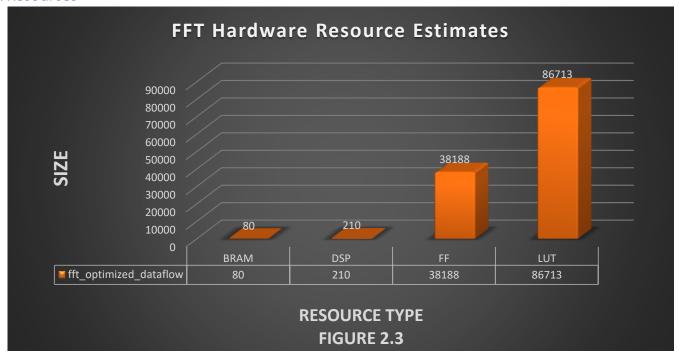
2.2. Implementation

```
void fft(DTYPE IN R[SIZE], DTYPE IN I[SIZE], DTYPE OUT R[SIZE], DTYPE OUT I[SIZE])
    DTYPE X R[SIZE], X I[SIZE];
    bit reverse(IN R, IN I, X R, X I);
    DTYPE Stage1 R[SIZE], Stage1 I[SIZE];
    DTYPE Stage2 R[SIZE], Stage2 I[SIZE];
    DTYPE Stage3_R[SIZE], Stage3_I[SIZE];
    DTYPE Stage4_R[SIZE], Stage4_I[SIZE];
    DTYPE Stage5_R[SIZE], Stage5_I[SIZE];
    DTYPE Stage6_R[SIZE], Stage6_I[SIZE];
DTYPE Stage7_R[SIZE], Stage7_I[SIZE];
DTYPE Stage8_R[SIZE], Stage8_I[SIZE];
DTYPE Stage9_R[SIZE], Stage9_I[SIZE];
    fft_stage_first(X_R, X_I, Stage1_R, Stage1_I);
    fft_stages(Stage1_R, Stage1_I, 2, Stage2_R, Stage2_I);
    fft stages (Stage2 R, Stage2 I, 3, Stage3 R, Stage3 I);
    fft_stages(Stage3_R, Stage3_I, 4, Stage4_R, Stage4_I);
fft_stages(Stage4_R, Stage4_I, 5, Stage5_R, Stage5_I);
    fft_stages(Stage5_R, Stage5_I, 6, Stage6_R, Stage6_I);
fft_stages(Stage6_R, Stage6_I, 7, Stage7_R, Stage7_I);
    fft_stages(Stage7_R, Stage7_I, 8, Stage8_R, Stage8_I);
fft_stages(Stage8_R, Stage8_I, 9, Stage9_R, Stage9_I);
    fft_stage_last(Stage9_R, Stage9_I, OUT_R, OUT_I);
void bit reverse(DTYPE X R[SIZE], DTYPE X I[SIZE], DTYPE OUT R[SIZE], DTYPE OUT I[SIZE])
    unsigned int reversed= 0;
    unsigned int i;
    DTYPE temp;
    DTYPE temp rev R[SIZE];
    DTYPE temp rev I[SIZE];
    int temp_rev_idx[SIZE];
    for (i = 0; i < SIZE; i++)</pre>
#pragma HLS UNROLL
         temp rev idx[i] = reverse bits(i); // Find the bit reversed index
         OUT R[i] = X R[temp rev idx[i]];
         temp rev R[i] = X R[i];
         OUT I[i] = X I[temp rev idx[i]];
         temp rev I[i] = X I[i];
    for (i = 0; i < SIZE; i++)</pre>
#pragma HLS UNROLL
         OUT R[temp rev idx[i]] = temp rev R[i];
         OUT I[temp rev idx[i]] = temp rev I[i];
```

```
void fft_stage_first(DTYPE X_R[SIZE], DTYPE X_I[SIZE], DTYPE OUT_R[SIZE], DTYPE OUT_I[SIZE])
#pragma HLS array partition variable=W real type=complete
#pragma HLS array partition variable=W imag type=complete
    int stage = 1;
    int DFTpts = 1 << stage; // DFT = 2^stage = points in sub DFT</pre>
    int numBF = DFTpts / 2; // Butterfly WIDTHS in sub-DFT
    int step = SIZE >> stage;
   int k = 0;
DTYPE e = -6.283185307178 / DFTpts;
    DTYPE a = 0.0;
   DTYPE c;
   DTYPE s;
   int twiddle index = 0;
   butterfly loop first:for (int j = 0; j < numBF; j++)</pre>
        dft loop first:for (int i = j; i < SIZE; i += DFTpts) {</pre>
#pragma HLS pipeline
                twiddle index = (k*j)%(DFTpts); // determines which twiddle factor is
                c = W real[twiddle index]; // twiddle factor
                s = W imag[twiddle index]; // twiddle factor
                int ilower = i + numBF; // index of lower point in butterfly
                DTYPE temp R = X R[ilower] * c - X I[ilower] * s;
                DTYPE temp I = X I[ilower] * c + X R[ilower] * s;
                OUT R[ilower] = X R[i] - temp R;
                OUT I[ilower] = X I[i] - temp I;
                OUT_R[i] = X_R[i] + temp_R;
                OUT I[i] = X I[i] + temp I;
        k += step;
void fft stages(DTYPE X R[SIZE], DTYPE X I[SIZE], int stage, DTYPE OUT R[SIZE], DTYPE
OUT I[SIZE]) {
#pragma HLS array partition variable=W real type=complete
#pragma HLS array partition variable=W imag type=complete
   int DFTpts = 1 << stage; // DFT = 2^stage = points in sub DFT</pre>
    int numBF = DFTpts / 2; // Butterfly WIDTHS in sub-DFT
    int step = SIZE >> stage;
    int k = 0;
    DTYPE e = -6.283185307178 / DFTpts;
    DTYPE a = 0.0;
   DTYPE c = 0;
    DTYPE s = 0;
    int twiddle_index = 0;
   butterfly loop stages:for (int j = 0; j < numBF; j++)</pre>
        // Compute butterflies that use same W^{**}k
        dft loop stages:for (int i = j; i < SIZE; i += DFTpts) {</pre>
#pragma HLS pipeline
                twiddle index = (k*j)%(DFTpts); // determines which twiddle factor is
```

```
c = W real[twiddle_index]; // twiddle
                 s = W imag[twiddle index]; // twiddle factor
                 int ilower = i + numBF; // index of lower point in butterfly
                 DTYPE temp R = X R[ilower] * c - X I[ilower] * s;
                 DTYPE temp_I = X_I[ilower] * c + X_R[ilower] * s;
                 OUT R[ilower] = X R[i] - temp R;
                 OUT I[ilower] = X I[i] - temp I;
                 OUT R[i] = X R[i] + temp R;
                 OUT I[i] = X I[i] + temp I;
        k += step;
void fft stage last(DTYPE X R[SIZE], DTYPE X I[SIZE], DTYPE OUT R[SIZE], DTYPE OUT I[SIZE])
#pragma HLS array partition variable=W real type=complete
#pragma HLS array_partition variable=W imag type=complete
    int stage = 10;
    int DFTpts = 1 << stage; // same as multiplying 1* 2^stage, DFT = 2^stage = points in</pre>
    int numBF = DFTpts / 2; // Butterfly WIDTHS in sub-DFT
    int step = SIZE >> stage; // same as dividing SIZE/(2^stage)
    int k = 0;
   DTYPE e = -6.283185307178 / DFTpts;
   DTYPE c = 0;
   DTYPE s = 0;
   int twiddle index = 0;
   butterfly loop last:for (int j = 0; j < numBF; j++)</pre>
        dft_loop_last:for (int i = j; i < SIZE; i += DFTpts) {</pre>
#pragma HLS pipeline
                 twiddle index = (k*j)% (DFTpts); // determines which twiddle factor is
                 c = W_real[twiddle_index]; // twiddle_factor
                 s = W_imag[twiddle_index]; // twiddle factor
int ilower = i + numBF; // index of lower point in butterfly
DTYPE temp_R = X_R[ilower] * c - X_I[ilower] * s;
                 DTYPE temp I = X I[ilower] * c + X R[ilower] * s;
                 OUT R[ilower] = X R[i] - temp R;
                 OUT_I[ilower] = X_I[i] - temp_I;
                 OUT R[i] = X R[i] + temp R;
                 OUT I[i] = X I[i] + temp I;
        k += step;
                      ====END: FFT==
```

2.3. Resources



2.4. Optimizations

- Added dataflow to top level function.
- Separated loop in bit reverse function into 2 loops and completely unrolled both loops.
- Completely partitioned the twiddle factors.

2.5. Analysis

This design provides an optimized version of the Fast Fourier Transform and achieves near target performance of 48Khz of throughput. The dataflow pragma was used to ensure that the FFT stages overlap thereby making use of task pipelining. Additional performance gains were achieved by completely partitioning the precomputed twiddle factors used in the inner loop of the FFT algorithm. The primary tradeoffs of this design were in the usage of hardware resources where a large amount of DSP's and Flip Flops were used.