LAB 2

OBJECTIVE: To design and simulate a 2-input OR gate using VHDL, and verify its functionality using a testbench.

TOOLS USED:

- VHDL (VHSIC Hardware Description Language)
- https://www.edaplayground.com/ (for simulation)

THEORY:

The aim of this lab is to create a simple 2-input OR gate in VHDL and simulate it using a testbench. The design code describes the logic of the OR gate, and the testbench applies all possible input combinations to validate the behavior of the gate.

VHDL CODE

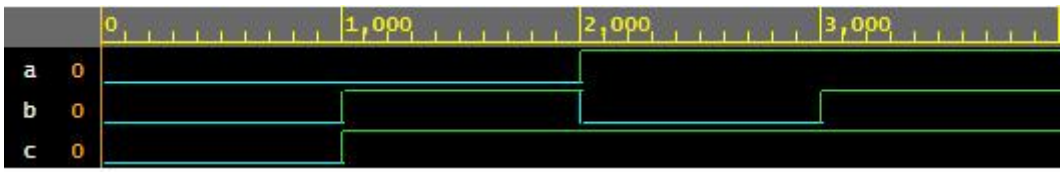
DESIGN:

```
library ieee;
use ieee.std_logic_1164.all;

entity orgate is
  port(  a,b:in std_logic;
         c: out std_logic);
end andgate;

architecture behavior of orgate is
         begin
         c <= a orb;
end behavior;
```

TESTBENCH

```
library ieee;
use ieee.std_logic_1164.all;

entity orgate_tb is
         ---> no content
end orgate_tb;

architecture test of orgate_tb is
         component orgate
         port(a,b: in std_logic;
                  c: out std_logic);
         end component;

         signal ak,bk,ck: std_logic;

         begin

         and_gate: orgate port map(a=>ak,
b=>bk, c=>ck);

         process begin

                  ak <= '0';bk <= '0';wait for 1 ns;

                  ak <= '0';bk <= '1';wait for 1 ns;

                  ak <= '1';bk <= '0';wait for 1 ns;

                  ak <= '1';bk <= '1';wait for 1 ns;

                  assert false report "Completed
successfully";
                  wait;
         end process;
end test;
```

Output:



CONCLUSION:

The 2-input OR gate was successfully simulated. The output matched the expected truth table for all input combinations. The use of a simple testbench allowed for effective verification of the circuit behavior in a VHDL simulation environment.