LAB 4

OBJECTIVE: To design and simulate a NAND gate using VHDL, and verify its functionality using a testbench.

TOOLS USED:

- VHDL (VHSIC Hardware Description Language)
- https://www.edaplayground.com/ (for simulation)

THEORY:

The aim of this lab is to create a NAND gate in VHDL and simulate it using a testbench. The design code describes the logic of the NAND gate, and the testbench applies both possible input combinations to validate the behavior of the gate.

VHDL CODE

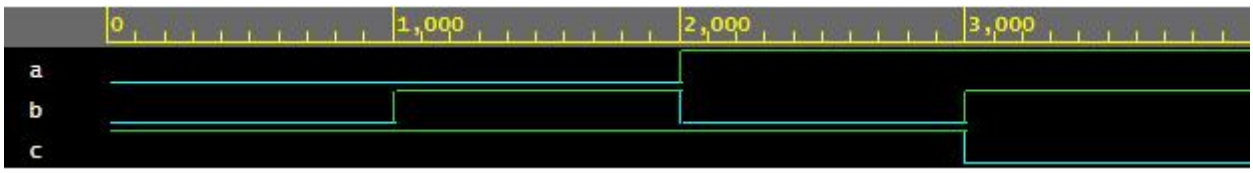
DESIGN

```
library ieee;
use ieee.std_logic_1164.all;

entity nandgate is
	port(
		a,b:in std_logic;
		c: out std_logic
	);
end nandgate;

architecture behavior of nandgate is
	begin
	c <= not (a and b);
end behavior;
```

TESTBENCH

```
library ieee;
use ieee.std_logic_1164.all;

entity nandgate_testbench is
end nandgate_testbench;

architecture test of nandgate_testbench is
	component nandgate
		port(
			a,b: in std_logic;
			c: out std_logic
		);
	end component;

	signal ak,bk,ck: std_logic;

	begin

	nand_gate: nandgate port map(a=>ak,
b=>bk, c=>ck);

	process begin

		ak <= '0';bk <= '0';wait for 1 ns;
		ak <= '0';bk <= '1';wait for 1 ns;
		ak <= '1';bk <= '0';wait for 1 ns;
		ak <= '1';bk <= '1';wait for 1 ns;

		assert false report "Completed
successfully";
		wait;
	end process;
end test;
```

Output:



CONCLUSION:

The NOT gate was successfully simulated. The output matched the expected behavior where ck is the inverse of ak for all input combinations. The use of a simple testbench allowed for effective verification of the circuit behavior in a VHDL simulation environment.