XUPV5-LX110T MIG Design Creation

Using ISE™ 10.1i SP3, MIG 2.3 and ChipScope™ Pro 10.1i

September, 2008

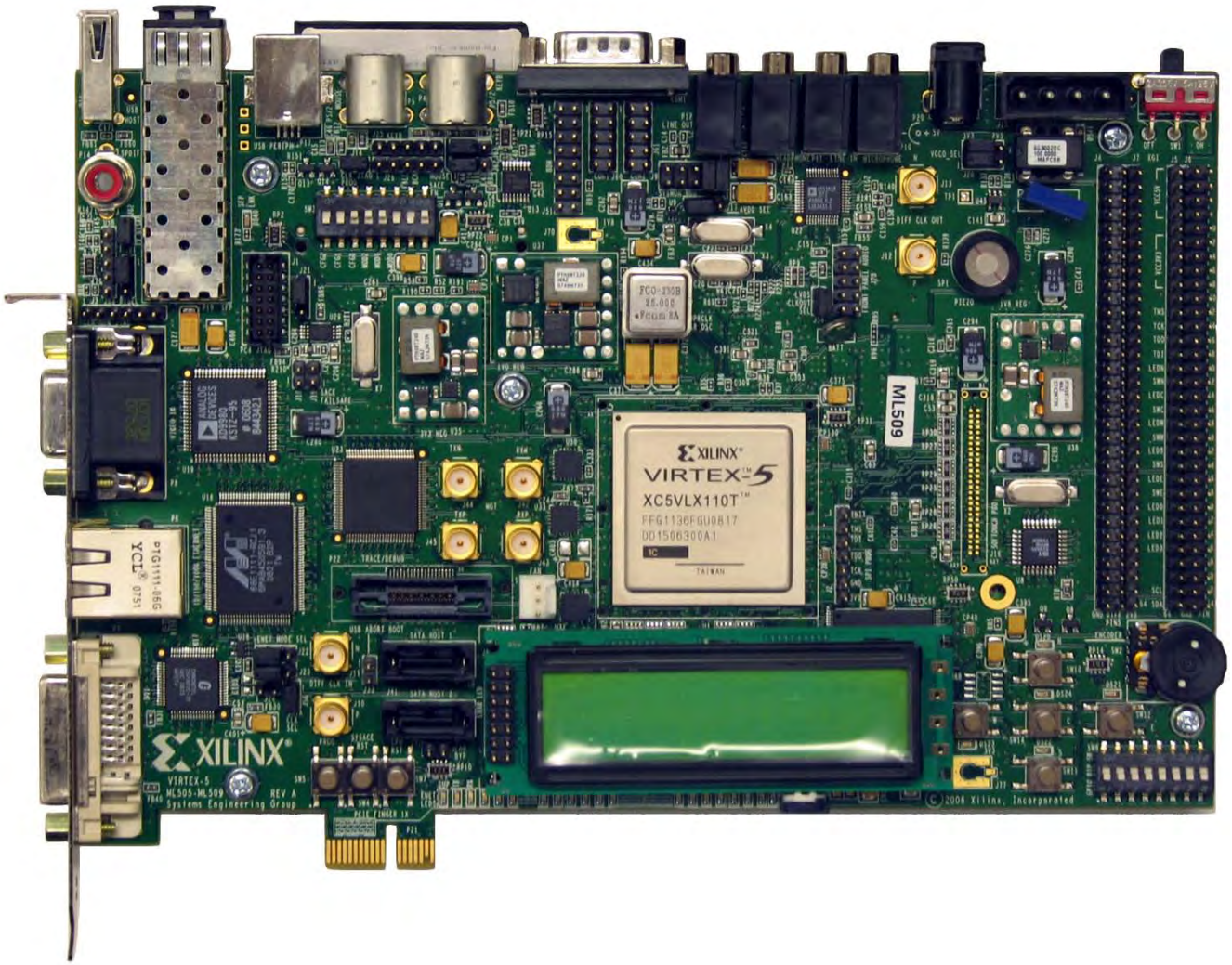
Overview

- Hardware Setup
- Software Requirements
- CORE Generator™ software
  - Memory Interface Generator (MIG)
- Modify Design
  - Add ChipScope Pro Cores to Design
- Compile and Test Memory Interface

Virtex-5 DDR2 Capabilities

- MIG DDR2 SDRAM design supports frequencies up to 333 MHz
  - The MIG user guide addresses MIG performance across device speed grades
- The XUPV5-LX110T ships with a –1 speed grade device
  - See the Virtex-5 Data Sheet for a list of Virtex-5 supported memory interface speeds

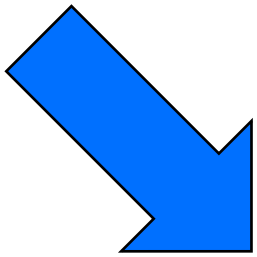
Xilinx XUPV5-LX110T Board



Note: The XUPV5-LX110T uses an XC5VLX110T FPGA.

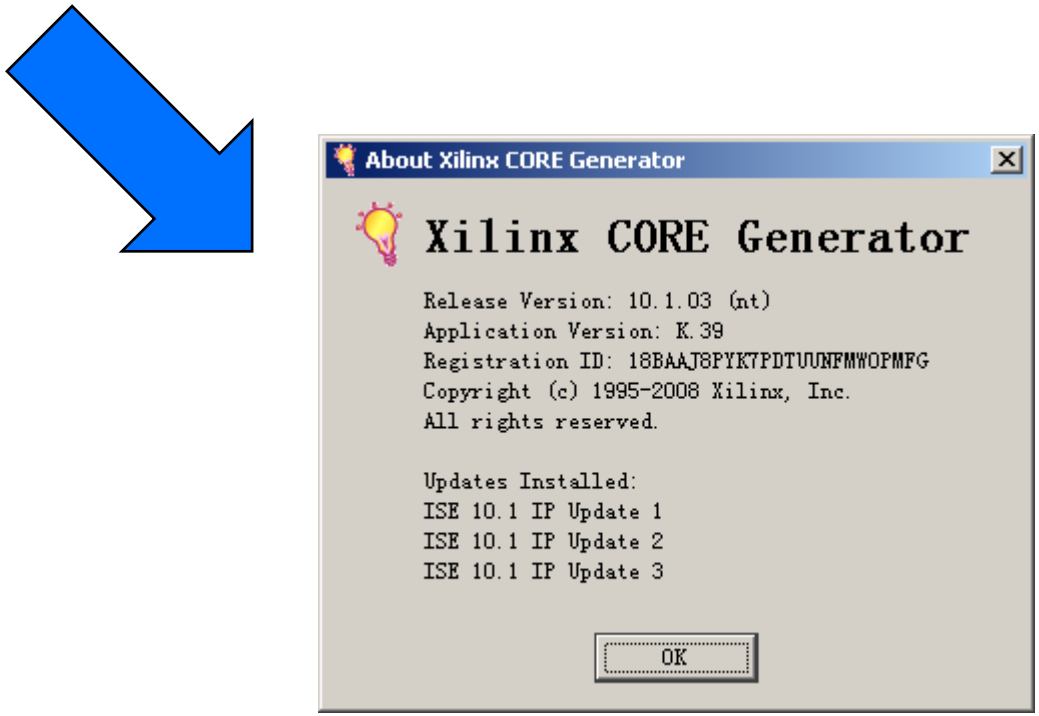
ISE Software Requirement

- Xilinx ISE 10.1i SP3 software



Coregen Software Requirement

- Install Xilinx Coregen 10.1i IP Update 3



ChipScope Software Requirement

- Xilinx ChipScope Pro 10.1i SP3

Setting Up the Hardware

- Connect the Xilinx Parallel Cable IV (PC4)
  - HW-PC4
- SMA Cable
  - www.flrst.com
  - P/N: ASPI-024-ASPI-S402
- Optional - Pancake Fan
  - Recommended for keeping the Virtex™-5 device cool

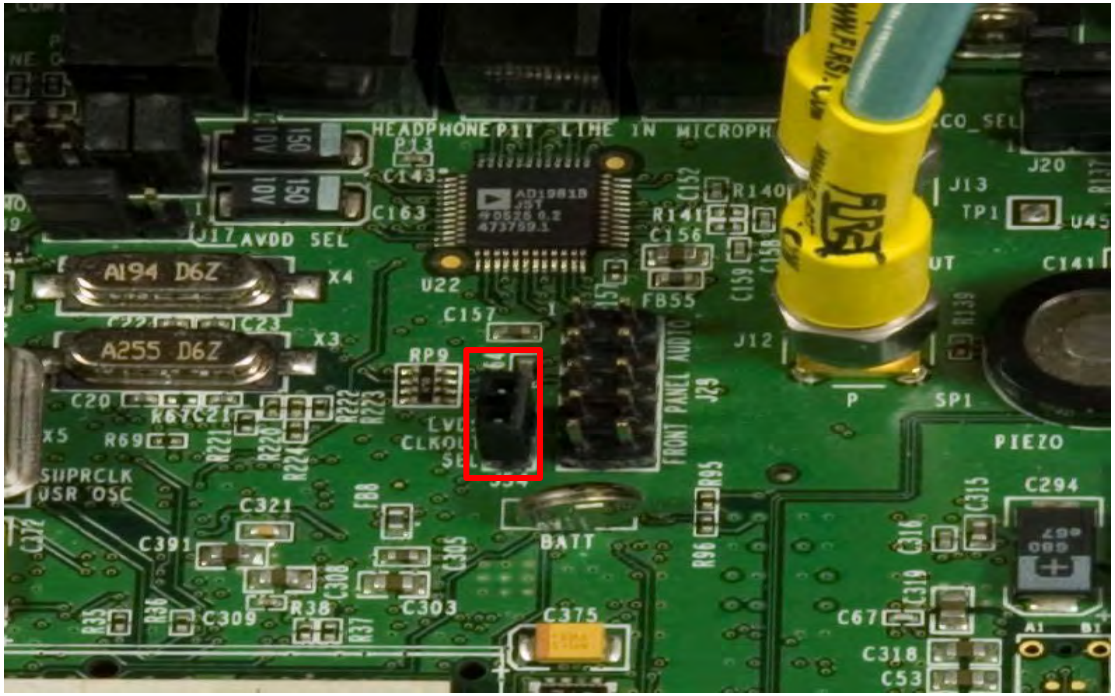
Setting Up the Hardware

- Connect SMA Cables from J12/13 to J10/11
  - This will serve as the 200 MHz clock source for the memory controller

Note: Alternately, an external differential clock source can be connected to J10/11.

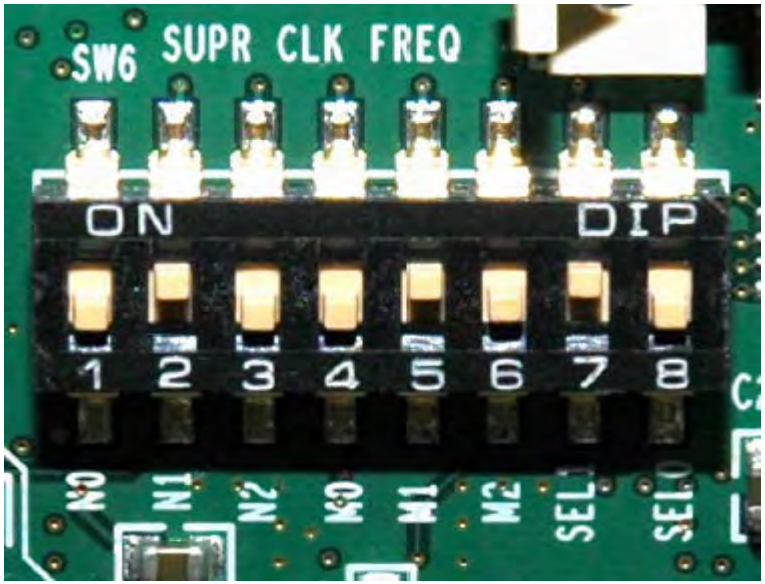
Setting Up the Hardware

- Jumper J54 must be connected
  - This enables the output of the on-board ICS frequency source



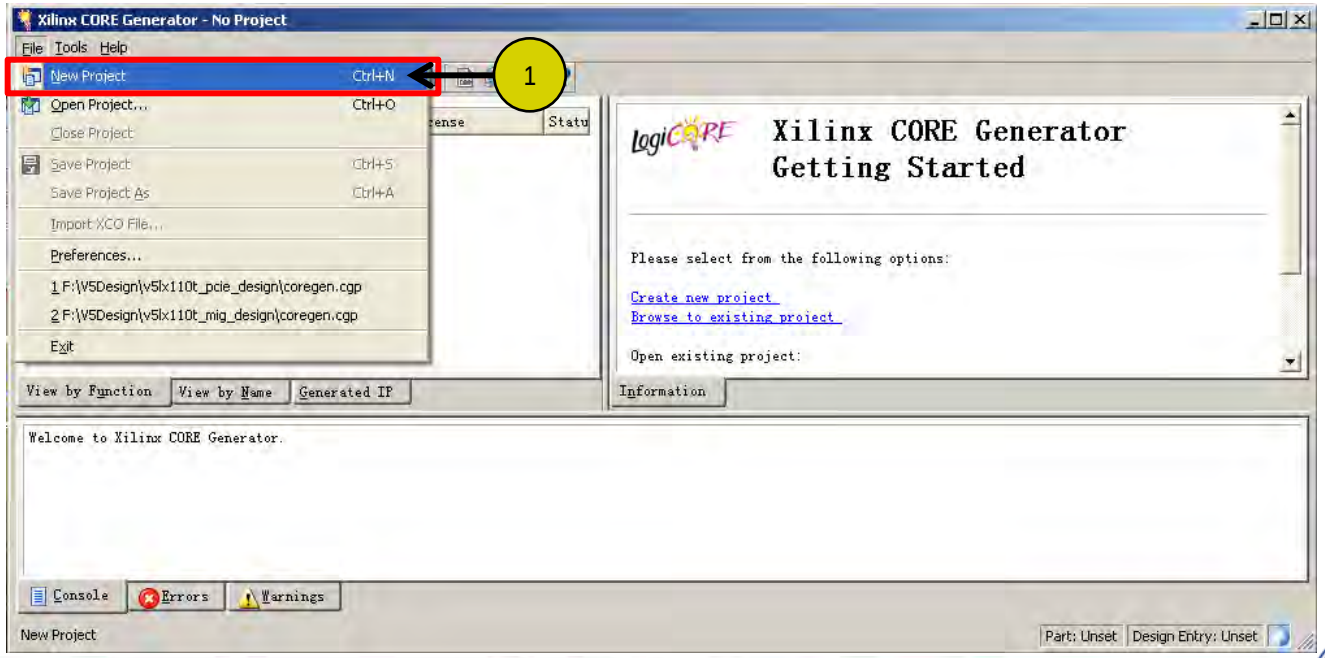
Setting Up the Hardware

- Use SW6 to set the memory clock frequency
- Set SW6 to 200 MHz (1)
  - 200 MHz = 010 010 10 (Max memory clock frequency for a -1 speed grade)



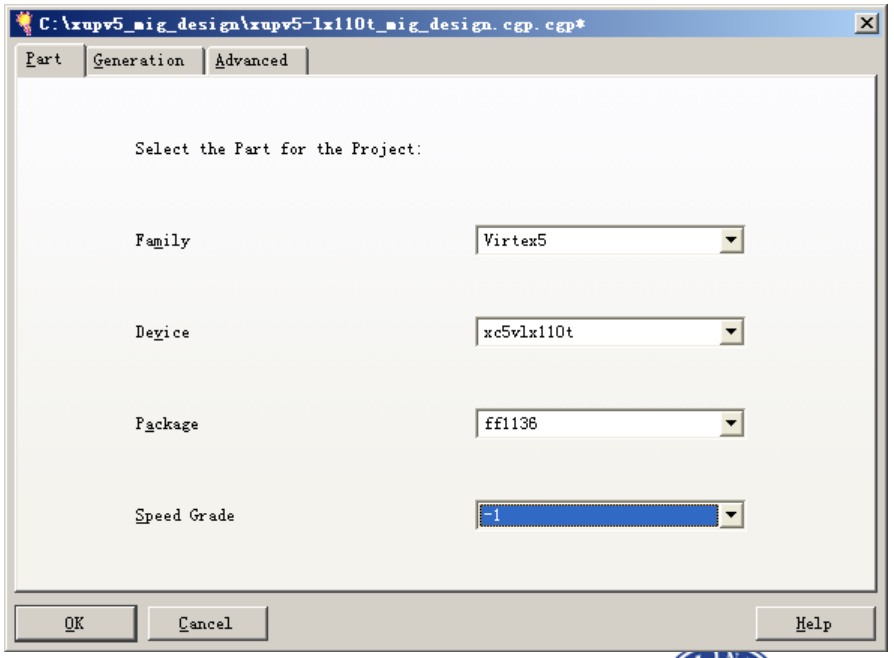
CORE Generator

- Open the CORE Generator
  - Start → All Programs → Xilinx ISE Design Suite 10.1i → ISE → Accessories → CORE Generator
- Create a new project; select File → New Project (1)



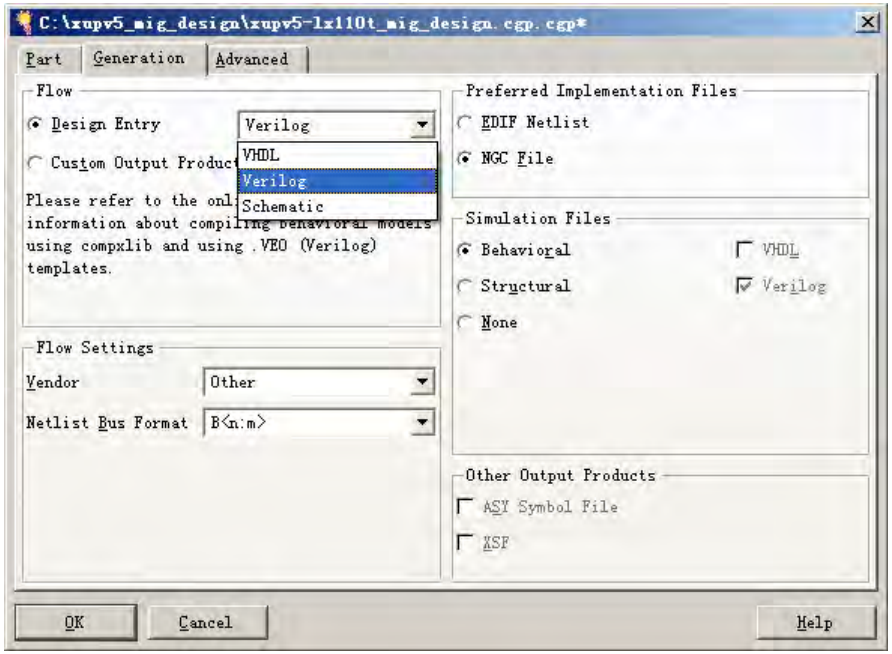
MIG Core Generation

- Create a project directory: xupv5_mig_design
- Name the project: xupv5-lx110t_mig_design.cgp
- Set the Part (as shipped on the XUPV5-LX110T):
  - Family: Virtex5
  - Device: xc5vlx110t
  - Package: ff1136
  - Speed Grade: -1



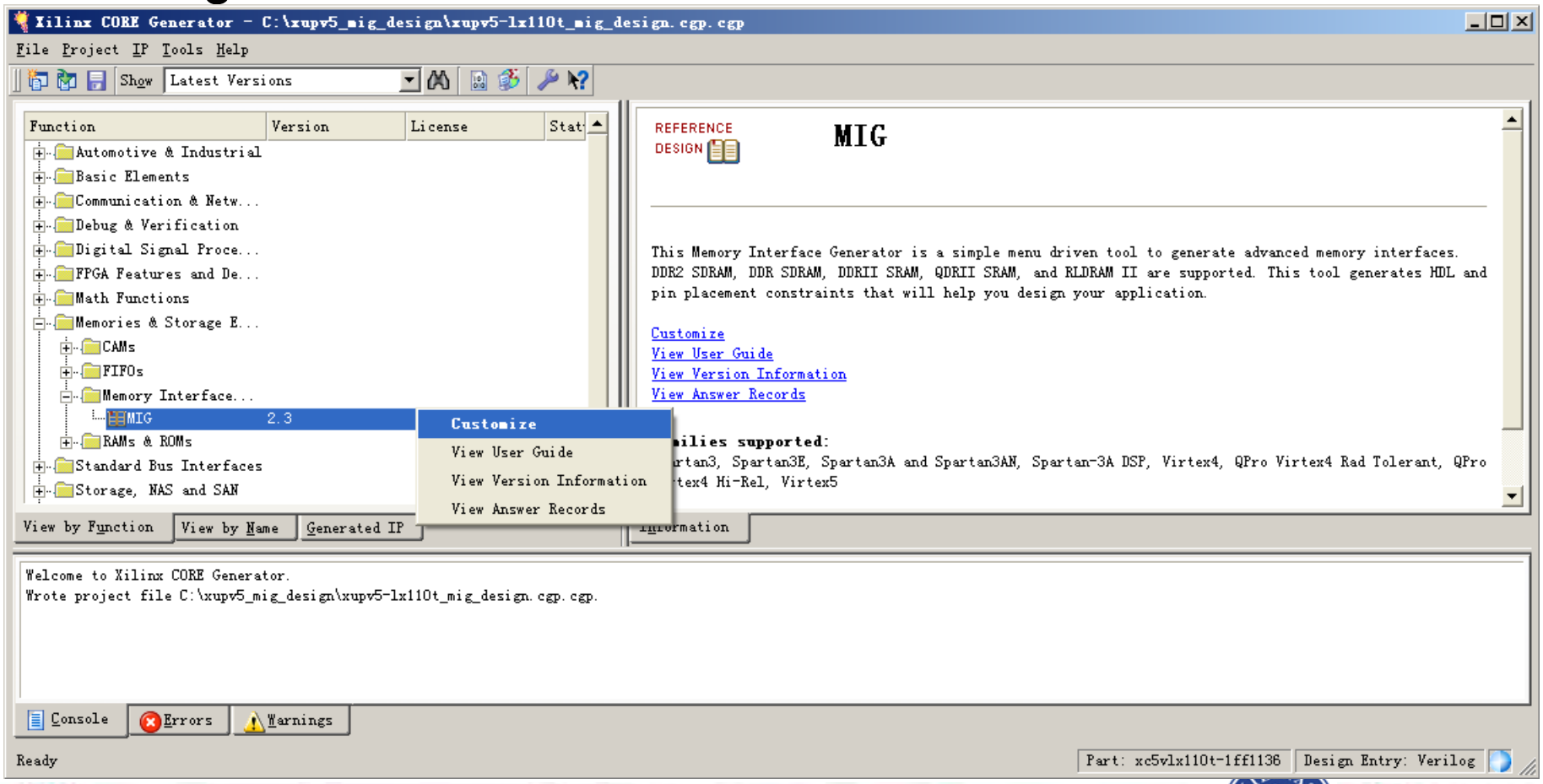
MIG Core Generation

- Set the Design Entry to Verilog
- Click OK



MIG Core Generation

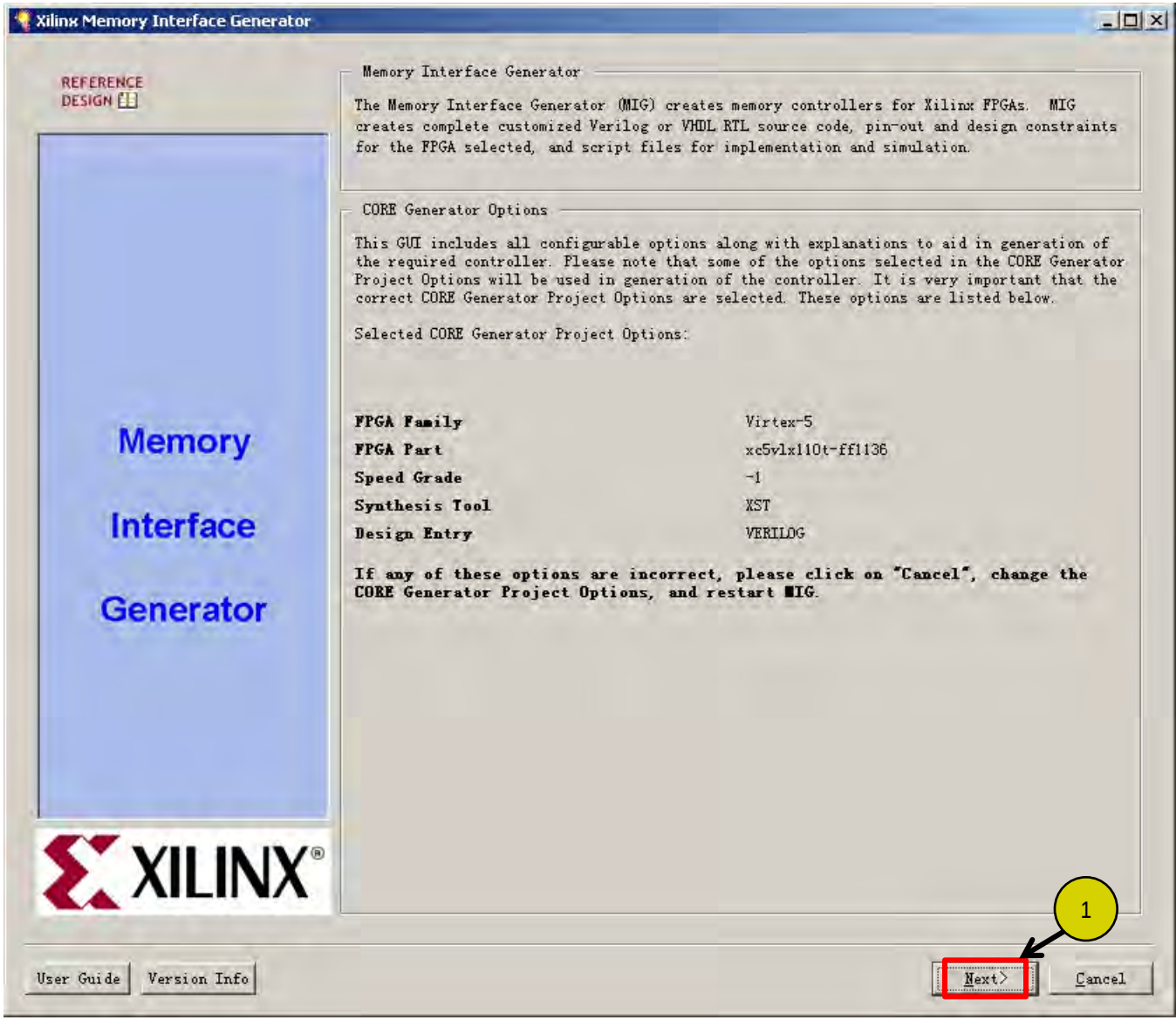
- Right click on the MIG 2.3 and select Customize



Note: See Demos On Demand for an online tutorial on the use of MIG.

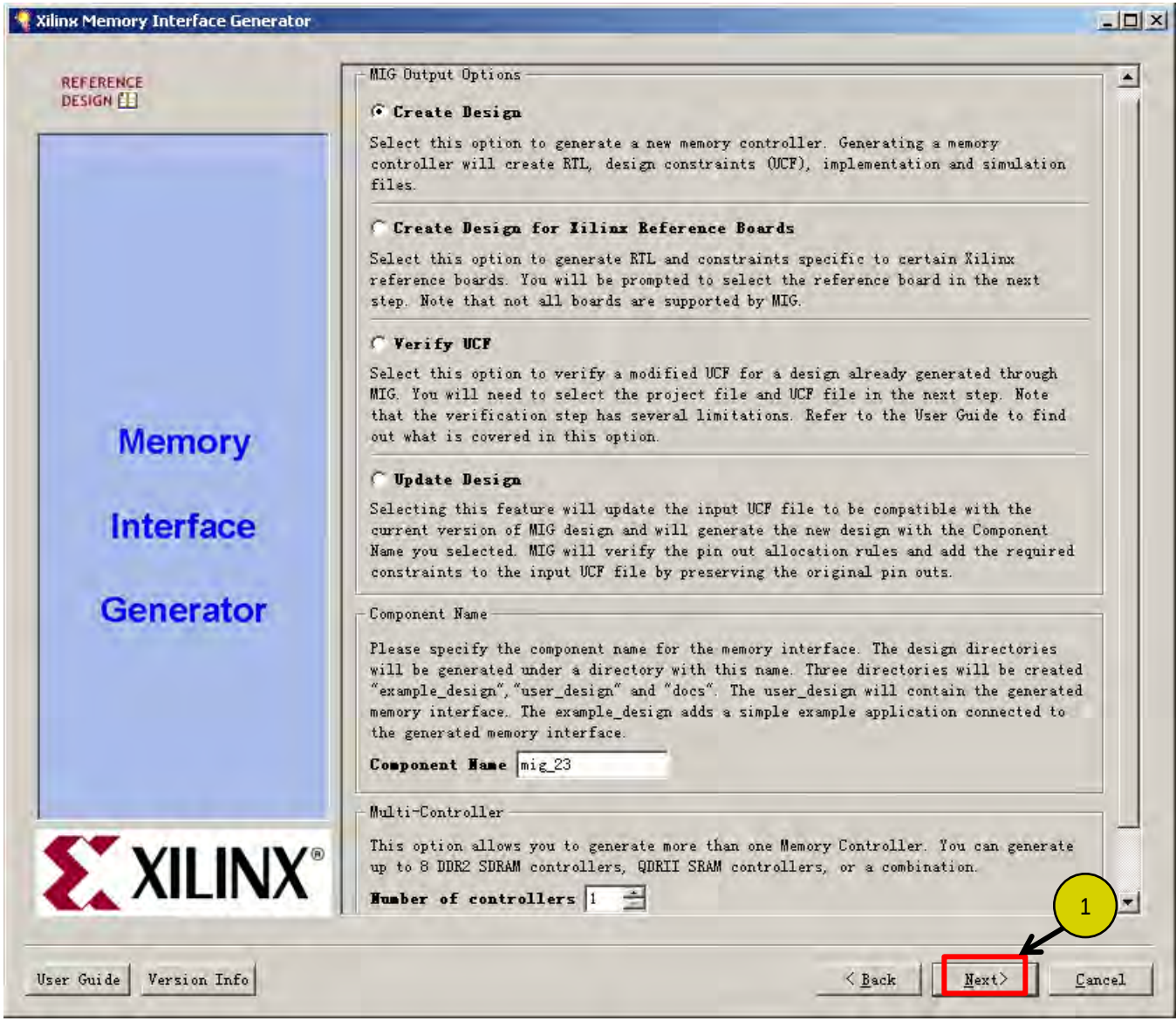
MIG

- Click Next(1)



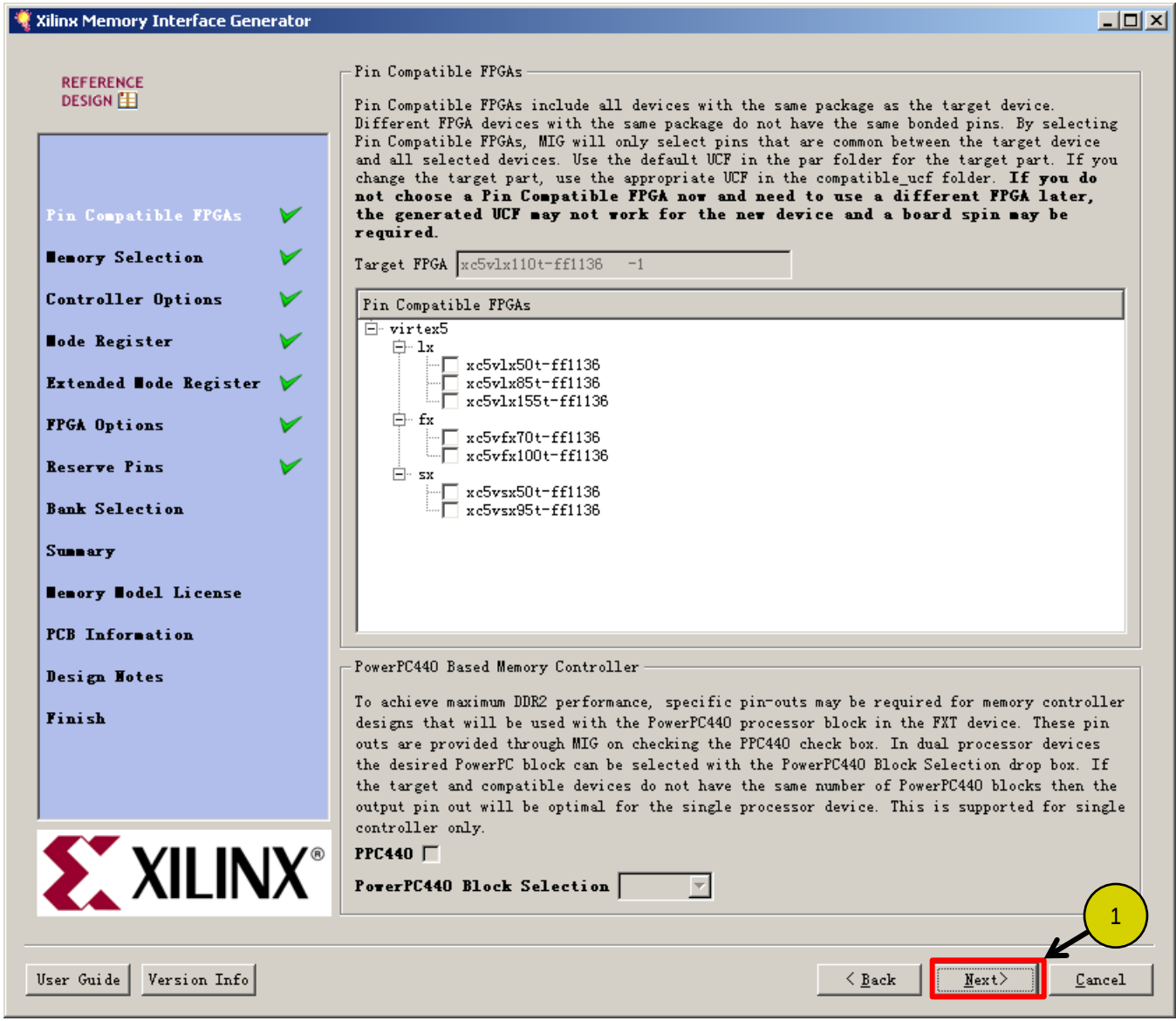
MIG

- Click Next(1)



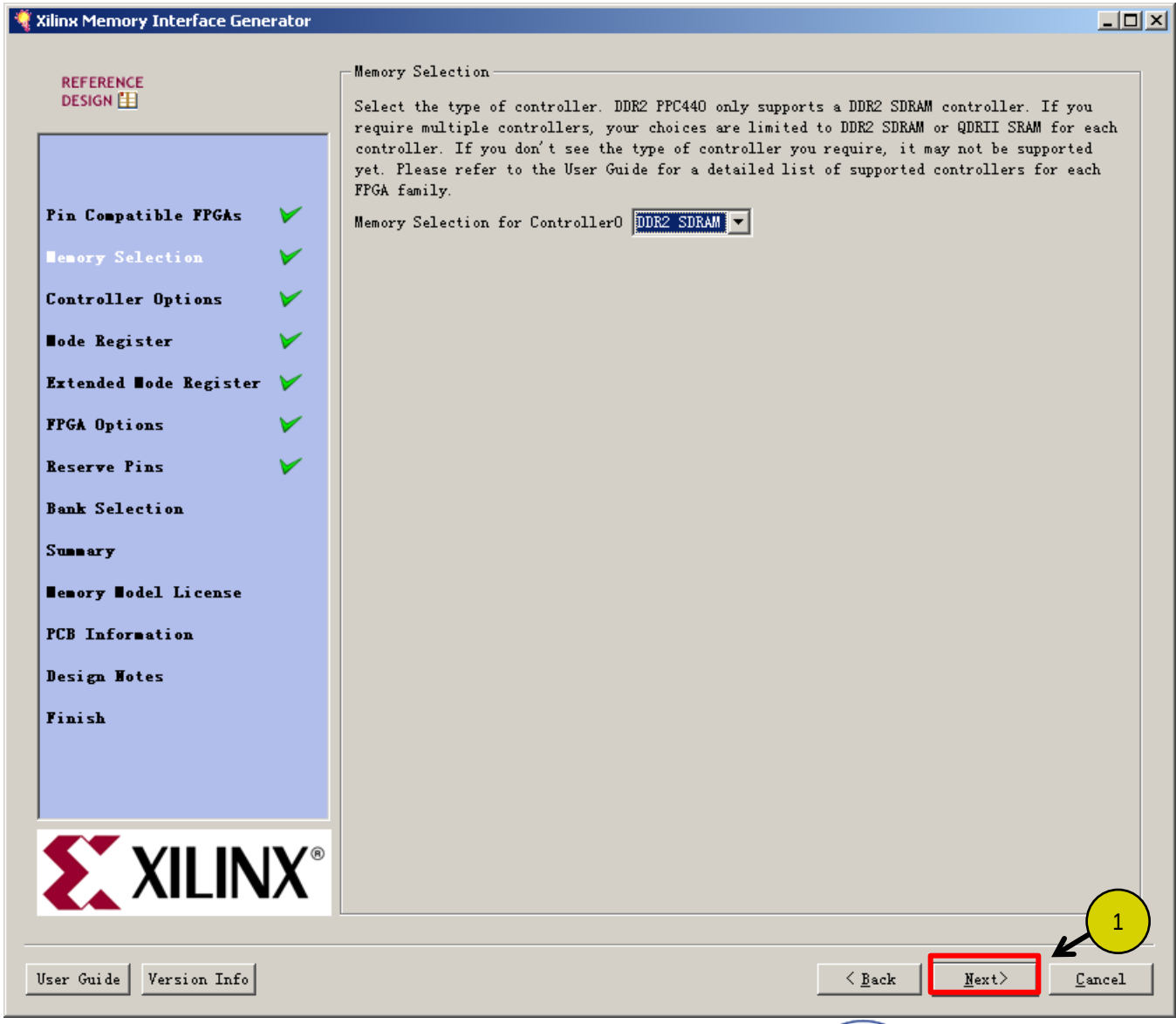
MIG

- Click Next(1)



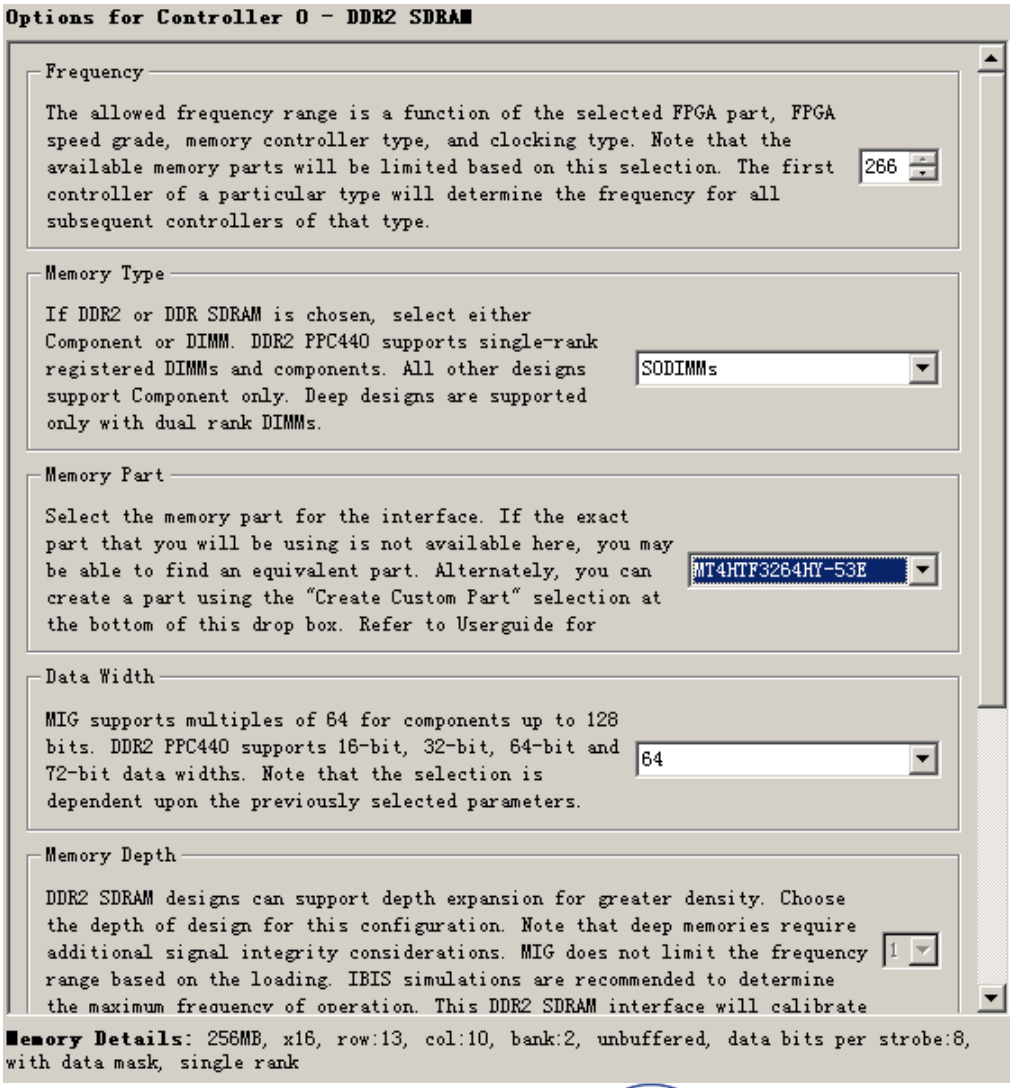
MIG

- Click Next(1)



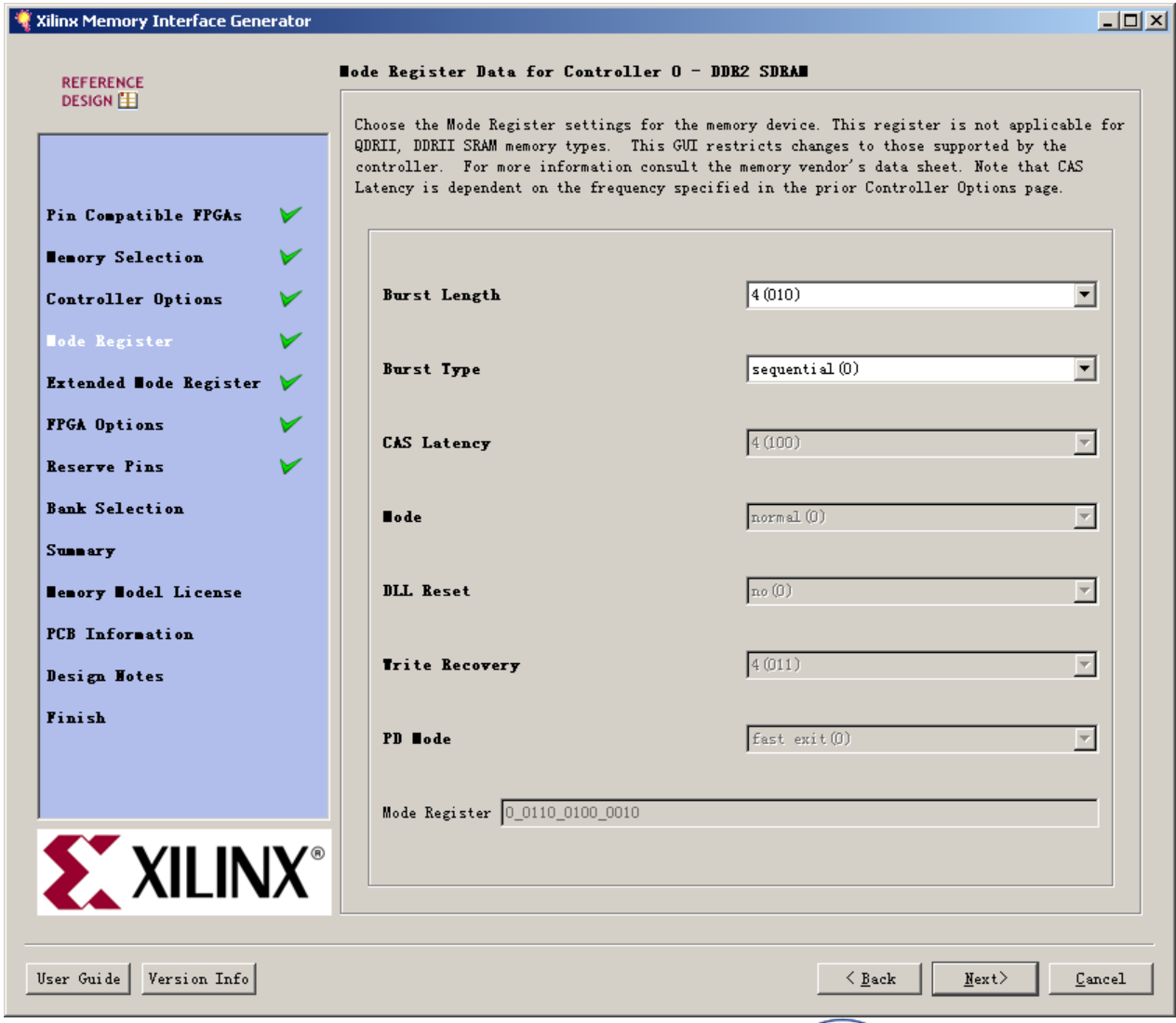
MIG

- MIG defaults to a maximum frequency of 266 for a Virtex-5 -1 speed grade selection
  - See UG086
- Set the Memory Type to SODIMMs
- Set the Memory part to MT4HTF3264HY-53E
- Click Next



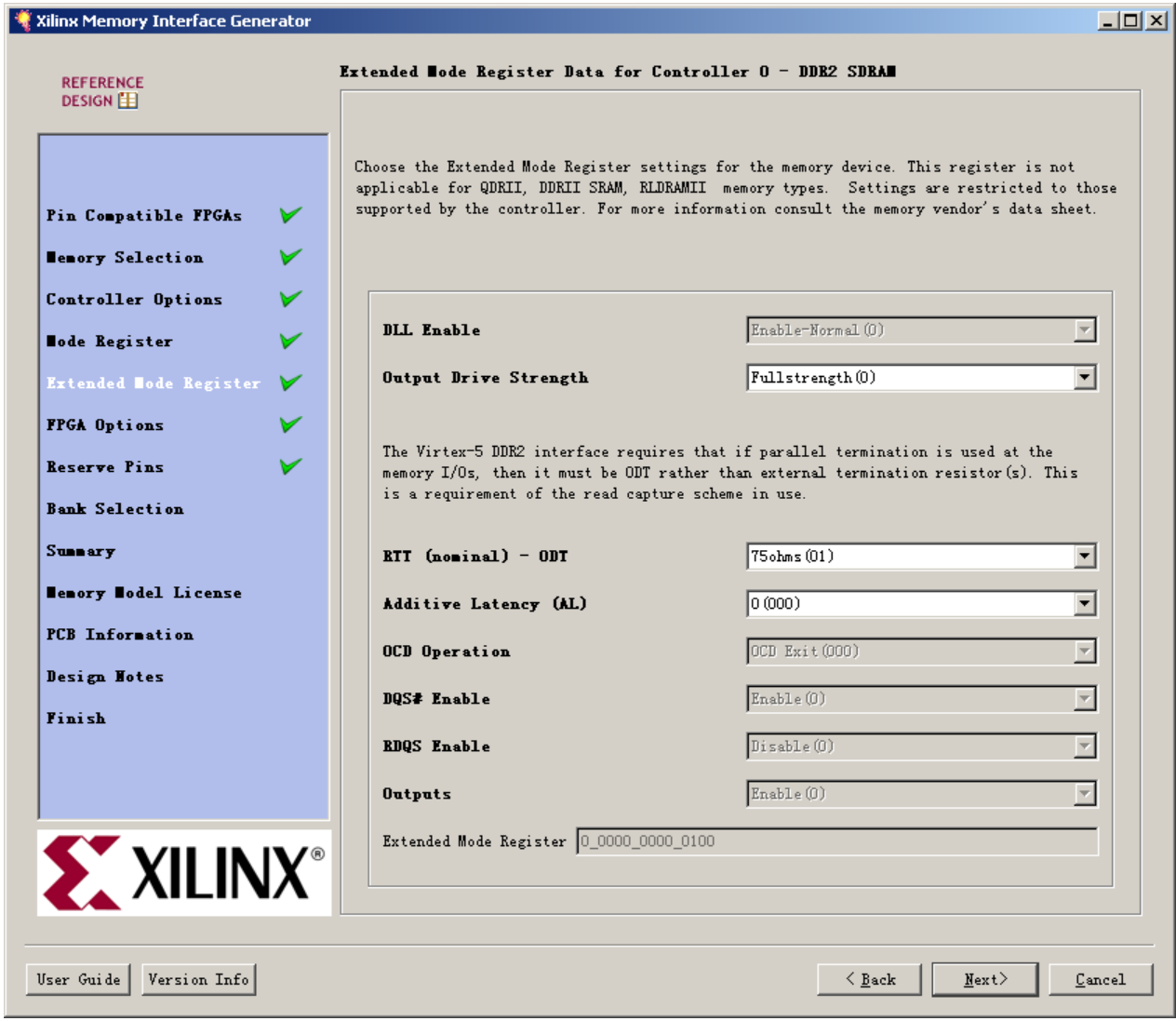
MIG

- Click Next on this screen



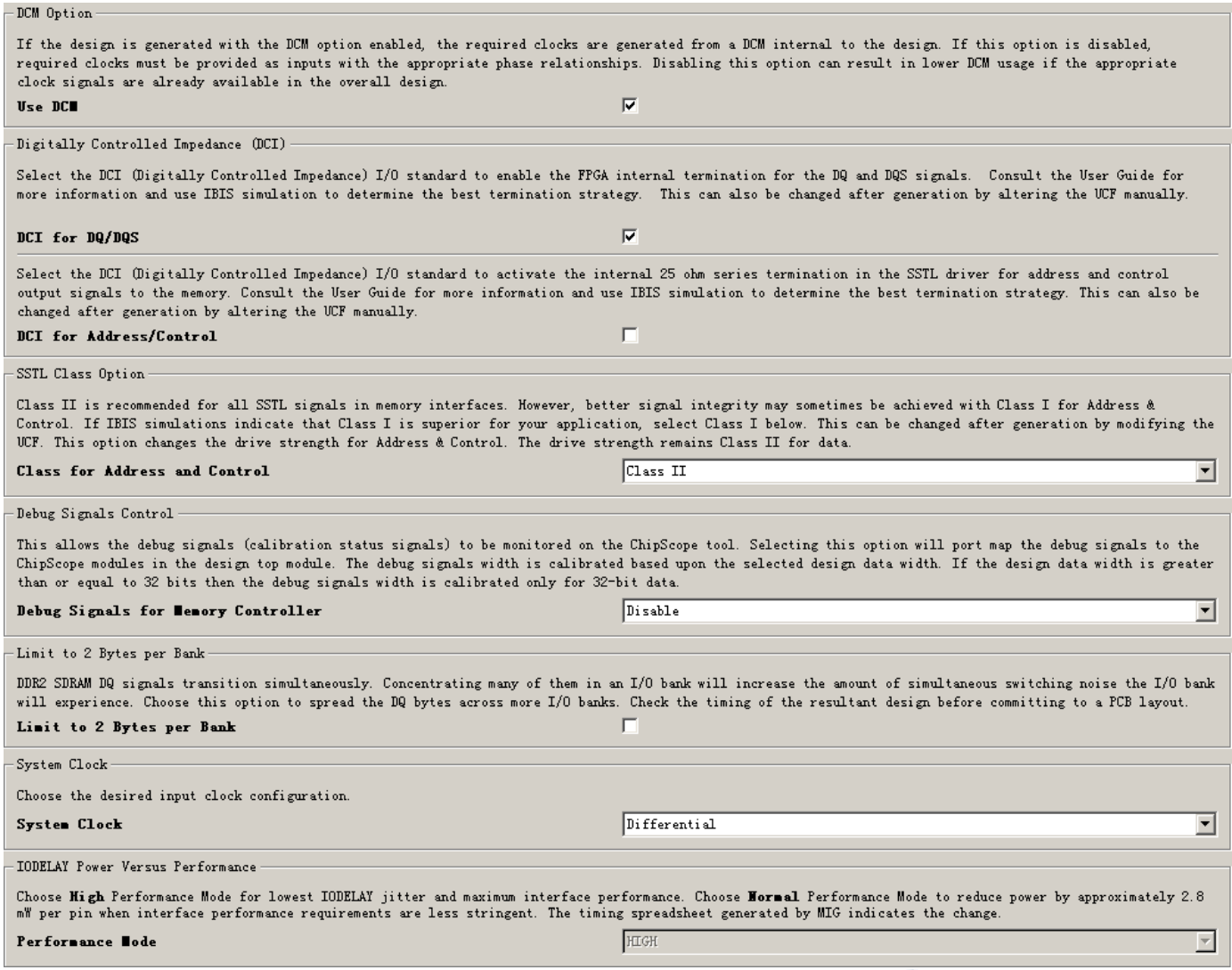
MIG

- Click Next on this screen



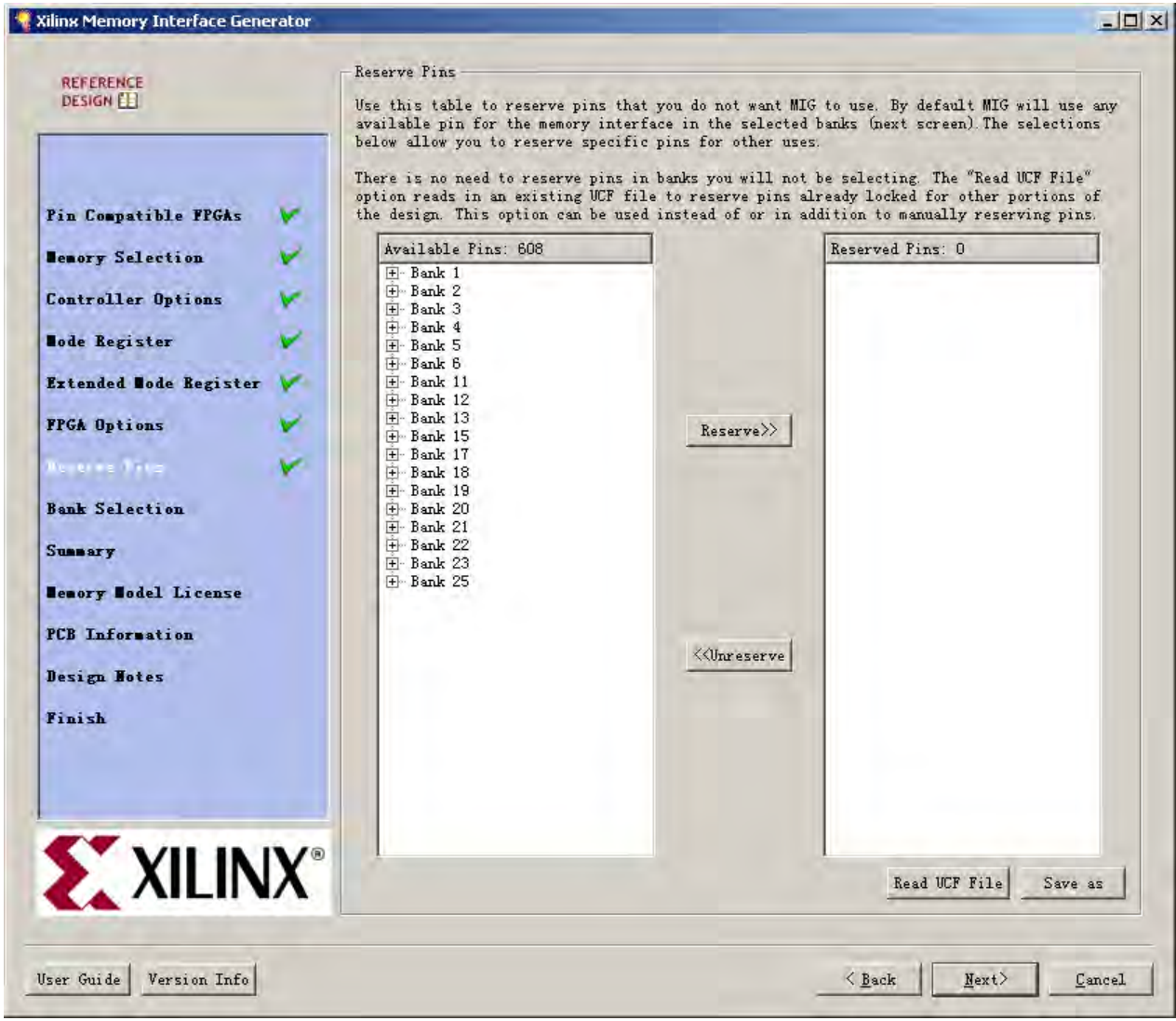
MIG

- Click Next on this screen



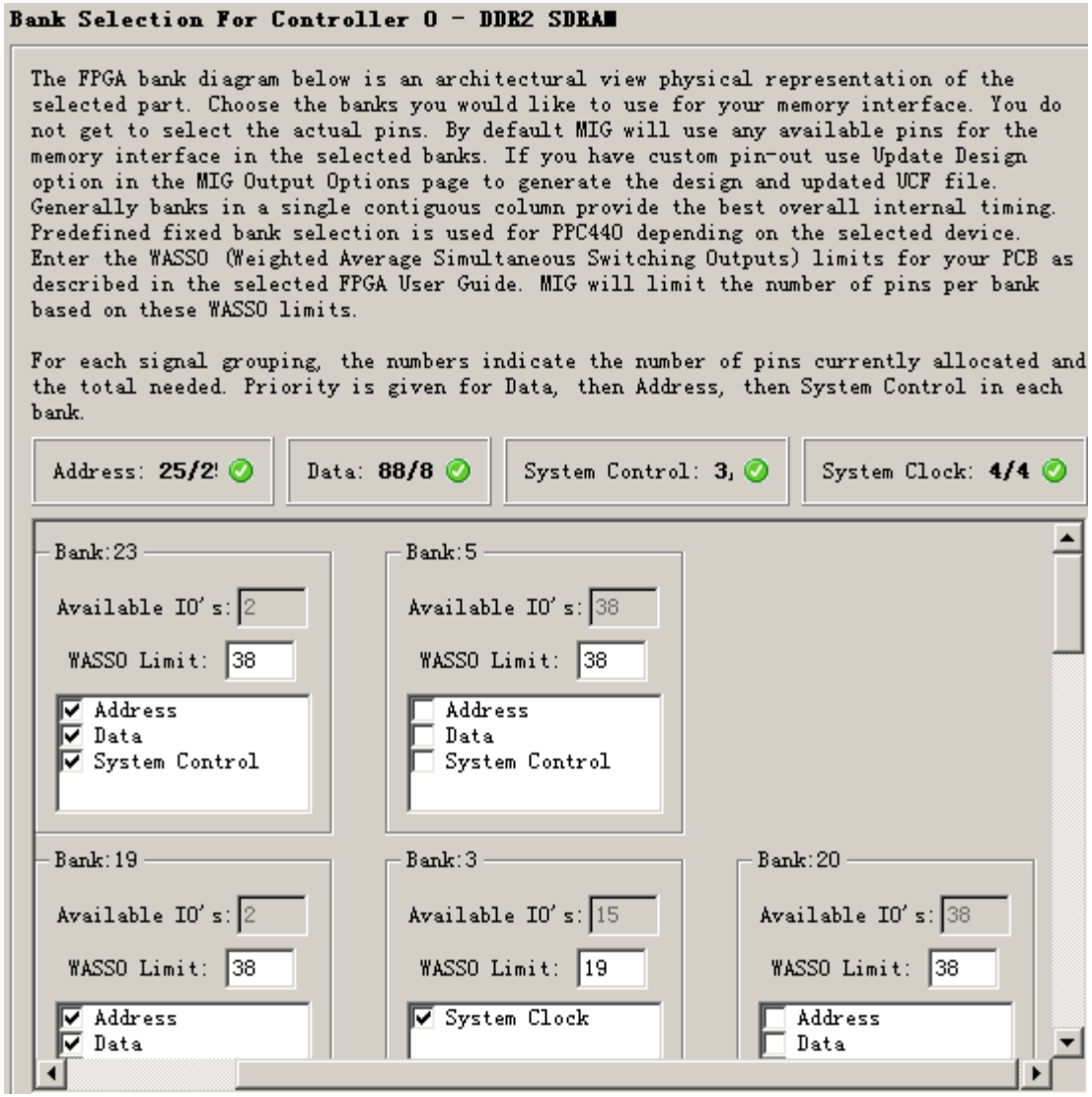
MIG

- Click Next on this screen



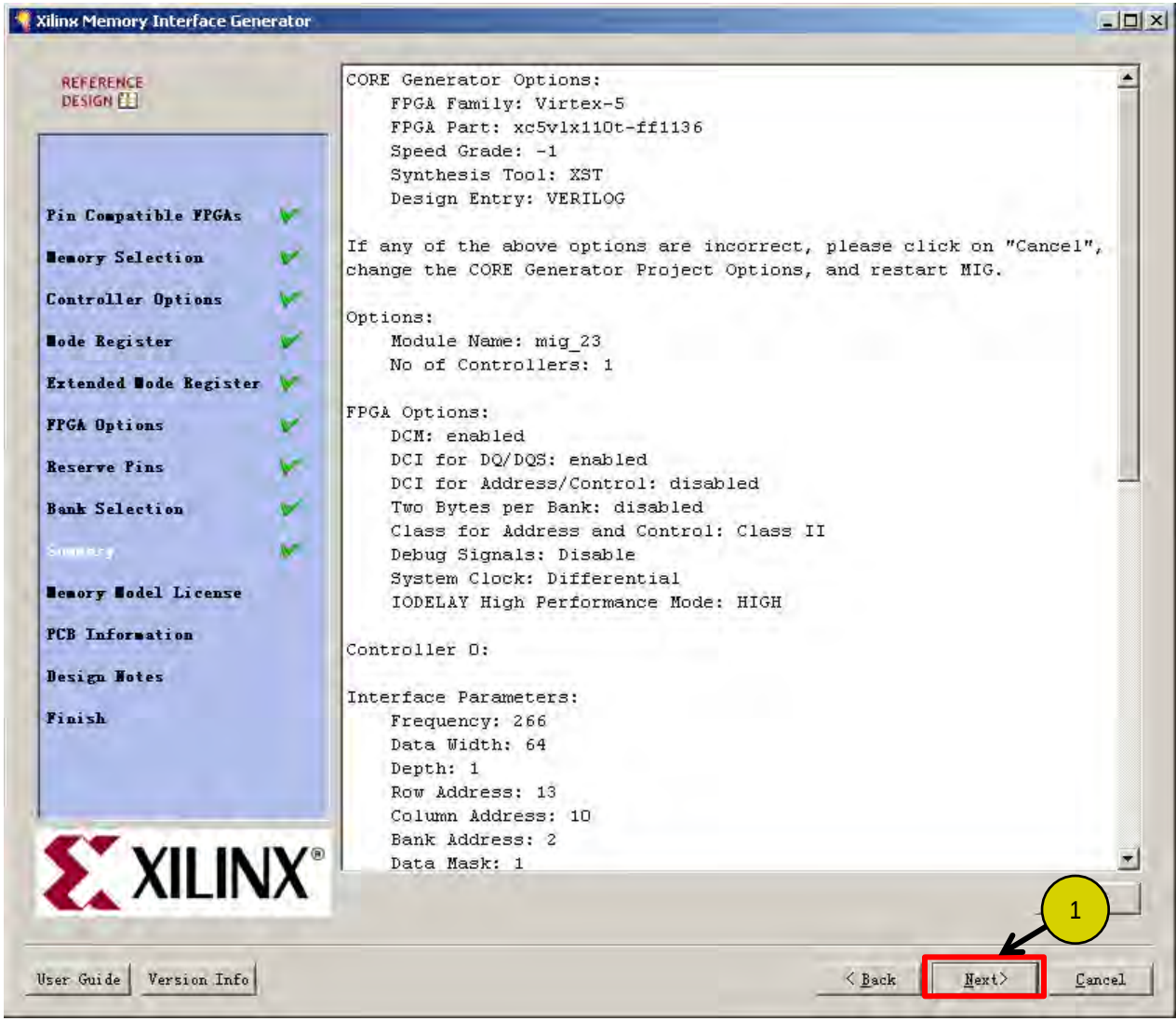
MIG

- Click Next on this screen



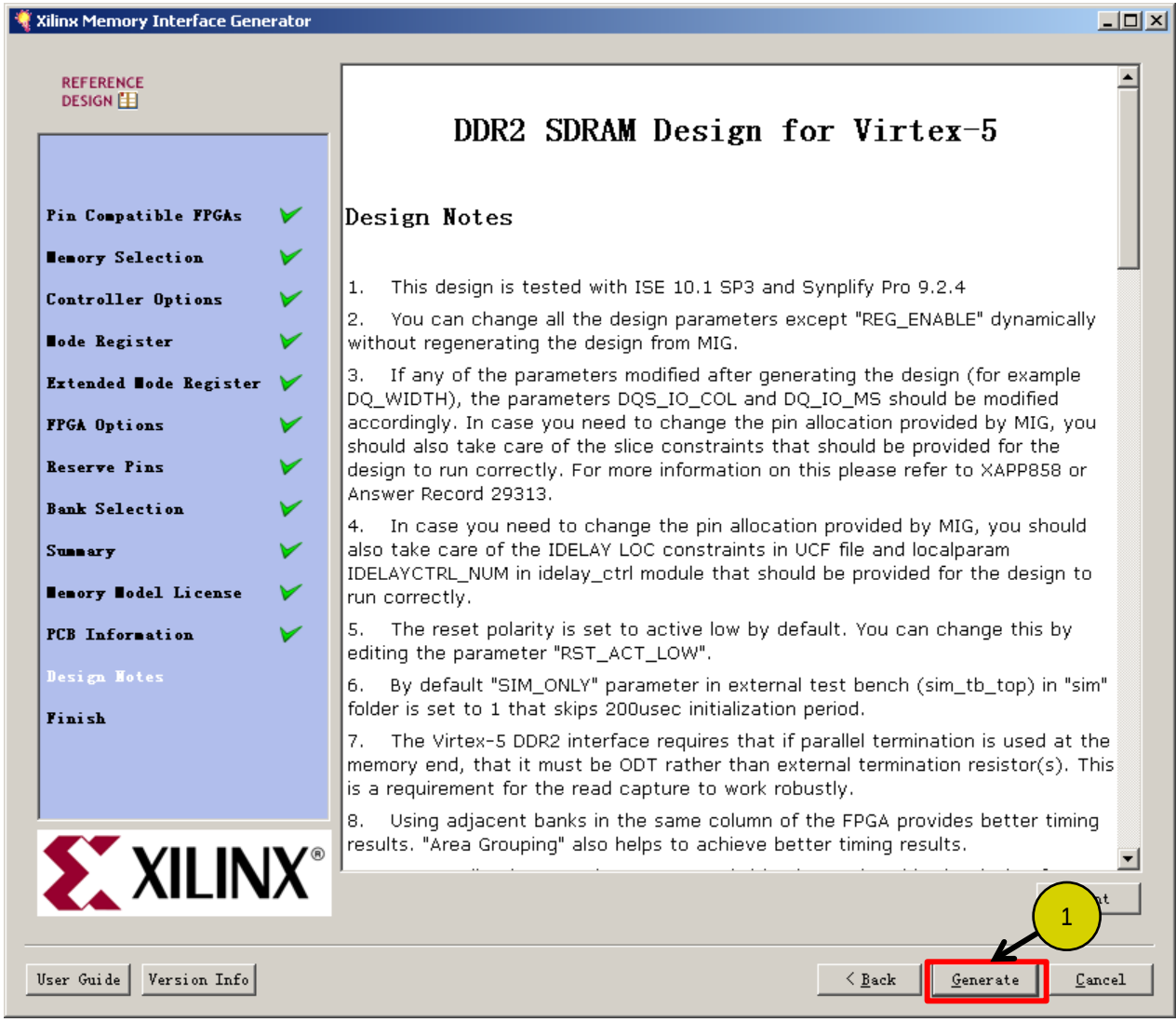
MIG

- Click Next(1)



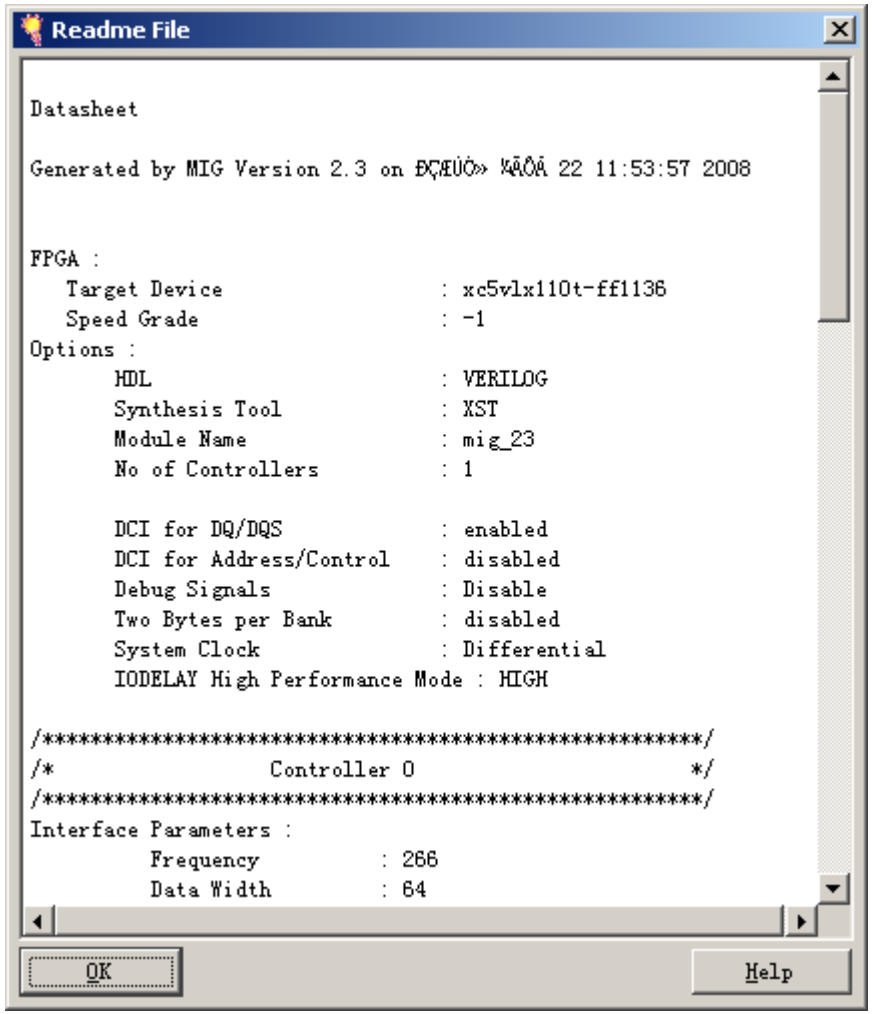
MIG

- Click Generate (1)
- Click Finish and select YES after generation



MIG

- After the MIG core finishes generating, click OK on the Datasheet window

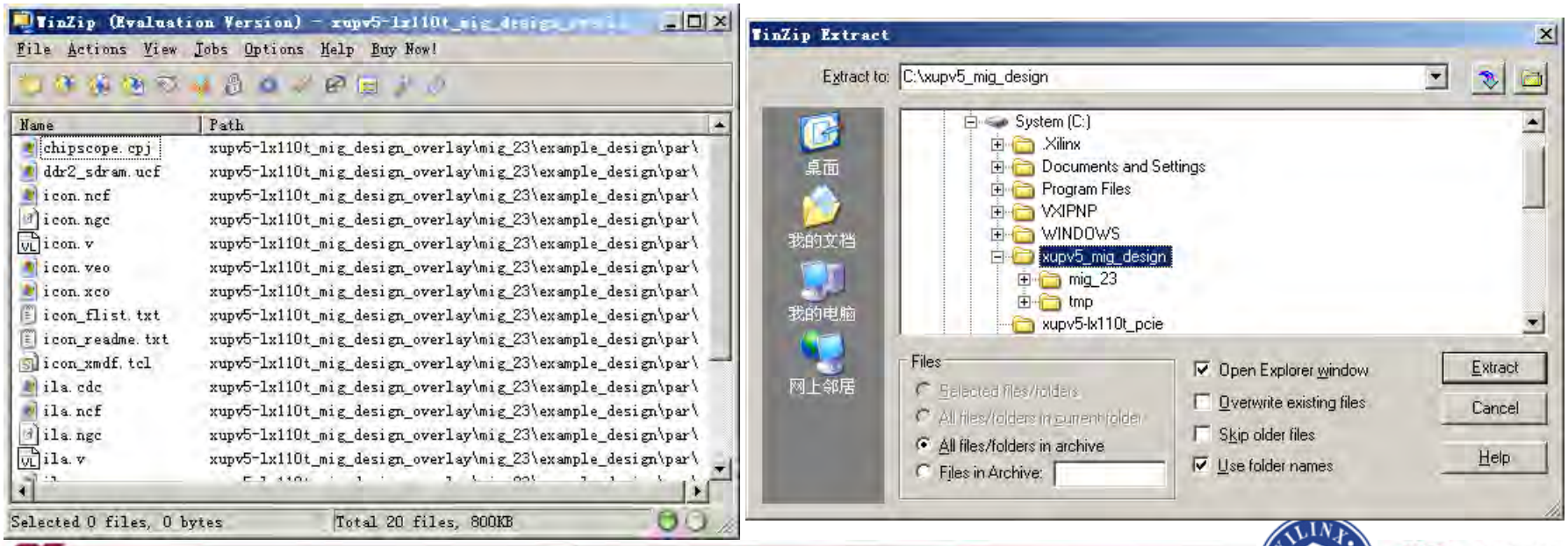


Design Modifications

- Add overlay files
  - XUPV5-LX110T specific UCF file as per Answer Record 29313
  - Pre-compiled ChipScope Pro design files used to validate the design
- Modify top level Verilog file
  - Support for XUPV5-LX110T Board as per AR 29313
  - Add ChipScope Pro to design

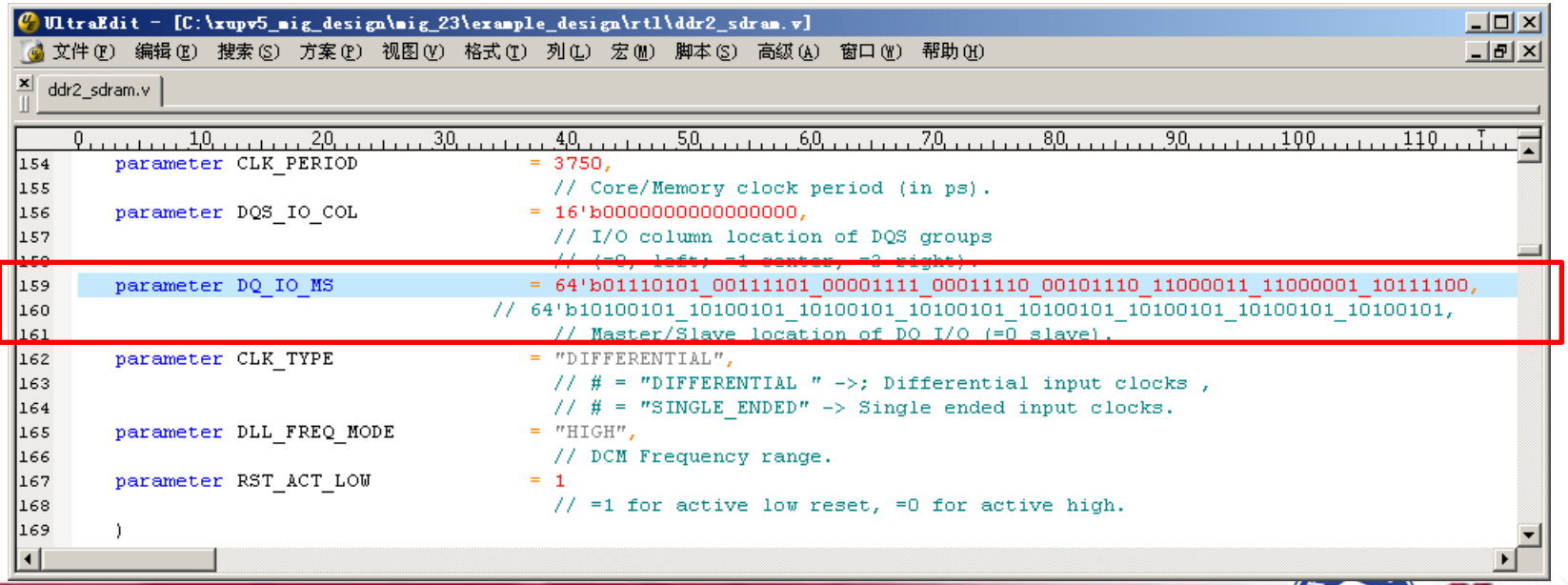
Add XUPV5-LX110T Files

- Unzip xupv5-lx110t_mig_design_overlay.zip file
  - Unzip to the xupv5_mig_design directory
  - See ChipScope Pro documentation for details on generating/instantiating the ICON and ILA cores



Modify Design for XUPV5-LX110T

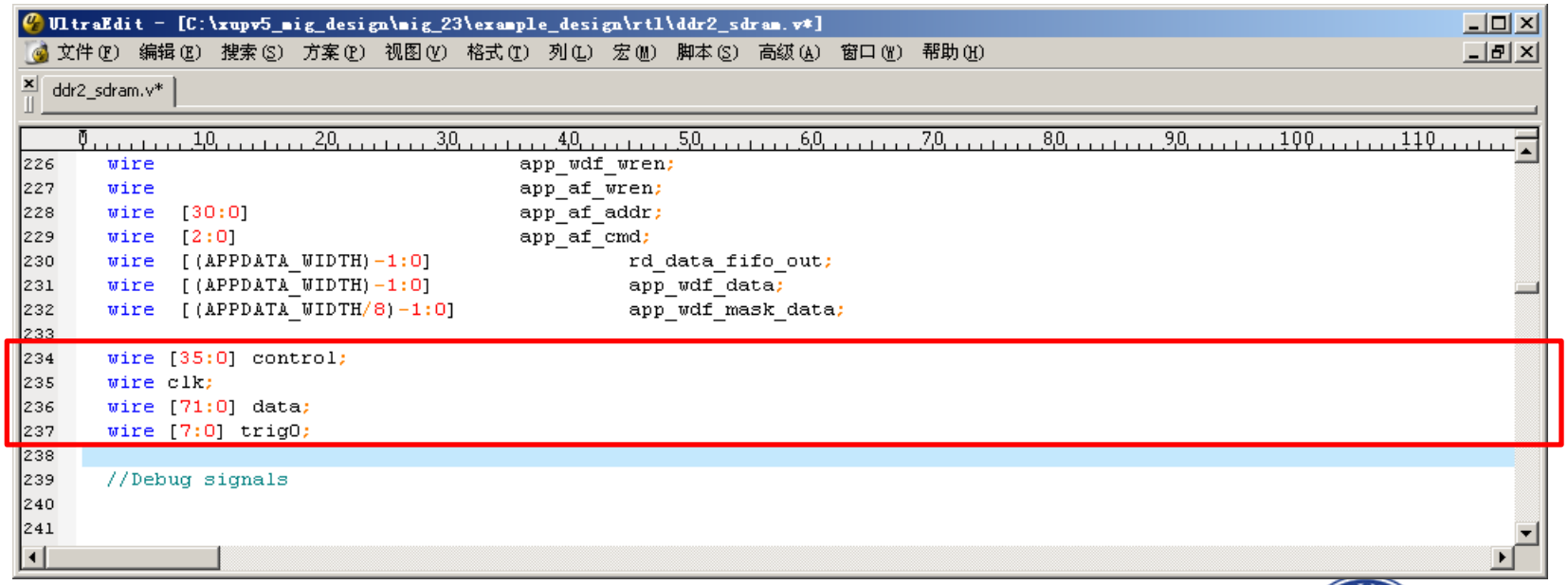
- Open the top-level Verilog file, mig_23\example_design\rtl\ddr2_sdram.v
  - Change the DQ_IO_MS parameter: 64'b10100101_10100101_10100101_10100101_10100101_10100101_10100101_10100101 To: 64'b01110101_00111101_00001111_00011110_00101110_11000011_11000001_10111100



Add ChipScope Pro

- Add these lines to the top-level Verilog file:

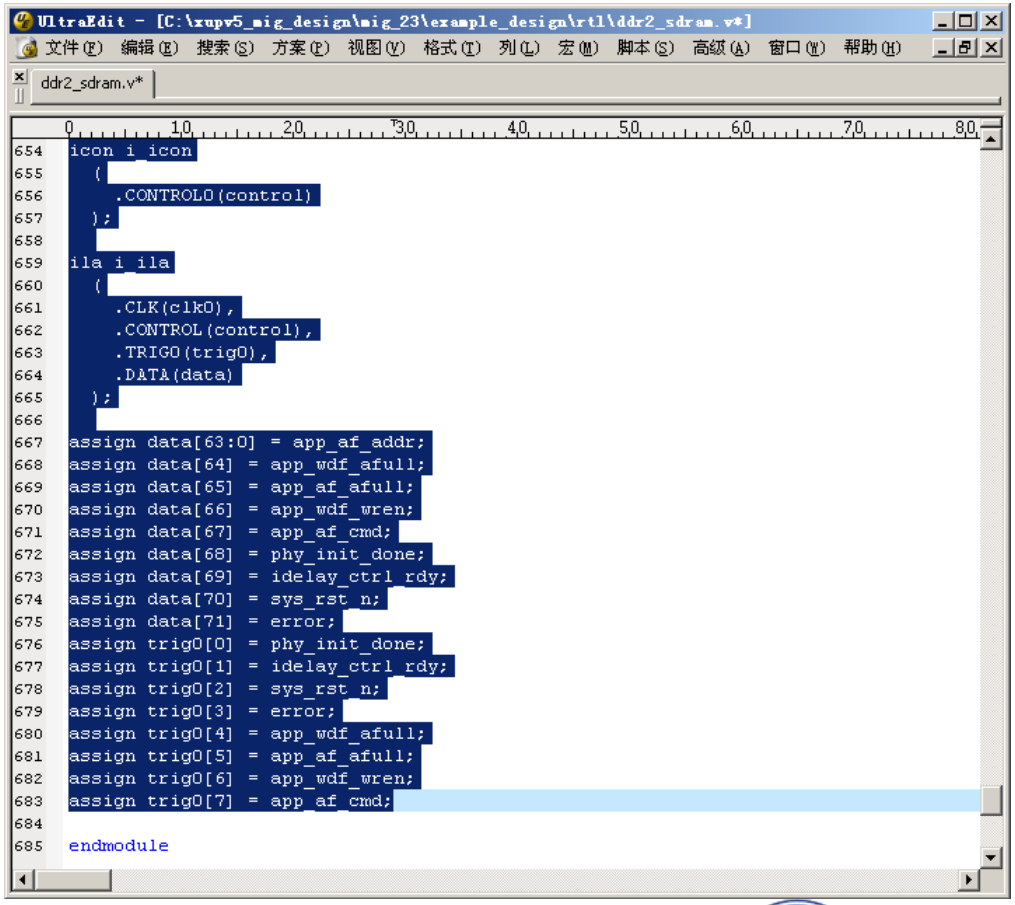
```
wire [35:0] control;
wire clk;
wire [71:0] data;
wire [7:0] trig0;
```



Add ChipScope Pro

- Add these lines to the top-level Verilog file before endmodule:

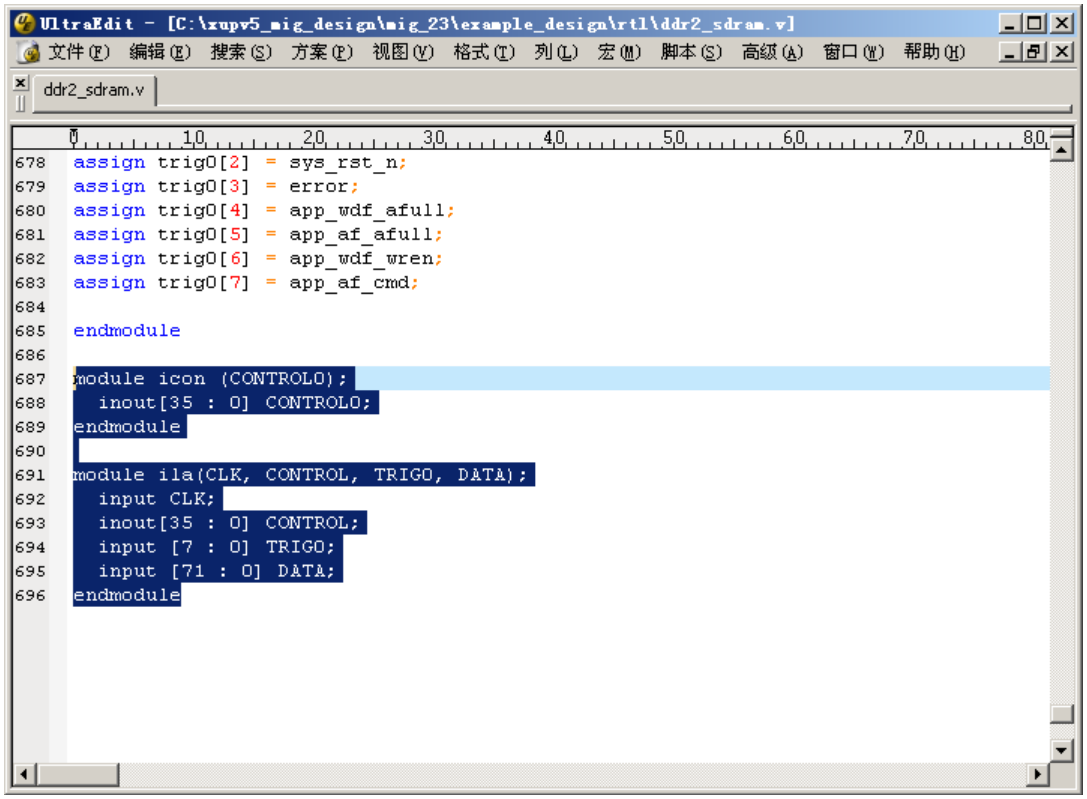
```
icon i_icon(.CONTROL0(control));
ila i_ila(.CLK(clk0),.CONTROL(control),
          .TRIG0(trig0),.DATA(data));
assign data[63:0] = app_af_addr;
assign data[64] = app_wdf_afull;
assign data[65] = app_af_afull;
assign data[66] = app_wdf_wren;
assign data[67] = app_af_cmd;
assign data[68] = phy_init_done;
assign data[69] = idelay_ctrl_rdy;
assign data[70] = sys_rst_n;
assign data[71] = error;
assign trig0[0] = phy_init_done;
assign trig0[1] = idelay_ctrl_rdy;
assign trig0[2] = sys_rst_n;
assign trig0[3] = error;
assign trig0[4] = app_wdf_afull;
assign trig0[5] = app_af_afull;
assign trig0[6] = app_wdf_wren;
assign trig0[7] = app_af_cmd;
```



Add ChipScope Pro

- Add these lines to the top-level Verilog file after endmodule:

```
module icon (CONTROL0);
inout[35 : 0] CONTROL0;
endmodule
module ila(CLK, CONTROL,
                TRIG0, DATA);
input CLK;
inout[35 : 0] CONTROL;
input [7 : 0] TRIG0;
input [71 : 0] DATA;
endmodule
```

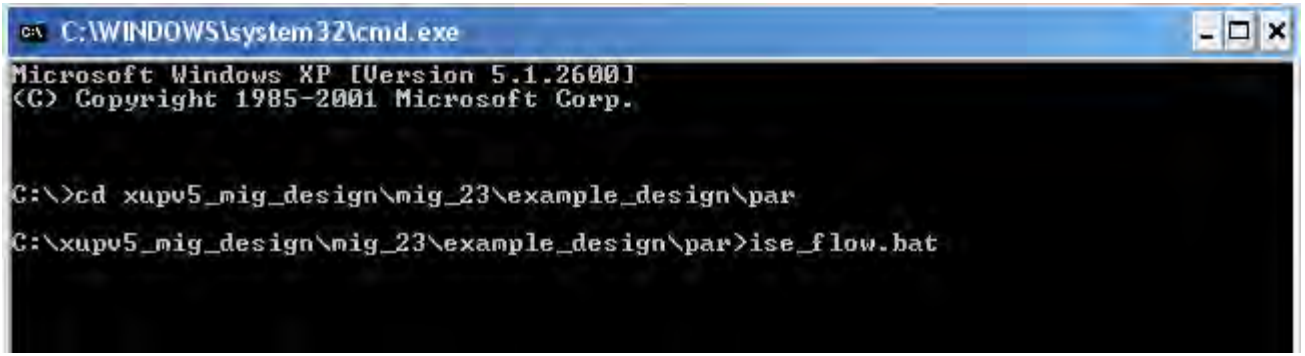


Generate Bitstream

- Start a windows command shell and enter these commands:

  cd xupv5_mig_design\mig_23\example_design\par

  ise_flow.bat

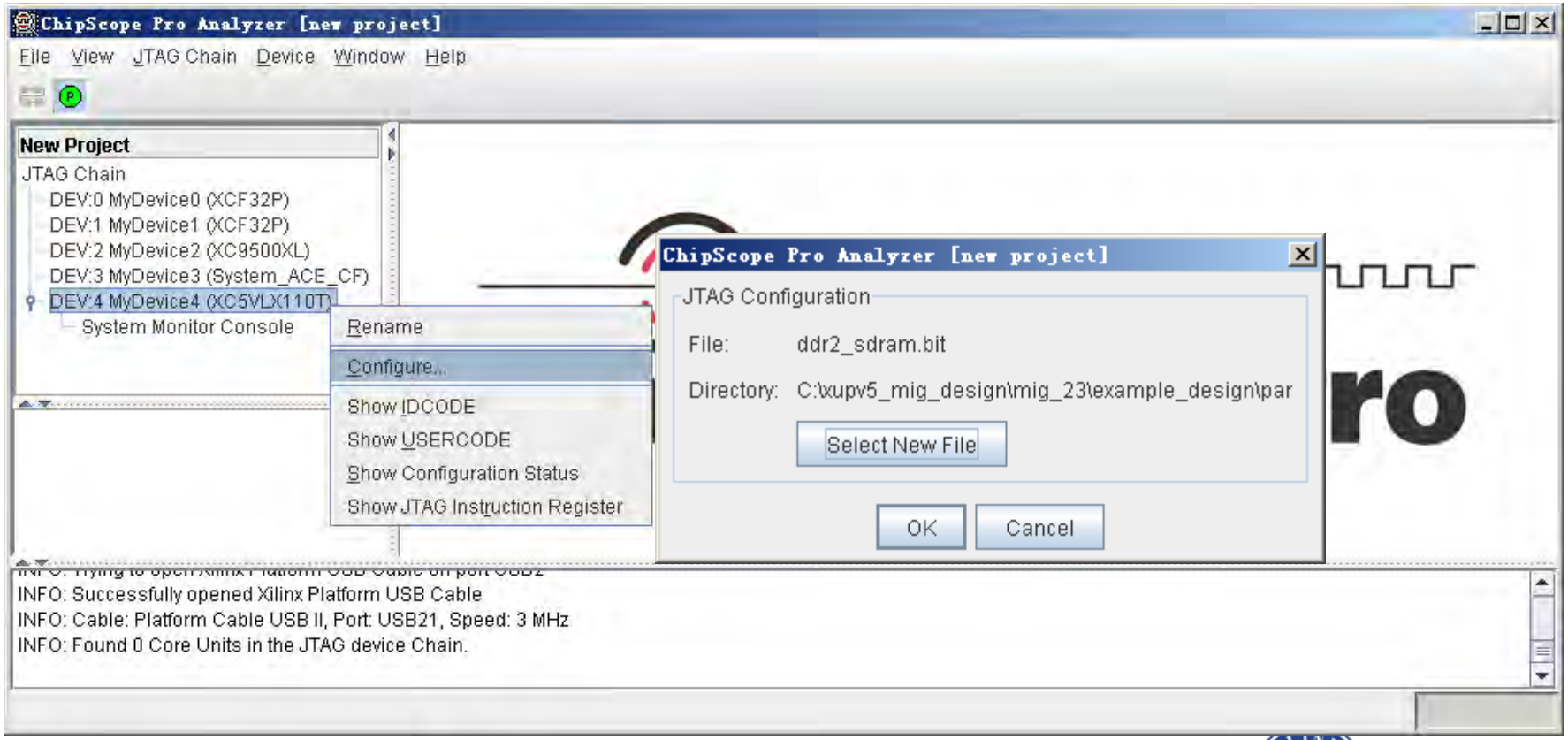


ChipScope Pro Setup

- After the design compiles, open ChipScope Pro Analyzer
- Click on the Open Cable Button (1)

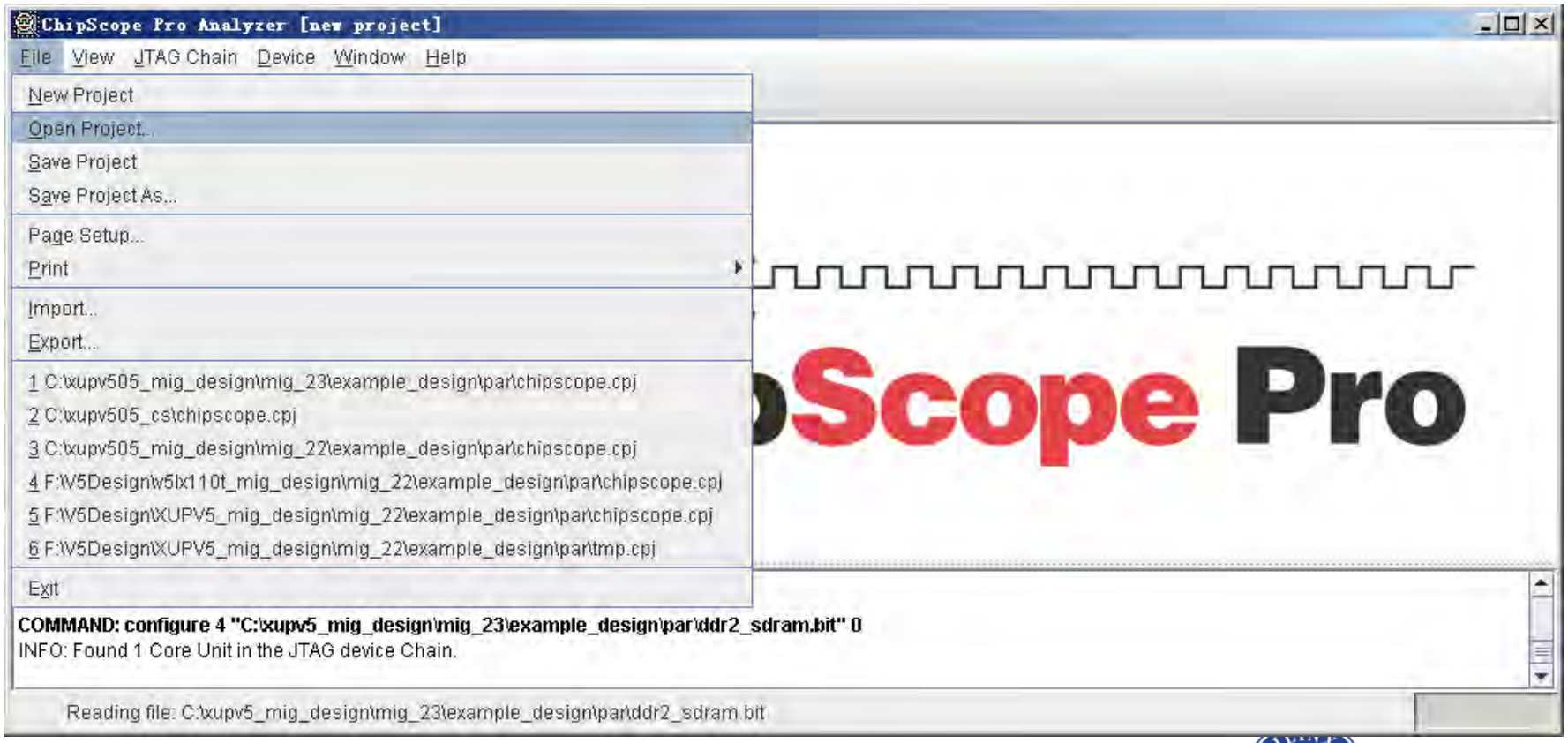
ChipScope Pro Setup

- Select Device →DEV:4 MyDevice4 (XC5VLX110T) →Configure…
- Select <Design Path>\mig_23\example_design\par\ddr2_sdram.bit



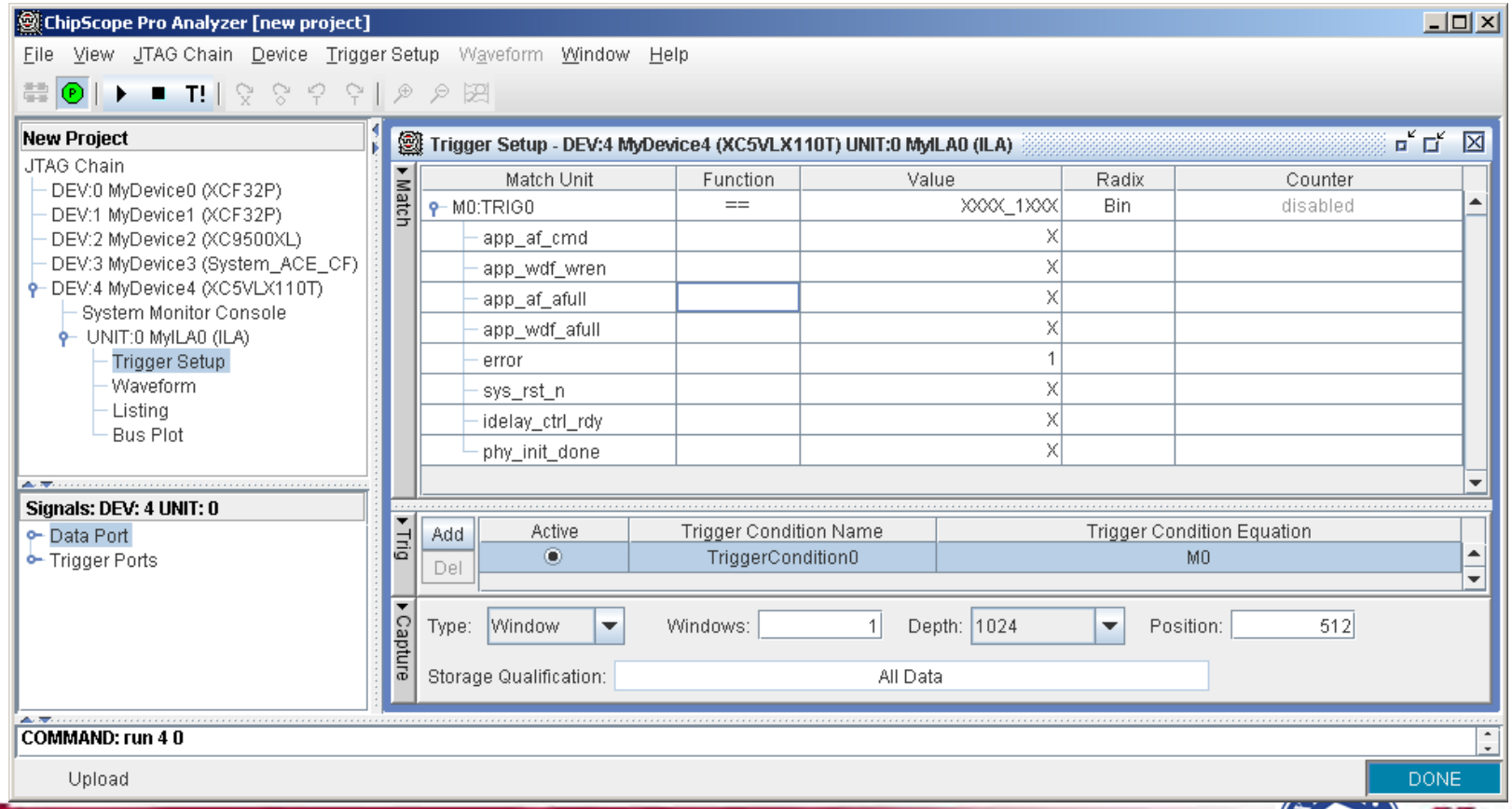
ChipScope Pro Setup

- Select File →Open Project…
- Select <Design Path>\mig_23\example_design\par\chipscope.cpj



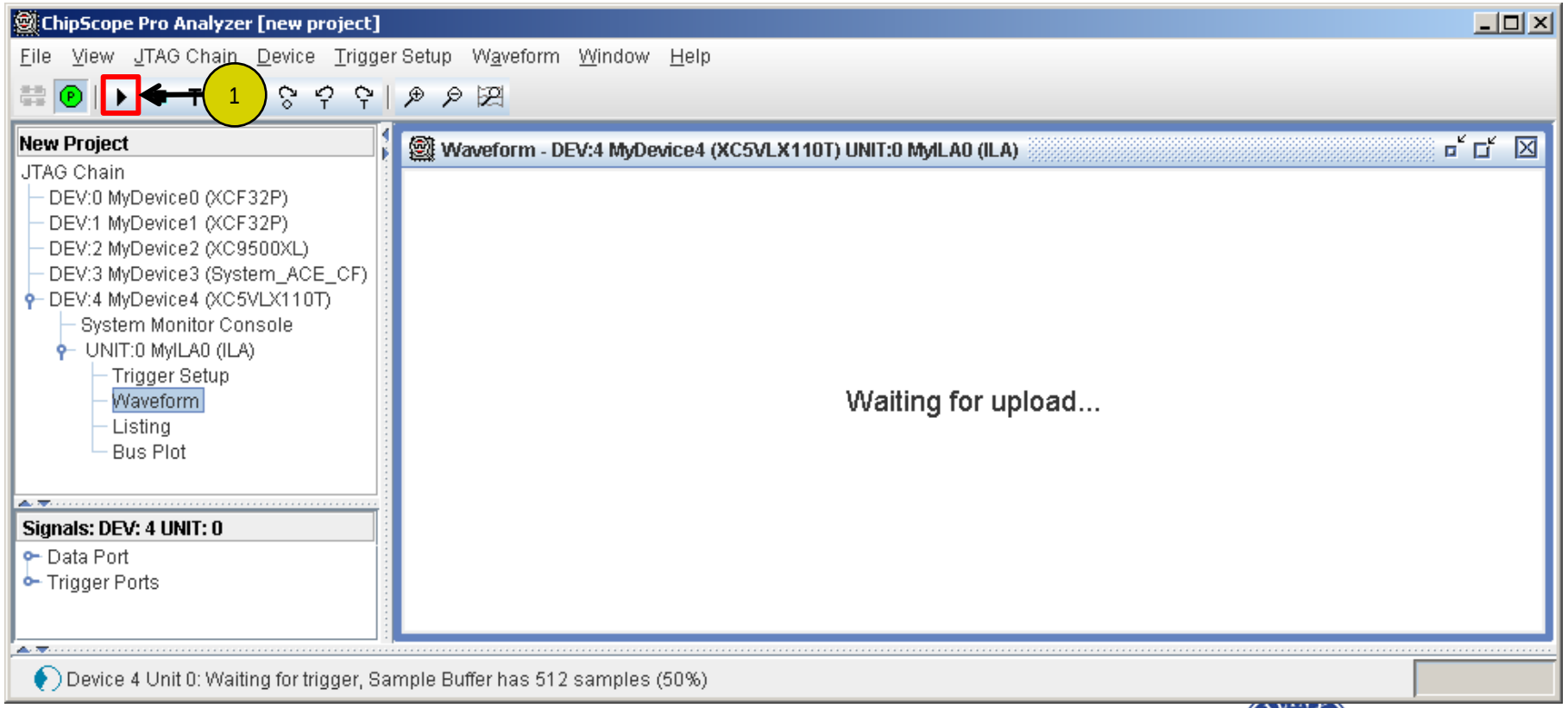
ChipScope Pro Setup

- Click on Trigger Setup to view trigger settings
- The error bit value should be set to 1



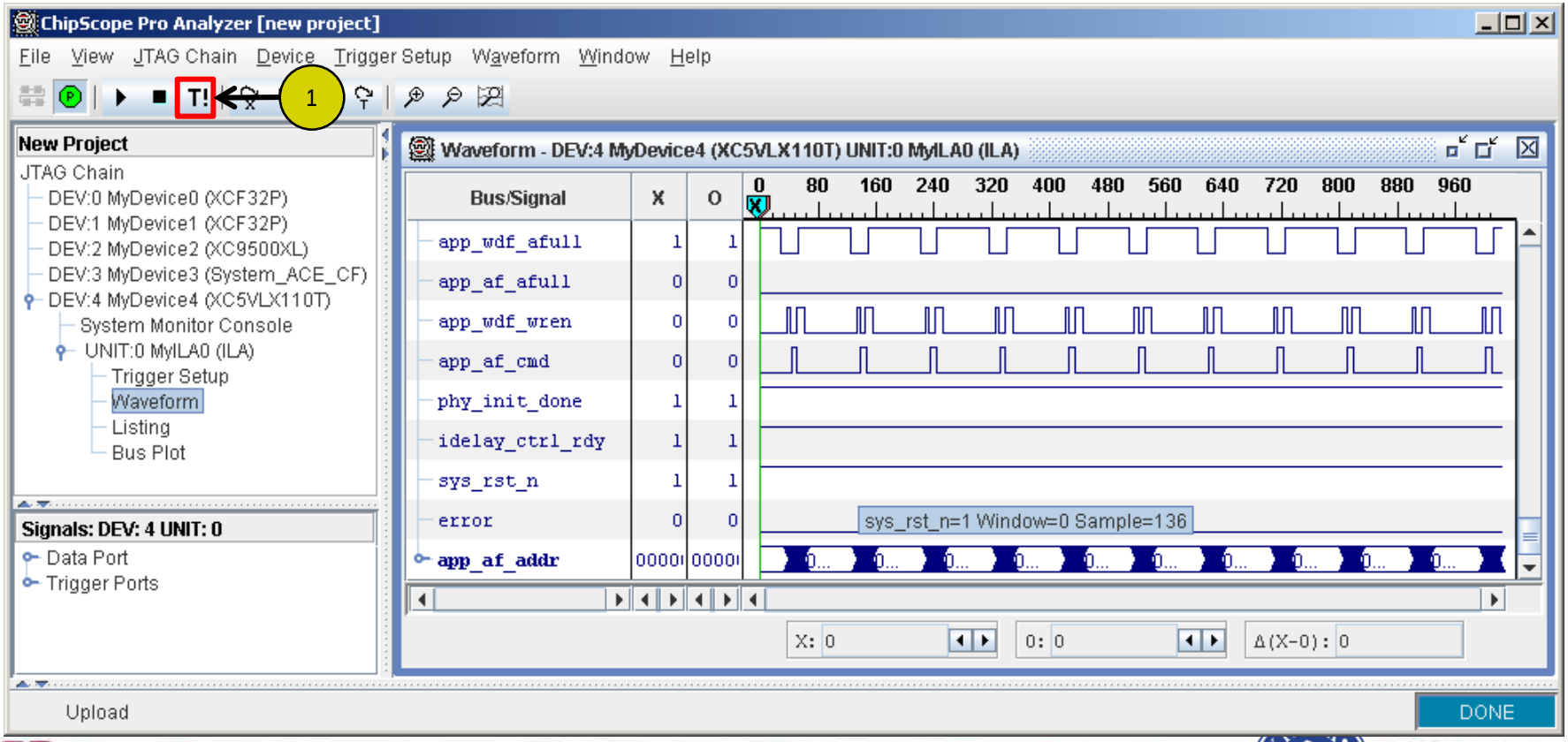
ChipScope Pro Setup

- Click on Waveform; click the Arm Trigger button (1)
- Detection of an error will cause ChipScope Pro to trigger



ChipScope Pro Setup

- To force a trigger, in order to view the waveform, click the T! button (1)



XUPV5-LX110T DDR2 Verified at 200 MHz

- Virtex-5 –1 speed grade device supports 200 MHz DDR2 operation as stated in the Virtex-5 datasheet
- The XUPV5-LX110T SODIMM supports 200 MHz
  - Supplied DDR2 SODIMM is rated for 266 MHz operation
- The MIG test design and ChipScope Pro Analyzer verify operation of the XUPV5-LX110T with a Virtex-5 –1 speed grade device, at the specified clock rate of 200 MHz

Appendix

XUPV5-LX110T DDR2 at 266 MHz

- An external signal generator was used to clock the MIG test design on the XUPV5-LX110T at the maximum clock rate selectable in the MIG tool, 266 MHz
- Supplied DDR2 SODIMM is rated for 266 MHz operation
- The MIG test design and ChipScope Pro Analyzer verify operation of the XUPV5-LX110T at the maximum selectable MIG clock rate of 266 MHz for a -1 speed grade device
  - See UG086

Documentation

- Virtex-5 FPGA User Guide
  http://www.xilinx.com/support/documentation/user_guides/ug190.pdf
- Virtex-5 Packaging and Pinout Specification
  http://www.xilinx.com/support/documentation/user_guides/ug195.pdf
- Demos on Demand–Memory Interface Solutions with Xilinx FPGAs
  http://www.demosondemand.com/clients/xilinx/001/page_new2/index.asp#35
- Xilinx Memory Interface Generator (MIG) 2.1 User Guide
  http://www.xilinx.com/support/software/memory/protected/ug086.pdf
- Memory Interfaces Made Easy with Xilinx FPGAs and the Memory Interface Generator
  http://www.xilinx.com/support/documentation/white_papers/wp260.pdf