ML505/ML506/ML507 Getting Started Tutorial

For ML505/ML506/ML507 Evaluation Platforms

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Revision History

The following table shows the revision history for this document.

Date	Version	Revision
11/29/06	1.0	Initial Xilinx release.
01/09/07	1.0.1	Minor typographical correction.
02/16/07	2.0	Added support for ML506 boards.
04/04/08	2.1	Updated “My Own Linear Flash Image Demonstration,” page 26.
05/19/08	3.0	Added support for ML507 boards.
07/29/08	3.0.1	Added document’s part number: PN 0402745-01.
10/09/08	3.0.2	Corrected step 5, page 29 for ML507 boards.
06/18/09	3.0.3	Updated tool versions and links.

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About This Guide

The *ML505/ML506/ML507 Getting Started Tutorial* provides step-by-step instructions for setting up and using the Virtex®-5 FPGA ML505, ML506, and ML507 Evaluation Platforms (referred to as the ML50*x* board in this guide). The ML50*x* board comes with a number of pre-installed demonstrations. This tutorial guides you through these demonstrations and provides instructions to run them on the ML50*x* platforms.

Additional Documentation

The following documents are also available for download at http://www.xilinx.com/virtex5.

- Virtex-5 Family Overview

  The features and product selection of the Virtex-5 family are outlined in this overview.

- Virtex-5 FPGA Data Sheet: DC and Switching Characteristics

  This data sheet contains the DC and Switching Characteristic specifications for the Virtex-5 family.

- Virtex-5 FPGA User Guide

  This user guide includes chapters on:

  - Clocking Resources
  - Clock Management Technology (CMT)
  - Phase-Locked Loops (PLLs)
  - Block RAM
  - Configurable Logic Blocks (CLBs)
  - SelectIO™ Resources
  - SelectIO Logic Resources
  - Advanced SelectIO Logic Resources

- Virtex-5 FPGA RocketIO™ GTP Transceiver User Guide

  This guide describes the RocketIO GTP transceivers available in the Virtex-5 LXT and SXT platforms.

- Virtex-5 FPGA RocketIO GTX Transceiver User Guide

  This guide describes the RocketIO GTX transceivers available in the Virtex-5 FXT platform.

- Embedded Processor Block in Virtex-5 FPGAs Reference Guide

  This reference guide is a description of the embedded processor block available in the Virtex-5 FXT platform.

- Virtex-5 FPGA Tri-Mode Ethernet Media Access Controller

  This guide describes the dedicated Tri-Mode Ethernet Media Access Controller available in the Virtex-5 LXT, SXT, and FXT platforms.

- Virtex-5 FPGA Integrated Endpoint Block User Guide for PCI Express Designs

  This guide describes the integrated Endpoint blocks in the Virtex-5 LXT, SXT, and FXT platforms used for PCI Express® designs.

- XtremeDSP Design Considerations

  This guide describes the XtremeDSP™ slice and includes reference designs for using the DSP48E slice.

- Virtex-5 FPGA Configuration Guide

  This all-encompassing configuration guide includes chapters on configuration interfaces (serial and SelectMAP), bitstream encryption, Boundary-Scan and JTAG configuration, reconfiguration techniques, and readback through the SelectMAP and JTAG interfaces.

- Virtex-5 FPGA Packaging and Pinout Specifications

  This specification includes the tables for device/package combinations and maximum I/Os, pin definitions, pinout tables, pinout diagrams, mechanical drawings, and thermal specifications.

- Virtex-5 PCB Designer's Guide

  This guide provides information on PCB design for Virtex-5 devices, with a focus on strategies for making design decisions at the PCB and interface level.

Additional Support Resources

To search the database of silicon and software questions and answers, or to create a technical support case in WebCase, see the Xilinx website at: http://www.xilinx.com/support.

Typographical Conventions

This document uses the following typographical conventions. An example illustrates each convention.

Convention	Meaning or Use	Example
Italic font	References to other documents	See the Virtex-5 *FPGA Configuration Guide* for more information.
	Emphasis in text	The address (F) is asserted *after* clock event 2.
Underlined Text	Indicates a link to a web page.	http://www.xilinx.com/virtex5

Online Document

The following conventions are used in this document:

Convention	Meaning or Use	Example
Blue text	Cross-reference link to a location in the current document	See the section "Additional Documentation" for details. Refer to "System Monitor Primitive" for details.
Red text	Cross-reference link to a location in another document	See Figure 2 in the *Virtex-5 Data Sheet*
Blue, underlined text	Hyperlink to a website (URL)	Go to http://www.xilinx.com for the latest documentation.

ML505/ML506/ML507 Getting Started Tutorial

Overview

The ML505, ML506, and ML507 Evaluation Platforms (referred to as ML50*x* boards in this guide [Ref 1]) come with a number of pre-installed demonstrations [Ref 2]. This tutorial guides you through these demonstrations and provides instructions to run them on ML50*x* boards.

Some demonstrations interact with a computer or an external device. The following additional equipment is also recommended:

- DVI or VGA monitor
- Computer speaker with audio cable
- Ethernet port and an RJ-45 Ethernet cable
- USB keyboard (without a built-in USB hub)
- Null modem serial cable
- CompactFlash (CF) reader/writer for the computer
- Xilinx download cable (Parallel Cable III/IV or Platform Cable USB) with JTAG flying wires adapter

Additional information and support material is located at:

- ML505 - http://www.xilinx.com/ml505
- ML506 - http://www.xilinx.com/ml506
- ML507 - http://www.xilinx.com/ml507

The procedures for running the pre-installed *Getting Started* demonstrations are identical for the ML505, ML506 and ML507. See the ML505/ML506/ML507 Known Issues Web page for pertinent board and tools related answer records.

Related Xilinx Documents

Prior to using the ML50*x* Evaluation Platform, users should be familiar with Xilinx resources. See "References," page 31 for direct links to Xilinx documentation. See the following locations for additional documentation on Xilinx tools and solutions:

- EDK: www.xilinx.com/edk
- ISE: www.xilinx.com/ise
- Answer Browser: www.xilinx.com/support
- Intellectual Property: www.xilinx.com/ipcenter

Board Setup

1. Position the ML50*x* board so the Xilinx logo is in the lower left corner.
2. Make sure the power switch located in the upper right corner is in the OFF position.
3. Locate the CF card slot (on the back side of the ML50*x* board), and carefully insert the System ACE™ CF card with its front label facing away from the board. Figure 1 shows the back side of the board with the CF card properly inserted.

   Note: The CF card provided with your board might differ.

   Caution! Be careful when inserting or removing the CF card from the slot. Do *not* force it.

Figure 1: **ML50*x* Evaluation Platform with CF Card**

4. Connect the AC power cord to the power supply brick. Plug the power supply adapter cable into the ML50*x* board. Plug in the power supply to AC power.
5. Set SW3, the configuration address and mode DIP switch, to `00010101` (Figure 2). DIP SW3 is located in the top left corner of the ML50*x* below the PS/2 connectors.

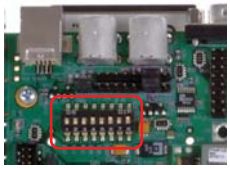

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Figure 2: **Configuration DIP Switch Settings**

6. Connect a null modem serial cable between your computer and the ML50*x* board, and open a serial terminal program:
   - Select **Start** → **Programs** → **Accessories** → **Communications** → **HyperTerminal**
   - In the Connection Description window, type **9600** in the Name box, then click **OK**
   - In the Connect To window, click **Cancel**
   - In the 9600-HyperTerminal window, select **File** → **Properties**
     - Select the **Connect To** tab
     - Select **COM1** in the Connect using box (see Figure 3)
     - Click **Configure...**

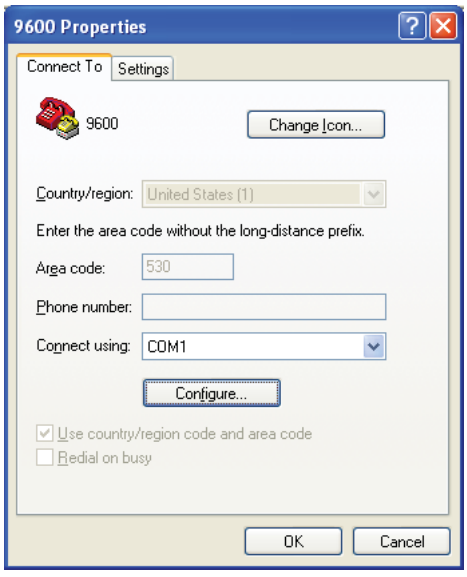

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Figure 3: **HyperTerminal Setup and Properties**

Use the pull-down menu to set the COM1 properties (Figure 4) to the following:

- Bits per second = 9600
- Data bits = 8
- Parity = None
- Stop bits = 1
- Flow control = None
- Click **OK** → **OK** to accept settings

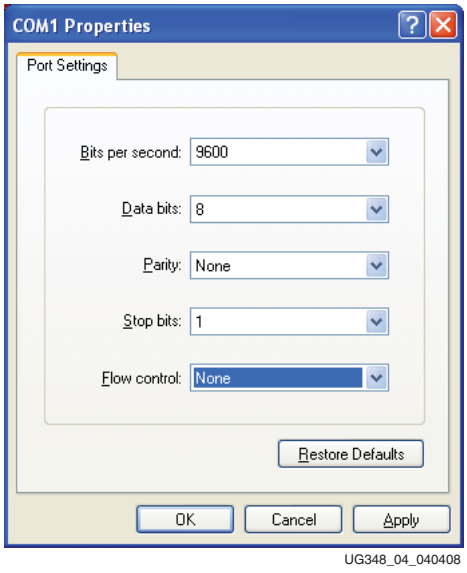


Figure 4: **COM1 Properties Setup**

7. Select **File** → **Properties**.
8. Select the Settings tab and click on **ASCII Setup** (Figure 5, page 13).

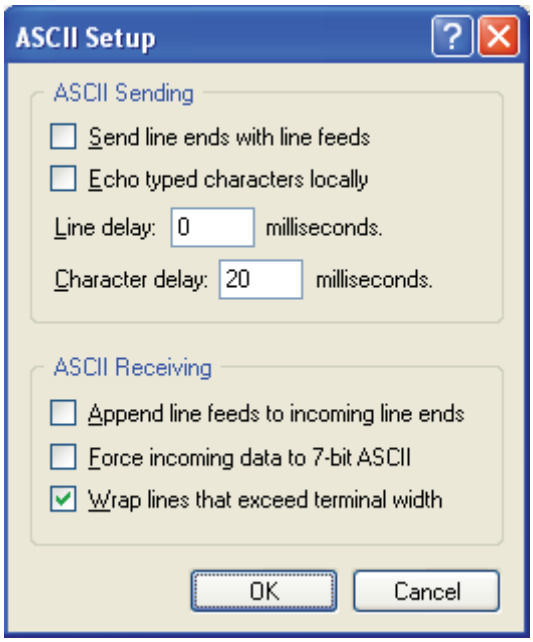


Figure 5: **ASCII Setup**

9. For Character delay, enter 20.
10. Click **OK** → **OK** to accept the settings.
11. Connect the DVI monitor or the VGA monitor with DVI-to-VGA adapter to the board, if available.
12. Turn on the ML50*x* board's main power switch and press the SYSACE RESET button. After the FPGA has been programmed, the LEDs in the lower left corner should be:
    - Bus Error 1 and 2 = off
    - FPGA INIT = green
    - FPGA DONE = green
    - System ACE "Err" = off
    - System ACE "Stat" = green

    Note: When the CF card is ejected or not installed, the System ACE "Err" LED blinks.
13. Extract the associated training lab files to your local computer. [Ref 3]

    Unzip the training lab files to a working directory, name the directory, and make note of the directory's name. This directory with the extracted files is referred to as <*LAB_DIR*> in this tutorial.

ML50*x* Demonstrations in System ACE CF

Bootloader Demonstrations

To select configuration using System ACE CF, set the configuration address and mode DIP switch (8-position DIP switch) to `00010101`. To return to the ML50*x* Bootloader at anytime, press the SYSACE RESET button.

Location

System ACE configuration address 0.

Description

The ML50*x* Bootloader demonstration displays a menu of demonstration designs that can be loaded by using the System ACE controller's reconfiguration feature. The menu is displayed on the serial terminal, LCD, and VGA.

To choose a demonstration, use the North-East-South-West-Center-oriented pushbuttons on the board (Figure 6), then press the center button to start the demonstration. Alternatively, you can select a demonstration by entering its number into the serial terminal.

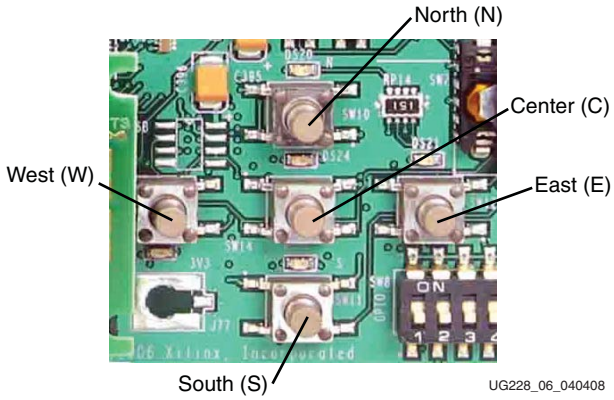


Figure 6: **User Pushbuttons**

The demonstrations are:

- "Virtex-5 FPGA Slide Show," page 15
- "Web Server (ML505/ML506 - Using Soft Ethernet MAC IP Core)," page 16
- "Web Server (ML507 - Using Integrated Tri-Mode Ethernet MAC Block)," page 18
- "Simon Game," page 20
- "Board Verification Using XROM," page 21
- "USB," page 22
- "My Own ACE File," page 23
- "Ring Tone Player," page 24

Virtex-5 FPGA Slide Show

Location

System ACE configuration address 1.

From the Bootloader menu, select option **1** to start the Virtex-5 FPGA Slide Show demonstration.

Description

This demonstration displays a sequence of picture files stored on the CF card accompanied by audio playback of a music file stored on the CF card. Pressing the East/West (E/W) buttons on the board manually switches to the previous/next slide. The North/South (N/S) buttons on the board change the volume. The center (C) button toggles between pausing and continuing the slide show.

Note: This demonstration requires a DVI monitor or a VGA monitor with a DVI-to-VGA adapter connected to the DVI port. It also requires a headphone or external speaker connected to the audio jacks.

In this program, the processor reads the CF file system through the System ACE MPU port and loads the audio/video data into DDR2 SDRAM. The processor then controls the flow of data to the VGA controller and audio controller connected to the internal CoreConnect bus.

Setup

To change or customize the side show, follow these instructions:

1. Place the picture files in the root directory.
2. Name the picture files `image<`*XX*`>.bmp` where <*XX*> is a numerical sequence starting from 01 and counting up.

   The program reads the picture files through the System ACE MPU interface starting from `image01.bmp` then counts upward. A maximum of 16 images can be read. The BMP files must be sized as 640 x 480 pixels with 24-bit color.
3. Give the sound file the name `sound.wav` and encode it as a 44.1 KHz, 16-bit stereo wave file (CD format). The sound file cannot be greater than 32 MB in size.

Note: When adding additional images or larger sound files, it might be necessary to use a higher capacity System ACE CF card than the one shipped with the ML50*x* board.

Try to add your own slides and music. For example, in Microsoft PowerPoint, you can export a presentation to HTML for a 640 x 480 screen. You can then convert the JPG or GIF slides to BMP format using Microsoft Photo Editor that is installed on many computers. Rename the BMP files to `image<`*XX*`>.bmp` and copy to the System ACE CF card. Now you can run your own customized slide show. For audio, try to extract a song from a CD into a WAV file. Copy the WAV file into the System ACE CF card and name it `sound.wav`.

Web Server (ML505/ML506 - Using Soft Ethernet MAC IP Core)

Location

System ACE configuration address 2.

From the Bootloader menu, select option **2** to start the Web Server demonstration.

Description

In this demonstration, an Ethernet-controlled GPIO interface application uses the ML505 or ML506 board as a Web server. A remote host, such as a computer running a Web browser, can communicate with the board using the Ethernet to read the value of the board's DIP switches or to set the LEDs on the board. Refreshing or reloading the remote computer's Web browser causes the background color to change and the current DIP switch values to be re-read. By default, the IP address of the ML505 and ML506 boards is **1.2.3.4**, but it can be changed by recompiling the software.

Setup

1. Connect an Ethernet cable (straight or crossover) from your host computer to the ML505 or ML506 board.

   Note: The Ethernet PHY chip on ML50*x* boards has an auto-crossover feature.

2. Configure the remote computer host's IP address to **1.2.3.9** (Subnet mask can be **255.0.0.0**).

   Note: Record the previous network settings so they will be easier to restore after the lab. The screen shots and icon names might be slightly different depending on your computer's operating system version.

   - Right-click **My Network Places** on your computer, and select **Properties**
   - Right-click **Local Area Connection,** and select **Properties**
   - Select **Internet Protocol (TCP/IP),** and click **Properties** (Figure 7)

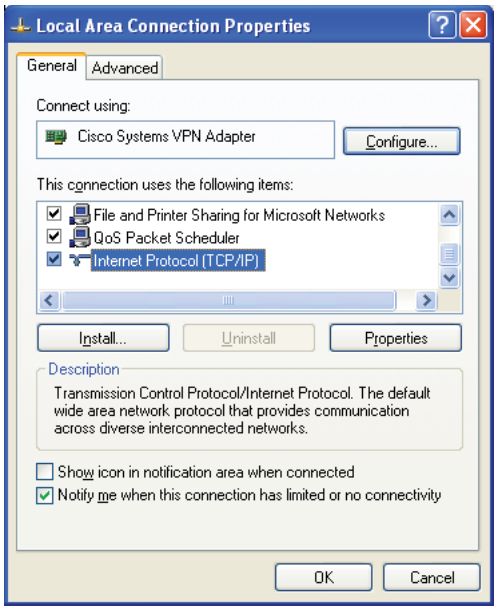


Figure 7: **Local Area Connection Properties Setup**

- Select **Use the following IP address:** (see Figure 8)
- Enter this information: IP address = **1.2.3.9** and Subnet mask = **255.0.0.0**
- Click **OK** → **OK** to accept settings

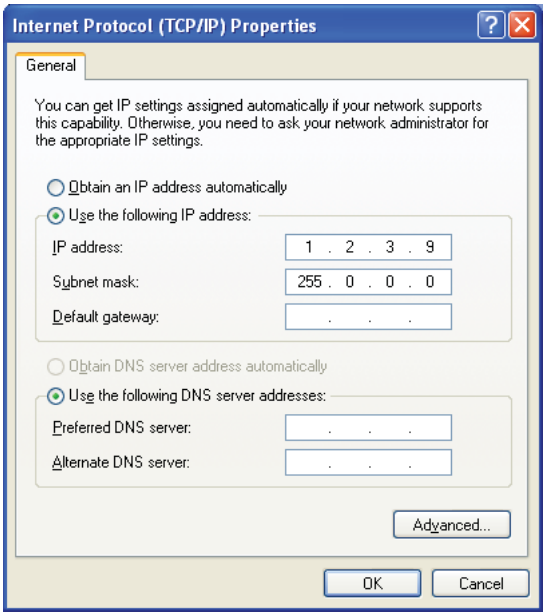


Figure 8: **IP Settings**

3. Make sure the connection is running at 10 or 100 Mb/s and the board's link lights are on (the lights are located in the upper left corner of the board). The link LEDs labeled 10, 100, and 1000 indicate the link is established at that speed.
   - You might need to force your computer to link in 10 or 100 Mb/s (duplex) mode. If so, then:

     Right-click **Local Area Connection** → **Properties** → **Configure** → **Advanced tab** → **Speed**
4. On the remote computer host, open a Web browser connection to **http://1.2.3.4:8080**, and follow the instructions on the loaded Web page.
   - You might need to turn off your browser's proxy (use direct Internet connection mode) especially if you have multiple networking devices on your computer.
   - On the remote computer host, you can ping **1.2.3.4** to confirm that the network connection is alive.
5. Restore your computer's network settings when finished.

Web Server (ML507 - Using Integrated Tri-Mode Ethernet MAC Block)

Location

System ACE configuration address 2.

From the Bootloader menu, select option **2** to start the Web Server demonstration.

Description

In this demonstration, an Ethernet-controlled GPIO interface application uses the ML507 board as a Web server. A remote host, such as a computer running a Web browser, can communicate with the board using the Ethernet to read the value of the board's DIP switches or to set the LEDs on the board. Refreshing or reloading the remote computer's Web browser causes the background color to change and the current DIP switch values to be re-read. By default, the IP address of the ML507 board is **192.168.1.10**, but it can be changed by recompiling the software.

Setup

1. Connect an Ethernet cable (straight or crossover) from your host computer to the ML507 board.

   Note: The Ethernet PHY chip on ML50*x* boards has an auto-crossover feature.

2. Configure the remote computer host's IP address to **192.168.1.10** (Subnet mask can be **255.255.255.0**).

   Note: Record the previous network settings so they will be easier to restore after the lab. The screen shots and icon names might be slightly different depending on your computer's operating system version.

   - Right-click **My Network Places** on your computer, and select **Properties**
   - Right-click **Local Area Connection,** and select **Properties**
   - Select **Internet Protocol (TCP/IP),** and click **Properties** (Figure 9)

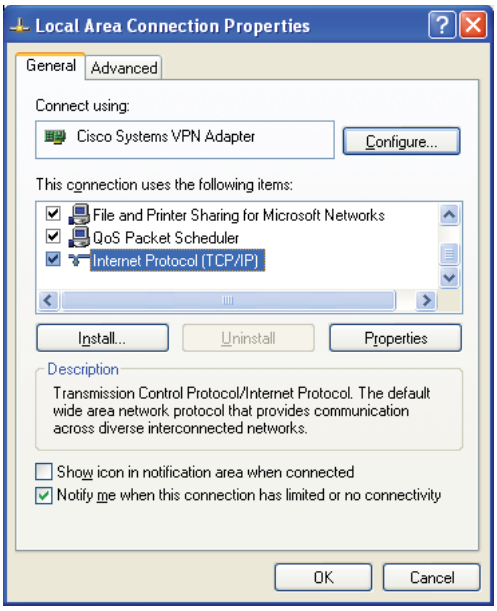


Figure 9: **Local Area Connection Properties Setup**

- Select **Use the following IP address:** (see Figure 10)
- Enter this information: IP address = **192.168.1.10** and Subnet mask = **255.255.255.0**
- Click **OK** → **OK** to accept settings

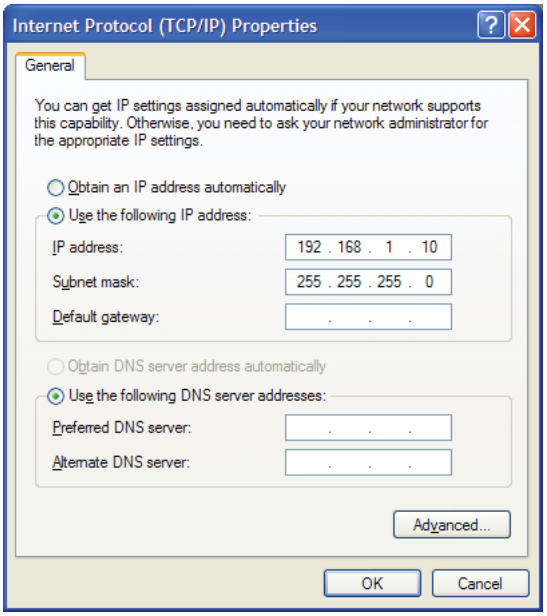


Figure 10: **IP Settings**

3. Make sure the connection is running at 10 or 100 Mb/s and the ML50*x* board's link lights are on (the lights are located in the upper left corner of the board). The link LEDs labeled 10, 100, and 1000 indicate the link is established at that speed.
   - You might need to force your computer to link in 10 Mb/s, 100 Mb/s, or 1000 Mb/s (duplex) mode. If so, then:

     Right-click **Local Area Connection** → **Properties** → **Configure** → **Advanced tab** → **Speed**
4. On the remote computer host, open a Web browser connection to **http://192.168.1.10**, and follow the instructions on the loaded Web page.
   - You might need to turn off your browser's proxy (use direct Internet connection mode) especially if you have multiple networking devices on your computer.
   - On the remote computer host, you can ping **192.168.1.10** to confirm that the network connection is alive.

Restore your computer's network settings when finished.

Simon Game

Location

System ACE configuration address 3.

From the Bootloader menu, select option **3** to start the Simon game demonstration.

Description

This demonstration displays the Simon game both through the DVI port and the button LEDs. Players input the correct sequence with the North-East-South-West-Center pushbuttons. Game sounds are produced on the piezo transducer. Messages are displayed on the character LCD and on the video screen.

Note: Note: This demonstration requires a DVI monitor or a VGA monitor with DVI-to-VGA adapter connected to the DVI port.

Instructions

At the beginning of the game, all the LEDs blink rapidly.

1. Press any button to start the game.
2. In each round, the LEDs blink and video graphics move in a given sequence. The player must press the buttons to repeat this displayed sequence.
3. Correctly repeating the sequence gives the player one point, and a new round is started. Each sequence becomes increasingly complex.
4. If a mistake is made, the score resets to 0 on the screen, the high score is updated, and all the LEDs blink rapidly to signify a new game.

Board Verification Using XROM

Location

System ACE configuration address 4.

From the Bootloader menu, select option **4** to start the XROM application.

Description

The XROM application performs board diagnostics and testing.

Instructions

On the terminal window associated with the serial port, enter the number 1 to select the Tests sub-menu. Make further selections as desired to run board diagnostic tests. The tests are numbered as follows:

1. Test DDR SDRAM
2. Test ZBT SRAM
3. Test LEDs
4. Test Pushbuttons
5. Test Dip Switches
6. Test Character LCD
7. Test PS/2 Keyboard
8. Test SMA Connectors
9. Test VGA Output

A. Test Flash Memory

B. Print IIC EEPROM Contents

C. Test Piezo

0. Return to the Main Menu

USB

Location

System ACE configuration address 5.

From the Bootloader menu, select option **5** to start the USB demonstration.

Description

This demonstration uses the processor and the USB controller chip on the ML50*x* board to communicate with a USB keyboard.

The program functions by first reading the file `demo.bin` from the CompactFlash card. This file contains the software for the internal microprocessor inside the USB controller (Cypress CY7C76300). The FPGA's processor reads this file and writes the data to the memory inside the USB controller through its HPI port. The USB controller's internal processor then starts and can begin implementing low-level USB commands to communicate with the USB keyboard. Data from the USB keyboard is transferred to the FPGA's processor using mailbox registers over the HPI port.

Setup

Connect a standard USB keyboard to the ML50*x* board. Keys typed on the USB keyboard are then displayed on the character LCD and serial port.

Note: This demonstration requires a USB keyboard without a built-in hub.

My Own ACE File

Location

System ACE configuration address 6.

From the Bootloader menu, select option **6** to start the demonstration of the *My own ACE file* program.

Description

This program is a placeholder design to be replaced by a user design.

Setup

Take a bitstream and make your own ACE file:

1. Open a DOS command shell. Click **Start Menu** → **Run**, then enter **`cmd`** as the program to run, and click **OK**.
2. Change directory to your lab directory. Type **`cd <LAB_DIR>`**.

   In this directory, there is a bitstream called `button_led_test_hw.bit`. This program tests the GPIO DIP switches and pushbuttons.
3. Convert this bitstream to an ACE file. On one line, type:

   ```
   xmd -tcl ./genace.tcl -jprog -hw button_led_test_hw.bit -board
   ml505 -ace my_button_led_test_hw.ace
   ```

   This creates the `my_button_led_test_hw.ace` file. The System ACE File Generator (GenACE) chapter in the *Embedded System Tools Reference Manual* contains details on how to create ACE files. [Ref 16]
4. Carefully remove the System ACE CF card from the ML50*x* board (preferably with the power off). Open the CF card on your computer. This requires either a PC card adapter or a USB CompactFlash reader (not included with ML50*x* board, but available at computer stores).
5. Copy `my_button_led_test_hw.ace` to the CF card into the **ML50X/cfg6** directory.
6. In the **ML50X/cfg6** directory on the CF card, rename `system_my_ace.ace` to `system_my_ace.bak`. This ensures that there is only one ACE file in this directory.
7. Eject the CF card from your computer (right-click on the CF card in Windows Explorer and click **Eject**). This shuts down the CF card to prevent data corruption. Carefully reinsert the CF card into the ML50*x* board (preferably with the power off).
8. Turn the power back on, if necessary, and press the SYSACE RESET button to restart the Bootloader. Select Option 6 to start the *My own ACE file* program. In this design, flipping a GPIO DIP switch or pressing a GPIO button will light a corresponding LED.

Ring Tone Player

Location

System ACE configuration address 7.

From the Bootloader menu, select option **7** to start the demonstration of the *Ring Tone Player* program.

Description

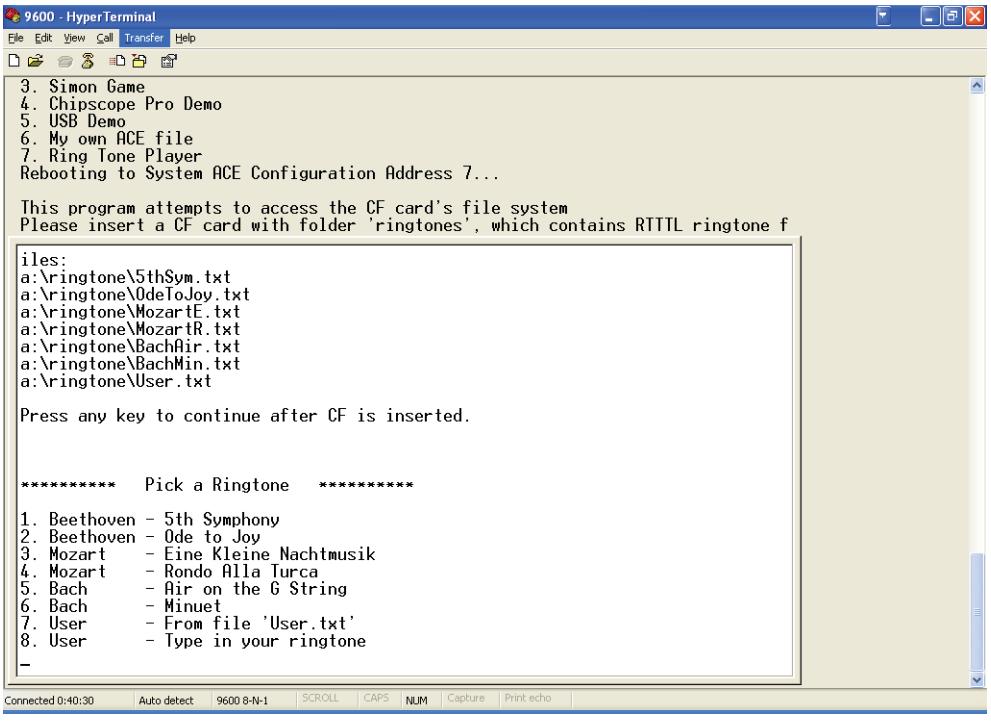
This program inputs a Ringing Tones Text Transfer Language (RTTTL) ring tone and creates the melody using the piezo transducer. Through a serial terminal program, users can play ring tones from a CF card or type in their ring tones.

Setup

1. The start screen ask you to insert the CF card, which contains the ring tones in the **ringtone** folder. When the CF is inserted, press any key.
2. A program menu appears with eight options. Entering 1, 2, 3, 4, 5, or 6 plays ring tones stored on the CF card.

   If you have the RTTTL code of a ring tone, you have two options to play it:

   - Replace the User.txt file on the CF card with the RTTTL code (Option 7)
   - With a serial terminal program, paste or type in the RTTTL code (Option 8)



UG348_09_040408

Figure 11: **RTTTL Setup**

RTTTL Specification

The RTTTL specification denotes the ring tone with a string containing three fields separated by a colon.

<Name Field>:<Options Field>:<Notes Field>

The following is an example of an RTTTL ring tone using the fields and parameters defined in Table 1:

```
Beethoven:d=4,o=6,b=100:16g5,16g5,16g5,d5,16f5,16f5,16f5,d5,16g5,16g5,
16g5,16d5,16g5,16g5,16g5,16g5,16d,16d,16d,c,16g5,16g5,16g5,16d5,16g5,
16g5,16g5,16g5,16f,16f,16f,d.
```

Table 1: **RTTTL Ring Tone Fields**

Field	Parameter	Description
Name		The *Name* field specifies the name of the ring tone.
Options		The *Options* field uses three parameters to specify the duration, octave, and tempo of each note.
	d = {1,2,4,8,16,32,64}	Parameter **d** specifies the duration of each note as follows: • 1 is a whole note • 2 is a half note • 4 is a quarter note, and so forth If the duration is not specified, the default is d = 4.
	o= {4,5,6,7}	Parameter **o** specifies the octave of a note. Note *a* for each octave is as follows: • Octave 4 is 440 Hz • Octave 5 is 880 Hz • Octave 6 is 1760 Hz • Octave 7 is 3520 Hz If the octave is not specified, the default is o=6.
	b = {0,1,2,3...}	Parameter **b** specifies the beats per minute (tempo). If the tempo is not specified, the default is b=63.
Notes		The *Notes* field uses the letter of the note plus three optional parameters to define each note using the following format: [duration] *note* [scale] [extend duration]
	note = {a,b,c,d,e,f,g,p}	The **note** parameter defines a note on the musical scale, except the letter p which represents a rest.
		The **duration** and **scale** parameters take on the range specified in the Options field. If unspecified, these parameters take on the default value of the Options field.
	.	The **extend duration** parameter (a dot) defines a dotted note and lengthens the duration by 50 percent.

ML50*x* Demonstrations in Linear Flash

Linear Flash LCD Demonstration

Description

This demonstration shows the FPGA being configured by an external linear flash device and a CPLD. This method of download is used in some embedded processor systems where it is necessary to keep software and bitstream data in one non-volatile device.

Setup

1. To load a pre-loaded bitstream, change to the corresponding address configuration / mode dip switches listed below.

   Configuration 0: **00001001**

   Configuration 1: **00101001**

   Configuration 2: **01001001**

   Configuration 3: **01101001**
2. Press the **Prog** button.
3. After the bitstream has loaded, the character LCD should say "Design #*x* Loaded using Flash," where x is the bitstream number.

My Own Linear Flash Image Demonstration

Description

This exercise shows you how to store your own design into linear flash and how to program it onto the FPGA using the Embedded Development Kit (EDK) GUI. A bitstream with a flash memory interface is provided in the `ml505_lab_resources.zip` file. The EDK Flashwriter is used to demonstrate how to overwrite the contents of the linear flash.

To program your own bit file into linear flash:

1. Extract the `ml505_lab_resources.zip` to your local computer. [Ref 3]

   Unzip the training lab files to a working directory, name the directory, and make note of the directory's name. This directory with the extracted files is referred to as <*LAB_DIR*> in this tutorial.
2. In EDK, open the `ml505_bsb_system.xmp` project file.
3. Open a Xilinx Cygwin Shell. From the EDK GUI menu, select **Project** → **Launch EDK Shell**
4. Copy the BIT file destined for the linear flash to <*LAB_DIR*>.

   ```
   cp -p <file_name>.bit .
   ```
5. Create a BIN file to program the linear flash device.

   ```
   promgen -w -p bin -o <file_name>.bin -u 0 <file_name>.bit
   ```

   Example using existing file in ZIP file:

   ```
   promgen -w -p bin -o flash_hello0.bin -u 0 flash_hello0.bit
   ```
6. Configure the FPGA.

```
impact -batch etc/download.cmd
```

7. Program the linear flash at a specific configuration location (Figure 12). From the EDK GUI menu, select **Device Configuration** → **Program Flash Memory**

   Enter the path of the flash image:

   `<LAB_DIR>/flash_hello0.bin`

   Set the Flash Memory Properties, Instance Name to `SRAM_c_mem1_baseaddr`

   Set the Flash Memory Properties, Program at Offset as follows:

   For Configuration 0, set the address to **`0x00000000`**

   For Configuration 1, set the address to **`0x00800000`**

   For Configuration 2, set the address to **`0x01000000`**

   For Configuration 3, set the address to **`0x01800000`**

   Set the Scratch Memory Properties, Instance Name to `DDR2_SDRAM_c_mpmc_baseaddr`

   Click **OK**. Repeat this step for each BIN file to be programmed into the linear flash.

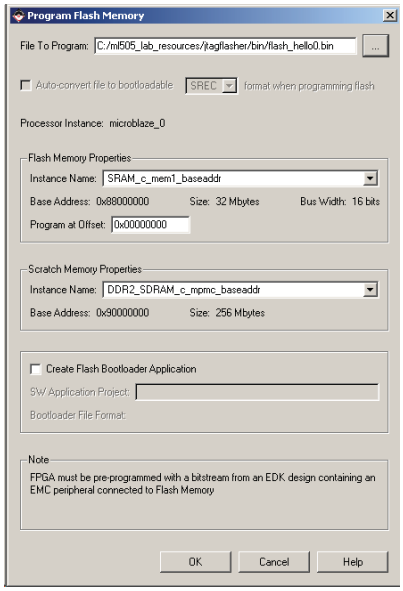


Figure 12: **Programming the Flash**

8. Select and set the CONFIG DIP switch values to indicate the desired linear flash configuration location:

   Configuration 0: **`00001001`**

   Configuration 1: **`00101001`**

   Configuration 2: **`01001001`**

   Configuration 3: **`01101001`**

9. Press the **PROG** pushbutton to configure the Virtex-5 FPGA from the linear flash using the configuration selected in step 8.

ML50*x* Demonstrations in Platform Flash

The Platform Flash PROM contains advanced features, such as revision control, and is a convenient and easy-to-use method of configuring FPGAs.

The Platform Flash on the ML50*x* board can hold multiple bitstreams:

- "Platform Flash LCD Demonstration"
- "Platform Flash XROM Demonstration"
- "My Own Platform Flash Image Demonstration"

To select configuration using Platform Flash, set the configuration address and mode DIP switch (8-position DIP switch) to `00011001`.

Platform Flash LCD Demonstration

Location

ML505/ML506: Platform Flash configuration address 0.

ML507: Platform Flash configuration address 1.

Description

This demonstration displays to the character LCD the message "Put Your Design Here".

Setup

1. Set the configuration address DIP switches to the following binary value:

   For ML505/ML506: `00011001`

   For ML507: `00111001`

2. Press the **Prog** button to see the message "Put Your Design Here" displayed on the character LCD.

Platform Flash XROM Demonstration

Location

ML505/ML506: Platform Flash configuration address 1.

ML507: Platform Flash configuration address 0.

Description

The XROM program presents a menu over the serial port offering various diagnostic tests of the ML50*x* board features.

Setup

1. Set the configuration address DIP switches to the following binary value:

   For ML505/ML506: `00111001`

   For ML507: `00011001`

2. Press the **Prog** button to run this demonstration.

3. Select from the menu presented on the serial terminal to run various diagnostic tests.

My Own Platform Flash Image Demonstration

Description

This exercise shows you how to store your own design revision into the non-volatile Platform Flash configuration device. This exercise overwrites the contents of Platform Flash.

To program your own BIT file into Platform Flash:

1. Change the Configuration Address / Mode DIP switches to the following binary value:

   For ML505/ML506: **`01011001`**

   For ML507: **`00111001`**

2. Open a DOS command shell. Click **Start Menu** → **Run**, then enter **`cmd`** as the program to run, and click **OK**.
3. Change directory to your lab directory. Type **`cd <LAB_DIR>`**.
4. Copy your bit file into this folder.

   ```
   Copy <file_name>.bit .
   ```

5. Format the BIT file to an MCS file.

   For an ML505 (or ML506) board, on one line type in the command prompt:

   ```
   promgen -w -p mcs -c FF -o ml505_production_platflash -ver 0
   my_plat_flash.bit -ver 1 xrom.bit -ver 2 <file_name>.bit -ver 3
   <file_name>.bit -x xcf32p xcf32p
   ```

   For an ML507 board, on one line type in the command prompt:

   ```
   promgen -w -p mcs -c FF -o ml507_production_platflash -ver 0
   xrom.bit -ver 1 my_plat_flash.bit -x xcf32p xcf32p
   ```

   Programming and informational files with extensions (.mcs, .cfi, .prm, .sig) are created.

6. Program the two Platform Flash devices on the ML50*x* by running the following batch file from the DOS command prompt:

   ```
   Program_ML505_PlatFlash.bat
   ```

7. Press **Prog** to configure the FPGA with the design programmed into the Platform Flash at:

   For ML505/ML506: configuration address 2

   For ML507: configuration address 1

Note: ISE iMPACT also offers a method for programming the Platform Flash.

ML50*x* Demonstrations in SPI Flash

SPI Flash memory can be used for FPGA configuration or to hold user data. The SPI Flash on the ML50*x* board contains the following bitstreams:

- "SPI Flash Hello Demonstration"
- "My Own SPI Flash Image Demonstration"

To select configuration using SPI Flash, set the configuration address and mode DIP switch (8-position DIP switch) to **00000101**.

SPI Flash Hello Demonstration

Location

SPI Flash configuration address 0.

Description

This program displays to the character LCD the "Design Loaded Using SPI Mem" message.

Setup

Press the **Prog** button to see the "Design Loaded Using SPI Mem" message displayed on the character LCD.

My Own SPI Flash Image Demonstration

SPI is a flash device that can store your configuration file and program it to the FPGA. This demonstration shows you how to store your own design into the SPI Flash and how to program it onto the FPGA. This exercise overwrites the contents of the SPI Flash.

1. Disconnect the cable attached to header J1 (the header on the left side of the board) from the Xilinx download cable.
2. Connect JTAG flying wires from the Xilinx download cable to the J2 header using the pin labels as a guide on how to make the connections. The 7-pin J2 header is located to the right of the FPGA and just above the LCD panel.
3. Set the configuration address DIP switches to **00010101**.
4. Remove the inserted ML50*x* CF card if present, and press the **Prog** button to erase the FPGA.
5. Open a DOS command shell. Click **Start Menu** → **Run**, then enter **cmd** as the program to run, and click **OK**.
6. Change directory to your lab directory. Type **cd <*LAB_DIR*>**.
7. Copy your BIT file into this folder.

   ```
   Copy <file_name>.bit   .
   ```

8. Format the BIT file to an MCS file.

   ```
   promgen -spi -p mcs -o <file>.mcs -s 16384 -u 0 <file>.bit
   ```

9. Launch iMPACT and double- click **Direct SPI Configuration** in the iMPACT Modes window to program the SPI Flash device.
10. Right-click the Direct SPI Configuration tab and select **Add SPI Device...**

11. Navigate to <*file_name*>.mcs created above and click **Open**.
12. In the Select Device Part Name drop-down dialog box, select M25P32 and click **OK**.
13. The Direct SPI Configuration tabbed window displays a diagram of a single SPI PROM. Right-click on the SPI PROM and select **Program**.
14. Click **OK** to program the SPI Flash device.
15. On the board, change the configuration address / mode DIP switches to **00000101**.
16. Press the **Prog** button. The design takes about 8 seconds to finish loading and begin to run.

References

Documents specific to the ML50*x* Evaluation Platform:

1. UG347, *ML505/ML506/ML507 Evaluation Platform User Guide.*
2. UG349, *ML505/ML506/ML507 Reference Design User Guide.*
3. Lab Resources: ML505, ML506, ML507.

Documents supporting Virtex-5 FPGAs:

4. DS100, *Virtex-5 Family Overview.*
5. DS202, *Virtex-5 FPGA Data Sheet: DC and Switching Characteristics.*
6. UG190, *Virtex-5 FPGA User Guide.*
7. UG200, *Embedded Processor Block in Virtex-5 FPGAs Reference Guide.*
8. UG196, *Virtex-5 FPGA RocketIO GTP Transceiver User Guide.*
9. UG198, *Virtex-5 FPGA RocketIO GTX Transceiver User Guide.*
10. UG194, *Virtex-5 FPGA Embedded Tri-Mode Ethernet Media Access Controller User Guide.*
11. UG197, *Virtex-5 FPGA Integrated Endpoint Block for PCI Express Designs User Guide.*
12. UG193, *Virtex-5 FPGA XtremeDSP Design Considerations.*
13. UG191, *Virtex-5 FPGA Configuration User Guide.*
14. UG192, *Virtex-5 FPGA System Monitor User Guide.*
15. UG195, *Virtex-5 FPGA Packaging and Pinout Specification.*

Documents supporting Xilinx Platform Studio (XPS):

16. UG111, *Embedded System Tools Reference Manual*
17. UG683, *EDK Concepts, Tools, and Techniques.*
18. UG081, *MicroBlaze Processor Reference Guide*.
19. UG643, OS and Libraries Document Collection