

# XUPV5-LX110T MIG Design Creation Using ISE™ 10.1i SP3, MIG 2.3 and ChipScope™ Pro 10.1i







September, 2008



#### **Overview**

- Hardware Setup
- Software Requirements
- CORE Generator™software
  - Memory Interface Generator (MIG)
- Modify Design
  - Add ChipScope Pro Cores to Design
- Compile and Test Memory Interface

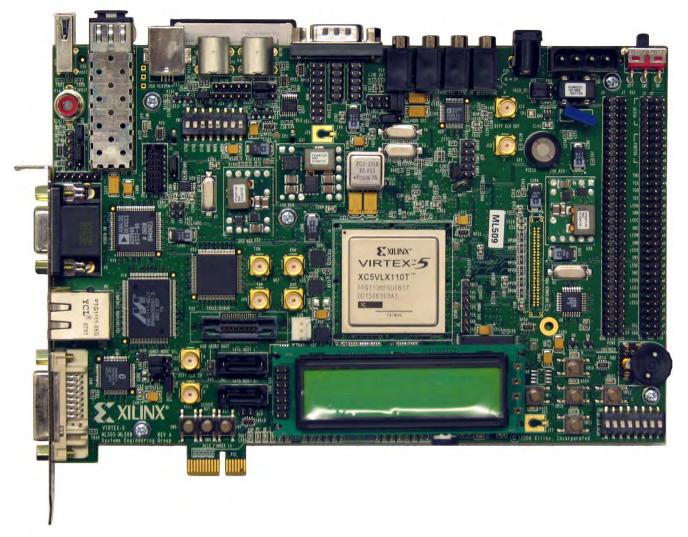


## Virtex-5 DDR2 Capabilities

- MIG DDR2 SDRAM design supports frequencies up to 333 MHz
  - The MIG user guide addresses MIG performance across device speed grades
- The XUPV5-LX110T ships with a –1 speed grade device
  - See the <u>Virtex-5 Data Sheet</u> for a list of Virtex-5 supported memory interface speeds



#### Xilinx XUPV5-LX110T Board





## ISE Software Requirement

Xilinx ISE 10.1i SP3 software



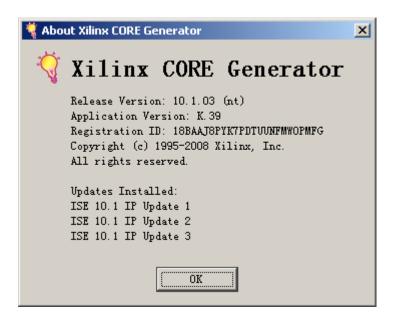




### Coregen Software Requirement

Install Xilinx Coregen 10.1i IP Update 3

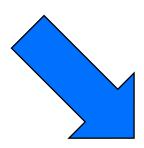






#### **ChipScope Software Requirement**

Xilinx ChipScope Pro 10.1i SP3







- Connect the Xilinx
   Parallel Cable IV (PC4)
  - <u>HW-PC4</u>
- SMA Cable
  - www.flrst.com
  - P/N: ASPI-024-ASPI-S402
- Optional Pancake Fan
  - Recommended for keeping the Virtex<sup>™</sup>-5 device cool







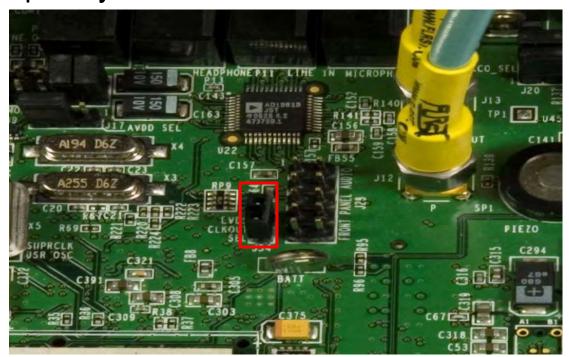


- Connect SMA Cables from J12/13 to J10/11
  - This will serve as the 200 MHz clock source for the memory controller



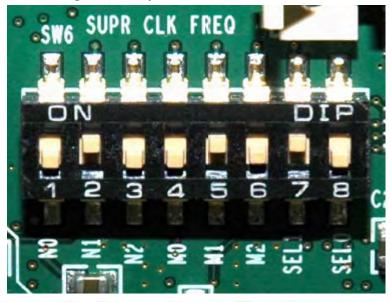


- Jumper J54 must be connected
  - This enables the output of the on-board ICS frequency source





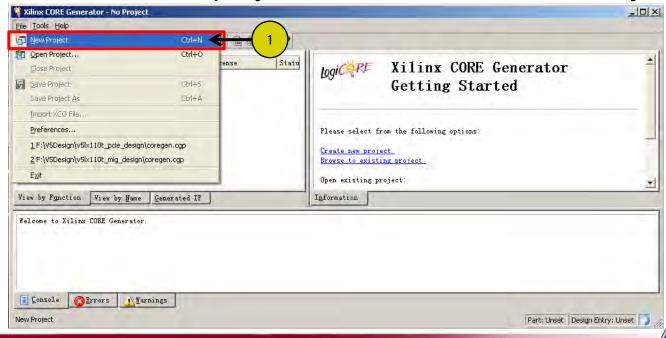
- Use SW6 to set the memory clock frequency
- Set SW6 to 200 MHz (1)
  - 200 MHz = 010 010 10 (Max memory clock frequency for a -1 speed grade)





#### **CORE** Generator

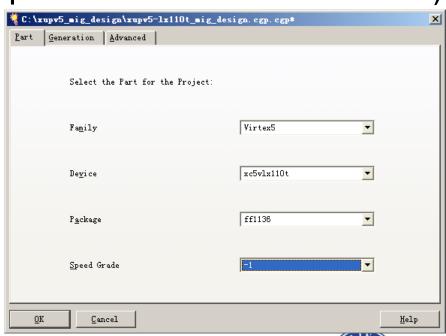
- Open the CORE Generator
  - Start → All Programs → Xilinx ISE Design Suite 10.1i → ISE
    - → Accessories → CORE Generator
- Create a new project; select File → New Project (1)





#### **MIG Core Generation**

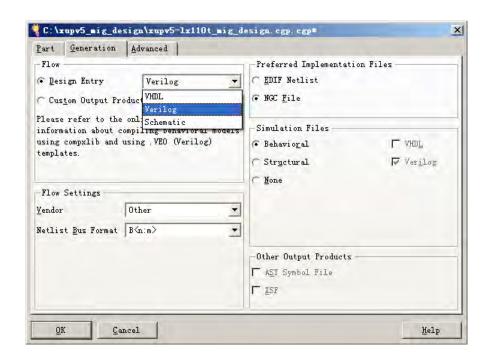
- Create a project directory: xupv5\_mig\_design
- Name the project: xupv5-lx110t\_mig\_design.cgp
- Set the Part (as shipped on the XUPV5-LX110T):
  - Family: Virtex5
  - Device: xc5vlx110t
  - Package: ff1136
  - Speed Grade: -1





#### **MIG Core Generation**

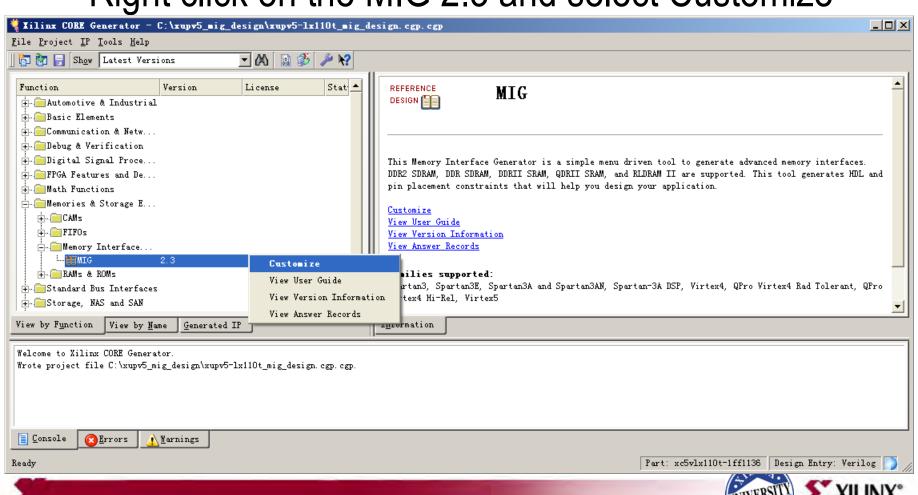
- Set the Design Entry to Verilog
- Click OK

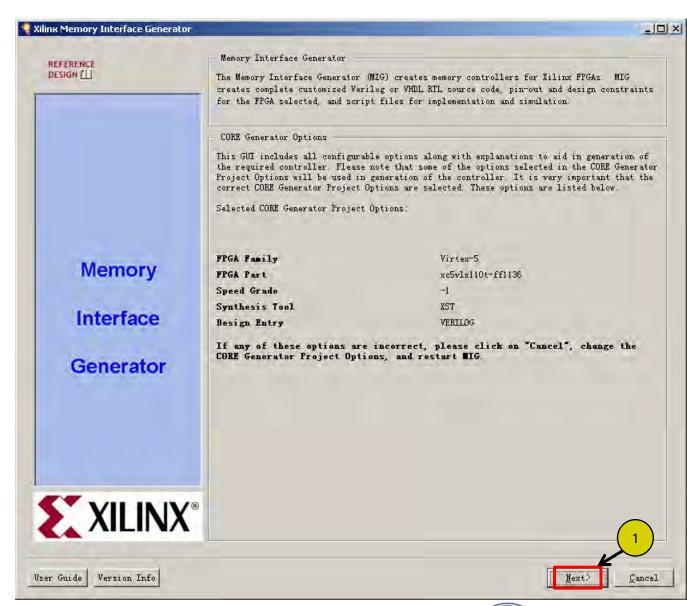




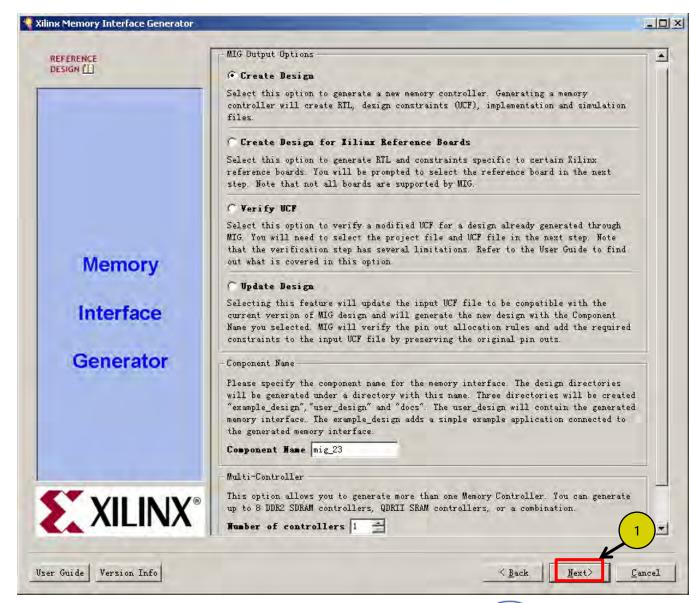
#### **MIG Core Generation**

Right click on the MIG 2.3 and select Customize

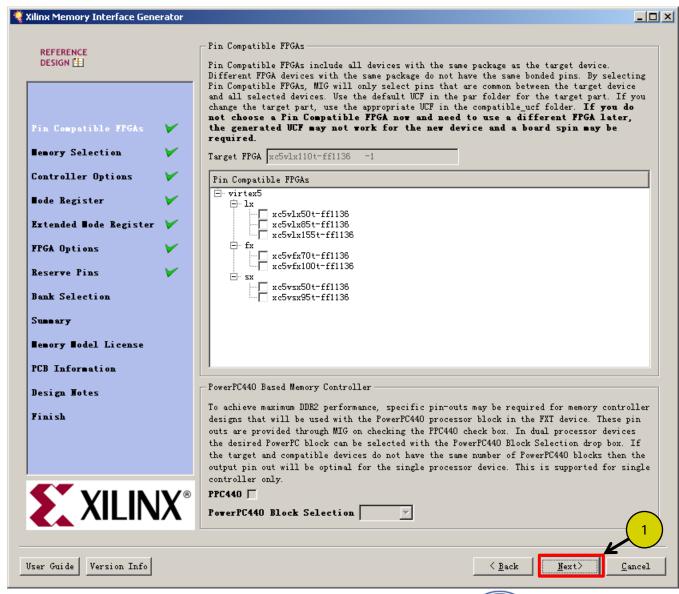




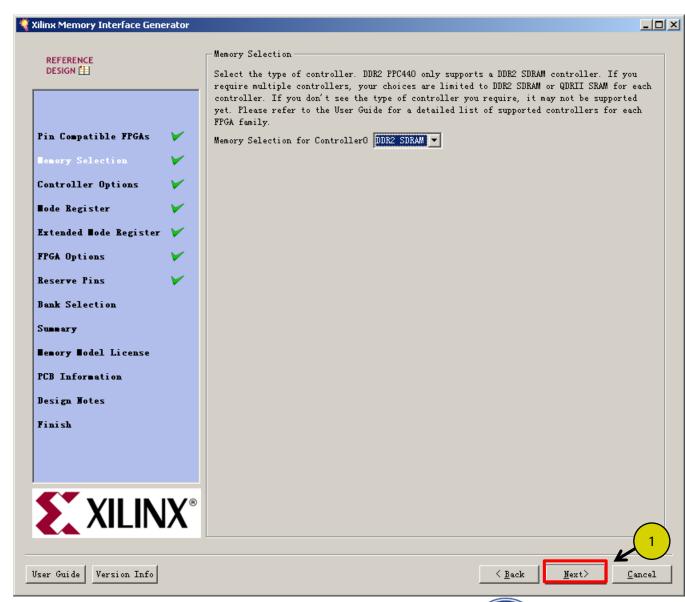






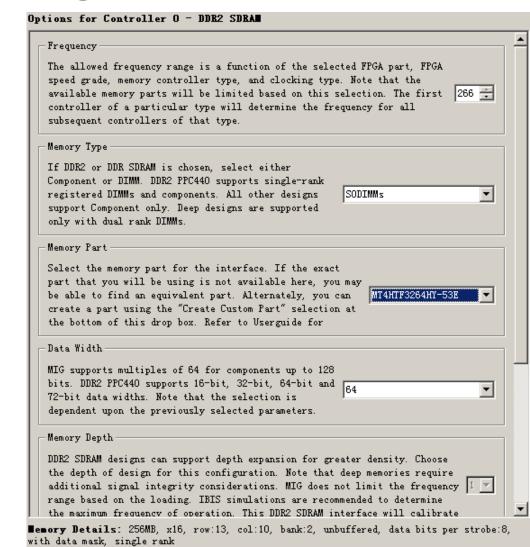




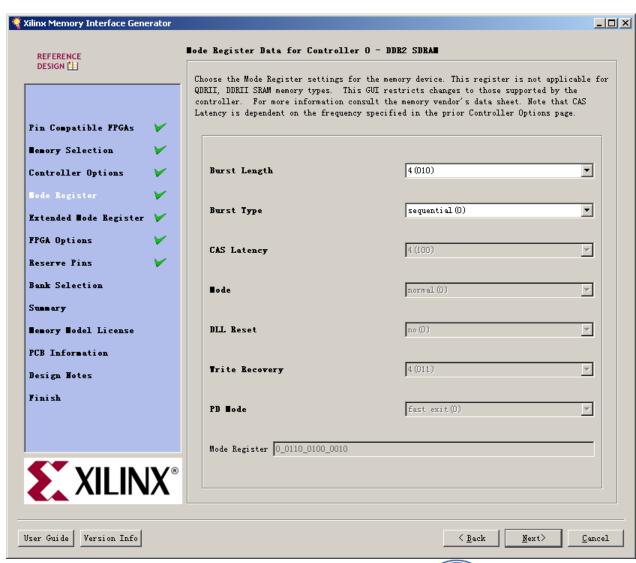




- MIG defaults to a maximum frequency of 266 for a Virtex-5 -1 speed grade selection
  - See UG086
- Set the Memory Type to SODIMMs
- Set the Memory part to MT4HTF3264HY-53E
- Click Next

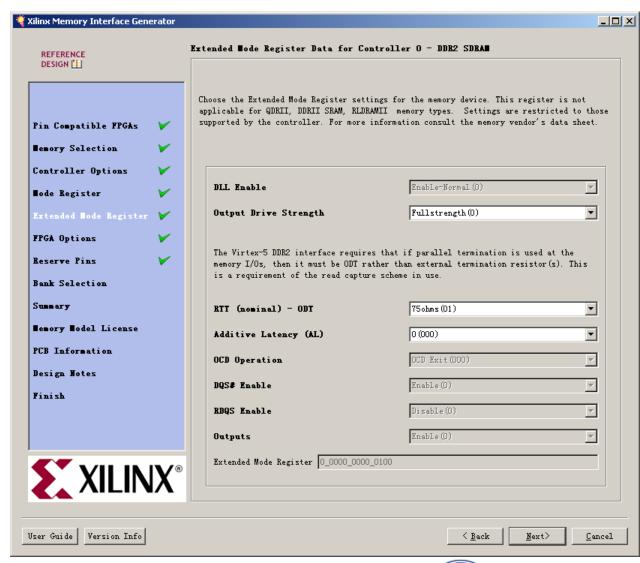


Click Next on this screen





•Click Next on this screen





## •Click Next on this screen

DCM Option	
If the design is generated with the DCM option enabled, the required clocks are generated from a DCM internal to the design. If this option is disabled, required clocks must be provided as inputs with the appropriate clock signals are already available in the overall design.	
Vse DC■	<b>▽</b>
Digitally Controlled Impedance (DCI)	
Select the DCI (Digitally Controlled Impedance) I/O standard to enable the FPGA internal termination for the DQ and DQS signals. Consult the User Guide for more information and use IBIS simulation to determine the best termination strategy. This can also be changed after generation by altering the UCF manually.	
DCI for DQ/DQS	▽
Select the DCI (Digitally Controlled Impedance) I/O standard to activate the internal 25 ohm series termination in the SSTL driver for address and control output signals to the memory. Consult the User Guide for more information and use IBIS simulation to determine the best termination strategy. This can also be changed after generation by altering the UCF manually.	
DCI for Address/Control	
SSTL Class Option	
Class II is recommended for all SSTL signals in memory interfaces. However, better signal integrity may sometimes be achieved with Class I for Address & Control. If IBIS simulations indicate that Class I is superior for your application, select Class I below. This can be changed after generation by modifying the UCF. This option changes the drive strength for Address & Control. The drive strength remains Class II for data.	
Class for Address and Control	Class II
Debug Signals Control	
This allows the debug signals (calibration status signals) to be monitored on the ChipScope tool. Selecting this option will port map the debug signals to the ChipScope modules in the design top module. The debug signals width is calibrated based upon the selected design data width. If the design data width is greater than or equal to 32 bits then the debug signals width is calibrated only for 32-bit data.	
Debug Signals for Memory Controller	Disable
Limit to 2 Bytes per Bank-	
DDR2 SDRAM DQ signals transition simultaneously. Concentrating many of them in an I/O bank will increase the amount of simultaneous switching noise the I/O bank will experience. Choose this option to spread the DQ bytes across more I/O banks. Check the timing of the resultant design before committing to a PCB layout.	
Limit to 2 Bytes per Bank	
System Clock-	
Choose the desired input clock configuration.	
System Clock	Differential
IODELAY Power Versus Performance	
Choose <b>High</b> Performance Mode for lowest IODELAY jitter and maximum interface performance. Choose <b>Hormal</b> Performance Mode to reduce power by approximately 2.8 mW per pin when interface performance requirements are less stringent. The timing spreadsheet generated by MIG indicates the change.	
Performance Hode	HIGH



Click Next on this screen

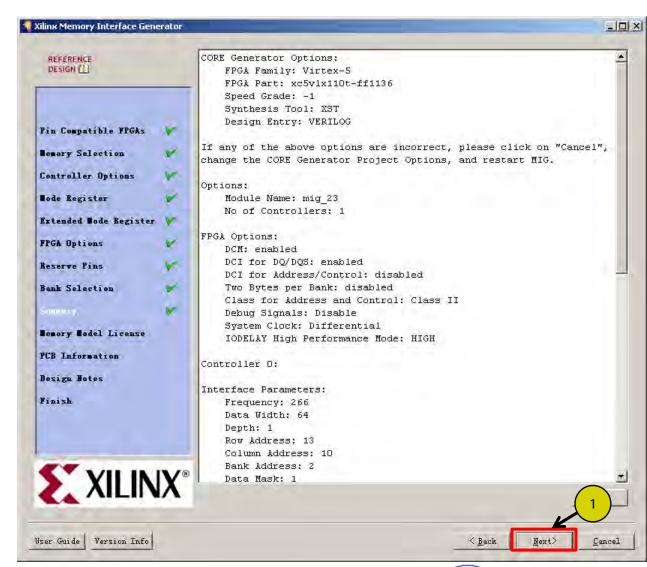




#### Click Next on this screen

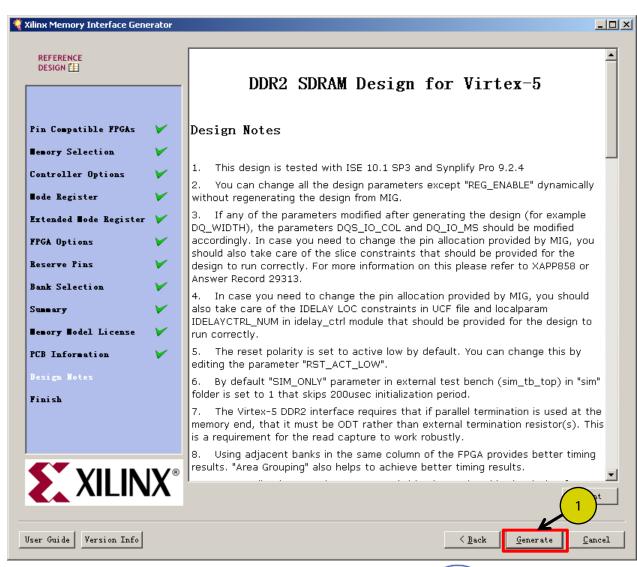
#### Bank Selection For Controller 0 - DDR2 SDRAM The FPGA bank diagram below is an architectural view physical representation of the selected part. Choose the banks you would like to use for your memory interface. You do not get to select the actual pins. By default MIG will use any available pins for the memory interface in the selected banks. If you have custom pin-out use Update Design option in the MIG Output Options page to generate the design and updated UCF file. Generally banks in a single contiguous column provide the best overall internal timing. Predefined fixed bank selection is used for PPC440 depending on the selected device. Enter the WASSO (Weighted Average Simultaneous Switching Outputs) limits for vour PCB as described in the selected FPGA User Guide. MIG will limit the number of pins per bank based on these WASSO limits. For each signal grouping, the numbers indicate the number of pins currently allocated and the total needed. Priority is given for Data, then Address, then System Control in each bank. Data: 88/8 🕗 Address: 25/2! 🕜 System Control: 3, 🕗 System Clock: 4/4 📀 Bank:23 Bank:5 Available IO's: 2 Available IO's: 38 WASSO Limit: 38 WASSO Limit: 38 ✓ Address Address 🔽 Data Data ✓ System Control System Control Bank: 19 Bank:3 Bank:20 Available IO's: 2 Available IO's: 15 Available IO's: 38 WASSO Limit: 38 WASSO Limit: 19 WASSO Limit: 38 ✓ Address ✓ System Clock Address 🔽 Data Data





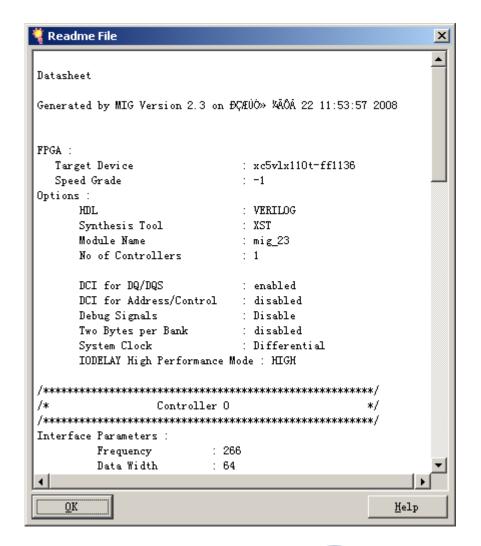


- Click Generate(1)
- Click Finish and select YES after generation





 After the MIG core finishes generating, click OK on the Datasheet window





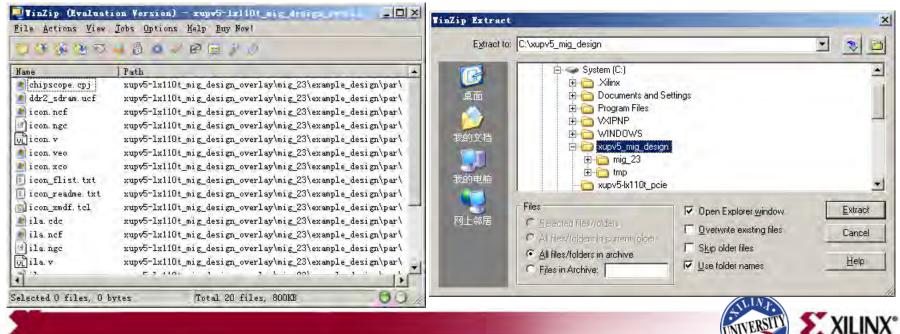
## **Design Modifications**

- Add overlay files
  - XUPV5-LX110T specific UCF file as per <u>Answer</u>
     Record 29313
  - Pre-compiled ChipScope Pro design files used to validate the design
- Modify top level Verilog file
  - Support for XUPV5-LX110T Board as per AR 29313
  - Add ChipScope Pro to design



#### Add XUPV5-LX110T Files

- Unzip <u>xupv5-lx110t mig design overlay.zip</u> file
  - Unzip to the xupv5\_mig\_design directory
  - See <u>ChipScope Pro documentation</u> for details on generating/instantiating the ICON and ILA cores



## **Modify Design for XUPV5-LX110T**

- Open the top-level Verilog file, mig\_23\example\_design\rtl\ddr2\_sdram.v

```
🥻 VItraEdit - [C:\xupv5_mig_design\mig_23\example_design\rt1\ddr2_sdram.v]
 궠 文件(P) 編輯(E) 捜索(S) 方案(P) 视图(V) 格式(T) 列(L) 宏(M) 脚本(S) 高級(A) 窗口(W) 帮助(H)
                                                                                                                 그림의
ddr2_sdram.v
    0, \dots, 10, \dots, 20, \dots, 30, \dots, 40, \dots, 50, \dots, 60, \dots, 70, \dots, 80, \dots, 90, \dots, 100, \dots, 110, \dots
       parameter CLK PERIOD
154
155
                                         // Core/Memory clock period (in ps).
156
       parameter DQS_IO_COL
                                        = 16'b000000000000000000000
157
                                          // I/O column location of DQS groups
                                        = 64'b01110101 00111101 00001111 00011110 00101110 11000001 11000001 10111100,
159
       parameter DQ IO MS
                                     160
                                          // Master/Slave location of DO I/O (=0 slave).
162
       parameter CLK TYPE
163
                                         // # = "DIFFERENTIAL " ->; Differential input clocks ,
164
                                         // # = "SINGLE ENDED" -> Single ended input clocks.
165
       parameter DLL FREQ MODE
166
                                          // DCM Frequency range.
167
       parameter RST ACT LOW
168
                                         // =1 for active low reset, =0 for active high.
169
```

## Add ChipScope Pro

Add these lines to the top-level Verilog file:

```
wire [35:0] control;
wire clk;
wire [71:0] data;
wire [7:0] trig0;
```

```
VItraEdit = [C:\xupv5_mig_design\mig_23\example_design\rt1\ddr2_sdram.v*]
  文件(P) 編辑(B) 搜索(S) 方案(P) 视图(V) 格式(T) 列(L) 宏(M) 脚本(S) 高級(A) 窗口(W) 帮助(H)
                                                                                                     _ B ×
 ddr2_sdram.v*
     226
                                  app wdf wren;
227
     wire
                                  app af wren;
228
                                  app af addr;
     wire
          [30:0]
229
          [2:0]
                                  app af cmd;
230
          [(APPDATA_WIDTH)-1:0]
                                          rd_data_fifo_out;
231
         [(APPDATA WIDTH)-1:0]
                                          app wdf data;
232
          [(APPDATA WIDTH/8)-1:0]
                                          app wdf mask data;
233
234
     wire [35:0] control;
235
     wire clk;
236
     wire [71:0] data;
237
     wire [7:0] trig0;
238
     //Debug signals
239
240
241
```



## Add ChipScope Pro

Add these lines to the top-level Verilog file before endmodule:

```
icon i icon(.CONTROL0(control));
ila i ila(.CLK(clk0),.CONTROL(control),
        .TRIG0(trig0),.DATA(data));
assign data[63:0] = app af addr;
assign data[64] = app_wdf_afull;
assign data[65] = app af afull;
assign data[66] = app wdf wren;
assign data[67] = app af cmd;
assign data[68] = phy_init_done;
assign data[69] = idelay_ctrl_rdy;
assign data[70] = sys rst n;
assign data[71] = error;
assign trig0[0] = phy init done;
assign trig0[1] = idelay_ctrl_rdy;
assign trig0[2] = sys_rst_n;
assign trig0[3] = error;
assign trig0[4] = app_wdf_afull;
assign trig0[5] = app_af_afull;
assign trig0[6] = app_wdf_wren;
assign trig0[7] = app_af_cmd;
```

```
🍓 文件 (P) 編辑 (B) 捜索 (S) 方案 (P) 视图 (V) 格式 (T) 列 (L) 宏 (M) 脚本 (S) 高級 (A) 窗口 (H) 帮助 (H)
                                                                        _ B ×
  ddr2 sdram.v*
    icon i icon
655
656
        .CONTROLO(control)
657
658
659
    ila i ila
660
661
        .CLK(c1k0),
662
        .CONTROL (control) ,
663
        .TRIGO(trigO),
664
        .DATA(data)
665
666
667
    assign data[63:0] = app af addr;
    assign data[64] = app wdf afull;
    assign data[65] = app af afull;
    assign data[66] = app wdf wren;
    assign data[67] = app af cmd;
    assign data[68] = phy init done;
    assign data[69] = idelay ctrl rdy;
    assign data[70] = sys rst n;
    assign data[71] = error;
    assign trig0[0] = phy init done;
    assign trig0[1] = idelay_ctrl_rdy;
    assign trigO[2] = sys rst n;
679
    assign trigO[3] = error;
    assign trigO[4] = app wdf afull;
    assign trigO[5] = app af afull;
    assign trigO[6] = app wdf wren;
682
    assign trig0[7] = app af cmd,
684
685
    endmodule
```

## Add ChipScope Pro

Add these lines to the top-level Verilog file after endmodule:

```
module icon (CONTROL0);
inout[35:0] CONTROL0;
endmodule
module ila(CLK, CONTROL,
         TRIGO, DATA);
input CLK;
inout[35:0] CONTROL;
input [7:0] TRIG0;
input [71:0] DATA;
endmodule
```

```
🖁 VItraEdit - [C:\xupv5_mig_design\mig_23\example_design\rtl\ddr2_sdram.v]
                                                                            |文件(F) 編輯(E) 捜索(S) 方案(P) 视图(V) 格式(T) 列(L) 宏(M) 脚本(S) 高級(A) 窗口(W) 帮助(H)
                                                                            _ | & | × |
  ddr2_sdram.v
      assign trig0[2] = sys rst n;
    assign trig0[3] = error;
    assign trig0[4] = app wdf afull;
    assign trig0[5] = app af afull;
    assign trigO[6] = app wdf wren;
683
    assign trig0[7] = app af cmd;
684
685
    endmodule
686
    module icon (CONTROLO);
687
688
      inout[35 : 0] CONTROLO;
    endmodule
689
690
691
    module ila(CLK, CONTROL, TRIGO, DATA);
692
      input CLK;
693
      inout[35 : 0] CONTROL;
694
      input [7:0] TRIGO;
695
      input [71 : 0] DATA;
     ndmodule
696
```



#### **Generate Bitstream**

 Start a windows command shell and enter these commands:

```
cd xupv5_mig_design\mig_23\example_design\par ise_flow.bat
```

```
C:\WINDOWS\system32\cmd.exe

Microsoft Windows XP [Version 5.1.2600]
(G) Copyright 1985-2001 Microsoft Corp.

C:\>cd xupv5_mig_design\mig_23\example_design\par

C:\xupv5_mig_design\mig_23\example_design\par>ise_flow.bat
```



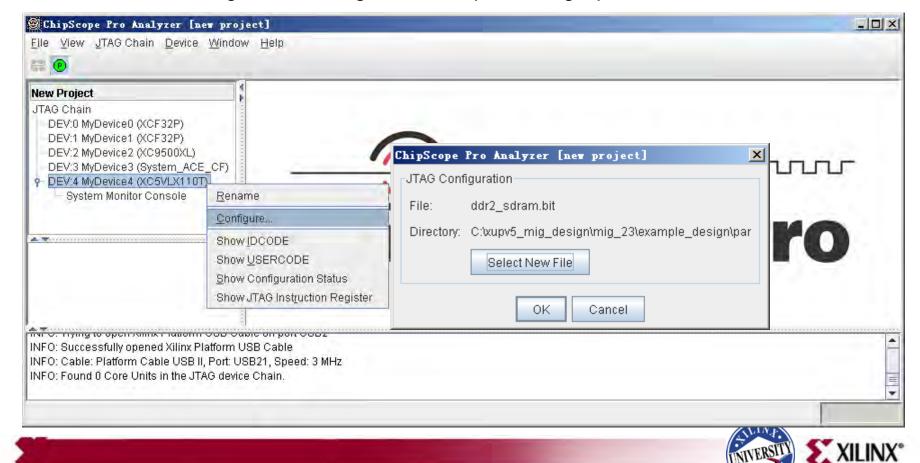
After the design compiles, open ChipScope Pro Analyzer

Click on the Open Cable Button (1)

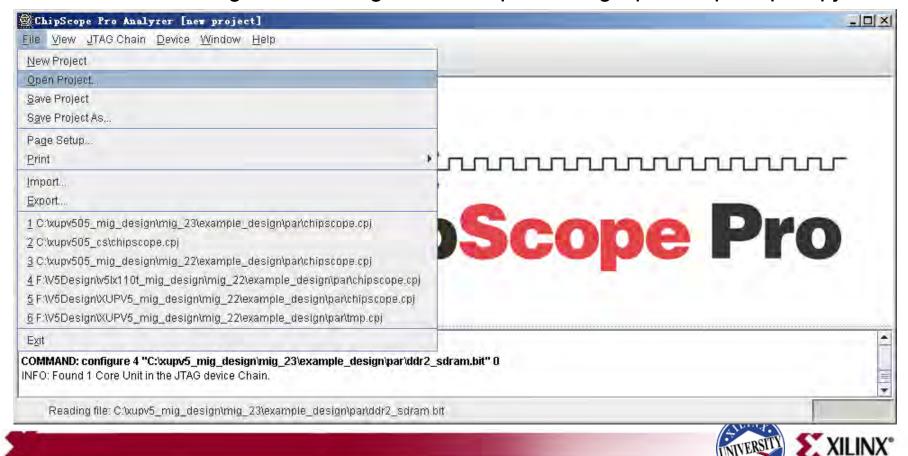




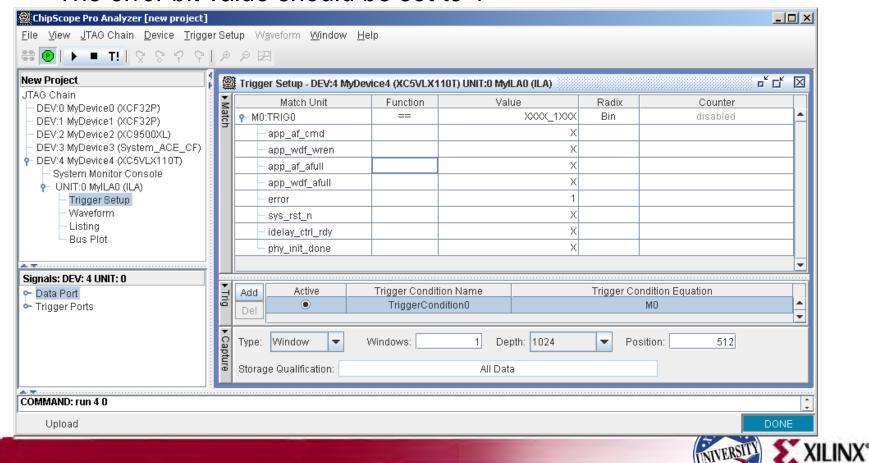
- Select Device → DEV:4 MyDevice4 (XC5VLX110T) → Configure...
- Select <Design Path>\mig\_23\example\_design\par\ddr2\_sdram.bit



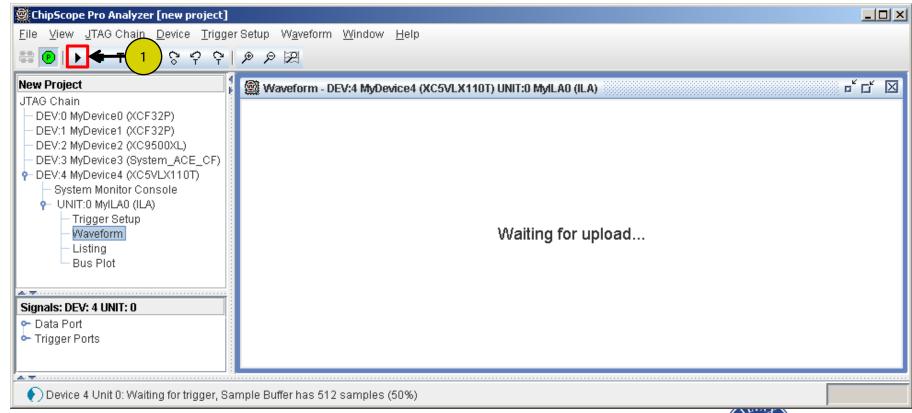
- Select File →Open Project...
- Select <Design Path>\mig\_23\example\_design\par\chipscope.cpj



- Click on Trigger Setup to view trigger settings
- The error bit value should be set to 1

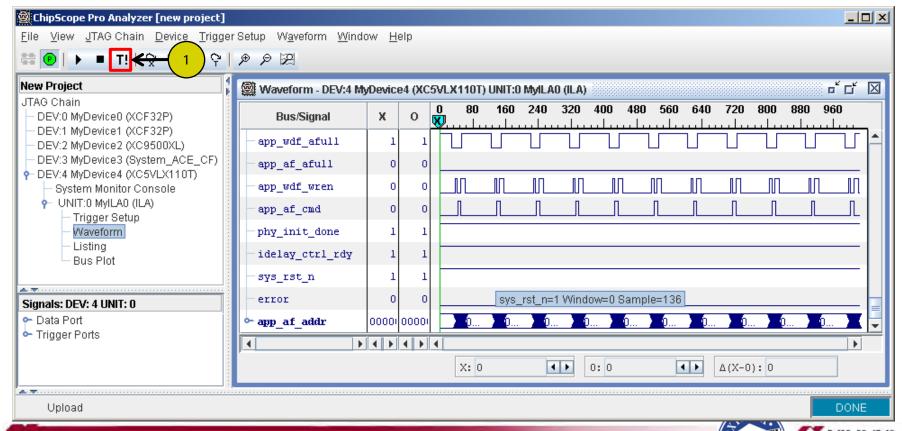


- Click on Waveform; click the Arm Trigger button (1)
- Detection of an error will cause ChipScope Pro to trigger





 To force a trigger, in order to view the waveform, click the T! button (1)



## XUPV5-LX110T DDR2 Verified at 200 MHz

- Virtex-5 –1 speed grade device supports 200 MHz
   DDR2 operation as stated in the <u>Virtex-5 datasheet</u>
- The XUPV5-LX110T SODIMM supports 200 MHz
  - Supplied DDR2 SODIMM is rated for 266 MHz operation
- The MIG test design and ChipScope Pro Analyzer verify operation of the XUPV5-LX110T with a Virtex-5
   –1 speed grade device, at the specified clock rate of 200 MHz



## **Appendix**



# XUPV5-LX110T DDR2 at 266 MHz

- An external signal generator was used to clock the MIG test design on the XUPV5-LX110T at the maximum clock rate selectable in the MIG tool, 266 MHz
- Supplied DDR2 SODIMM is rated for 266 MHz operation
- The MIG test design and ChipScope Pro Analyzer verify operation of the XUPV5-LX110T at the maximum selectable MIG clock rate of 266 MHz for a -1 speed

grade device

- See <u>UG086</u>





#### **Documentation**

- Virtex-5 FPGA User Guide
   <a href="http://www.xilinx.com/support/documentation/user\_guides/ug190.pdf">http://www.xilinx.com/support/documentation/user\_guides/ug190.pdf</a>
- Virtex-5 Packaging and Pinout Specification
   http://www.xilinx.com/support/documentation/user\_guides/ug195.pdf
- Demos on Demand–Memory Interface Solutions with Xilinx FPGAs <a href="http://www.demosondemand.com/clients/xilinx/001/page\_new2/index.asp#35">http://www.demosondemand.com/clients/xilinx/001/page\_new2/index.asp#35</a>
- Xilinx Memory Interface Generator (MIG) 2.1 User Guide <a href="http://www.xilinx.com/support/software/memory/protected/ug086.pdf">http://www.xilinx.com/support/software/memory/protected/ug086.pdf</a>
- Memory Interfaces Made Easy with Xilinx FPGAs and the Memory Interface Generator

http://www.xilinx.com/support/documentation/white\_papers/wp260.pdf

