Fundamentals of Computer Systems

Finite State Machines

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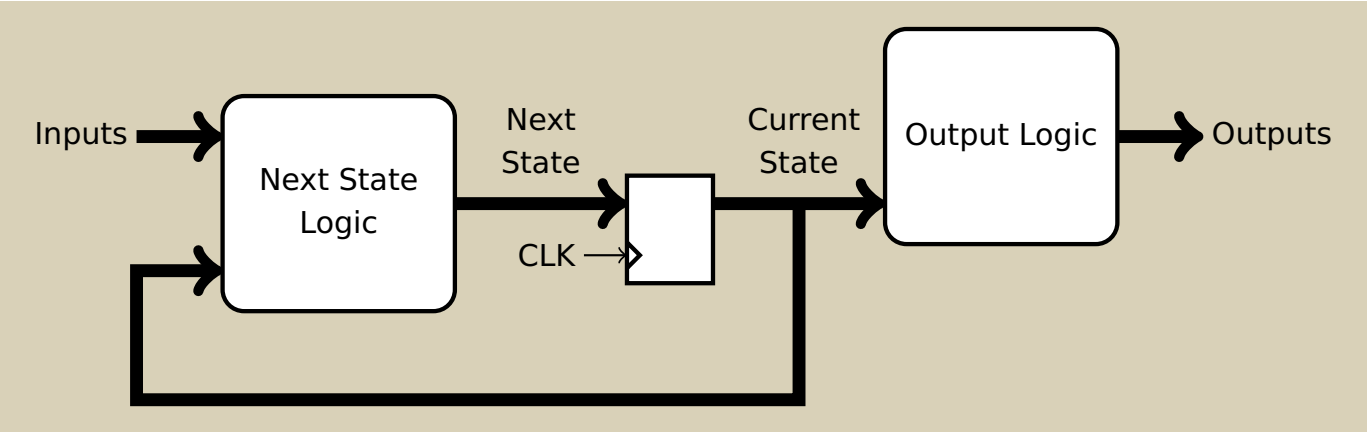
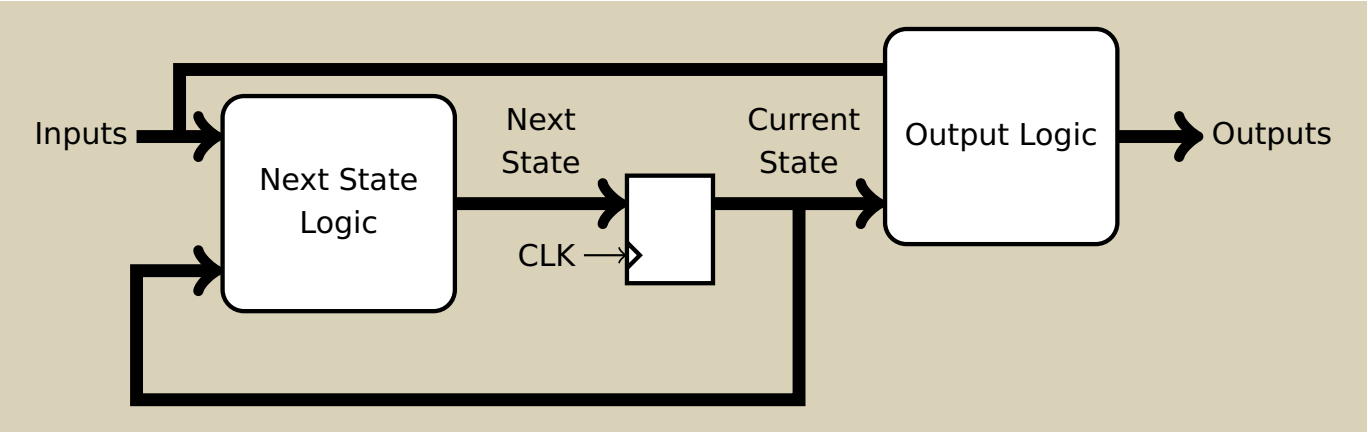
Moore and Mealy Machines



The Moore Form:

Outputs are a function of *only* the current state.

Moore and Mealy Machines

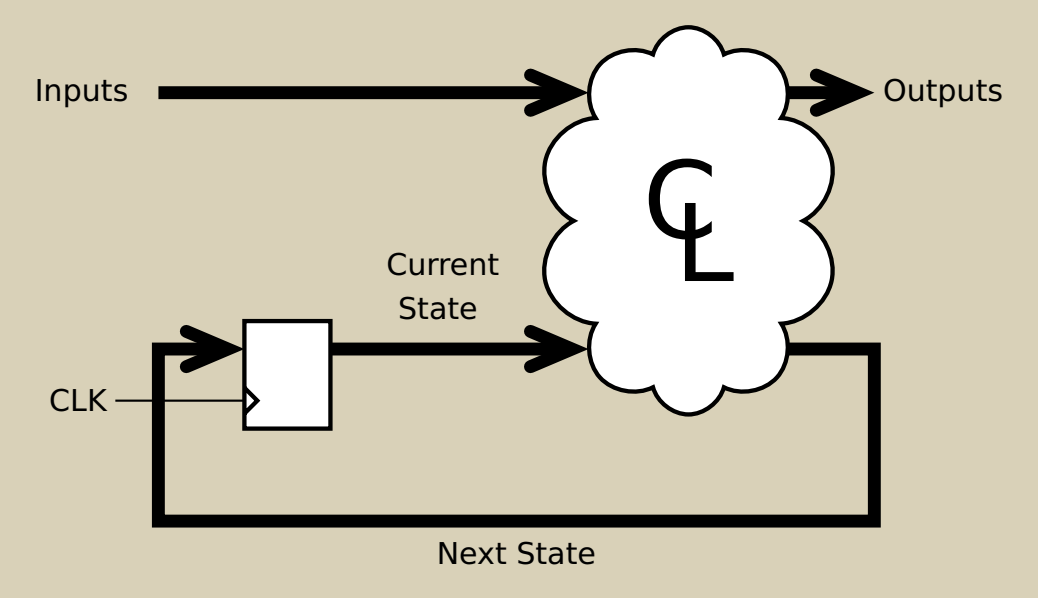


The Mealy Form:

Outputs may be a function of *both* the current state and the inputs.

A mnemonic: *Moore* machines often have *more* states.

Mealy Machines are the Most General

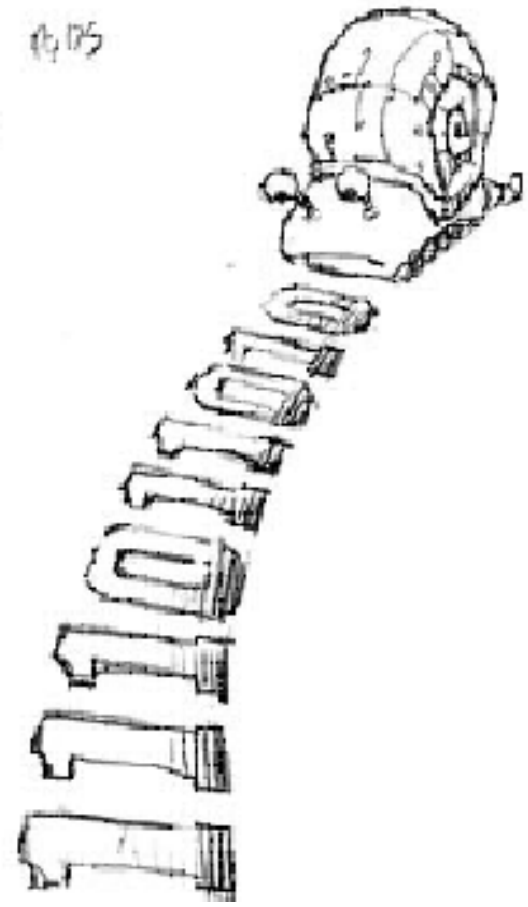


Another, equivalent way of drawing Mealy Machines

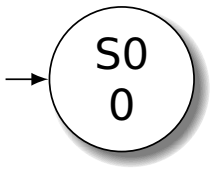
This is exactly the synchronous digital logic paradigm

Moore vs. Mealy FSMs

Alyssa P. Hacker has a snail that crawls down a paper tape with 1’s and 0’s on it. The snail smiles whenever the last four digits it has crawled over are 1101. Design Moore and Mealy FSMs of the snail’s brain.

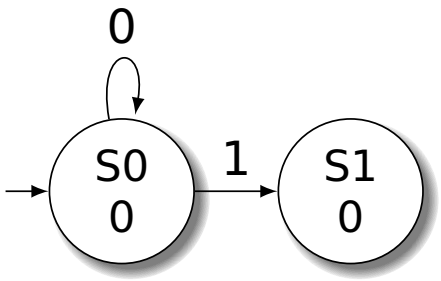


State Transition Diagrams: Looking for “1101”



Moore Machine: States indicate output

State Transition Diagrams: Looking for “1101”



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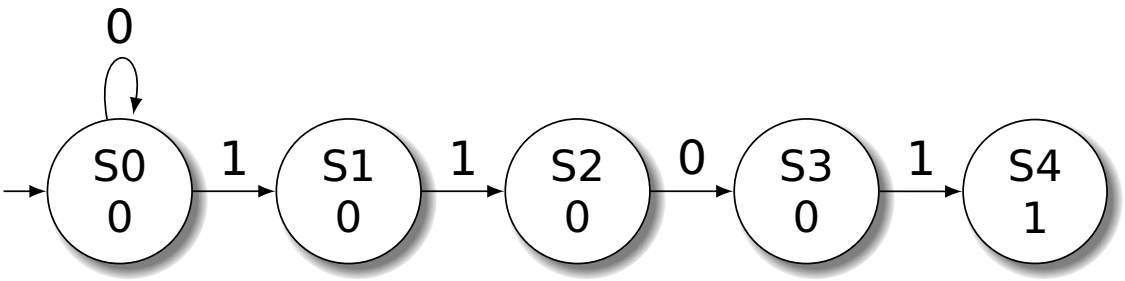

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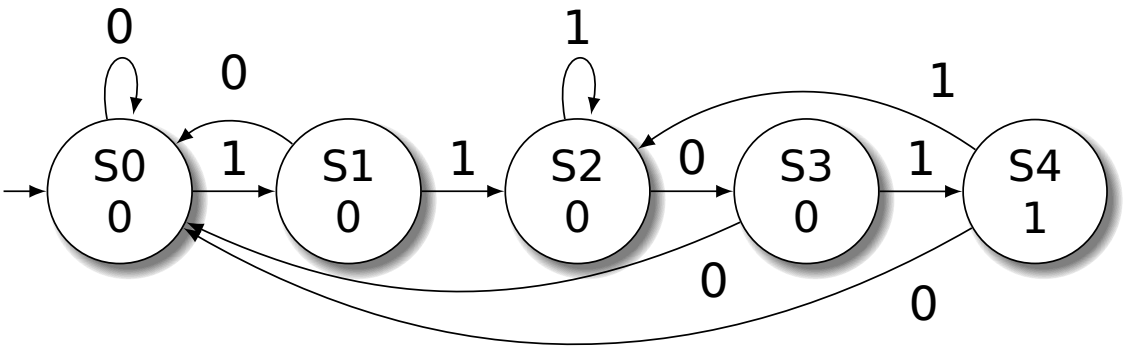

Moore Machine: States indicate output

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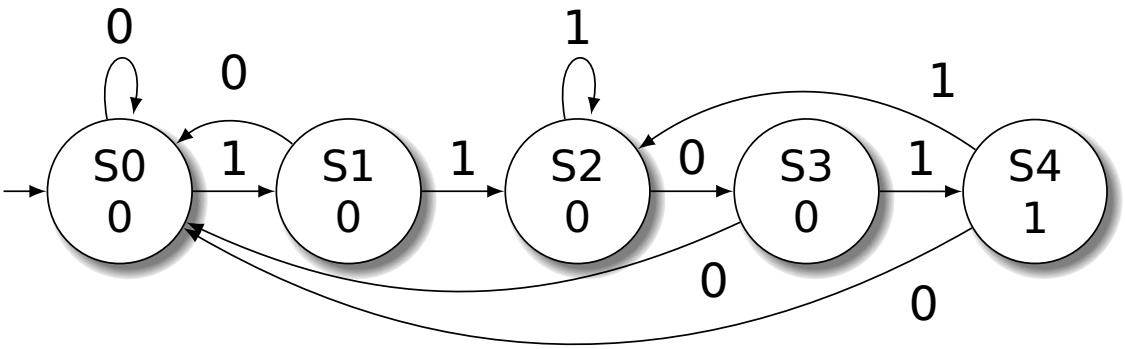
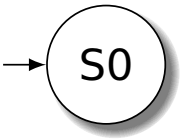
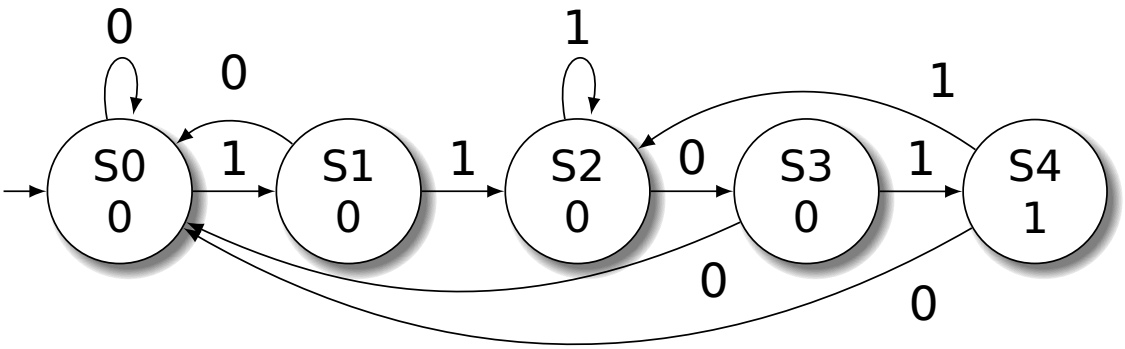


Moore Machine: States indicate output



Mealy Machine: Arcs indicate input/output

State Transition Diagrams: Looking for “1101”



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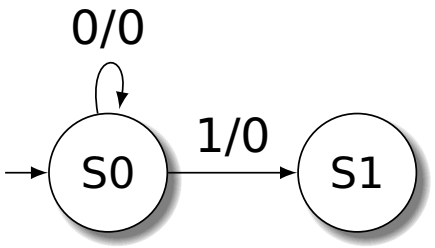

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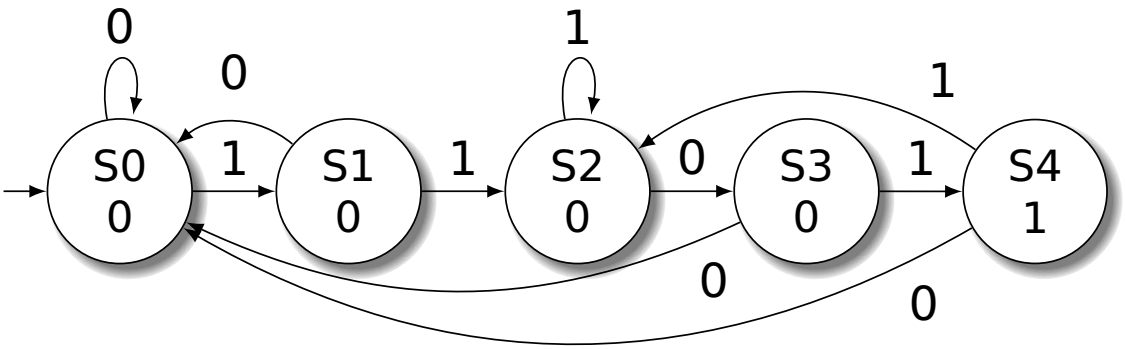

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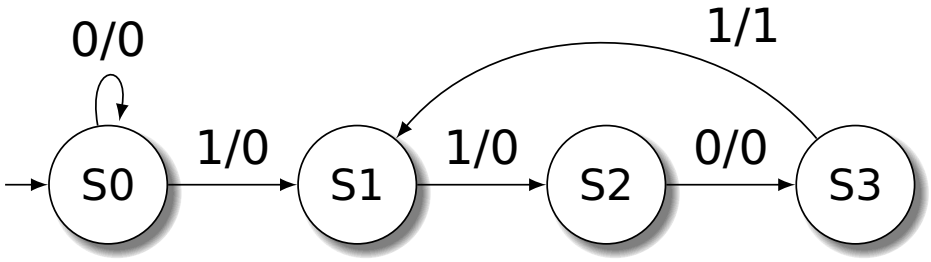
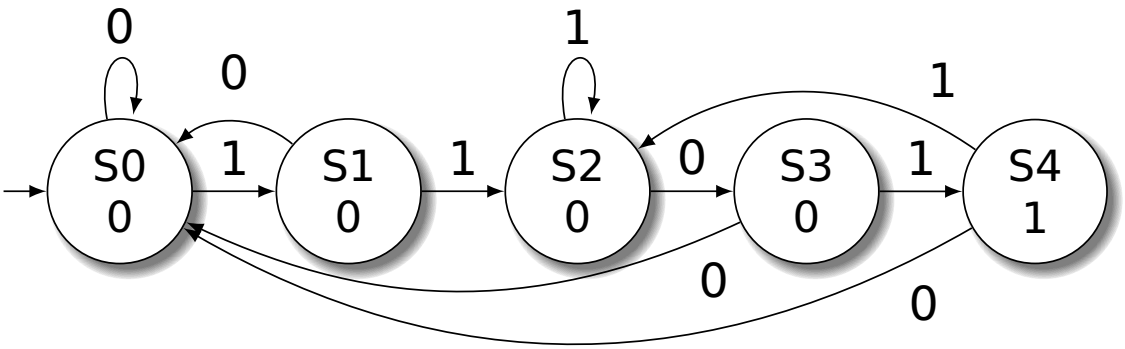
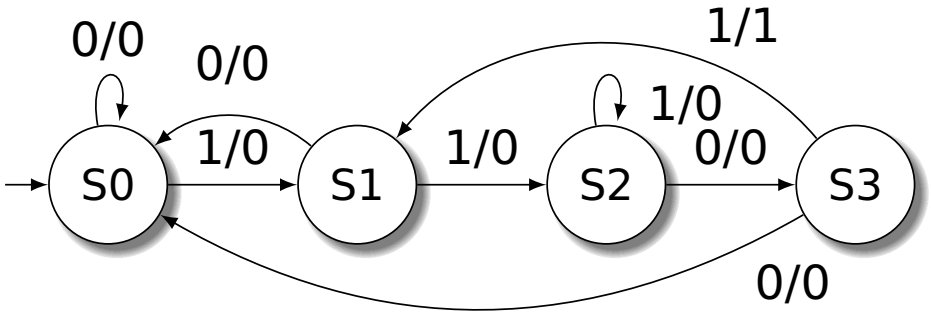


Mealy Machine: Arcs indicate input/output

State Transition Diagrams: Looking for “1101”



Moore Machine: States indicate output



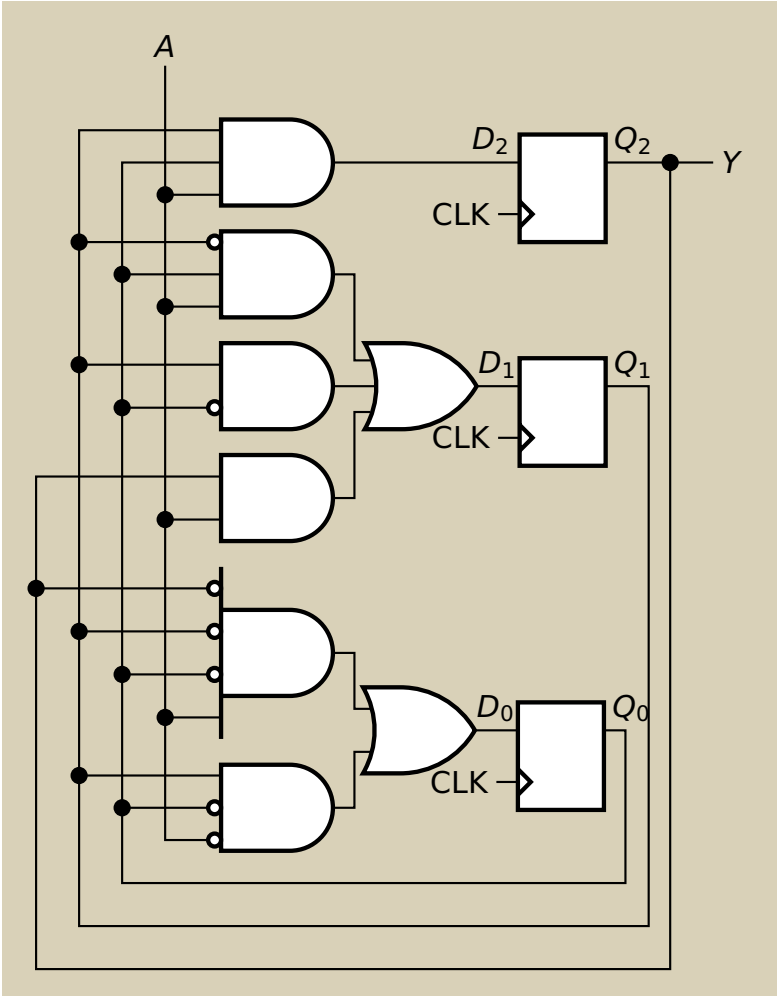
Mealy Machine: Arcs indicate input/output

Moore Machine

Next State			Output	
Q	**A**	**D**	**Q**	**Y**
S0	0	S0	S0	0
S0	1	S1	S1	0
S1	0	S0	S2	0
S1	1	S2	S3	0
S2	0	S3	S4	1
S2	1	S2		
S3	0	S0		
S3	1	S4		
S4	0	S0		
S4	1	S2		

Moore Machine

Next State			Output	
Q	**A**	**D**	**Q**	**Y**
000	0	000	000	0
000	1	001	001	0
001	0	000	010	0
001	1	010	011	0
010	0	011	100	1
010	1	010		
011	0	000		
011	1	100		
100	0	000		
100	1	010		

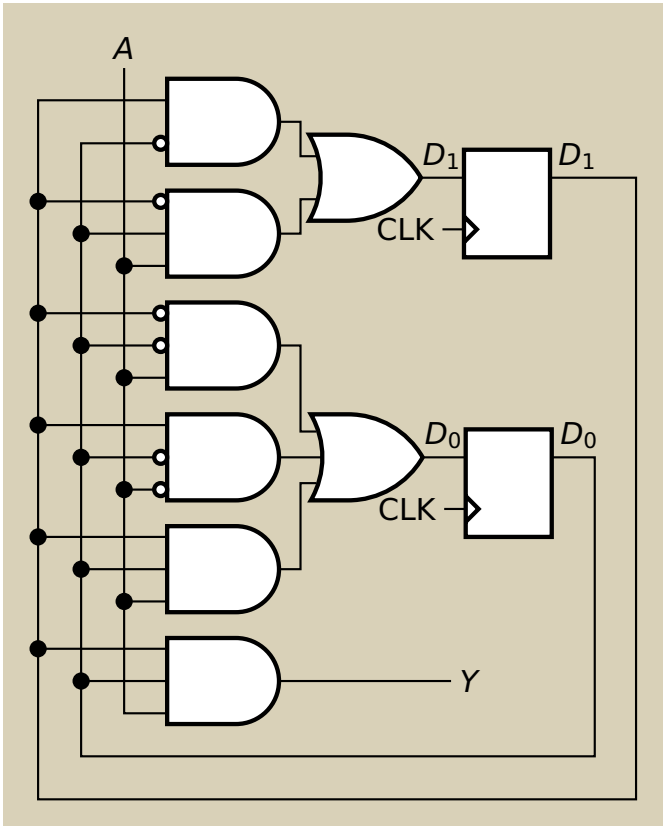


Mealy Machine

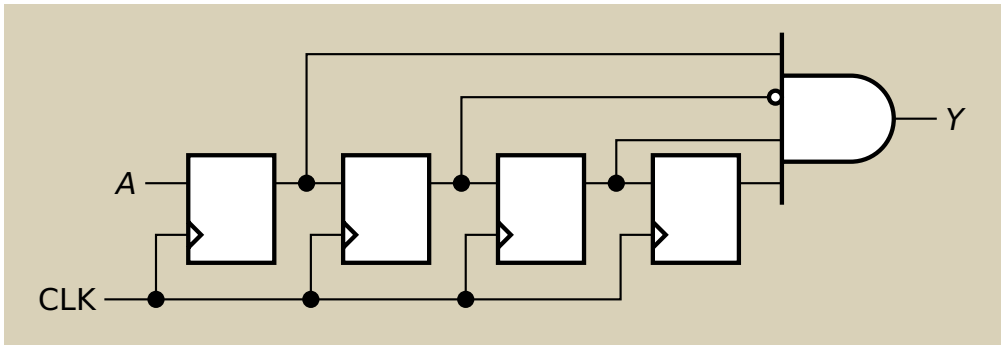
Q	A	D	Y
S0	0	S0	0
S0	1	S1	0
S1	0	S0	0
S1	1	S2	0
S2	0	S3	0
S2	1	S2	0
S3	0	S0	0
S3	1	S1	1

Mealy Machine

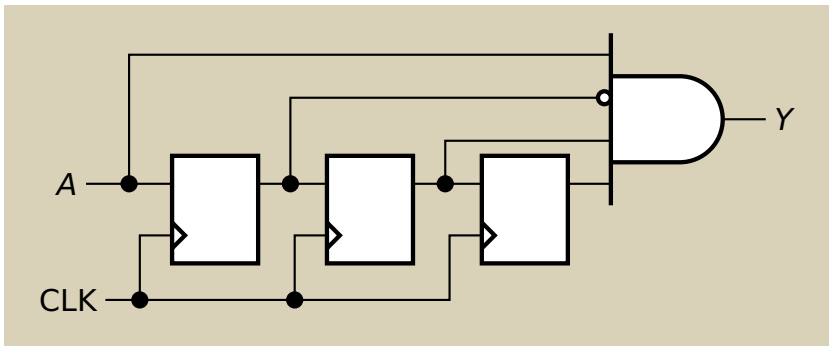
Q	A	D	Y
00	0	00	0
00	1	01	0
01	0	00	0
01	1	10	0
10	0	11	0
10	1	10	0
11	0	00	0
11	1	01	1



More Intuitive (Non-Minimal) Solutions



Moore Form: Output Depends Only on State



Mealy Form: Output Depends on Input Immediately

Finite State Machine Design Process

1. Create state transition diagram (abstract implementation of spec)
2. Select state encoding
3. Create tables for output and next state logic
4. Minimize output and next state logic
5. Wire up design (produce schematic)