Week 16

Performance

Data Size: 64x768 768x64

	bc_matmul	matmul	Change
4 lanes	92.28%	65.67%	1.4x
8 lanes	85.63%	34.22%	2.5x
16 lanes	74.85%	17.03%	4.4x

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    - Memory bandwidth = 32 x NrLanes
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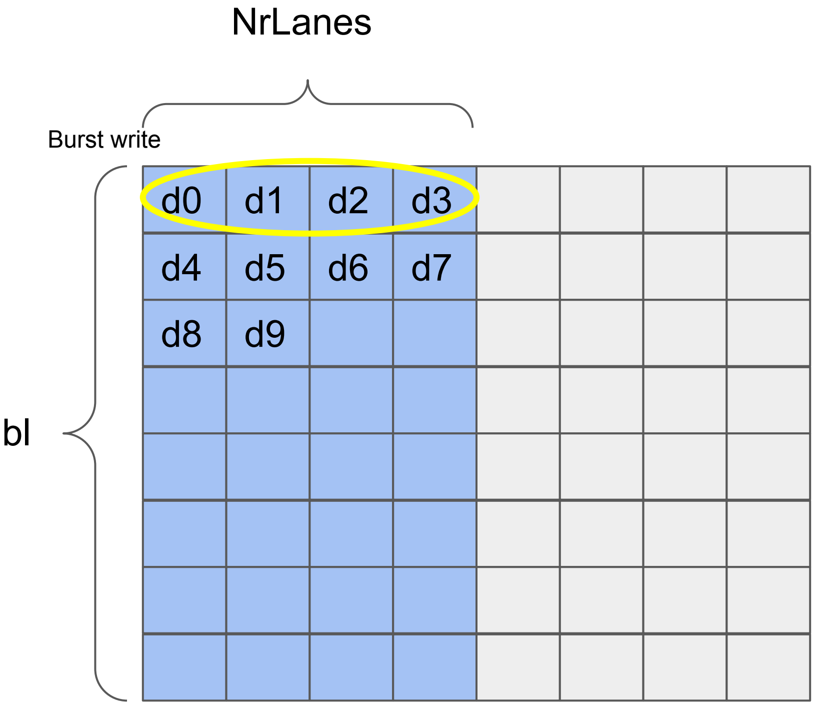

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  - Performance of ReLU & Dropout ⬇
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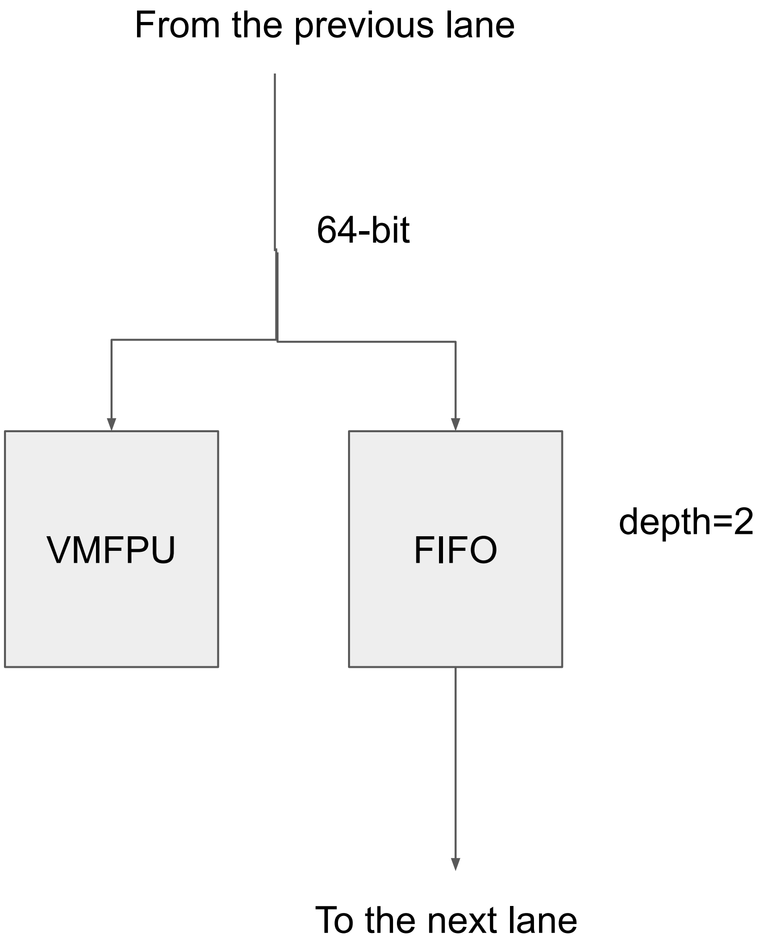
- Use different registers to load matrix A
    - false data dependency

Hardware Update

- Broadcast data
    - FIFO not full & VMFPU ready → ACK
    - If the next lane is not ready, the current lane can still execute.
    - Cut the InOut path.
        - ready_o = vmfpu_ready & ready_next



Analysis of Decreasing Utilization

- NrLanes ↑ Utilization ↓
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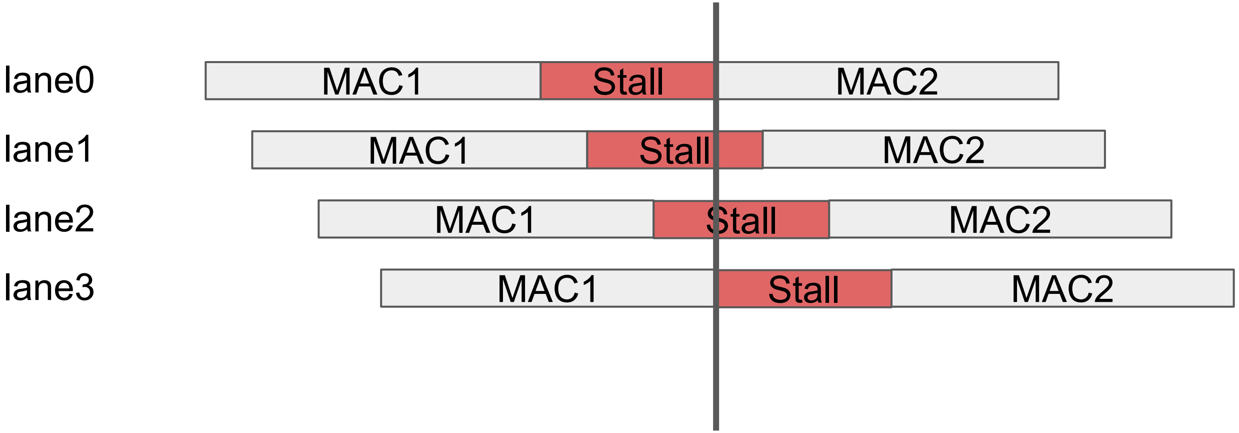

lane0
MAC1
Stall
MAC2
lane1
MAC1
Stall
MAC2
lane2
MAC1
Stall
MAC2
lane3
MAC1
Stall
MAC2