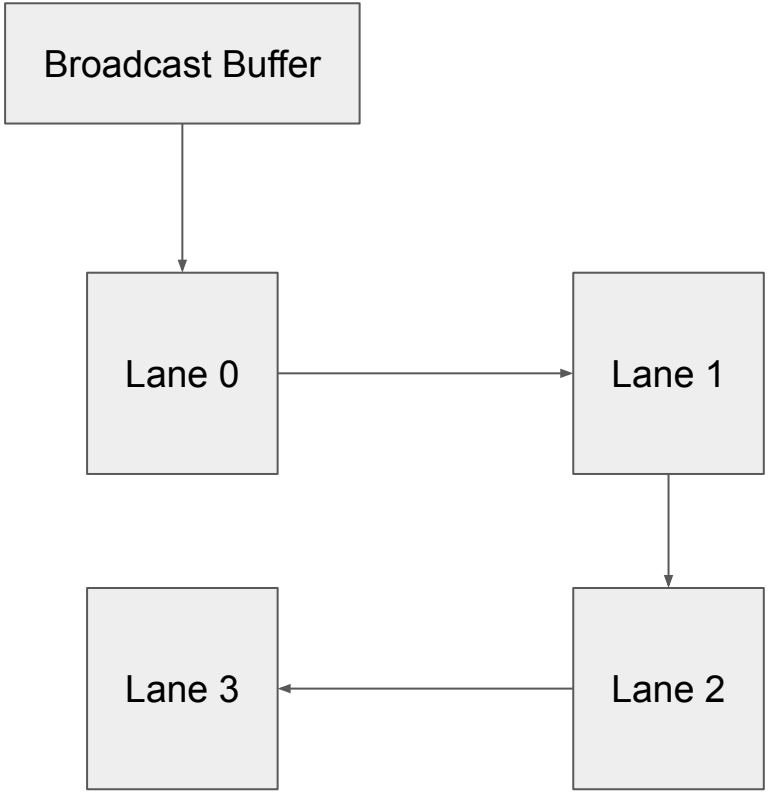
Week 15

Progress

- Finished all RTL design
- Verification (riscv_tests, new instruction test, new MatMul with unit REUSE_SIZE)
- The case of REUSE_SIZE = 4 still has some bugs
  - Some values are incorrect
  - Utilization = 98% (64x768x64, 4 lanes)
  - Old MatMul: 64%

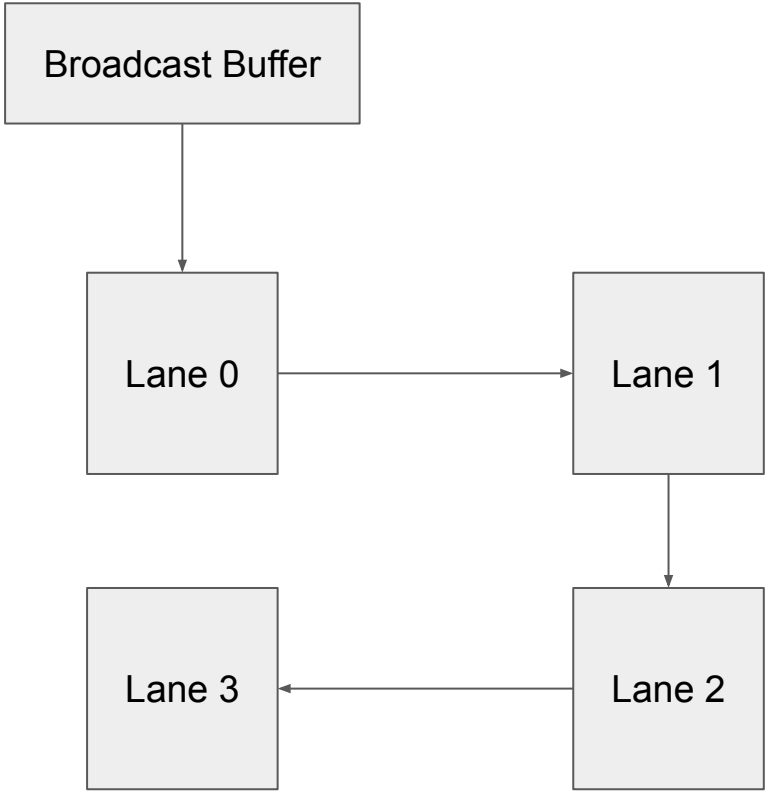
Broadcast Ring

- Lane 0
  - data_in[0] = bc_data
- Others
  - data_in[i] = data_out[i-1]
  - data_out[i] = reg(data_in[i])
- This structure requires each lane to be able to process data immediately
- When the lane is not ready, it will miss data



Broadcast Ring

- Also add a ready signal
- &ready[] = 0 →stall



Some Questions

- Hazard
  - If REUSE_SIZE = 4, vd = v8
  - Add v8, v9, v10, v11 to the hazard table in ara_sequencer
  - What else?
- AXI address misaligned in addrgen
- RTL lint