MASSACHUSETTS INSTITUTE OF TECHNOLOGY

Department of Electrical Engineering and Computer Science

6.301 Solid State Circuits

Fall 2013 — Issued : Dec 10, 2013

Problem Set 9 — Due : Not due

Problem 1: In this problem, a transistor is controlled by supplying a base current drive as seen in Figure 1. Analyze the dynamics of the transistor and sketch q_F, q_S, i_C, and i_B versus time. Each sketch should clearly indicate important slopes, final values, time constants, etc. Read this whole problem before starting to solve the first part.

1. Assume that the transistor remains in the forward active region. Determine the time constants and final values etc, and sketch the curves.

2. Since $\beta_F i_B > i_{C_{SAT}}$, the device will not remain in the forward active region for all time. Indicate on your graphs the point at which saturation occurs. Find q_{BO}, the final values (in saturation) for i_C and q_S and evaluate the time constant τ_S. Continue the sketches. How long does it take to traverse the active region?

3. Now consider turning off the device, $i_B = 0$. Assume that athe transistor remains saturated, that is $i_C = i_{C_{SAT}}$ for all time. Determine the final values for q_S and sketch the curves.

4. Obviously, the transistor does not remain saturated but enters the forward active region when q_S equals zero. Determine the storage delay time, that is, the time during which the device remains saturated even though $i_B = 0$. Determine the time spent crossing the active region. Sketch the curves.

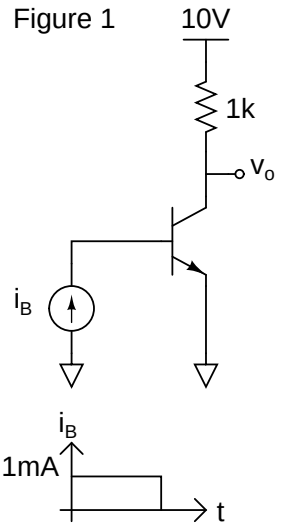
5. Compare turn-on times and turn-off times: explain the difference.

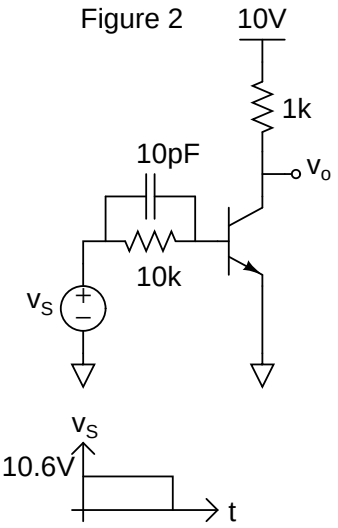
6. It is observed that the storage delay time decreases if the input pulse duration is reduced. Explain.

Problem 2: Charge Control

1. Sketch q_F, q_S, i_C, and i_B versus time for the circuit shown in Figure 2.

2. Now assume that you are free to choose the capacitor value. what value should be chosen so that final conditions for both the turn on and the turn off transient are established as quickly as possible?





For both circuits: $\tau_F = 2ns$ $\beta_F = 200$
$\tau_R = 10ns$ $\beta_R = 10$
$v_{CE(SAT)} = 0V$ $v_{BE} = 0.6V$ for $i_C > 0$
Ignore SCL's

Problem 3: Charge Control

1. Initially, the circuit shown in Figure 3 is assumed to be in equilibrium with the switch open. Calculate: q_F, q_S, i_C.

2. At $t = 0$, the switch is closed, assume instantaneous slosh. Also assume that, after the slosh transition, the circuit is quasistatic. Sketch and dimension graphs of $q_F(t)$, $q_S(t)$ and $i_C(t)$. Be sure to indicate relevant slopes, initial and final values, time constants, etc. Approximately sketch the distribution of charge in the base. Clearly illustrate the slosh transition and the equilibrium distribution.

Assume: $\tau_{BF} = 100ns$ $\beta_F = 100$
$\tau_{BR} = 10ns$ $\beta_R = 5$
$v_{CE(SAT)} = 0V$
Ignore SCL's

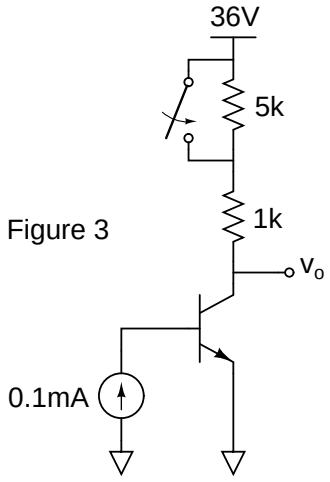
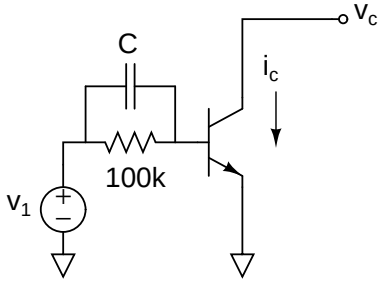


Figure 3

Problem 4: A transistor is connected in the circuit shown below.



The voltage v_1 has made a 0 to $10.6V$ step. The approximate collector current waveform that results is $i_C(t) = 1mA + 2mA(1 - e^{-t/100ns})$, $t > 0$. Determine the parameters τ_F, τ_{BF}, and β for the transistor. Also find the value of capacitor C. You may assume that $v_{BE} = 0.6V$ for any significant value of i_C.

Problem 5: The circuit shown below is driven by a voltage source, $v_s(t)$. You may assume that $v_{BE} = 0.6V$ for any I_C, when the transistor is in the forward active region. All space charge layer capacitances are zero.

1. Assume that $C = 0$. Sketch and dimension $v_o(t)$ and $q_B(t)$. Note that $q_b(t)$ is the excess minority charge in the base.

2. If $C = 1pF$, sketch and dimension $v_o(t)$ and $q_B(t)$. You may assume that the quasistatic approximation is valid.

3. Suppose that when you assembled the circuit, you inadvertently inserted the transistor upside down. The emitter and collector leads are now reversed. Recalculate parts 1 and 2 for $v_o(t)$ and $q_R(t)$.

Assume: $\tau_F = 1ns$ $\beta_F = 100$
$\tau_R = 20ns$ $\beta_R = 5$