

Resistor Network Sensing Breadboard

by

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Submitted to the Department of Electrical Engineering and Computer
Science

in partial fulfillment of the requirements for the degree of
Master of Engineering in Electrical Science and Engineering

at the

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Abstract

Blah Blah Blah

Thesis Supervisor: Gerald Jay Sussman

Title: Panasonic Professor of Electrical Engineering

Acknowledgments

For Jim

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Chapter 1

Introduction

Blah Blah Blah

1.1 History of Breadboards

Blah Blah

1.2 Modern Breadboards

Blah Blah

1.3 Proposed Solution

Blah Blah

1.4 Implementation to Date

Blah Blah

Chapter 2

Theory

Blah Blah

2.1 RLC Elements

Blah Blah

2.2 Frequency Domain Perspective

Blah Blah

2.3 Network Analysis

Blah Blah

Chapter 3

Network Sensing Algorithm

Blah Blah

3.1 Grounding Clause

Blah Blah

3.2 Two Node Network

Blah Blah

3.3 Three Node Network

Blah Blah

3.4 N Node Network

Blah Blah

3.5 Element Identification

Blah Blah

3.5.1 From Resistance to Impedance

Blah Blah

3.5.2 Parallel RLC Branches

Blah Blah

3.5.3 Finite Difference Stencil

Blah Blah

3.5.4 Component Value Calculation

Blah Blah

3.6 Reconstructing the Network

Blah Blah

Chapter 4

Simulation

Overview + Block Diagram Blah Blah

4.1 NgSpice and Netlists

Blah Blah

4.2 Methods

4.2.1 Generate Random Netlist

4.2.2 Inserting Voltage Sources

4.2.3 Inserting Voltage Probes

4.2.4 Inserting Grounds

4.3 Executing NSA

Wouldn't we all?

4.3.1 Calculate $Z_{||}(f)$

4.3.2 Calculate $V_n(f)$

4.3.3 Calculate $Z_{nm}(f)$

4.3.4 Finite Difference

4.3.5 Element Identification

4.3.6 Network Reconstruction

4.4 Output to JSON

Blah Blah

4.5 D3?

???? maybe

Chapter 5

Hardware

Block diagram / Schematic

5.1 Low Cost

'cause we're cheap!

5.2 Node Voltage Reading

ADC+multiplexer

5.3 Signal Generator

V_{source} + buffer

5.4 Test Voltage Current Sensing

Diff amp + current sense + ADC

5.5 High-side Switches

hi

5.6 Low-side Switches

lo

5.7 PCB Mounted Breadboard

5.8 Hardware Prototypes

Chapter 6

Firmware

Block Diagram

6.1 Fast and Scalable [rename]

16 1MSPS ADCs all at once, multiplexed out.

6.2 ADC

6.2.1 ADC Timers

6.2.2 ADC DMA

6.2.3 Data Reconstruction

6.3 DAC

6.3.1 DAC Timer

6.3.2 DAC DMA

6.3.3 DAC Wavetables

6.4 USB

6.4.1 USBACM

6.4.2 Command List

Chapter 7

Software Control

7.1 Medicine Routine

The routine that sends the obtuse control commands given a small number of sensible inputs

7.1.1 Data Reconstruction

10-bits from 8-bit serial data

7.2 Finding Amplitude

7.2.1 Tracking Method?

This one didn't work so well.

7.2.2 FFT

Yeah, this one works real well.

7.3 Node Iteration Loop

7.3.1 Sampling

7.3.2 Finite Differencing

7.3.3 Resistor Characterizing

7.4 JSON Update

Chapter 8

Results

8.1 Simulation Performance

8.2 Hardware Performance

8.2.1 Block Performance

How each block of hardware performed individually and why

8.2.2 Capacitive Coupling

8.2.3 Limits of Operation

Theoretical limits of system performance based on block performance

8.3 System Performance

8.3.1 Speed of Operation

8.3.2 Accuracy

8.3.3 Dynamic Range

8.3.4 Odd Behavior

Capacitors

8.4 Improvements

8.4.1 L, C, D

8.4.2 VGA for ADC's, DAC, and Differential Amplifier

8.4.3 Variable Sense Resistor

8.4.4 Better Switches

8.4.5 Three Terminal Devices

Try Transistors

8.4.6 Better Schematic Display

8.4.7 Faster Algorithm

Appendix A

Tables

Table A.1: Armadillos

Armadillos	are
our	friends

Appendix B

Figures

Figure B-1: Armadillo slaying lawyer.

Figure B-2: Armadillo eradicating national debt.