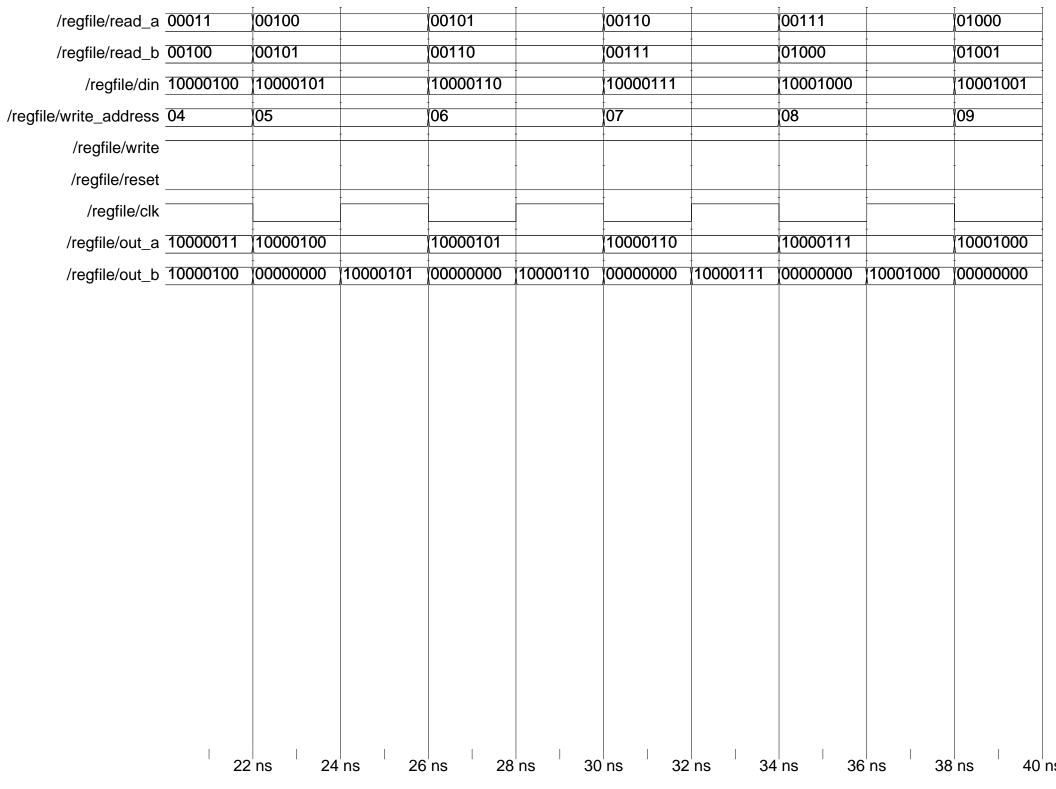
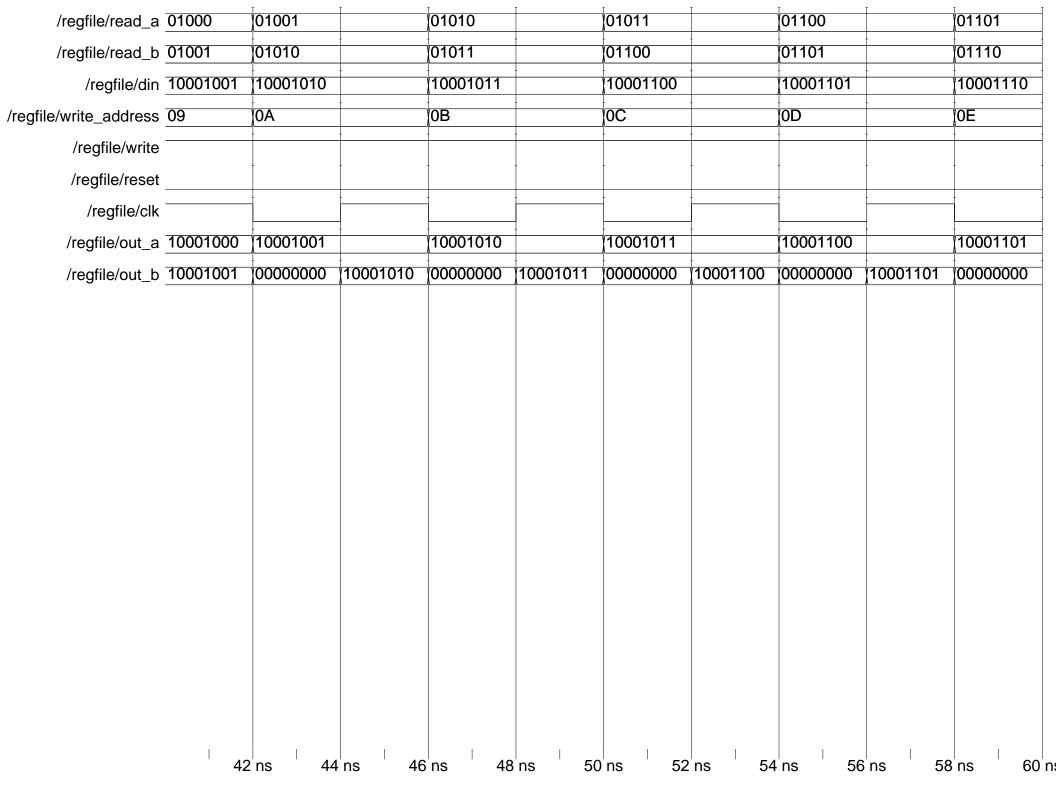


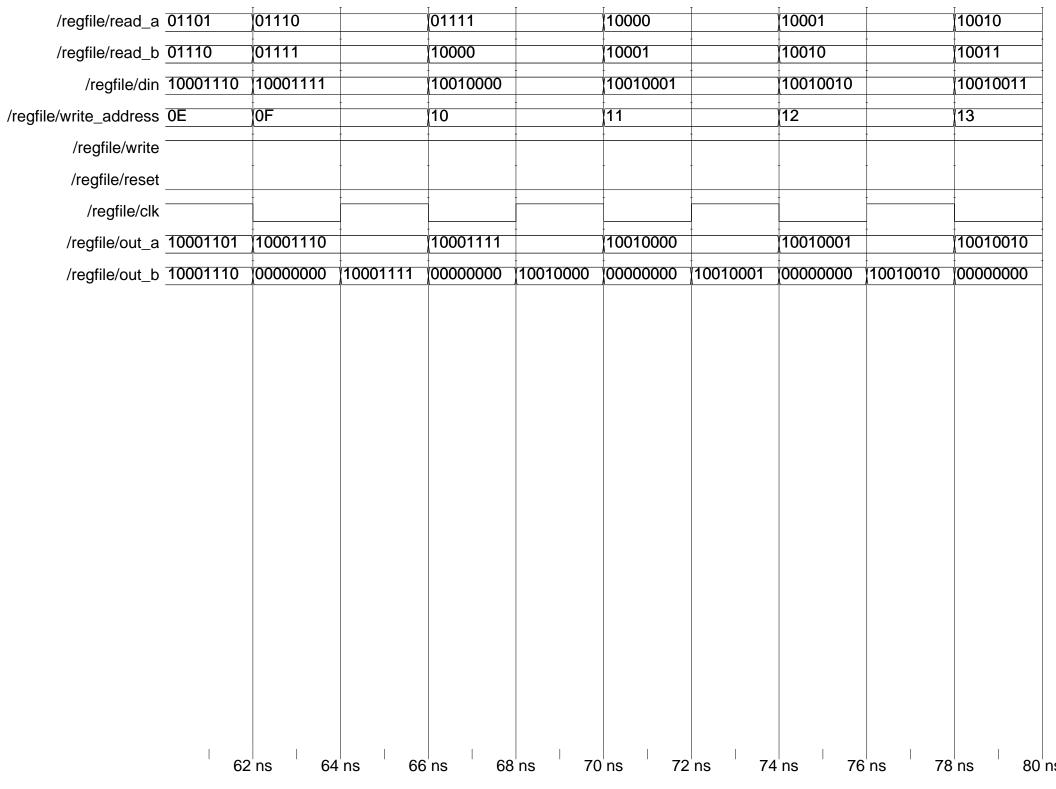
Entity:regfile Architecture:regfile_arch Date: Tue Oct 26 03:06:59 PM EDT 2021 Row: 1 Page: 1



Entity:regfile Architecture:regfile_arch Date: Tue Oct 26 03:06:59 PM EDT 2021 Row: 2 Page: 2



Entity:regfile Architecture:regfile_arch Date: Tue Oct 26 03:06:59 PM EDT 2021 Row: 3 Page: 3



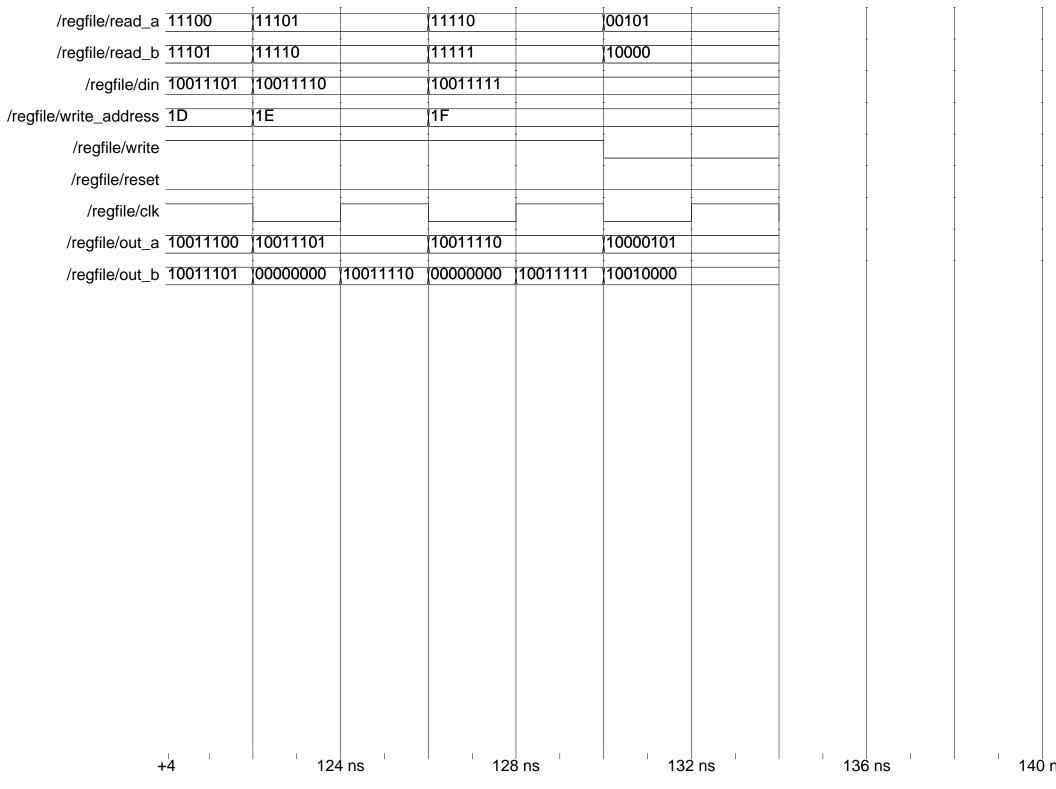
Entity:regfile Architecture:regfile_arch Date: Tue Oct 26 03:06:59 PM EDT 2021 Row: 4 Page: 4

/regfile/read_a	10010	10011		10100		10101		10110		10111
/regfile/read_b	10011	10100		10101		10110	-	10111		11000
/regfile/din	10010011	10010100		10010101		10010110		10010111		10011000
/regfile/write_address	13	14	+	15	-	16		17	-	18
/regfile/write		+	<u> </u>	-	-	†	-	<u> </u>	•	
/regfile/reset						<u> </u>		1		
/regfile/clk		-								
/regfile/out_a	10010010	10010011		10010100		10010101		10010110		10010111
/regfile/out_b	10010011	00000000	10010100	00000000	10010101	00000000	10010110	00000000	10010111	0000000
-	+4	84	ns	88	ns	92	2 ns	96	3 ns	100 n

Entity:regfile Architecture:regfile_arch Date: Tue Oct 26 03:06:59 PM EDT 2021 Row: 5 Page: 5

/regfile/read_a	10111	11000		11001		11010		11011		11100
/regfile/read_b	11000	11001		11010		11011		11100	•	11101
/regfile/din	10011000	10011001		10011010		10011011		10011100		10011101
/regfile/write_address	18	19		1A	-	1B	_	1C	-	1D
/regfile/write		-	-	-		-	-	-	+	
/regfile/reset									+	
/regfile/clk										
/regfile/out_a	10010111	10011000		10011001		10011010	+	10011011	+	10011100
/regfile/out_b	10011000	0000000	10011001	0000000	10011010	00000000	10011011	00000000	10011100	0000000
4	-4	104	l ns	108	ns '	112	2 ns	110	6 ns	120 r

Entity:regfile Architecture:regfile_arch Date: Tue Oct 26 03:06:59 PM EDT 2021 Row: 6 Page: 6



Entity:regfile Architecture:regfile_arch Date: Tue Oct 26 03:06:59 PM EDT 2021 Row: 7 Page: 7