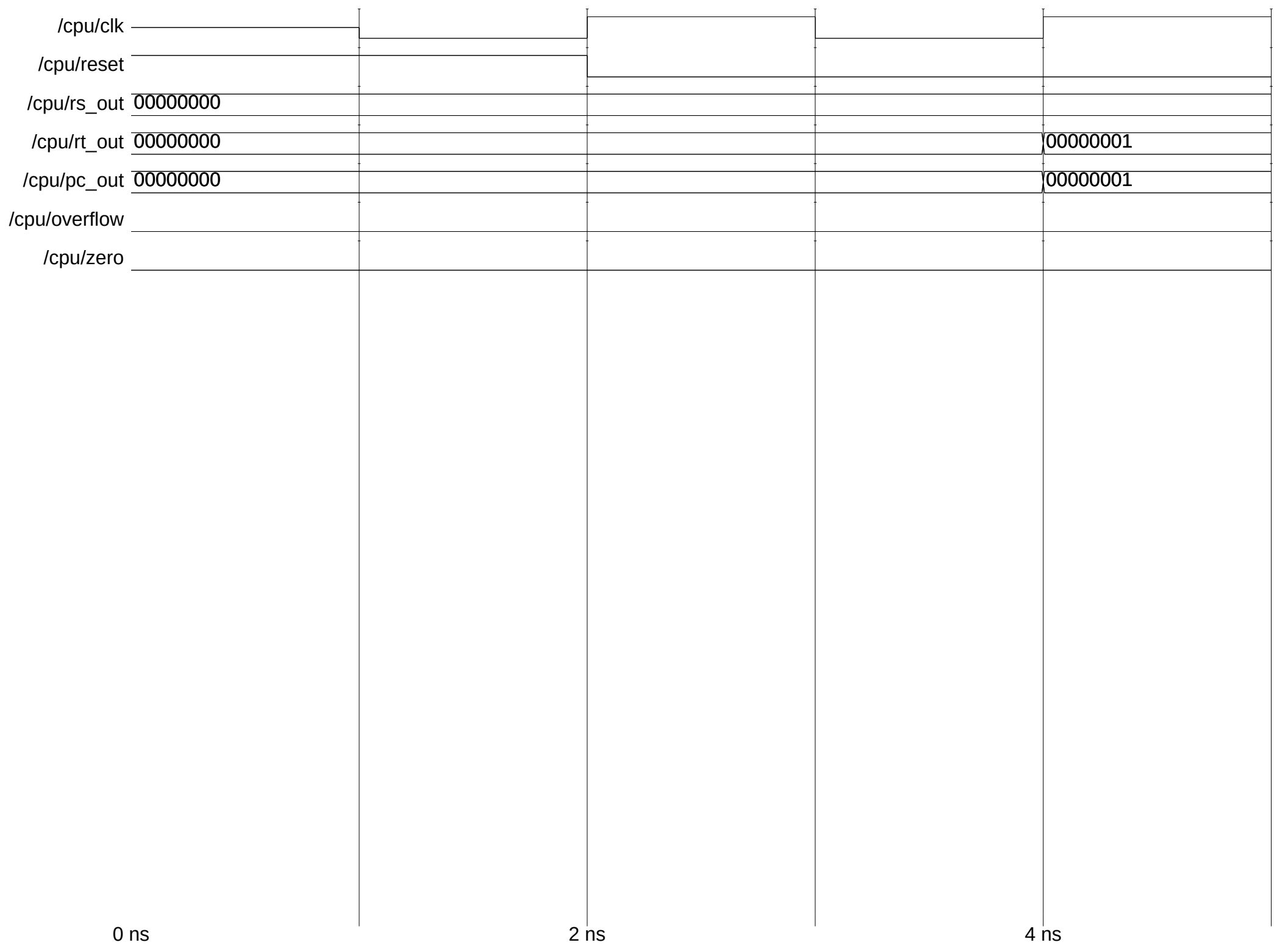

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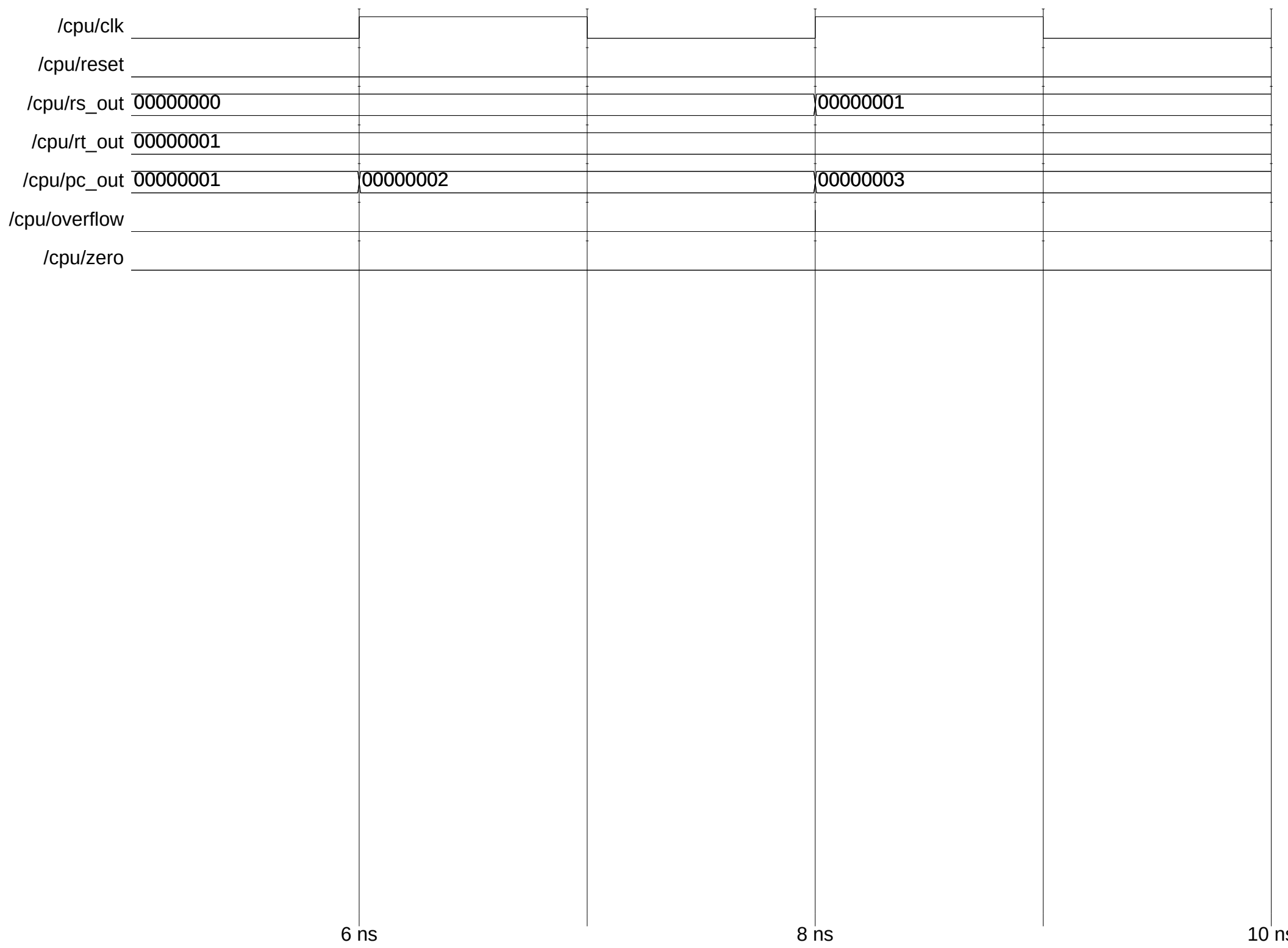
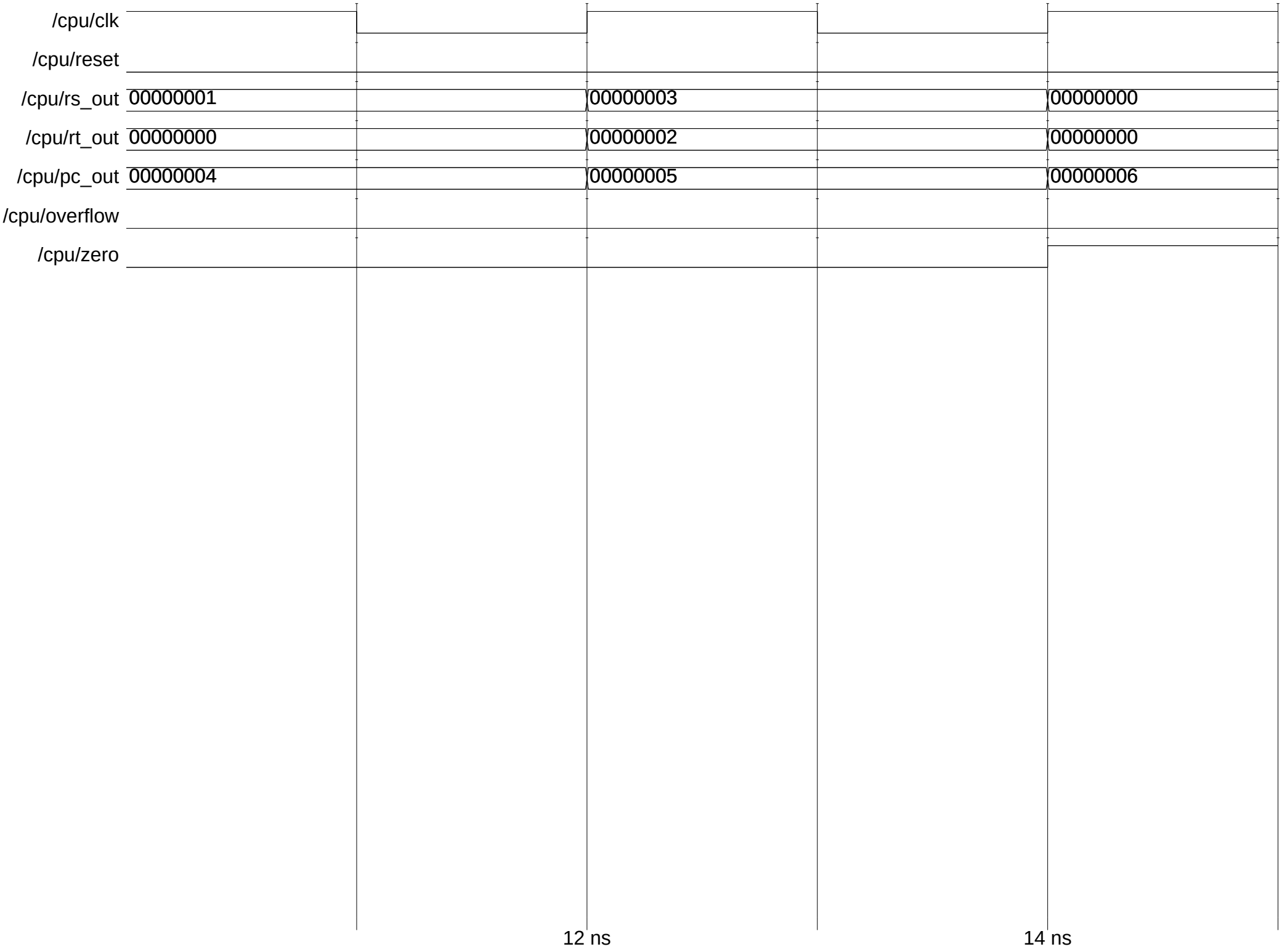
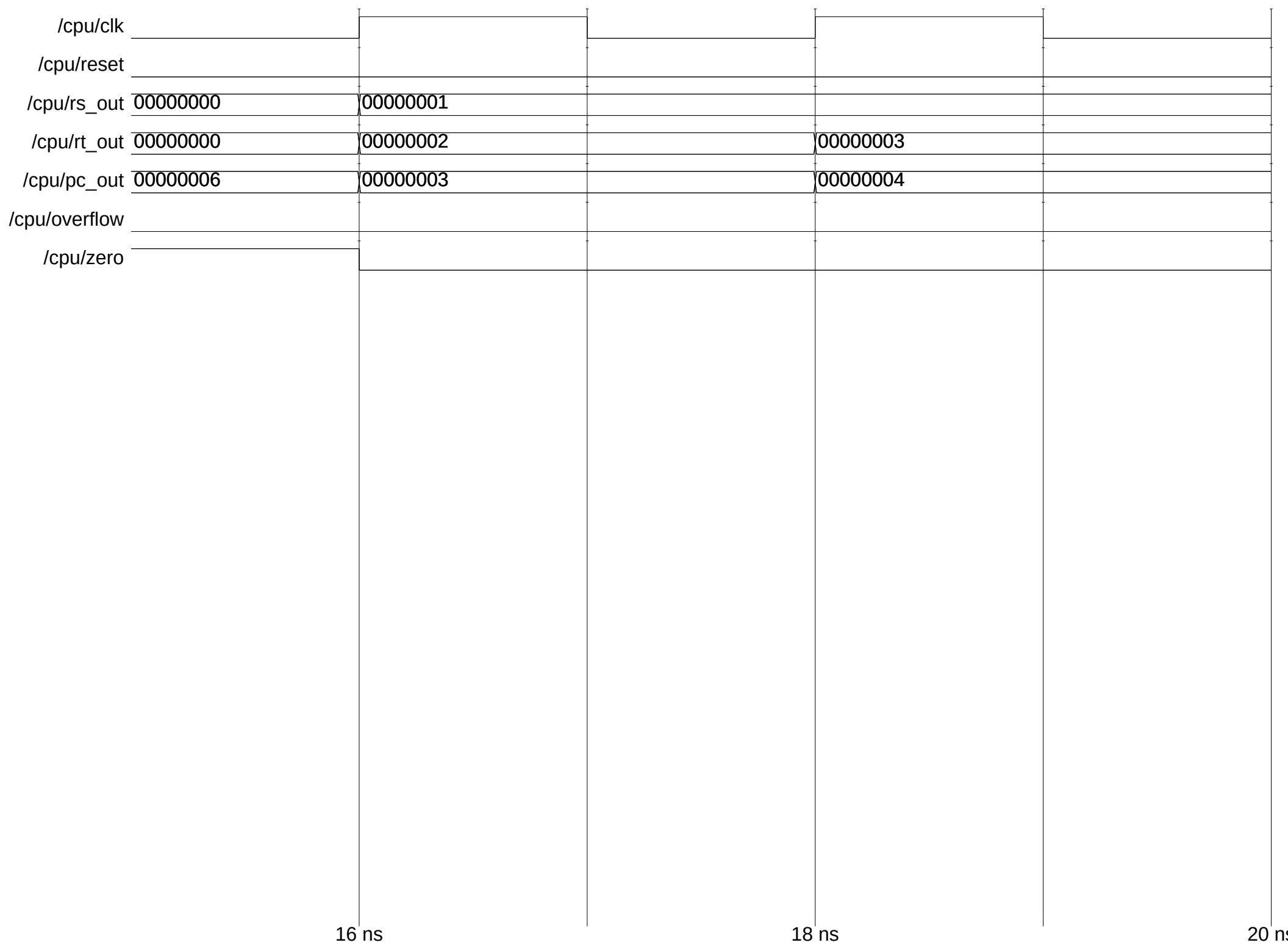
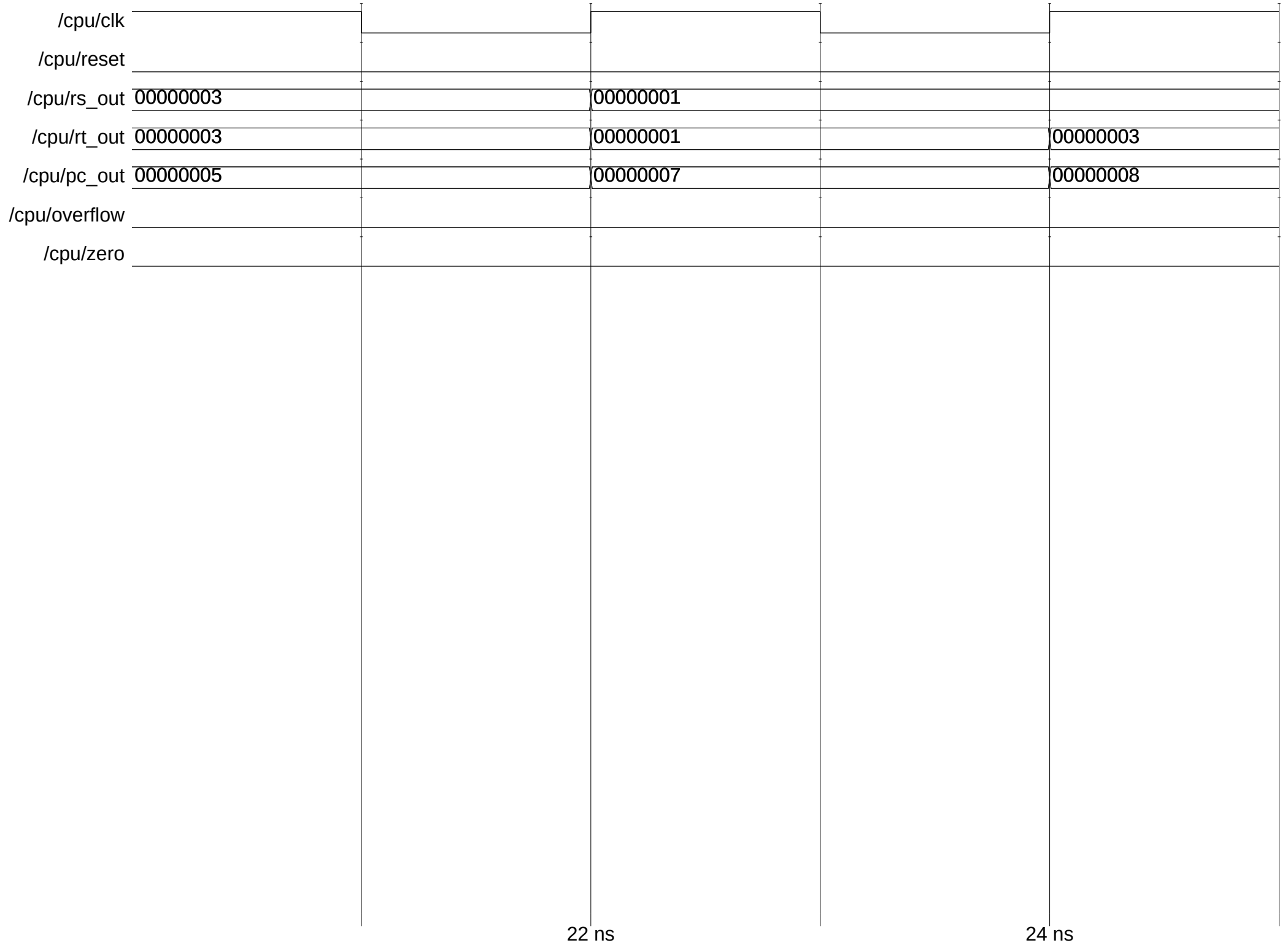
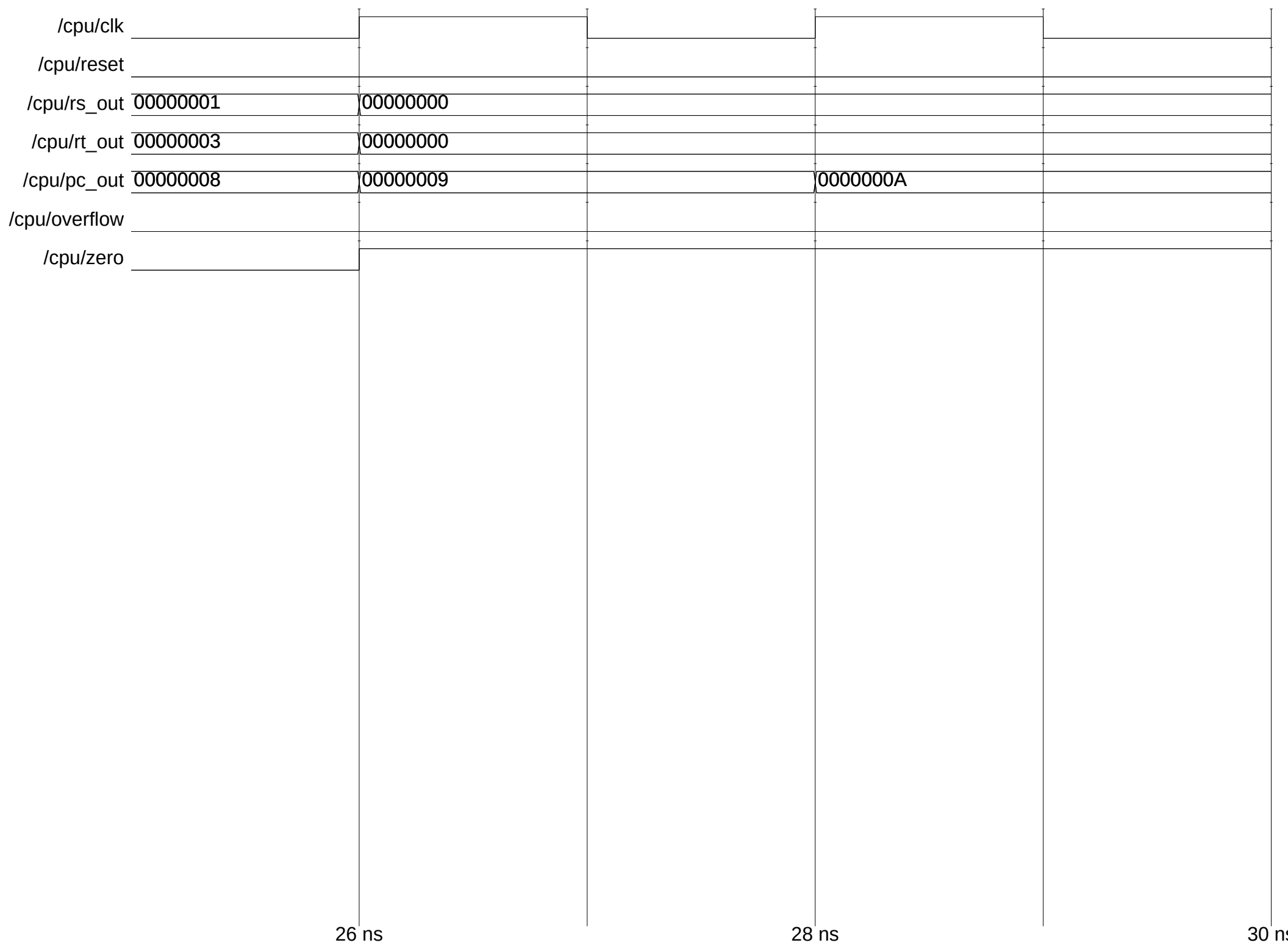

/cpu/clk
/cpu/reset
/cpu/rs_out
00000000
00000001
/cpu/rt_out
00000001
/cpu/pc_out
00000001
00000002
00000003
/cpu/overflow
/cpu/zero
6 ns
8 ns
10 ns


/cpu/clk
/cpu/reset
/cpu/rs_out
00000001
00000003
00000000
/cpu/rt_out
00000000
00000002
00000000
/cpu/pc_out
00000004
00000005
00000006
/cpu/overflow
/cpu/zero
12 ns
14 ns


/cpu/clk
/cpu/reset
/cpu/rs_out
00000000
00000001
/cpu/rt_out
00000000
00000002
00000003
/cpu/pc_out
00000006
00000003
00000004
/cpu/overflow
/cpu/zero
16 ns
18 ns
20 ns


/cpu/clk
/cpu/reset
/cpu/rs_out
00000003
00000001
/cpu/rt_out
00000003
00000001
00000003
/cpu/pc_out
00000005
00000007
00000008
/cpu/overflow
/cpu/zero
22 ns
24 ns


/cpu/clk
/cpu/reset
/cpu/rs_out
00000001
00000000
/cpu/rt_out
00000003
00000000
/cpu/pc_out
00000008
00000009
0000000A
/cpu/overflow
/cpu/zero
26 ns
28 ns
30 ns