# An ultra-low noise, high-voltage piezo driver

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We present an ultra-low noise, high voltage driver suited for use with piezoelectric actuators and other low-current applications. The architecture leverages a commercially available, small-form-factor integrated circuit (IC) for generating high voltage outputs. The IC uses a flyback configuration switching regulator to generate up to 250V in our design (but up to 1kV or more with small modification), and a high slew-rate op-amp capacitively coupled to the output compensates for the switching noise. A low-voltage ($\pm 10\,\mathrm{V}$), high bandwidth modulation input is capable of summing small voltage corrections onto the output, making the driver well suited for use in closed-loop feedback applications.

## I. INTRODUCTION

Many instrumentation applications in the modern laboratory require agile, low-noise voltage sources capable of supplying hundreds of volts or more. For example, piezo-actuated mirrors and diffraction gratings play an important role in many atomic physics experiments (used, e.g., in scanning Fabry-Peròt cavities and extended-cavity diode lasers). Avalanche photodiodes require a low-noise reverse bias of a few hundred volts or more (cite paper Alessandro/Prasoon are using?). Other applications...? biophysics? medical devices?

Often, these applications are operated in a closed feedback loop, where small voltage changes on top of a large DC voltage are necessary to stabilize the output of a particular system. For example, extended-cavity diode lasers adjust their lasing frequency by changing the angle of a piezo-actuated diffraction grating that supplies optical feedback to the diode. High-voltage piezoelectric drivers typically provide a "modulation input" for such closed-loop applications, where the input voltage is either DC coupled and gained such that the input range spans the entire output range of the driver, or AC coupled directly to the output. While this may have certain advantages, many applications would benefit from an architecture that provides a unity gain, DC-coupled feedback path to the high voltage output – such a device would make closed-loop piezoelectric systems less susceptible to noise contributions from the servo controller. Indeed, in our laboratory, we often find this to be the limiting factor in the stability of our laser frequency locks.

Traditionally, laboratory electronics capable of supplying high voltages fall under one of two architectural umbrellas: switching converters, and "linear" amplifiers. DC-DC converters are efficient and can work at very high voltages, but suffer from switching noise and limited control bandwidths. Linear-type devices are typically constructed from a high-voltage operational amplifier (op-amp), powered either from a high voltage linear regulator or more typically from a secondary switching converter. While the op-amp provides 100 dB or more of power-supply noise rejection, a high-voltage op-amp requires substantially more power than an equivalent switching circuit and is thus more cumbersome to deploy in the laboratory.

Here, we present an architecture which combines the best of both worlds: a high-voltage piezoelectric driver with excellent noise characteristics that can be powered from a standard low-current, low-voltage supply. The DC operating point is controlled digitally, and an analog input provides a DC-coupled, unity-gain feedback path ($\pm 10\,\mathrm{V}$) to the output. The following design is versatile and easy to deploy throughout the lab in a variety of high-voltage applications.

## II. CIRCUIT DESIGN

The design is based on the newly-available Texas Instruments DRV2700 piezo driver[?] , however it is easily modified to work with any galvanically isolated DC-DC converter. This single-chip integrated circuit (IC) can be operated as a boost converter to drive an on-chip differential amplifier up to 100 V, or as a flyback converter up to 1 kV. In flyback configuration, the internal-boost switch of the DRV2700 drives a step-up transformer. When the switch closes, current begins to flow through the primary coil of the transformer and induces a corresponding voltage across the secondary coil. In this state, the output diode is reverse-biased, and the capacitor ($C_{HV}$ in Fig. 1) holds its charge. When the switch opens, the voltage across the secondary coil is inverted, putting the diode into conduction and charging the capacitor. By changing the rate at which the switch is engaged, the DRV2700 is able to regulate a particular voltage at the output.

In isolation, the DRV2700 is not suited for low-noise laboratory instrumentation. The output ripple, even after heavy filtering, can be as high as a few volts, and standard filtering techniques to reduce this noise simultaneously reduce the modulation bandwidth of the flyback regulator. Even if this were not the case, it remains unlikely that the RMS noise could be brought below 1 mV, which is the operating regime we require for certain low-noise applications in the laboratory. Despite this draw-

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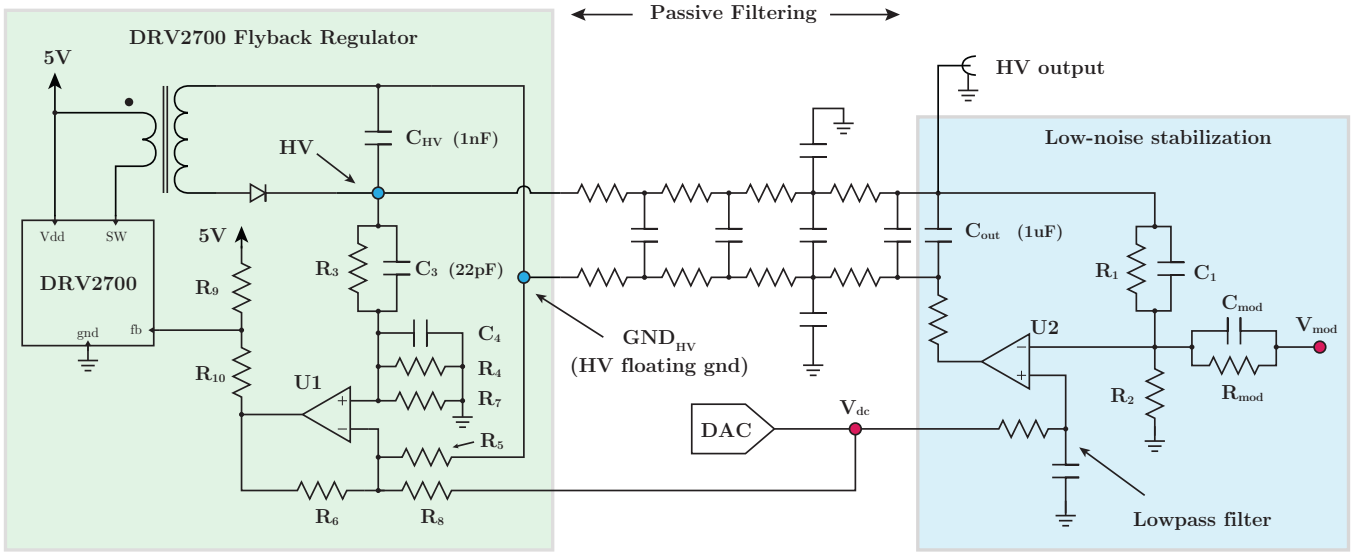


FIG. 1. Schematic of the high voltage stabilization. The voltage HV is generated using a Texas Instruments DRV2700 high voltage driver in flyback configuration (see Fig. **??**). A fast, very high slew-rate op-amp senses the output voltage across $R_1$ and $R_2$, and servos it by modulating the node at "HV floating gnd". The $V_{\rm DC}$ gain is set by $(1 + R_1/R_2)$, while the modulation gain is set by $-R_{\rm mod}/R_1$. The capacitor linking the floating ground node to the output allows the op-amp to remove residual switching noise and stabilize the DC output according to the transfer function given in Eq. (**??**). – Add back in second set of shunt caps!

back, the flyback converter requires very little current to operate and leverages a compact IC to generate high voltages without the need of an auxiliary supply.

The architecture presented in this paper uses an active feedback element (U2, described in Sec. II B) to remove switching noise and residual ripple at the high-voltage output of the flyback regulator. Additionally, U2 provides a DC-coupled, unity-gain feedback path to the high voltage node, which can be used for closed-loop servo applications and high-bandwidth modulation. This design shows how researchers might leverage the versatility of galvanically isolated switching regulators (such as the DRV2700) in a low-noise laboratory environment. [versatile and easy to deploy in the lab.]

In the next few sections, we provide details on each sub-block of the circuit and draw attention to important design details. The full schematic, including Gerbers, bill of materials, and layout design files, can be found on GitHub[?] .

### A. DRV2700 flyback regulator

We based the flyback regulator design off the suggested schematic in the DRV2700 datasheet and evaluation module application note. At a basic level, the DRV2700 flyback circuit requires a transformer (ATB3225; 1:10 step-up winding, 7 µH inductance, rated for 0.6 A) connected to an output diode and capacitor, and a "sense" voltage supplied to the feedback (FB) node of the IC. Internally, the DRV2700 boost controller tries to drive the FB node to 1.3 V. The op-amp U1 senses the voltage at node HV and $\rm GND_{HV}$, and adjusts its output such that

$$\rm HV = G \cdot V_{dc} + GND_{HV}\,, \tag{1}$$

where the gain $G$ is set by the resistor ratio $R_3/R_4 \equiv R_5/R_6$. The capacitors $C_3$ and $C_4$ are chosen such that $C_3 = 22\,\rm pF$ and

$$\frac{C_4}{C_3} = \frac{R_3}{R_4 \,||\, R_5}\,, \tag{2}$$

as suggested by the datasheet. This pseudo-differential configuration ensures that, in the equilibrium given by Eq. (1), the output of U1 is driven to 0 V; the resistive divider $R_9$ and $R_{10}$ is then chosen such that $R_9/(R_9 \,||\, R_{10}) = 1.3\,\rm V/5\,V \approx 0.26$.

The galvanically isolated output of the flyback regulator is passed through a four-pole, low-pass RC filter (corner frequency $f_c \approx 3\,\rm kHz$). Additional capacitors on both the HV and $\rm GND_{HV}$ resistor networks shunt high frequency noise to ground. The DRV2700 IC, combined with the feedback provided by U1, regulates the voltage difference $(\rm HV - GND_{HV}) = G \cdot V_{dc}$. The gain $G = 50$ for the design implemented in our lab, allowing a 5 V DAC to span 0 V – 250 V.

Careful attention was paid to the layout...

Notes here about expected, measured bandwidth??

### B. Low-noise stabilization

The low-noise stabilization circuit is crucial to the performance of the design, as it is responsible for removing noise at the output of the flyback converter. To accomplish this task, a high slew-rate op-amp (Texas Instruments LM7171, $4100\,\mathrm{V\,\mu s^{-1}}$) drives the galvanically isolated ground node of the flyback converter (see U2 in Fig. 1). This op-amp enforces the HV output voltage

$$\mathrm{V_{HV}} = \left(1 + \frac{R_1}{R_2 \,||\, R_{\mathrm{mod}}}\right)\mathrm{V_{DC}} - \left(\frac{R_{\mathrm{mod}}}{R_1}\right)\mathrm{V_{mod}} \quad (3)$$

We choose $R_1, R_{\mathrm{mod}} = 1\,\mathrm{M\Omega}$, $R_2 = 20.5\,\mathrm{k\Omega}$ such that the DC gain is $\approx 50$ and the modulation gain is unity. Depending on the application, however, other gain configurations would work equally well provided the non-inverting gain of U2 closely matches the gain of the flyback regulator since they derive from the same control voltage. Ultimately, the op-amp U2 sets the operating voltage of the output, while the flyback converter regulates the high voltage difference between $\mathrm{GND_{HV}}$ and the output. Because the output of the flyback regulator is galvanically isolated, U2 is free to control the $\mathrm{GND_{HV}}$ node at "low" voltages, which are transferred directly to the high voltage output.

The choice of component for resistors $R_1$ and $R_2$ is crucial for the low-noise performance of the system, because this resistive divider is responsible for accurately sensing the high voltage output and noise contributions thus appear directly at the output. Resistors are fundamentally limited by Johnson noise, in which thermal fluctuations contribute to a white noise power spectrum given by $\sqrt{k_B T R}$. However, resistors also exhibit $1/f$ current noise caused by equilibrium fluctuations of the resistance[? ?] . The magnitude of this "excess noise" is highly dependent on the resistor composition, and varies from manufacturer to manufacturer. Reference[?] characterized $1/f$ noise in a variety of resistors, and found that the Vishay TNPW 0.1 %-series resistors showed a noise spectrum almost consistent with Johnson noise down to 1 Hz. A previous iteration of this design used Panasonic ERJ-8ENF resistors (1206, 1 %), and we noticed substantial low-frequency noise correlated with varying strain on the PCB. This is consistent with the findings in[?] , which showed this Panasonic series to exhibit voltage noise two orders of magnitude larger than the TNPW series at 1 Hz.

For a detailed noise analysis, see Sec. II D.

### C. Digital control and auxiliary design features

The DC setpoint is controlled by a low-noise digital-to-analog (DAC) converter. This has several advantages: digital control enhances repeatability, and makes it easy to interface with a wide variety of control electronics to, eg, implement a slow infinite integrator [expand on this?]. A wide array of high-resolution DACs are available with very good noise characteristics. We initially chose to use an AD5563R, but found that our performance was ultimately limited by $1/f$ noise in the DAC itself. The final design uses an XXX, with XXX external reference, such that the noise contribution from the DAC is comparable to the noise contribution from the LM7171 (see Sec. II D).

The DAC is controlled by an integrated microcontroller, which also interfaces with the frontpanel control switches, encoders, and LCD display. The microcontroller is also attached via the backplane [talk about eurocard rack somewhere?] to a secondary microcontroller which can be addressed over TCP/IP. This vastly expands the conceivable control scenarios; for example, in our lab we implement a slow-feedback lock of two ECDL repumping lasers to a wavemeter. LabView code on the computer attached to the wavemeter computes an error signal and corrective control voltage, which can then be passed over our internal network to the piezo driver to correct for frequency drift in the laser. Other similar schemes are possible, enabling complete remote control of the laser electronics.

Control via the frontpanel is provided by a rotary encoder/push button, and a single on/off switch. The rotary encoder/push button switch allows interaction with a user-definable menu system. For example, this allows the user to quickly switch the piezo driver into "ramp" mode to scan a laser over some resonance feature.

In addition to the digital setpoint control, a voltage proportional to the high voltage output is connected to a GPIO line on the backplane. This is fed to a low-noise current controller (based on the design in **??**) to implement feed-forward (cite?). An optional analog voltage from the backplane can also be summed with the modulation voltage supplied via BNC on the front panel to generate $V_{\mathrm{mod}}$. This may be useful, eg, with servo controllers that reside in the same rack as the other control electronics.

Finally, the high voltage output is interlocked with a signal on the back plane (which can optionally be overridden by placing a jumper onboard); this allows easy integration into existing laboratory interlock schemes.

### D. Noise Analysis

We analyze the noise performance of the circuit according to the model shown in Figure 2, where noise spectral densities are calculated at the node HV. Here, we consider contributions from the intrinsic op-amp noise, the DAC (injected at the node $V_{\mathrm{DC}}$), Johnson-Nyquist noise of the passive components, and any additional noise injected at the modulation input node $V_{\mathrm{mod}}$. We also discuss, given our choice of op-amp, the noise rejection ratio from the DRV2700 flyback regulator.

First, the noise gain ($NG$) for this amplifier configura-

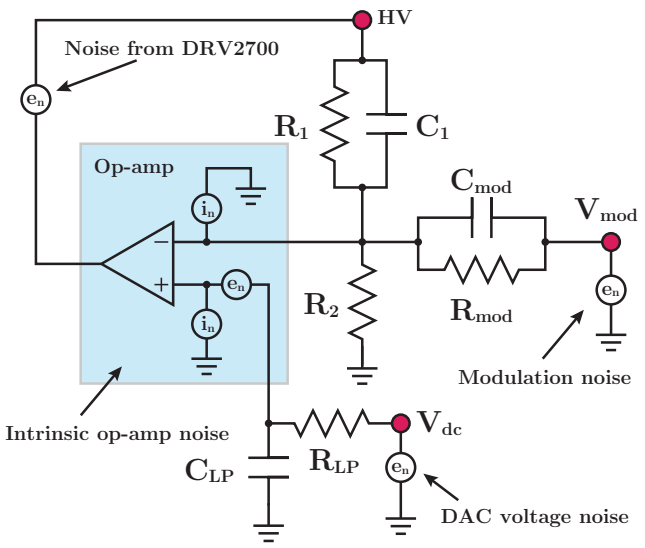


FIG. 2. Noise model.

tion is given by

$$NG(s) = 1 + \frac{Z_1}{R_2 \,||\, Z_{\rm mod}} \tag{4}$$

where we've defined the equivalent impedances $Z_1 = R_1/(1 + R_1 C_1 s)$ and $Z_{\rm mod} = R_{\rm mod}/(1 + R_{\rm mod} C_{\rm mod} s)$, and $s = i\omega$ is the frequency in the Laplace domain. By design, we've chosen $Z_1 \equiv Z_{\rm mod}$ such that the signal gain from the node $V_{\rm mod}$ is unity. This reduces Eq. (4) to

$$NG(s) = 2 + \frac{Z_1}{R_2} \tag{5}$$

The op-amp noise is parametrized by two noise contributions – $e_n$, the input voltage noise power spectral density (PSD), and $i_n$, the input current noise PSD. For the LM7171, $e_n = 14\,\mathrm{nV}/\sqrt{\mathrm{Hz}}$ and $i_n = 1.5\,\mathrm{pA}/\sqrt{\mathrm{Hz}}$ at 10 kHz. The voltage noise is summed in at the non-inverting input, while the current noise is present at both inputs. To convert $i_n$ to an equivalent voltage noise $e_n$, we multiply by the impedances $Z_n$, $Z_p$ seen by the inverting and non-inverting nodes, respectively. These are calculated as

$$\begin{aligned} Z_n &= Z_1 \,||\, Z_{\rm mod} \,||\, R_2 = \frac{Z_1}{2} \,||\, R_2 \\ Z_p &= R_{\rm LP} \Big|\Big| \frac{1}{s\, C_{\rm LP}} \end{aligned} \tag{6}$$

The total noise contribution of the op-amp (referenced to the output) is

$$e_{n,\text{op-amp}} = NG(s)\sqrt{e_n^2 + (Z_n i_n)^2 + (Z_p i_n)^2} \tag{7}$$

We now calculate the noise contribution of the DAC.

TABLE I. Various noise contributions. – should we just tabulate RMS?

| Noise source | Voltage PSD ($\mathrm{nV}/\sqrt{\mathrm{Hz}}$) | |
|---|---|---|
| | (input-referred) | (output-referred) |
| $e_n$ (op-amp) | 14 (white); 30 $(1/f)$ | |
| $i_n$ (op-amp) | | |
| DAC | | |
| Johnson-Nyquist | | |
| **total** | | |

The noise signal gain from the node $V_{\rm DC}$ is given by

$$\begin{aligned} G_{\rm DC} &= \left(\frac{1}{1 + sR_{\rm LP}C_{\rm LP}}\right)\left(1 + \frac{Z_1}{R_2 \,||\, Z_{\rm mod}}\right) \\ &= \left(\frac{1}{1 + sR_{\rm LP}C_{\rm LP}}\right) NG(s) \end{aligned} \tag{8}$$

Thus, the DAC voltage noise contribution is just $e_{n,\rm DAC} = G_{\rm DC} v_{n,\rm DAC}$. The AD5663 has a white noise floor of $100\,\mathrm{nV}/\sqrt{\mathrm{Hz}}$ (1 kHz corner frequency). For our circuit, this is the dominant noise contribution. Each noise source is shown and tabulated in Table I.

## III. RESULTS

Noise analysis, bandwidth, (DC) stability, etc.

We characterized the performance of the high-voltage piezo driver with a few different metrics. In Fig. XX, you can see the noise power spectral density. This trace was taken on an SRSXXX spectrum analyzer, AC coupled to the high-voltage output with a 0.5 Hz high-pass filter circuit shown in Fig. XX(b).

- $1/f \rightarrow$ white noise corner frequency
- white noise spectral density
- RMS noise (0.1 - 10 Hz; 10 Hz - 10 kHz, or something similar) – use SRS voltage preamp?
- How effective is the LM7171 at reducing switching noise? look at FFT power before final filter resistor, and at output of op amp (dBc spec)
- compare noise to predicted values
- longterm trace on kiethly – across voltage divider at output? Monitor vs temperature? – need to find low Tc resistors, at least.
- see what dependence is on power source – eg, JQI power supply vs lab supply vs very quiet voltage regulator?
- current draw – display in some "bottom line" specs table?

- bandwidth measurements – full scale triangle ramp, small signal bandwidth – discuss limitations on this (eg, also versus different piezo loads)
- Lock a laser, show RMS noise fluct vs. old piezo?

## IV. CONCLUSION