

An ultra-low noise, high-voltage piezo driver

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We present an ultra-low noise, high voltage driver suited for use with piezoelectric actuators and other low-current applications. The architecture uses a flyback switching regulator to generate up to 250V in our current design, with an output of 1kV or more possible with small modifications. A high slew-rate op-amp suppresses the switching noise by XX dB (MEASURE), yielding a total RMS noise of $\approx 100 \mu\text{V}$ (1 Hz–100 kHz). A low-voltage ($\pm 10 \text{ V}$), high bandwidth signal can be summed directly onto the output, making the driver well-suited for closed-loop feedback applications. Digital control enables repeatable setpoints or sophisticated control logic, and the circuit consumes less than 150 mA at $\pm 15 \text{ V}$.

I. INTRODUCTION

Many instrumentation applications in the modern laboratory require agile, low-noise voltage sources capable of supplying hundreds of volts or more. For example, piezo-actuated mirrors and diffraction gratings play an important role in atomic physics experiments (used, e.g., in Fabry-Perot cavities^{1,2} and extended-cavity diode lasers³), while avalanche photodiodes and photomultiplier tubes require large bias voltages for proper operation. In the realm of biophysics, electrokinetic separation methods such as free-flow or capillary electrophoresis⁴ require large electric field gradients, and the recent push to develop lab-on-a-chip devices could benefit from miniaturized high voltage sources⁵.

Laboratory devices are often operated in a closed feedback loop, where small voltage changes on top of a large DC voltage are necessary to stabilize the output of a particular system. For example, the frequency of an extended-cavity diode laser can be locked by feeding back to a piezo-actuated diffraction grating or mirror, which in turn supplies optical feedback to the diode. Commercially available piezoelectric drivers typically provide a modulation input for such closed-loop applications, but the input voltage is gained such that it spans the entire output range of the device. While this has certain advantages, many applications would benefit from an architecture that provides a unity gain, DC-coupled feedback path to the high voltage output. Such a device could make closed-loop systems less susceptible to noise contributions from the servo controller, which we often find in our laboratory to be the limiting factor in laser lock stability.

Instrumentation electronics capable of supplying high voltages traditionally fall under one of two architectural umbrellas: DC-DC switching converters, and linear-type amplifiers. While DC-DC converters are efficient and can work at very high voltages, they suffer from switching noise and limited control bandwidths. Linear-type devices are typically constructed from a high-voltage operational amplifier (op-amp), powered either from a high

voltage linear regulator or more typically from a secondary switching converter. While the op-amp provides 100 dB or more of power-supply noise rejection, high-voltage op-amps require substantially more power than an equivalent switching circuit and are more cumbersome to deploy in the laboratory.

We present a circuit with a hybrid architecture. The high voltage is generated by a galvanically isolated DC-DC converter (described in Sec. II A), while a low-noise, high slew-rate op-amp removes noise at the output (see Sec. II B). The op-amp additionally provides a low-gain, high-bandwidth modulation input for closed-loop feedback applications. This architecture is able to achieve extremely low noise performance ($\approx 100 \mu\text{V}_{\text{RMS}}$) over the entire output range, draws very little current, and fits comfortably onto a small-footprint PCB. Complete design files, including the schematic, bill of materials, and board layout, can be found on Github⁶. The board manufacture and component cost is less than \$200, making it a cost-effective alternative to commercial options.

II. CIRCUIT DESIGN

The design principles discussed below show how we leverage the versatility of galvanically isolated switching regulators in a low-noise laboratory environment. Our design targets a 250 V output, but straightforward modifications to the schematic make it possible to tailor the gain and output range to a specific application. The entire electronics package fits comfortably into a 12HP eurocard rack module (with the high voltage section taking only a fraction of the PCB), and draws less than 150 mA at 15 V.

Figure 1 shows the schematic overview. A digital-to-analog converter (DAC) generates a voltage setpoint, which is sent to the high-voltage flyback regulator and to the low-noise stabilization circuit. The flyback regulator (Sec. II A) controls the potential between circuit nodes V_{HV} and V_{FG} , while the low-noise stabilization circuitry (Sec. II B) serves the output node V_{out} relative to the true circuit ground. The DAC is controlled by an integrated microcontroller, and can be programmed to output slow ($\approx 10 \text{ Hz}$) rail-to-rail voltage ramps in ad-

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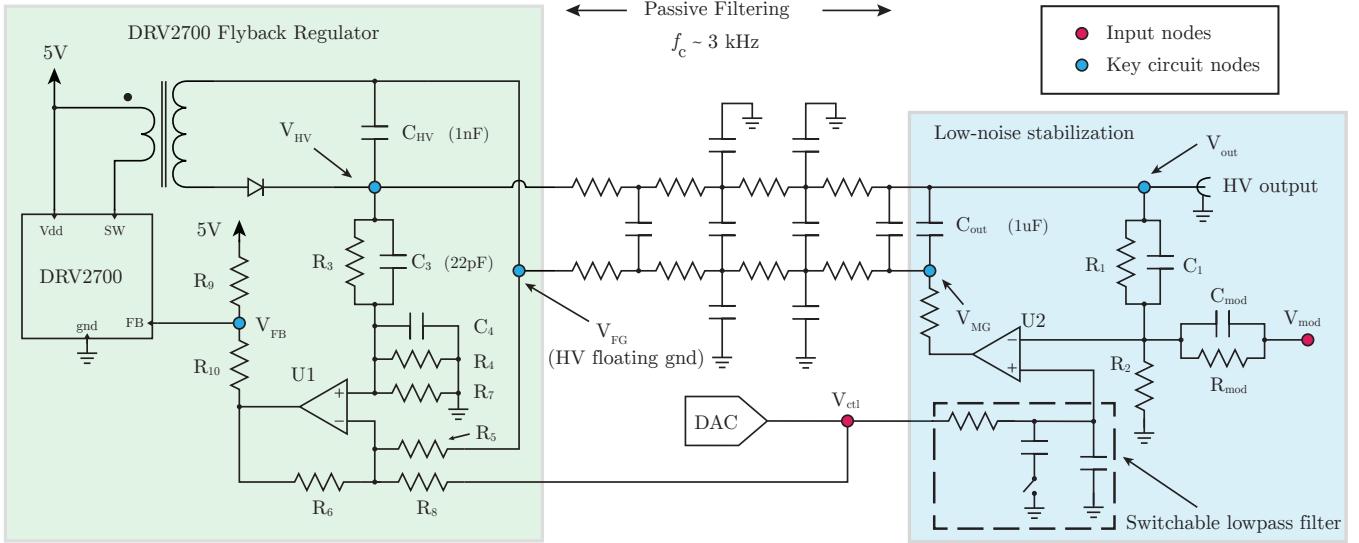


FIG. 1. Schematic of the high voltage supply and stabilization. The voltage HV is generated using a Texas Instruments DRV2700 high voltage driver in flyback configuration. A high slew-rate op-amp senses the output voltage across R_1 and R_2 , and servos it by modulating the node at “HV floating gnd”. The DC control signal for this op-amp, V_{ctl} , is supplied by a digital-to-analog (DAC) converter, which is passed through a switchable low-pass filter. This allows for very heavy filtering of the DAC $1/f$ noise during steady-state operation, but the corner frequency can be increased if the output needs to be scanned more quickly. The V_{ctl} gain is set by $(1 + R_1/R_2)$, while the modulation gain is set by $-R_{mod}/R_1$. The capacitor linking the floating ground node to the output allows the op-amp to remove residual switching noise and stabilize the DC output according to the transfer function given in Eq. (3). Op-amps U1 and U2 are powered at ± 15 V (not shown).

dition to setting the DC operating point. Because $1/f$ voltage noise in the DAC contributes heavily to the output noise, a low-pass filter can be engaged during DC operation to mitigate this effect (see Sec. III). To improve the large-voltage slew rate, a MOSFET “quench” circuit is included to shorten the RC time constant of the high voltage node V_{HV} when needed (Figure 2, described in Sec. II C). Fast output modulation over ± 10 V can be achieved through the input node V_{mod} . This node is DC-coupled to the high voltage output, and is useful for closed-loop feedback control. The bandwidth under various loads is shown in Figure 7.

A. Flyback regulator

The high voltage DC-DC converter used here is based on the Texas Instruments DRV2700 piezo driver⁷. This single-chip integrated circuit (IC) can be operated as a boost converter to drive an on-chip differential amplifier up to 100 V, or as a flyback converter up to 1 kV or more. In flyback configuration, the internal-boost switch of the DRV2700 (pin SW in Fig. 1) drives a step-up transformer. When the switch closes, current begins to flow through the primary coil of the transformer and induces a corresponding voltage across the secondary coil. In this state, the output diode is reverse-biased, and the capacitor (C_{HV} in Fig. 1) holds its charge. When the switch opens, the voltage across the secondary coil is in-

verted, putting the diode into conduction and charging the capacitor. By changing the switching duty cycle, the DRV2700 is able to regulate the voltage across the galvanically isolated output (nodes V_{FG} and V_{HV} in Fig. 1).

The DRV2700 implements output voltage control by comparing the feedback input pin at node V_{FB} with an internal 1.3 V reference. The resistors R_9 and R_{10} are chosen such that pin FB is at 1.3 V when the output of U1 is at ground: $R_{10}/(R_9 + R_{10}) = 1.3\text{ V}/5\text{ V} \approx 0.26$. The op-amp U1 subtracts V_{FG} and $G \cdot V_{ctl}$ from the voltage at node V_{HV} , ensuring the DRV2700 regulates the output voltage such that

$$V_{HV} - V_{FG} = G \cdot V_{ctl}, \quad (1)$$

where the gain G is set by the resistor ratio $R_3/R_4 \equiv R_5/R_6$, and V_{ctl} is the control voltage set by the DAC. The capacitors C_3 and C_4 are chosen such that $C_3 = 22\text{ pF}$ and

$$\frac{C_4}{C_3} = \frac{R_3}{R_4 \parallel R_7}, \quad (2)$$

as suggested by the DRV2700 datasheet⁸, where $R_6 = R_7 = R_8$, and $R_i \parallel R_j \equiv R_i R_j / (R_i + R_j)$. In our lab, we implement a gain $G \approx 50$ ($R_3 = R_5 = 499\text{ k}\Omega$; $R_4 = R_{6,7,8} = 10\text{ k}\Omega$), allowing a 5 V control signal V_{ctl} to span 250 V at the output. A different DAC and/or a different gain factor could be chosen to adjust the maximum output voltage⁹. The transformer (ATB3225, 1:10

step-up winding), diode, and RC feedback network are all based on values suggested in the DRV2700 datasheet^{8,10}.

The output of the flyback regulator is passed through a four-pole, low-pass RC filter. The corner frequency $f_c \approx 3\text{ kHz}$ is chosen to be high enough that a slow ($\approx 10\text{ Hz}$) rail-to-rail triangle ramp can be applied by the DAC at V_{ctl} (for, e.g., sweeping over a spectroscopy resonance), but low enough that the $\approx 100\text{ kHz}$ switching noise is substantially attenuated. Additional capacitors on both the V_{HV} and V_{FG} resistor networks shunt high frequency noise to ground. This filter topology, modeled on a lossy transmission line, is sufficient for our application, but other corner frequencies or topologies could also be used.

B. Low-noise stabilization and fast modulation

The low-noise stabilization circuit is crucial to the performance of the design, as it is responsible for removing noise at the output of the flyback converter. To accomplish this, a high slew-rate op-amp (Texas Instruments LM7171, $4100\text{ V}/\mu\text{s}$) drives the galvanically isolated ground node of the flyback converter (see U2 in Fig. 1). This op-amp enforces the HV output voltage

$$V_{\text{out}} = \left(1 + \frac{R_1}{R_2 \parallel R_{\text{mod}}}\right) V_{\text{ctl}} - \left(\frac{R_{\text{mod}}}{R_1}\right) V_{\text{mod}}. \quad (3)$$

Here, V_{mod} is the applied modulation, which can vary between $\pm 10\text{ V}$. We choose $R_1 = R_{\text{mod}} = 1\text{ M}\Omega$ and $R_2 = 20.5\text{ k}\Omega$ such that the DC gain is ≈ 50 and the modulation gain $\Delta V_{\text{out}}/\Delta V_{\text{mod}}$ is unity. Depending on the application, other gain configurations could work equally well provided the non-inverting gain of U2 closely matches the gain of the flyback regulator (since they both derive from V_{ctl}). Ultimately, the op-amp U2 sets the operating voltage of the output (referenced to true circuit ground) while the flyback converter regulates the high voltage relative to V_{FG} . Because the output of the flyback regulator is galvanically isolated, U2 is able to control V_{FG} . At low frequencies, this amounts to changing the “zero-volt” reference for the flyback regulator, while at high frequencies the capacitor C_{HV} provides a low-impedance pathway to the HV output. Thus, U2 simultaneously servos residual switching noise from the flyback converter and provides a DC-coupled, high-bandwidth modulation of the output.

The choice of component for resistors R_1 and R_2 is crucial for the low-noise performance of the system. Because this resistive divider is responsible for accurately sensing the voltage V_{out} , noise introduced by these resistors cannot be corrected by the op-amp. In general, resistors are fundamentally limited by Johnson noise, in which thermal fluctuations contribute to a white noise power spectrum given by $\sqrt{4k_B T R}$, where T is the temperature and k_B is Boltzmann’s constant¹¹. However, resistors also exhibit $1/f$ current noise caused by equilibrium fluctuations of the resistance^{12,13}. This excess noise depends on the applied voltage, and therefore is an important

consideration in a high-voltage circuit. It is also highly dependent on the resistor composition and varies from manufacturer to manufacturer. Seifert, et. al.¹⁴ characterized $1/f$ noise in a variety of resistors, and found that the Vishay TNPW 0.1 %-series resistors showed a noise spectrum almost consistent with Johnson noise down to 1 Hz. Our current design uses this series in a 1206 package, but we noticed substantial low-frequency noise correlated with varying strain on the PCB, potentially due to the relatively large footprint of this package. Future boards will instead use three TNPW 0.1 % 0603 resistors in series for both R_1 and R_2 to minimize strain-induced output noise.

The value of capacitor C_1 is a tradeoff between two competing design considerations. On the one hand, larger C_1 extends the bandwidth where the suppression of switching noise from the DRV2700 is maximal. However, large values of C_1 limit the bandwidth of V_{ctl} and increase the reverse transfer function from the load to the control, thereby limiting the directivity. We empirically settled on $C_1 = 1\text{ nF}$. This value is large enough to saturate the feedback gain in the 40 kHz – 100 kHz range where switching noise dominates, but not so large that we limit the bandwidth of V_{ctl} . Once this value was chosen, capacitor C_{mod} was calculated to match the impedances $R_1 \parallel C_1 = R_{\text{mod}} \parallel C_{\text{mod}}$. For our circuit, this means $C_{\text{mod}} = C_1$.

C. Digital control and slow modulation

The high-voltage setpoint (absent voltages summed in at V_{mod}) is controlled by a low-noise DAC. This has two advantages: digital control enhances setpoint repeatability, and makes it easy to integrate with a wide variety of computerized control electronics or implement more sophisticated servo loops. So while the modulation input V_{mod} has a limited range of $\pm 10\text{ V}$, larger voltage swings

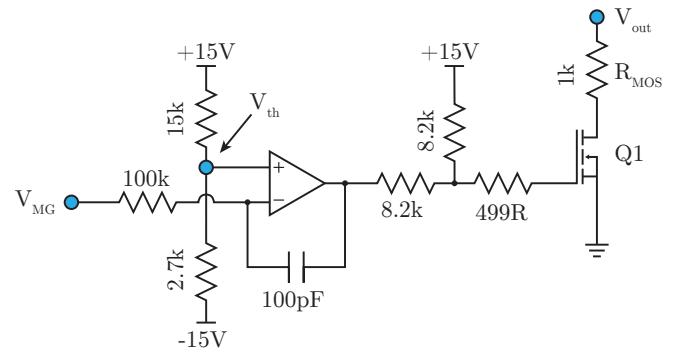


FIG. 2. MOSFET “quench” circuit. When the mid-ground node V_{MG} (see Fig. 1) goes below the threshold value set at V_{th} , the op-amp puts the HV MOSFET Q1 into conduction. Now, the time constant for capacitor C_{out} in Fig. 1 is given by $R_{\text{MOS}} C_{\text{out}}$, which for our circuit is set to 1 ms.

can be achieved by reprogramming the DAC.

One downside of the flyback regulator presented above is that while the switched transformer is very efficient at charging the capacitor C_{HV} , discharge of the high-voltage line is limited by the RC time constant of the circuit. To get around this limitation, we have added an auxiliary MOSFET “quench” circuit, as suggested in the DRV2700 datasheet, to quickly shunt V_{out} to ground (see Figure 2). This works by monitoring the voltage at V_{MG} , the mid-ground node controlled by op-amp U2. If that voltage drops below the threshold V_{th} , the comparator op-amp in Fig. 2 changes the gate voltage of the MOSFET to put it into conduction. Now, the time constant is given by $\tau \approx R_{MOS}C_{out}$. For our circuit, this is about 1 ms and the threshold $V_{th} \approx -10$ V but other values could be chosen depending on the design requirements.

D. Auxiliary design features

Here, we discuss some additional features of our circuit that are independent of the high-voltage design but make it nicer to work with in the laboratory. The on-board microcontroller responsible for setting the DAC control voltage, V_{ctl} , also interfaces with frontpanel controls including a switch, LCD, and rotary encoder with an integrated push button. The encoder/push button provide menu navigation, and the switch toggles between DC and scanning operation. However, other user interfaces can easily be designed to work with the existing hardware. Arduino-based code written in C++ defines the entire software interaction, and can be modified depending on the needs of the researcher.

The entire circuit fits into a standard Eurocard rack, which supplies power at ± 15 V. While not required, the rack provides a backplane with analog lines to communicate with other modules (e.g., to implement a current feed-forward for laser diodes, see description below). We are presently designing a backplane with a secondary microcontroller that can be addressed over TCP/IP. This vastly expands the conceivable control scenarios. For example, in our lab we implement a slow-feedback lock of two external-cavity diode lasers to a wavemeter for repumping strontium. LabView code on the computer attached to the wavemeter computes an error signal and corrective control voltage, which will be passed over our internal network to the piezo driver to correct for frequency drifts in the laser. Other similar schemes are possible, enabling complete remote control of the laser electronics.

The modulation voltage V_{mod} can be supplied either from a BNC on the frontpanel, or from the backplane. This may be useful, e.g., with servo controllers that reside in the same rack as the other control electronics. In either case, this voltage is differentially buffered to break ground loops. An output voltage monitor (sensed at the inverting node of U2 in Figure 1) is buffered and con-

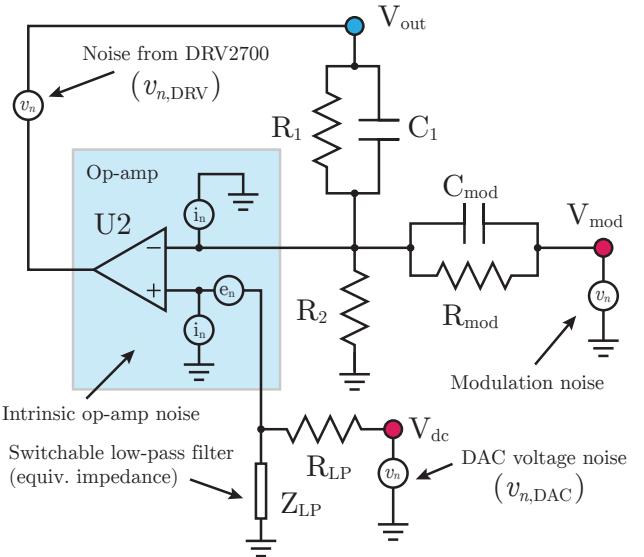


FIG. 3. Noise model (see text). The element labeled Z_{LP} is comprised of a 47 nF capacitor in parallel with a 10 μ F capacitor connected to ground through a switch, such that the corner frequency of the filter can be changed depending on the mode of operation. The on-resistance of the switch introduces a zero in the transfer function at ≈ 23 kHz, which has negligible effect on the computed RMS noise.

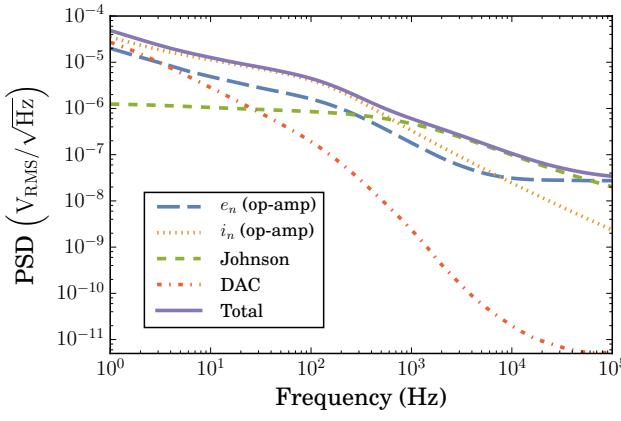
nected to a BNC on the frontpanel, a GPIO line on the backplane, and to the microcontroller. This enables the microcontroller to digitally implement an infinite integrator, driving V_{mod} to 0 V in closed-loop operation and preventing the servo controller from railing. In our lab, the GPIO voltage monitor is fed to a low-noise current controller (based on the design in¹⁵) to implement a laser diode current feed-forward. The high voltage output is interlocked with a signal on the backplane (which can optionally be bypassed by placing an onboard jumper), permitting easy integration with existing laboratory interlock schemes if desired.

For more details, see the design files and documentation on Github⁶.

III. NOISE ANALYSIS

We analyze the noise performance of the circuit according to the model shown in Fig. 3, where noise spectral densities are calculated at the node V_{out} . A summary of each noise contribution (op-amp, DAC, Johnson-Nyquist) is shown in Fig. 4, along with the cumulative root-mean-square (RMS) noise estimates in different frequency bands.

To treat the intrinsic op-amp noise contributions, we first compute the noise gain (NG) for this amplifier con-



Noise source	RMS Voltage (1 Hz – 10 Hz)	RMS Voltage (10 Hz – 100 kHz)
e_n (op-amp)	26 pV	31 pV
i_n (op-amp)	51 pV	73 pV
DAC	28 pV	8 pV
Johnson-Nyquist	3 pV	31 pV
total (calculated)	64 pV	86 pV

FIG. 4. Noise Contributions (color online). Plotted are the noise contributions from each source in our model, along with the total calculated noise. Power spectral density (PSD) is referred to the high voltage output, and the table shows the integrated RMS noise due to each noise source in different frequency bands. The total RMS noise (summed in quadrature) over the entire 1 Hz – 100 kHz range is calculated to be 107 pV.

figuration according to

$$NG(s) = 1 + Z_1 \left(\frac{1}{R_2} + \frac{1}{Z_{\text{mod}}} \right), \quad (4)$$

where we've defined the equivalent impedances $Z_1 = R_1/(1 + R_1 C_1 s)$ and $Z_{\text{mod}} = R_{\text{mod}}/(1 + R_{\text{mod}} C_{\text{mod}} s)$, and $s = i\omega$ is the frequency in the Laplace domain. By design, we've chosen $Z_1 \equiv Z_{\text{mod}}$ such that the signal gain from the node V_{mod} is unity. This reduces Eq. (4) to

$$NG(s) = 2 + \frac{Z_1}{R_2}. \quad (5)$$

The op-amp noise is parametrized by two noise contributions: e_n , the input voltage noise power spectral density (PSD), and i_n , the input current noise PSD. For the LM7171, $e_n = 14 \text{ nV}/\sqrt{\text{Hz}}$ and $i_n = 1.5 \text{ pA}/\sqrt{\text{Hz}}$ at 10 kHz, with a $1/f$ noise character below this frequency¹⁶. The voltage noise is summed in at the non-inverting input, while the current noise is present at both inputs. To convert i_n to an equivalent voltage noise e_n , we multiply by the impedances Z_n , Z_p seen by the inverting and non-inverting nodes, respectively. These are

calculated as

$$\begin{aligned} Z_n &\equiv \left(\frac{1}{Z_1} + \frac{1}{Z_{\text{mod}}} + \frac{1}{R_2} \right)^{-1} = \frac{Z_1 R_2}{2R_2 + Z_1} \\ Z_p &\equiv \left(\frac{1}{R_{\text{LP}}} + \frac{1}{Z_{\text{LP}}} \right)^{-1}. \end{aligned} \quad (6)$$

The impedance Z_{LP} is determined by the corner frequency of a switchable low-pass filter between the DAC and the non-inverting node of U2 (discussed below).

The total noise contribution of the op-amp (referenced to the output) is

$$e_{n,\text{op-amp}} = NG(s) \sqrt{e_n^2 + (Z_n i_n)^2 + (Z_p i_n)^2} \quad (7)$$

We now calculate the noise contribution of the DAC. The noise signal gain from the node V_{ctl} is given by

$$G_{\text{ctl}} = \left(\frac{Z_{\text{LP}}}{R_{\text{LP}} + Z_{\text{LP}}} \right) NG(s), \quad (8)$$

where the first term represents the contribution to the transfer function from the switchable low-pass filter. Without the addition of this low-pass filter, the voltage noise of the DAC would dominate both the low- and high-frequency noise performance of the circuit. But if we were to simply place a fixed-corner filter at this node, we would severely restrict the AC performance of V_{ctl} . Thus, the switchable low-pass filter is necessary to achieve low-noise performance during “DC” operation, while still permitting the DAC to modulate V_{ctl} more quickly when needed. In our circuit, the high-corner filter is comprised of a 20.5 kΩ resistor and 47 nF capacitor, with $f_c \approx 165 \text{ Hz}$. In “DC” mode, a secondary 10 pF capacitor in parallel with the 47 nF capacitor mentioned above can be shorted to ground through a low resistance digital switch. This changes the corner frequency to 0.8 Hz. The non-zero resistance of the digital switch contributes a zero to the transfer function at high frequencies, but has negligible effect on the performance. The DAC voltage noise contribution can now be calculated as $e_{n,\text{DAC}} = G_{\text{ctl}} v_{n,\text{DAC}}$, where $v_{n,\text{DAC}}$ is the frequency dependent output voltage noise of the DAC. In subsequent calculations, we take the “DC mode” operation for the switchable low-pass filter.

The low-noise stabilization circuit is limited in its ability to reject residual switching noise $v_{n,\text{DRV}}$ from the DRV2700 regulator by the total loop gain analyzed from node V_{out} . The LM7171 has an open-loop gain of 85 dB, with a dominant pole at $\approx 10 \text{ kHz}$. We model the open loop gain, A_{OL} , as

$$A_{\text{OL}} = \frac{10^{85/20}}{1 + s/(2\pi \cdot 10 \text{ kHz})} \quad (9)$$

Thus, noise appearing at V_{out} is attenuated by a factor

$$\frac{1}{1 + A_{\text{OL}} \left(\frac{R_2 || Z_{\text{mod}}}{Z_1 + R_2 || Z_{\text{mod}}} \right)} \quad (10)$$

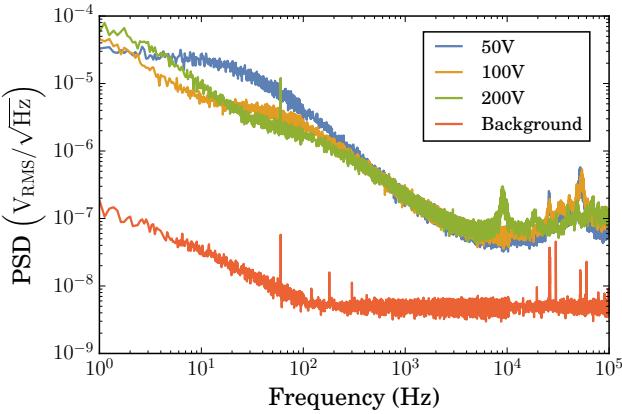


FIG. 5. Voltage power spectral density at various output voltages. The integrated RMS voltage noise (1 Hz – 100 kHz) is $\{138, 80, 101\}$ μV measured at $\{50, 100, 200\}$ V.

For $R_1 = 1\text{ M}\Omega$ and $C_1 = 1\text{ nF}$, $v_{n,\text{DRV}}$ is attenuated by as much as 76 dB at 6.3 kHz, with a rolloff of 10 dB/decade at higher frequencies. (INCLUDE DRV NOISE MODEL IN CALCULATION??)

Given the noise model discussed above, our circuit is dominated by Johnson noise at intermediate to high frequencies, and the op-amp's intrinsic current noise at lower frequencies. Both of these contributions could be suppressed by using lower resistances R_1, R_{mod} , however one must be careful about power and current limitations when dealing with such high voltages. Each noise source is tabulated and plotted in Fig. 4, and the total voltage noise is calculated to be 107 μV (1 Hz – 100 kHz).

IV. RESULTS

In this section, we show the measured performance of the high-voltage piezo driver. In Fig. 5, we plot the noise power spectral density measured at several different output voltages. These traces were taken on a Stanford Research Systems SR780 spectrum analyzer, with the piezo output coupled through a 0.5 Hz high-pass filter. At 100 V, the integrated noise (1 Hz – 100 kHz) was measured to be 80 μV_{RMS} (138 μV_{RMS} , 101 μV_{RMS} for 50 V, 200 V outputs). This matches well with the expected total RMS noise calculated in Section III.

Figure 6 shows the performance at both short- and long-time scales. At long times, voltage fluctuations on the order of a few mV can be observed. This is due generically to $1/f$ noise, but also correlates with the external temperature. A cross-correlation between measured temperature and output voltage (trace not shown) yields an effective temperature coefficient of $-24\text{ ppm}/^\circ\text{C}$ at 100 V. The short-term trace was taken on a PicoScope 5442B (ac-coupled, 100 V output). Points are colored based on their normally distributed statistical probability, and thus give a visual estimation of the RMS width.

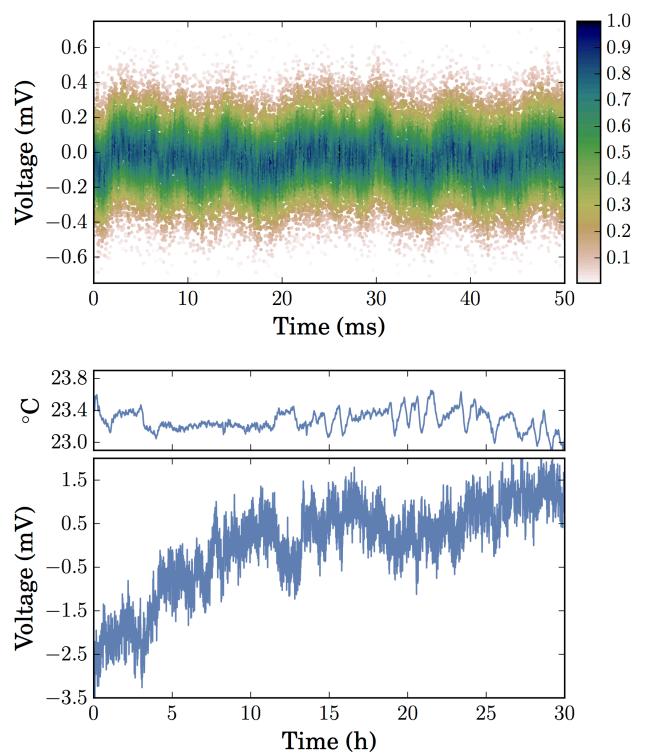


FIG. 6. Time-domain traces of the high voltage output (100 V). Top: short-time scatterplot (AC coupled). Points are colored based on the Gaussian spread in acquired voltages, thus indicating the RMS width of the trace. Bottom: long-term trace, measured on a Keithly 2010 digital multimeter. A 100 V DC offset is subtracted from the plotted values. The top trace shows the lab temperature during the same time period.

Figure 7 shows the measured frequency response under different load conditions. The unloaded bandwidth is as high as a few megahertz, while a 1 μF capacitive load can still be driven at ≈ 100 kHz. Several mechanical resonances can be seen with a 700 nF piezoelectric load, as expected. In a laboratory setting, these resonances can be mitigated by using a digital feedback controller with notch filters tuned to match the exact resonance frequencies observed in the system¹⁷, thereby extending the usable bandwidth out to ≈ 100 kHz.

V. CONCLUSION

We have designed, built, and characterized a high-voltage piezoelectric driver optimized for use in a modern atomic physics laboratory. It is based on a flyback configuration switching regulator, but is able to achieve very low noise performance by active stabilization from a

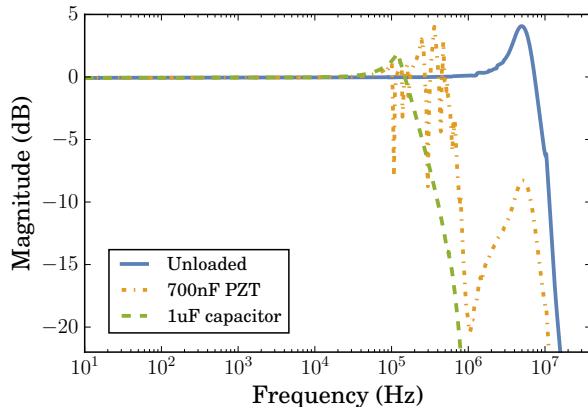


FIG. 7. Modulation input transfer function (color online). The blue line indicates the unloaded frequency response, while the dash-dotted orange trace shows the response with a Thorlabs piezoelectric actuator (PN AE0505D08F). Mechanical resonances above ≈ 50 kHz are clearly visible. The dashed green trace shows the response under a $1\ \mu\text{F}$ purely capacitive load. Loaded response bandwidth is ≈ 100 kHz, while the unloaded bandwidth is ≈ 1 MHz.

high slew-rate op-amp. This hybrid architecture makes it small and easy to deploy in a variety of situations, without requiring an external, bulky high-voltage power supply. The design principles discussed here can be adapted to fit the exact application, and all design files are freely available on GitHub for others to use and modify.

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