

An ultra-low noise, high-voltage piezo driver

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We present an ultra-low noise, high voltage driver suited for use with piezoelectric actuators and other low-current applications. The architecture leverages a commercially available, small-form-factor integrated circuit (IC) for generating high voltage outputs. The IC uses a flyback configuration switching regulator to generate up to 250V in our design (but up to 1kV or more with small modification), and a high slew-rate op-amp capacitively coupled to the output compensates for the switching noise. A low-voltage (± 10 V), high bandwidth modulation input is capable of summing small voltage corrections onto the output, making the driver well suited for use in closed-loop feedback applications.

I. INTRODUCTION

Many instrumentation applications in the modern laboratory require agile, low-noise voltage sources capable of supplying hundreds of volts or more. For example, piezo-actuated mirrors and diffraction gratings play an important role in atomic physics experiments (used, e.g., in scanning Fabry-Perot cavities and extended-cavity diode lasers), while avalanche photodiodes and photomultiplier tubes require large bias voltages for proper operation. In the realm of biophysics, electrokinetic separation methods such as free-flow or capillary electrophoresis require large electric field gradients, and the recent push to develop lab-on-a-chip devices could benefit from miniaturized high voltage sources¹. (ion traps? charge multiplier tubes?)

Often, laboratory devices are operated in a closed feedback loop, where small voltage changes on top of a large DC voltage are necessary to stabilize the output of a particular system. For example, extended-cavity diode lasers can adjust their lasing frequency by changing the angle of a piezo-actuated diffraction grating that supplies optical feedback to the diode. Commercially available piezoelectric drivers typically provide a modulation input for such closed-loop applications, but the input voltage is either AC coupled to the output or gained such that it spans the entire voltage range of the device. While this has certain advantages, many applications would benefit from an architecture that provides a unity gain, DC-coupled feedback path to the high voltage output. Such a device could make closed-loop systems less susceptible to noise contributions from the servo controller, which we often find in our laboratory to be the limiting factor in laser lock stability.

Traditionally, instrumentation electronics capable of supplying high voltages fall under one of two architectural umbrellas: DC-DC switching converters, and linear-type amplifiers. While DC-DC converters are efficient and can work at very high voltages, they suffer from switching noise and limited control bandwidths. Linear-type devices are typically constructed from a high-voltage

operational amplifier (op-amp), powered either from a high voltage linear regulator or more typically from a secondary switching converter. While the op-amp provides 100 dB or more of power-supply noise rejection, high-voltage op-amps require substantially more power than an equivalent switching circuit and are more cumbersome to deploy in the laboratory.

Here, we present a hybrid architecture: the high voltage is generated by a galvanically isolated DC-DC converter (described in Sec. II A), while a low-noise, high slew-rate op-amp removes noise at the output by modulating the OUT- node of the switching converter (see Sec. II B). The op-amp additionally provides a low-gain, high-bandwidth modulation input for closed-loop feedback applications. This architecture is able to achieve extremely low noise performance, draws very little current, and fits comfortably onto a small-footprint PCB. Complete design files, including the schematic, bill of materials, and board layout, can be found on Github.²

II. CIRCUIT DESIGN

The design principles discussed below show how researchers might leverage the versatility of galvanically isolated switching regulators in a low-noise laboratory environment. Our design targets a 250 V output, but straightforward modifications to the schematic make it possible to tailor the gain and output range to a specific application. The entire electronics package fits comfortably into a 12HP eurocard rack module (with the high voltage section taking only a fraction of the PCB), and draws less than 150 mA at 15 V.

A. Flyback regulator

The high voltage DC-DC converter used here is based on the Texas Instruments DRV2700 piezo driver³. This single-chip integrated circuit (IC) can be operated as a boost converter to drive an on-chip differential amplifier up to 100 V, or as a flyback converter up to 1 kV or more. In flyback configuration, the internal-boost switch of the DRV2700 drives a step-up transformer. When the switch

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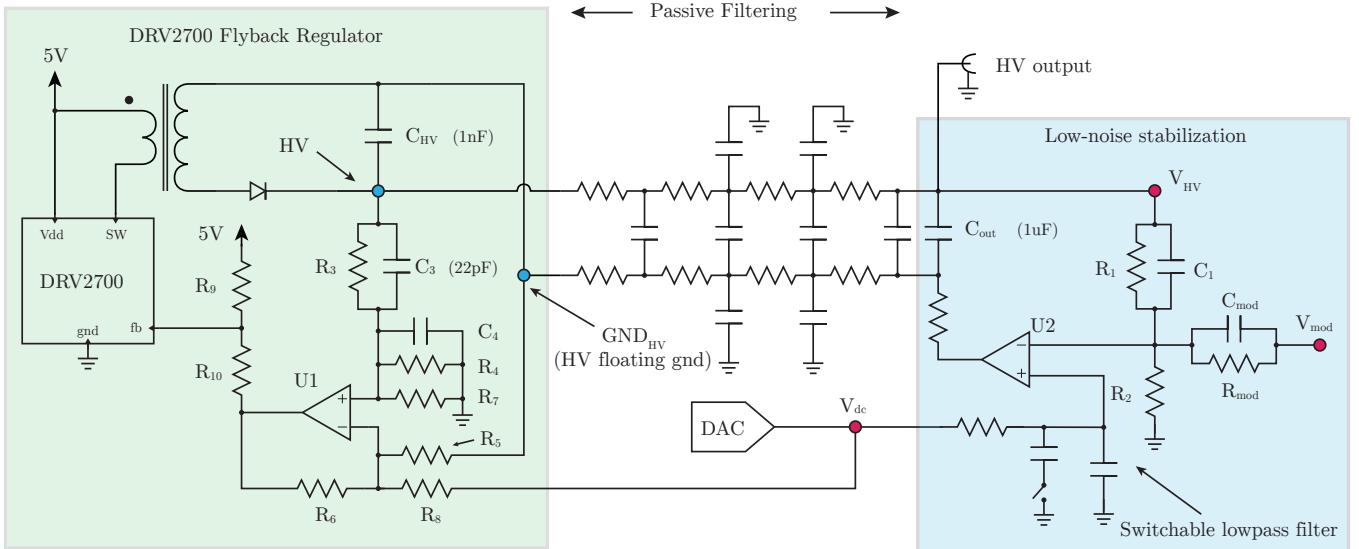


FIG. 1. Schematic of the high voltage stabilization. The voltage HV is generated using a Texas Instruments DRV2700 high voltage driver in flyback configuration. A fast, very high slew-rate op-amp senses the output voltage across R_1 and R_2 , and servos it by modulating the node at “HV floating gnd”. The DC control signal for this op-amp is supplied by a digital-to-analog (DAC) converter, which is passed through a switchable low-pass filter. This allows for very heavy filtering of the DAC 1/f noise during steady-state operation, but the corner frequency can be increased if the output needs to be scanned more quickly. The V_{DC} gain is set by $(1 + R_1/R_2)$, while the modulation gain is set by $-R_{mod}/R_1$. The capacitor linking the floating ground node to the output allows the op-amp to remove residual switching noise and stabilize the DC output according to the transfer function given in Eq. (3).

closes, current begins to flow through the primary coil of the transformer and induces a corresponding voltage across the secondary coil. In this state, the output diode is reverse-biased, and the capacitor (C_{HV} in Fig. 1) holds its charge. When the switch opens, the voltage across the secondary coil is inverted, putting the diode into conduction and charging the capacitor. By changing the rate at which the switch is engaged, the DRV2700 is able to regulate a particular voltage across the galvanically isolated output (nodes GND_{HV} and HV in Fig. 1).

The transformer (ATB3225, 1:10 step-up winding), diode, and RC feedback network are based on values suggested in the DRV2700 datasheet^{4,5}. Internally, the DRV2700 boost controller tries to drive the FB node to 1.3 V. The op-amp U1 senses the voltage at nodes HV and GND_{HV} , and adjusts its output such that

$$HV - GND_{HV} = G \cdot V_{dc}, \quad (1)$$

where the gain G is set by the resistor ratio $R_3/R_4 \equiv R_5/R_6$. This pseudo-differential feedback configuration ensures that, in the equilibrium given by Eq. (1), the output of U1 is driven to 0 V; the resistive divider R_9 and R_{10} is then chosen such that $R_{10}/(R_9 \parallel R_{10}) = 1.3\text{V}/5\text{V} \approx 0.26$. The capacitors C_3 and C_4 are chosen such that $C_3 = 22\text{pF}$ and

$$\frac{C_4}{C_3} = \frac{R_3}{R_4 \parallel R_7} \quad (2)$$

as suggested by the datasheet, and $R_6 = R_7 = R_8$. In our lab, we implement a gain $G \approx 50$ ($R_3 = R_5 = 499\text{k}\Omega$; $R_4 = R_{6-8} = 10\text{k}\Omega$) such that a 5 V digital-to-analog converter (DAC) controlling the node V_{DC} can span 250 V at the output.

The output of the flyback regulator is passed through a four-pole, low-pass RC filter. The corner frequency $f_c \approx 3\text{kHz}$ is chosen to be high enough that a slow ($\approx 10\text{Hz}$) rail-to-rail triangle ramp can be applied by the DAC at V_{DC} (for, e.g., sweeping over a spectroscopy resonance), but low enough that the $\approx 100\text{kHz}$ switching noise is substantially attenuated. Additional capacitors on both the HV and GND_{HV} resistor networks shunt high frequency noise to ground.

B. Low-noise stabilization

The low-noise stabilization circuit is crucial to the performance of the design, as it is responsible for removing noise at the output of the flyback converter. To accomplish this, a high slew-rate op-amp (Texas Instruments LM7171, 4100 V/ μ s) drives the galvanically isolated ground node of the flyback converter (see U2 in Fig. 1). This op-amp enforces the HV output voltage

$$V_{HV} = \left(1 + \frac{R_1}{R_2 \parallel R_{mod}}\right) V_{DC} - \left(\frac{R_{mod}}{R_1}\right) V_{mod}. \quad (3)$$

We choose $R_1, R_{\text{mod}} = 1 \text{ M}\Omega$, $R_2 = 20.5 \text{ k}\Omega$ such that the DC gain is ≈ 50 and the modulation gain $V_{\text{HV}}/V_{\text{mod}}$ is unity. Depending on the application, other gain configurations would work equally well provided the non-inverting gain of U2 closely matches the gain of the flyback regulator (since they derive from the same control voltage). Ultimately, the op-amp U2 sets the operating voltage of the output (referenced to true circuit ground) while the flyback converter regulates the high voltage relative to the pseudoground node GND_{HV} . Because the output of the flyback regulator is galvanically isolated, U2 is free to control GND_{HV} . At low frequencies, this amounts to changing the “zero-volt” reference for the flyback regulator, while at high frequencies the capacitor C_{HV} provides a low-impedance pathway to the HV output. In this manner, U2 is simultaneously able to servo residual switching noise and provide a DC-coupled, high-bandwidth modulation of the output.

As a final note, it is worth mentioning that the choice of component for resistors R_1 and R_2 is crucial for the low-noise performance of the system, because this resistive divider is responsible for accurately sensing the voltage V_{HV} ; noise introduced by these resistors cannot be corrected by the op-amp, and thus appears directly at the output. Resistors are fundamentally limited by Johnson noise, in which thermal fluctuations contribute to a white noise power spectrum given by $\sqrt{k_B T R}$. (Cite art of electronics?)⁶ However, resistors also exhibit $1/f$ current noise caused by equilibrium fluctuations of the resistance^{7,8}. The magnitude of this “excess noise” is highly dependent on the resistor composition, and varies from manufacturer to manufacturer. Seifert, et. al.⁹ characterized $1/f$ noise in a variety of resistors, and found that the Vishay TNPW 0.1 %-series resistors showed a noise spectrum almost consistent with Johnson noise down to 1 Hz. A previous iteration of this design used Panasonic ERJ-8ENF resistors (1206, 1 %), and we noticed substantial low-frequency noise correlated with varying strain on the PCB. This is consistent with the findings in⁹, which showed this Panasonic series to exhibit voltage noise two orders of magnitude larger than the TNPW series at 1 Hz. The final board design utilizes three TNPW 0.1 % 0603 resistors in series for both R_1 and R_2 .

C. Digital control and auxiliary design features

The DC setpoint is controlled by a low-noise digital-to-analog converter (DAC). This has several advantages: digital control enhances setpoint repeatability, and makes it easy to integrate with a wide variety of computerized control electronics. The DAC itself is controlled by an onboard microcontroller, which also interacts with the frontpanel control switches, encoders, and LCD display. The entire circuit is designed to fit in a standard Eurocard rack, which supplies power at $\pm 15 \text{ V}$ and contains a backplane with analog lines to communicate with other modules (e.g., to implement a current feed-forward for

laser diodes, see description below). The backplane also contains a secondary microcontroller, which can be addressed over TCP/IP. This vastly expands the conceivable control scenarios. For example, in our lab we implement a slow-feedback lock of two ECDL repumping lasers to a wavemeter. LabView code on the computer attached to the wavemeter computes an error signal and corrective control voltage, which can then be passed over our internal network to the piezo driver to correct for frequency drifts in the laser. Other similar schemes are possible, enabling complete remote control of the laser electronics.

In addition to software-defined control via the backplane, frontpanel control is provided by a rotary encoder/push button, and a single SPDT switch. The encoder/push button provide menu navigation, and the switch toggles between DC and scanning operation. However, other user interfaces can easily be designed to work with the existing hardware. Arduino-based code written in C++ defines the entire software interaction, and can be modified depending on the needs of the researcher.

A voltage proportional to the output (sensed at the inverting node of U2) is buffered and connected to a monitor BNC on the frontpanel and a GPIO line on the backplane. In our lab, this GPIO line is fed to a low-noise current controller (based on the design in¹⁰) to implement a current feed-forward. An optional analog voltage from the backplane can also be summed with the modulation voltage supplied via BNC on the frontpanel to generate V_{mod} . This may be useful, e.g., with servo controllers that reside in the same rack as the other control electronics.

Finally, the high voltage output is interlocked with a signal on the back plane (which can optionally be overridden by placing a jumper); this allows easy integration into existing laboratory interlock schemes, if desired. For more details, see the design files and documentation on Github⁷.

D. Noise Analysis

We analyze the noise performance of the circuit according to the model shown in Fig. 2, where noise spectral densities are calculated at the node V_{HV} . A summary of each noise contribution (op-amp, DAC, Johnson-Nyquist, external modulation input) is shown in Fig. 3, along with the cumulative root-mean-square (RMS) noise estimates in different frequency bands.

To treat the intrinsic op-amp noise contributions, we first compute the noise gain (NG) for this amplifier configuration according to

$$NG(s) = 1 + \frac{Z_1}{R_2 || Z_{\text{mod}}} , \quad (4)$$

where we’ve defined the equivalent impedances $Z_1 = R_1/(1 + R_1 C_1 s)$ and $Z_{\text{mod}} = R_{\text{mod}}/(1 + R_{\text{mod}} C_{\text{mod}} s)$,

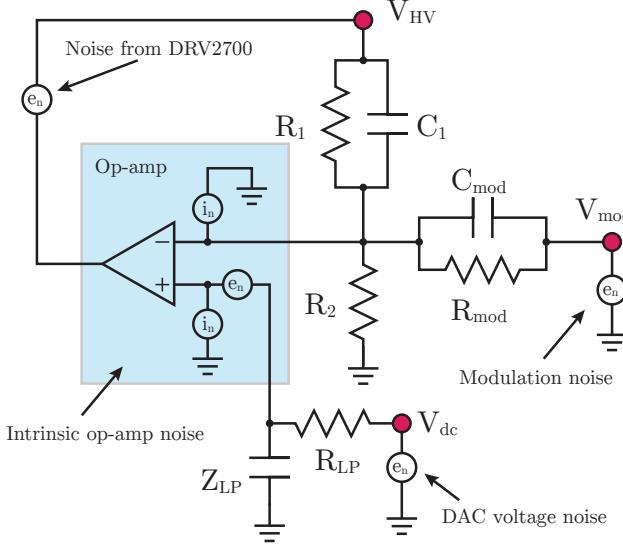


FIG. 2. Noise model (see text). In reality, the capacitor labeled Z_{LP} is comprised of a 47 nF capacitor in parallel with a switchable 10 μ F capacitor, such that the corner frequency of the filter can be changed depending on the mode of operation. The R_{on} resistance of the switch introduces a zero in the transfer function at ≈ 23 kHz, which has negligible effect on the computed RMS noise.

and $s = i\omega$ is the frequency in the Laplace domain. By design, we've chosen $Z_1 \equiv Z_{mod}$ such that the signal gain from the node V_{mod} is unity. This reduces Eq. (4) to

$$NG(s) = 2 + \frac{Z_1}{R_2}. \quad (5)$$

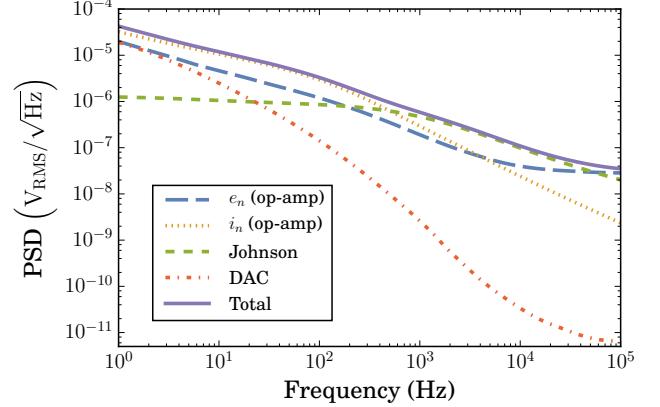
The op-amp noise is parametrized by two noise contributions: e_n , the input voltage noise power spectral density (PSD), and i_n , the input current noise PSD. For the LM7171, $e_n = 14 \text{ nV}/\sqrt{\text{Hz}}$ and $i_n = 1.5 \text{ pA}/\sqrt{\text{Hz}}$ at 10 kHz, with a $1/f$ noise character below this frequency¹¹. The voltage noise is summed in at the non-inverting input, while the current noise is present at both inputs. To convert i_n to an equivalent voltage noise e_n , we multiply by the impedances Z_n , Z_p seen by the inverting and non-inverting nodes, respectively. These are calculated as

$$\begin{aligned} Z_n &= Z_1 \parallel Z_{mod} \parallel R_2 = \frac{Z_1}{2} \parallel R_2 \\ Z_p &= R_{LP} \parallel \frac{1}{s C_{LP}} \end{aligned} \quad (6)$$

The total noise contribution of the op-amp (referenced to the output) is

$$e_{n,\text{op-amp}} = NG(s) \sqrt{e_n^2 + (Z_n i_n)^2 + (Z_p i_n)^2} \quad (7)$$

We now calculate the noise contribution of the DAC.



Noise source	RMS Voltage (1 Hz – 10 Hz)	RMS Voltage (10 Hz – 100 kHz)
e_n (op-amp)	26 μ V	27 μ V
i_n (op-amp)	49 μ V	59 μ V
DAC	22 μ V	7 μ V
Johnson-Nyquist	3 μ V	31 μ V
total (calculated)	60 μV	73 μV

FIG. 3. Noise Contributions (color online). Plotted are the noise contributions from each source in our model, along with the total calculated noise. Power spectral density is referred to the high voltage output, and the table shows the integrated RMS noise due to each noise source in different frequency bands. The total RMS noise (summed in quadrature) over the entire 1 Hz – 100 kHz range is calculated to be 94 μ V.

The noise signal gain from the node V_{DC} is given by

$$\begin{aligned} G_{DC} &= \left(\frac{Z_{LP}}{R_{LP} + Z_{LP}} \right) \left(1 + \frac{Z_1}{R_2 \parallel Z_{mod}} \right) \\ &= \left(\frac{Z_{LP}}{R_{LP} + Z_{LP}} \right) NG(s), \end{aligned} \quad (8)$$

where the first term represents the contribution to the transfer function from the switchable low-pass filter (discussed above). The DAC voltage noise contribution is then simply $e_{n,DAC} = G_{DC} v_{n,DAC}$. The DAC used in our design (Analog devices, AD5663R) has a white noise floor of $100 \text{ nV}/\sqrt{\text{Hz}}$ with an ≈ 1 kHz corner frequency. Without the addition of the low-pass filter after V_{DC} , this DAC would dominate both the low- and high-frequency noise performance of the circuit. However, we are instead dominated by Johnson noise at intermediate to high frequencies, and the op-amp's intrinsic current noise at lower frequencies. Both of these contributions could potentially be suppressed by using lower resistances R_1, R_{mod} , however one must be careful about power and current limitations when dealing with such high voltages. Each noise source is tabulated and plotted in Fig. 3.

III. RESULTS

Here, we show the measured performance of the high-voltage piezo driver. In Fig. 4, we plot the noise power spectral density measured at several different output voltages. These traces were taken on an SR780 spectrum analyzer, with the piezo output coupled through a 0.5 Hz high-pass filter. At 100 V, the integrated noise (1 Hz – 100 kHz) was measured to be $80 \mu\text{V}_{\text{RMS}}$ ($138 \mu\text{V}_{\text{RMS}}$, $101 \mu\text{V}_{\text{RMS}}$ for 50 V, 200 V outputs). This matches well with the expected total RMS noise calculated in Section II D.

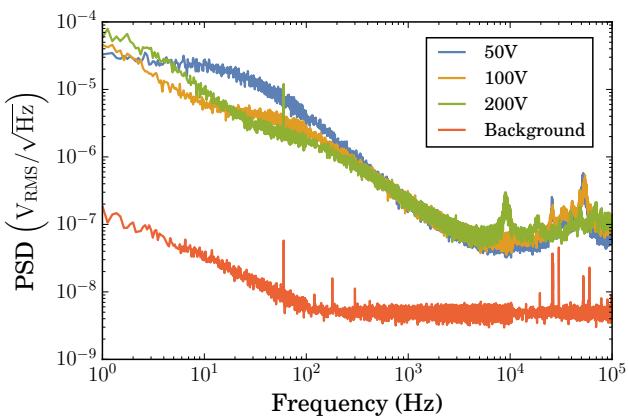


FIG. 4. Voltage power spectral density at various output voltages. The integrated RMS voltage noise (1 Hz – 100 kHz) is $\{138, 80, 101\} \mu\text{V}$ measured at $\{50, 100, 200\} \text{ V}$.

Figure 5 shows the performance at both short- and long-time scales. At long times, voltage fluctuations on the order of a few mV can be observed. This is due generically to $1/f$ noise, but also correlates with the external temperature. A cross-correlation between measured temperature and output voltage fluctuation yields an effective temperature coefficient of $-24 \text{ ppm}/^\circ\text{C}$ at 100 V. The short-term trace was taken on a PicoScope 5442B (ac-coupled, 100 V output). Points are colored based on their normally distributed statistical probability, and thus give a visual estimation of the RMS width.

Finally, Figure 6 shows the measured frequency response under different load conditions. The unloaded bandwidth is as high as a few megahertz, while a $1 \mu\text{F}$ capacitive load can still be driven at $\approx 100 \text{ kHz}$. Several mechanical resonances can be seen with a 700 nF piezoelectric load, as might be expected. In a laboratory setting, these resonances can be mitigated by using a digital feedback controller with notch filters tuned to match the exact resonance frequencies observed in the system¹², thereby extending the usable bandwidth out to $\approx 100 \text{ kHz}$.

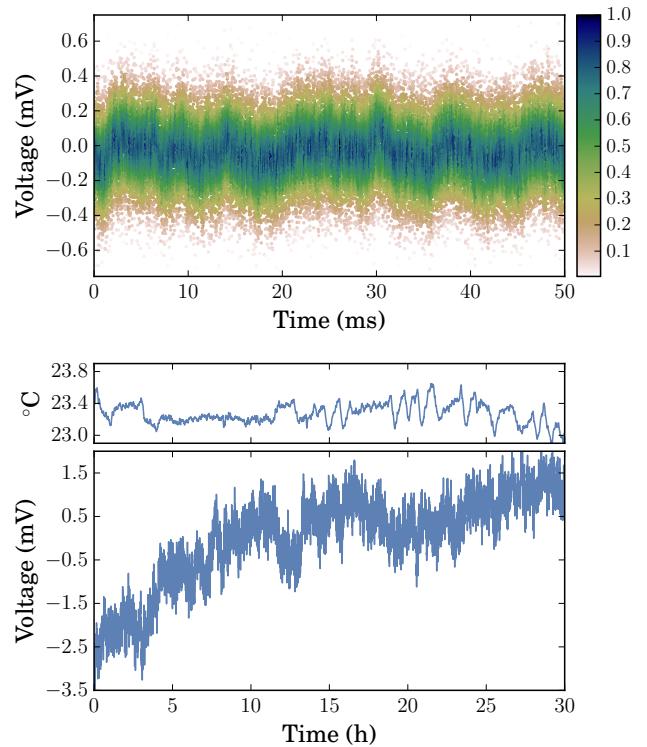


FIG. 5. Time-domain traces of the high voltage output (100 V). Top: short-time scatterplot (AC coupled). Points are colored based on the Gaussian spread in acquired voltages, thus indicating the RMS width of the trace. Bottom: long-term trace, measured on a Keithly 2010 digital multimeter. A 100 V DC offset is subtracted from the plotted values. The top trace shows the lab temperature during the same time period.

IV. CONCLUSION

We have designed, built, and characterized a high-voltage piezoelectric circuit optimized for use in a modern atomic physics laboratory. It is based on a flyback configuration switching regulator, but is able to achieve very low noise performance by active stabilization from a high slew-rate op-amp. This hybrid architecture makes it small and easy to deploy in a variety of situations, without requiring an external, bulky high-voltage power supply. The design principles discussed here can be adapted to fit the exact application, and all design files are freely available on GitHub for others to use and modify.

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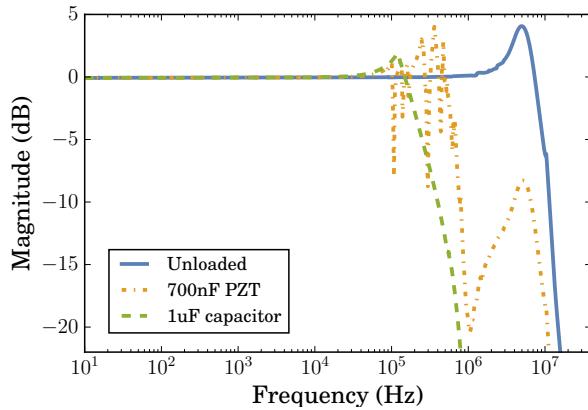


FIG. 6. Modulation input transfer function. Green trace shows the response with a ThorLabs piezoelectric actuator (PN AE0505D08F); the mechanical resonances above ≈ 50 kHz are clearly visible. The red trace shows the response under a $1\ \mu\text{F}$ purely capacitive load. Loaded response bandwidth is ≈ 100 kHz, while unloaded the bandwidth is ≈ 1 MHz.

²<https://github.com/JQIamo/hv-piezo-driver>.

³The identification of commercial products is for information only and does not imply recommendation or endorsement by the National Institute of Standards and Technology.

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