CS M51A, Sec. 1, Class Exercises No. 4

Ex. 4.7 Show that the operation (gate) represented by the switching expression $x'yz + xy' + y'z$ is universal. You can use the constants 0 and 1.

Ex. 4.14 Analyze the network shown in Figure 4.25. Obtain:

a) Switching expressions for each of the outputs.

b) A high-level description assuming that the bit-vector $\underline{s} = (s_2, s_1, s_0)$ represents an integer in the radix-2 representation.

c) For the gate characteristics given in Table 4.1, determine (decompose the gates not available in the table):

- the load factor of each input;
- the load for each gate output; and
- the delay of the network. Give this delay in terms of the load of the output.

d) Give a timing diagram showing the delays in the critical path.

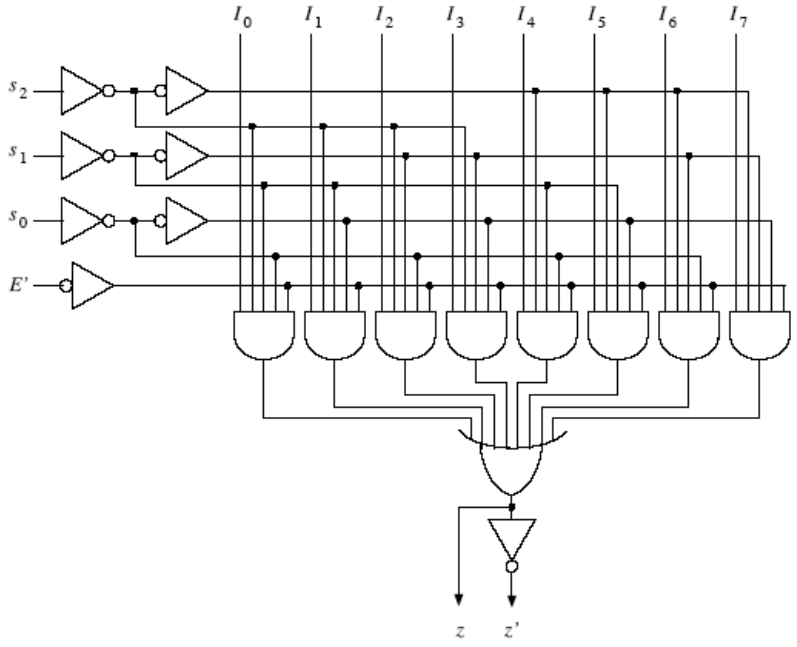

Figure 4.25: Network for Exercise 4.14.