UCLA Computer Science Department: CS M51A / EE M16 Prof. Miloš D. Ercegovac
Logic Design of Digital Systems Engineering VI 468B
Fall 2018, TR 8:00 - 9:50am, MS5200 825-5414; e-mail: milos@cs.ucla.edu
Office hours: Engineering VI, Rm 466, Tue 2:00pm - 3:00pm, or by appt. http://www.cs.ucla.edu/~milos

Course material: Lecture viewgraphs and class notes; readings; solutions; sample exams will be posted on the **CourseWeb.**
Textbook: M.D. Ercegovac, T. Lang and J. Moreno, *Introduction to Digital Systems*, John Wiley & Sons, New York, 1999. Available as reader at UCLA Bookstore and on the Web.

Grading: Homeworks 10%, quizzes 20%, midterm 30%, final 40% .
TAs: Dis 2A - Gurupavan Mazumdar; Dis 2B - Sonali Garg; Dis 2C - Arulsaravana Jeyaraj
• **Homeworks must be turned in at the beginning of discussion sessions - no exceptions!**
• **LogiSim Design Tool:** used in discussion sessions. LogiSim is an easy to use schematic editor and logic simulator; free download at **LogiSim**.

CS M51A Fall 2018: Syllabus and Schedule - REVISED 11/7/2018.

Week 1

- Thursday, 9/27. About the course. About digital systems. Combinational and sequential systems. Specification, design, and analysis of systems. Hierarchy of levels in specification, analysis and design: algorithmic (computational), register-transfer level (RTL), logic level, circuit (transistor - physical) level. Readings: Chapter 1.
Specification of combinational systems. High-level and binary-level specifications. Data representation: numbers, characters, and sets. Readings: Chapter 2, Appendix A.
Friday, 10/28: Discussions: Binary and decimal number systems and conversions. Boolean Algebra.

- Tuesday, 10/2. Combinational systems: Binary specification of inputs/outputs and functions. Central concept of functional description: switching function (SF). Incompletely specified SFs. Basis of hierarchical specification and design: Composition of SFs. Switching algebra, switching expressions (SEs, evaluation of SEs, equivalent SEs, and algebraic transformations of SEs. Standard forms for SEs: sum of products (SOP) and product of sums (POS). Readings: Chapter 2, Appendix A.

Week 2

- Thursday, 10/4. Canonical forms: Sum of minterms and product of maxterms. Examples of combinational system specifications. Readings: Chapter 2.
HW1 posted. Friday, 10/5: Discussions.

- Tuesday,10/9. Physical level: CMOS transistor switches and gates: NOT, NAND/NOR, AND/OR, and XOR. Readings: Chapter 3.

Week 3

- Thursday, 10/11. Complex gates. Transmission gates and their use. Timing parameters, load, load factors, and propagation delays. Three-state drivers and buses. VLSI design styles and packaging.
Readings: Chapter 3. HW2 posted. Friday, 10/12: Discussions; HW1 due.

- Tuesday, 10/16. Gate networks definition and description. Universal gate sets. Functional analysis. Timing analysis. Logic levels and critical path. Readings: Chapter 4.

Week 4

- Thursday, 10/18. Design of combinational systems: minimal two-level networks. Graphical minimization of expressions (Karnaugh Maps).
  Readings: Chapter 5. HW3 posted. Friday, 10/19: Discussions, Quiz 1; HW2 due.

- Tuesday,10/23. NAND and NOR networks. Programmable logic arrays (PLAs) and Field Programmable Gate Arrays (FPGAs). Readings: Chapter 5 and Chapter 12 (Sec on FPGAs). Examples of designs.

Week 5

- Thursday, 10/25.

  Friday, 10/26: Discussions, HW3 due.

- Tuesday, 10/30. MIDTERM EXAM – in class – .
  The exam covers Chapters 2, 3, 4, and 5. Closed books and notes. Four cheat sheets allowed. Tables and identities given if needed.
  HW4 posted.

Week 6

- Thursday, 11/1. Synchronous sequential systems. Main types of sequential systems: Moore and Mealy Machines. Finite-state machines (FSM). State description: state table and state diagram. Time behavior. Finite memory machines. Readings: Chapter 7. Friday, 11/2, Quiz 2.

- Tuesday, 11/6. Reduction of the state set. Binary specification. Types of sequential systems. Readings: Chapter 7.

Week 7

- Thursday, 11/8. Implementation of sequential systems: sequential networks. Canonical form: Huffman-Moore. Latches and Edge-triggered cells. D flip-flop. Timing characteristics.
  Readings: Chapter 8.
  Friday, 11/9, HW4 due.

- Tuesday, 11/13. Analysis and design of canonical networks. Flip-flops: SR, JK, and T. Analysis of sequential networks with flip-flops. Design of sequential networks with flip-flops. Excitation functions. Special state assignments: ”one flip-flop per state” and shifting register. Examples. Readings: Chapter 8. HW5 posted.

Week 8

- Thursday, 11/15.

  Standard combinational modules and networks: Decoders and Encoders. Implementation and uses. Large decoders: coincident and tree. Readings: Chapter 9.
  Friday, 11/16: Quiz 3.

- Tuesday, 11/20. Multiplexers, implementation and uses. Large multiplexers. Demultiplexers, implementation and uses. Shifters, types, and implementations. Uses of standard modules. Readings: Chapter 9.

Week 9

- Tuesday, 11/27. Arithmetic combinational modules. Addition of positive integers. Binary adders and basic modules: Full adder and half adder. Carry-ripple adder. Representation of signed integers: Two's complement and ones' complement systems. Readings: Chapter 10. Sample Final posted.

- Thursday, 11/29. Operations in two's complement system: addition/subtraction, change of sign, sign and overflow detection. Comparators, arithmetic-logic units (ALUs), and multipliers for positive integers. Readings: Chapter 10. HW6 posted.

  Friday, 11/30: Discussion. HW5 due.

Week 10

- Tuesday, 12/4. Standard sequential modules and networks: registers, shift registers, and counters. Their specifications, implementations, implementation of larger modules, and uses. Readings: Chapter 11.

- Thursday, 12/6.

  Course Review: Q and A Session.

  Friday, 12/7: Quiz 4. HW6 due. Solutions to Sample Final posted.

- **FINAL EXAM, December 11, 8:00am - 11:00am, in class.** The exam is comprehensive with emphasis on Chapters 7, 8, 9, 10, and 11. Closed textbook and notes. Four cheat sheets allowed. Tables provided if needed.
