[CS M51A F18] Homework 5

Due: 11/30/18

This homework covers Chapters 7 and 8.

Homework Problems (55 points total)

Problem 1 (5 points)

Exercise 7.16

Problem 2 (5 points)

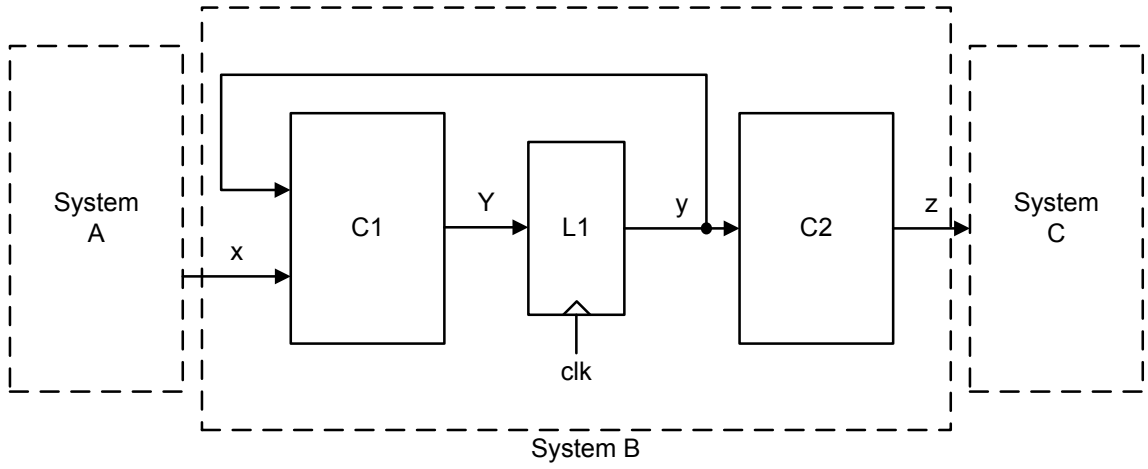
Exercise 7.18

Problem 3 (5 points)

Exercise 7.22

Problem 4 (10 points)

We would like to analyze the timing required for the following sequential system. All registers in the system are positive edge triggered flip-flops. Propagation delays of all registers are equal at $t_p = 1.5$ ns, and setup times for all registers are also fixed at $t_{su} = 0.4$ ns.



For System A, the delay from the output of the state register to signal x is $d2_A = 2.5$ ns.

For System B, the delay with respect to input x is $d1^x = 3.5$ ns, the delay with respect to state register value y is $d1^y = 4.5$ ns, and the delay of the output combinational logic is $d2_B = 2.5$ ns.

For System C, the delay for signal z to reach the state register of System C is $d1^z = 2.7$ ns.

1. Assume no clock skew for the three systems. What is the minimum clock period required in regard to signal x?

2. What is the minimum clock period required in regard to signal y?

3. What is the minimum clock period required in regard to signal z?

4. Considering all the three previous values, what is the minimum clock period required for the whole system?

5. Now, increased distance between the three systems has caused clock skew, and we need to take it into consideration. System C is the closest to the clock source, and the clock arrives at System C the fastest. The clock arrives at System B 0.3 ns later than it arrives at System C, and it arrives at System A 0.6 ns later than System C.

   Of the three clock periods related to signals x, y and z, calculate the adjusted minimum clock period of the affected signals. Also, what is the minimum clock period for the whole system with clock skew?

Problem 5 (5 points)

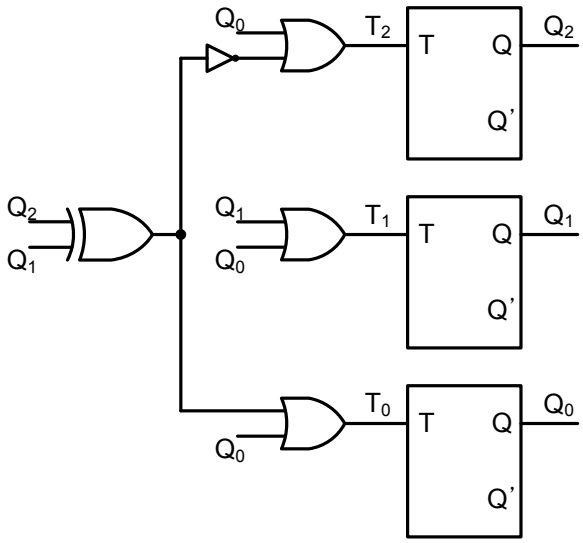
1. Create a D flip-flop using a JK flip-flop. Use the excitation tables on page 221 of the textbook.

2. Create a T flip-flop using an SR flip-flop.

3. Create a JK flip-flop using a T flip-flop.

Problem 6 (5 points)

We would like to analyze the sequential system shown below. It is a autonomous counter which outputs a fixed string of numbers. The output changes at every clock cycle.



1. Write the expressions for T_2, T_1, and T_0.

2. Write the table of T_2, T_1 and T_0. Using this table, show the state transition table.

3. Draw the state transition diagram of the system.

Problem 7 (10 points)

We want to design a cyclic counter which has an output sequence of period 8 as shown:
$0000 \rightarrow 0001 \rightarrow 0011 \rightarrow 0111 \rightarrow 1111 \rightarrow 1110 \rightarrow 1100 \rightarrow 1000 \rightarrow 0000 \rightarrow 0001 \rightarrow ...$

The counter does not have an input signal, but moves to the appropriate next state at every clock. Code the states so that the output at each state will be the same as the state assignment, in other words, $z(t) = s(t)$. Assume that the counter will always start at 0000 and will never enter an unused state.

1. Design the counter using T flip-flops. Write the state transition table, show the table of flip-flop inputs, draw the K-maps, and write switching expressions for each state bit T_i.

2. Repeat the same process using JK flip-flops. The state transition table is the same as part 1. Show the table of flip-flop inputs, K-maps, and switching expressions for each J_i and K_i.

Problem 8 (10 points)

We would like to design a pattern recognizer with a binary stream as input. The system has a binary output bit, which is 1 whenever $x(t-3, t) = 0010$ or 0001 and 0 otherwise.

1. Draw the state transition diagram. Try to minimize the number of states. (*Hint: The system can be designed using only 5 states.*)

2. Encode the states into binary bits. From the encoding, write the state transition table and table of JK flip-flop inputs.

3. Using K-maps, derive the switching expressions for each flip-flop input J_i, K_i, and the output bit z.

4. Draw the sequential flip-flop network.