CS M51A, Sec. 1, Class Exercises No. 4 - SOLUTIONS

Exercise 4.7:
The operation specified by

$$g(x, y, z) = x'yz + xy' + y'z$$

is universal because $g(x, 1, 1) = x'$ realizes the NOT operation, and $g(x, 0, z) = x + z$ realizes the OR operation. Since the set $\{OR, NOT\}$ is universal, the g operation is also universal.

Exercise 4.14 (a) The switching expression for output z is

$$z = E(I_0 s_2' s_1' s_0' + I_1 s_2' s_1' s_0 + I_2 s_2' s_1 s_0' + I_3 s_2' s_1 s_0 + I_4 s_2 s_1' s_0' + I_5 s_2 s_1' s_0 + I_6 s_2 s_1 s_0' + I_7 s_2 s_1 s_0)$$

or

$$z = E \sum_{i=0}^{7} I_i m_i(s_2, s_1, s_0)$$

(b) A high-level description is

$$z = \begin{cases} I_s & \text{if E=1} \\ 0 & \text{otherwise} \end{cases}$$

where $s = 4s_2 + 2s_1 + s_0$.

This function corresponds to an 8-input multiplexer (selector), that is discussed in Chapter 9 of the textbook.

(c) The load factor of each input is 1, since each input is connected to only one gate input in the circuit.

The load applied to each gate is:

gate	Load
NOT connected to E'	8
NOT gates connected to s_i	5
NOT gates to restore s_i	4
AND gates	1
OR gate	$L_1 + 1$
NOT used to generate z'	L_2

where, L_1 and L_2 are the Load imposed to the outputs z and z' respectively.

The delay of this network cannot be calculated based on the table given because there are no expressions for an AND gate with 5 inputs and an OR gate with 8 inputs. Calling these delays:

$$\begin{aligned} t_{pLH}(\text{AND-5}) &= T_1 \\ t_{pHL}(\text{AND-5}) &= T_2 \\ t_{pLH}(\text{OR-8}) &= T_3 \\ t_{pHL}(\text{OR-8}) &= T_4 \end{aligned}$$

the critical path delay is:

$$\begin{aligned} t_{pLH}(s_2, z') &= t_{pLH}(\text{NOT}) + t_{pHL}(\text{NOT}) + t_{pHL}(\text{AND-5}) + t_{pHL}(\text{OR-8}) + t_{pLH}(\text{NOT}) \\ &= 0.02 + 0.038 \times 5 + 0.05 + 0.017 \times 4 + T_2 + T_4 + 0.02 + 0.038 \times L_2 \\ &= 0.35 + T_2 + T_4 + 0.038 \times L_2 \\ t_{pHL}(s_2, z') &= t_{pHL}(\text{NOT}) + t_{pLH}(\text{NOT}) + t_{pLH}(\text{AND-5}) + t_{pLH}(\text{OR-8}) + t_{pHL}(\text{NOT}) \\ &= 0.05 + 0.017 \times 5 + 0.02 + 0.038 \times 4 + T_1 + T_3 + 0.05 + 0.017 \times L_2 \\ &= 0.36 + T_1 + T_3 + 0.017 \times L_2 \end{aligned}$$

The values of T_1, T_2, T_3 and T_4 are obtained by decomposition of the AND-5 and OR-8 gates into the gates listed in Table 3.1 of the book. This decomposition is:

$$AND(x_4, x_3, x_2, x_1, x_0) = AND(AND(x_4, x_3, x_2), AND(x_1, x_0))$$

and

$$OR(x_7, x_6, \ldots, x_1, x_0) = OR(OR(x_7, x_6, x_5, x_4), OR(x_3, x_2, x_1, x_0)$$

The resulting delays are:

$$\begin{aligned} T_1 &= t_{pLH}(\text{AND-3}) + t_{pLH}(\text{AND-2}) = 0.2 + 0.038 + 0.15 + 0.037 = 0.43 \\ T_2 &= t_{pHL}(\text{AND-3}) + t_{pHL}(\text{AND-2}) = 0.18 + 0.018 + 0.16 + 0.017 = 0.38 \\ T_3 &= t_{pLH}(\text{OR-4}) + t_{pLH}(\text{OR-2}) = 0.13 + 0.038 + 0.12 + 0.037(L_1 + 1) = 0.33 + 0.037L_1 \\ T_4 &= t_{pHL}(\text{OR-4}) + t_{pHL}(\text{OR-2}) = 0.45 + 0.025 + 0.2 + 0.019(L_1 + 1) = 0.69 + 0.019L_1 \end{aligned}$$

(d) timing diagram presented in figure 4.7.

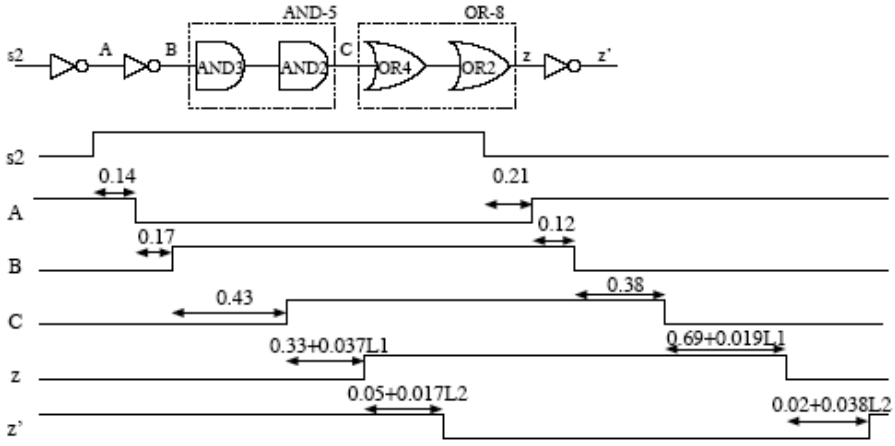

Figure 4.7: Timing diagram of Exercise 4.14