CS M51A, Sec. 1, Class Exercises No. 3

Ex. 3.2 As stated in Section 3.2.3, the p-net is the complement of the n-net; that is, when the n-net has a path to ground the p-net should not have a path to V_{DD}, and vice versa. Show that this requirement is not satisfied for the network in Figure 3.20. (Hint: consider the case $a = b = 1$ and $c = d = 0$). Consequently, this network is not satisfactory to implement the expression $z = (a' + b')c'd'$.

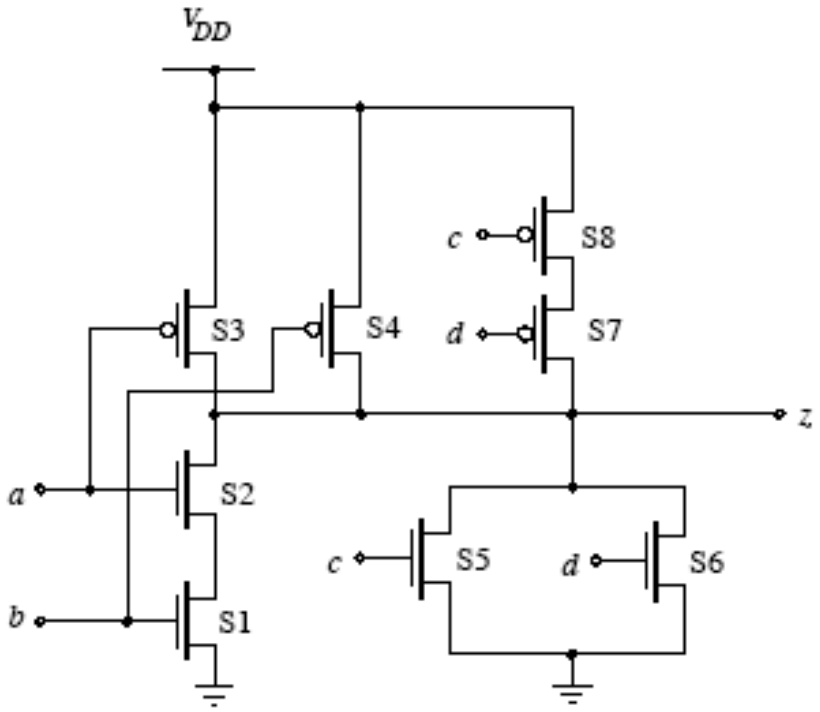

Figure 3.20: Network for Exercise 3.2.

Ex. 3.4 Show a CMOS circuit that implements the following function for positive logic:

x_1	x_0	z
0	0	0
0	1	1
1	0	0
1	1	0