CS M51A, Sec. 1, Class Exercises No. 3 - SOLUTIONS

Exercise 3.2 We can see from the figure that the switches S1 to S4 form a NAND gate and the switches S5 to S8 implement a NOR gate. The organization of switches is such that we have the NAND and the NOR gate implementations with the outputs connected together. This indicates that the circuit was intended to implement the expressions $((ab)+(c+d)')' = (a'+b')c'd'$. However, as indicated in the hint, for the case $a = b = 1$ and $c = d = 0$, there is a path from V_{DD} to ground passing through transistors S8, S7, S2, and S1. Consequently, this circuit does not operate correctly. A correct circuit circuit for this function is shown in figure 3.1.

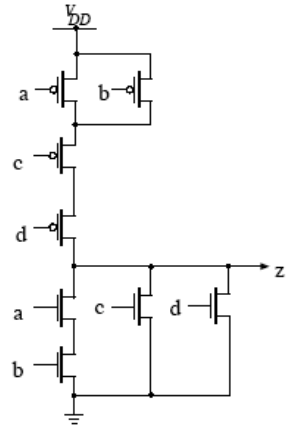

Figure 3.1: Network the implements the function $z = (a' + b')c'd'$ – Exercise 3.2

Exercise 3.4 The circuit that implements the function $z = x_0x_1' = (x_0' + x_1)'$ is presented in figure 3.3.

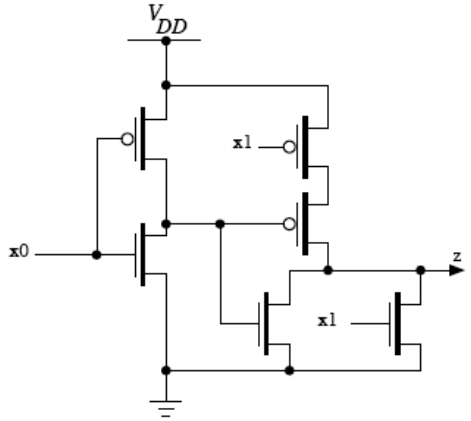

Figure 3.3: Exercise 3.4 - Circuit that implements $z = (x_0' + x_1)'$