[CS M51A F18] Solution to Homework 5

Due: 11/30/18

This homework covers Chapters 7 and 8.

Homework Problems (55 points total)

Problem 1 (5 points)

Exercise 7.16

Solution

Exercise 7.16

Based on the outputs for each state we get the first partition P_1 as:

$$P_1 = (A, D, E)(B, F, G)(C, H)$$

Let's call (A,D,E) as group 1, (B,F,G) as group 2 and (C,H) as group 3.
We can construct a table representing the next group for each state transition:

	group 1			group 2			group 3	
	A	D	E	B	F	G	C	H
0	2	2	2	3	3	3	3	3
1	3	3	3	1	1	1	1	1

From the table we can see that the columns for each group of states are the same, and so, the states in each group are also 2-equivalent. $P_2 = P_1$. Renaming the states in group 1 as α, the states in group 2 as β and in group 3 as γ, we can represent the reduced sequential system as:

PS	$Input$	
	$x = 0$	$x = 1$
α	$\beta, 0$	$\gamma, 0$
β	$\gamma, 1$	$\alpha, 1$
γ	$\gamma, 0$	$\alpha, 1$

Problem 2 (5 points)

Exercise 7.18

Solution

Exercise 7.18 Based on the outputs for each state we get the first partition

$$P_1 = (N, O, Q, R, X, Z)(P, U, V, Y)(S, T, W)$$

To obtain P_2, we determine the class of P_1 to which the successors of the states belong.

	group 1						group 2				group 3		
	N	O	Q	R	X	Z	P	U	V	Y	S	T	W
a	3	3	3	3	3	3	2	2	2	2	1	1	1
b	1	2	2	2	1	1	1	1	1	1	2	2	2

Partition P_2 is

	group 1			group 2			group 3				group 4		
	N	X	Z	O	Q	R	P	U	V	Y	S	T	W
a	4	4	4	4	4	4	3	3	3	3	1	1	1
b	1	1	1	3	3	3	2	2	1	1	3	3	3

Partition P_3 is

	group 1			group 2			group 3		group 4		group 5		
	N	X	Z	O	Q	R	P	U	V	Y	S	T	W
a	5	5	5	5	5	5	4	4	3	3	1	1	1
b	1	1	1	4	4	4	2	2	1	1	4	4	3

Partition P_4 is

	group 1			group 2			group 3		group 4		group 5		group 6
	N	X	Z	O	Q	R	P	U	V	Y	S	T	W
a	5	6	5	5	6	6	4	4	3	3	1	1	
b	1	1	1	4	4	4	2	2	1	1	4	4	

Partition P_5 is

	group 1		group 2	group 3	group 4		group 5		group 6		group 7		group 8
	N	Z	X	O	Q	R	P	U	V	Y	S	T	W
a	7	7			8	8	6	6	5	5	1	1	
b	1	1			6	6	4	4	1	1	6	6	

STOP!

Equivalent states: {N,Z}, {O}, {P,U}, {Q,R}, {S,T}, {V,Y}, {W}, {X}

Minimal state transition table:

PS	*input*	
	$x = a$	$x = a'$
N	S/f	N/e
O	S/f	V/e
P	V/e	Q/f
Q	W/f	V/e
S	N/e	V/e
V	P/f	N/f
W	X/e	P/e
X	W/f	N/e
	$NS/output$	

Problem 3 (5 points)

Exercise 7.22

Solution

Exercise 7.22

The input set is $I = \{0, 1, 2, 3, 4, 5, 6, 7, 8, 9\}$ and the output set $O = \{0, 1, 2, 3, 4\}$. The state is formed of two components: s_1 to detect the pattern 358, and s_2 to count *mod* 5 the number of instances. For the pattern recognizer, we need three states as follows:

$$\begin{aligned}
s_1(t) &= A \textbf{ if } x(t-1) = 3 \\
s_1(t) &= B \textbf{ if } x(t-2, t-1) = 35 \\
s_1(t) &= C \textbf{ if none of above} \\
s_1(0) &= C
\end{aligned}$$

The state description of this component is

$$s_1(t+1) = \begin{cases} A & \textbf{if } x(t) = 3 \\ B & \textbf{if } s_1(t) = A \textbf{ and } x(t) = 5 \\ C & \textbf{otherwise} \end{cases}$$

The second component is a modulo 5 counter. Consequently, the state has five values which we label with the integers 0, 1, 2, 3 and 4 to be able to write the state transition as the arithmetic expression:

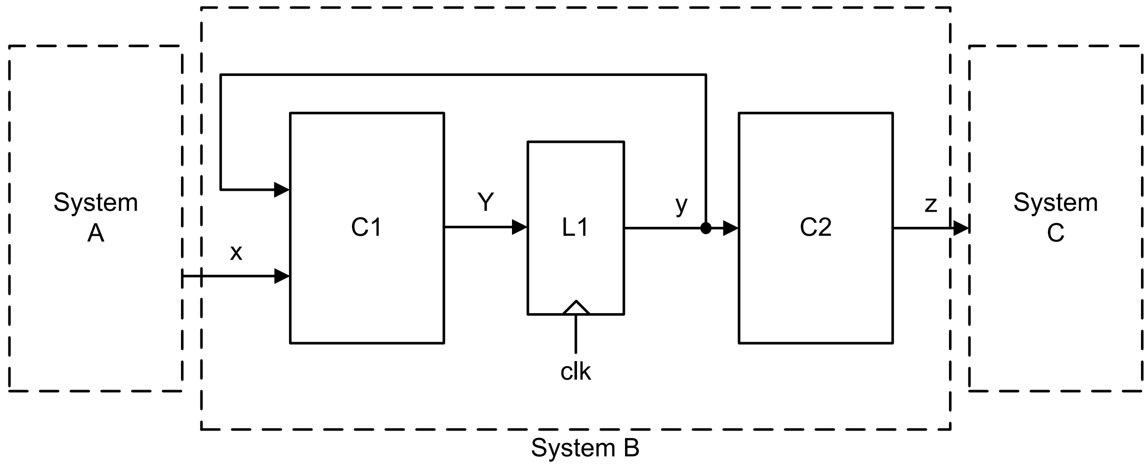
$$s_2(t+1) = \begin{cases} (s_2(t)+1) \; mod \; 5 & \textbf{if } s_1(t) = B \textbf{ and } x(t) = 8 \\ s_2(t) & \textbf{otherwise} \end{cases}$$

$$s_2(0) = 0$$

Finally, the output function is $z(t) = s_2(t)$.

Problem 4 (10 points)

We would like to analyze the timing required for the following sequential system. All registers in the system are positive edge triggered flip-flops. Propagation delays of all registers are equal at $t_p = 1.5$ ns, and setup times for all registers are also fixed at $t_{su} = 0.4$ ns.



For System A, the delay from the output of the state register to signal x is $d2_A = 2.5$ ns.

For System B, the delay with respect to input x is $d1^x = 3.5$ ns, the delay with respect to state register value y is $d1^y = 4.5$ ns, and the delay of the output combinational logic is $d2_B = 2.5$ ns.

For System C, the delay for signal z to reach the state register of System C is $d1^z = 2.7$ ns.

1. Assume no clock skew for the three systems. What is the minimum clock period required in regard to signal x?

   Solution Regarding signal x:

$$\begin{aligned} & t_{in} + d1^x + t_{suB} \\ = \; & t_{pA} + d2_A + d1^x + t_{suB} \\ = \; & 1.5 + 2.5 + 3.5 + 0.4 \\ = \; & 7.9 \text{ (ns)} \end{aligned}$$

2. What is the minimum clock period required in regard to signal y?

   Solution Regarding signal y, we have:

$$\begin{aligned} & t_{pB} + d1^y + t_{suB} \\ = \; & 1.5 + 4.5 + 0.4 \\ = \; & 6.4 \text{ (ns)} \end{aligned}$$

3. What is the minimum clock period required in regard to signal z?

   Solution Regarding signal z, we get:

$$\begin{aligned} & t_{pB} + d2_B + t_{out} \\ = \; & t_{pB} + d2_B + d1^z + t_{suC} \\ = \; & 1.5 + 2.5 + 2.7 + 0.4 \\ = \; & 7.1 \text{ (ns)} \end{aligned}$$

4. Considering all the three previous values, what is the minimum clock period required for the whole system?

   Solution T_{min} should be larger than all three values, thus the minimum $T_{min} = max\{7.9, 6.4, 7.1\} = 7.9$ (ns).

5. Now, increased distance between the three systems has caused clock skew, and we need to take it into consideration. System C is the closest to the clock source, and the clock arrives at System C the fastest. The clock arrives at System B 0.3 ns later than it arrives at System C, and it arrives at System A 0.6 ns later than System C.

   Of the three clock periods related to signals x, y and z, calculate the adjusted minimum clock period of the affected signals. Also, what is the minimum clock period for the whole system with clock skew?

   Solution Two clock periods are affected by the clock skew, the delay regarding signal x, and signal z. In both cases, the clock arrives faster at the system setup, thus in effect we need longer clock periods to make up for the lost time.

   Therefore, the new delay values are:

$$\begin{aligned} delay_x &= 7.9 + 0.3 = 8.2 \text{ (ns)} \\ delay_y &= 6.4 \text{ (ns) (no change)} \\ delay_z &= 7.1 + 0.3 = 7.4 \text{ (ns)} \end{aligned}$$

   The new $T_{min} = 8.2$ ns.

Problem 5 (5 points)

1. Create a D flip-flop using a JK flip-flop. Use the excitation tables on page 221 of the textbook.

   Solution First, we know that a D flip-flop works like this:

$Q(t)$	$D(t) = 0$	$D(t) = 1$
0	0	1
1	0	1
	$Q(t+1)$	

   To make the transition from $Q(t)$ to $Q(t+1)$, we need to figure out the inputs to our JK flip-flop. The inputs should be generated by a combinational circuit with inputs $Q(t)$ and $D(t)$.

$Q(t)$	$Q(t+1) = 0$	$Q(t+1) = 1$
0	0-	1-
1	-1	-0
	$J(t)K(t)$	

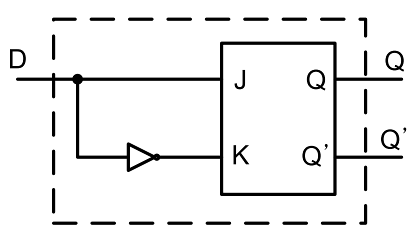
   As we know the excitation table of a JK flip-flop is as shown in the above table, we can write:

$Q(t)$	$D(t) = 0$	$D(t) = 1$	$D(t) = 0$	$D(t) = 1$
0	0	1	0-	1-
1	0	1	-1	-0
	$Q(t+1)$		$J(t)K(t)$	

   Looking at this table we can write:

$$\begin{aligned} J(t) &= D(t) \\ K(t) &= D(t)' \end{aligned}$$

   The final D flip-flop would look like this.



2. Create a T flip-flop using an SR flip-flop.

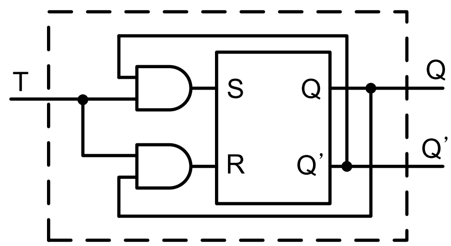
Solution The excitation table of an SR flip-flop is as shown:

$Q(t)$	$Q(t+1)=0$	$Q(t+1)=1$
0	0-	10
1	01	-0
	$S(t)R(t)$	

Following a similar procedure as above, we get the following:

$Q(t)$	$T(t)=0$	$T(t)=1$	$T(t)=0$	$T(t)=1$
0	0	1	0-	10
1	1	0	-0	01
	$Q(t+1)$		$S(t)R(t)$	

$$\begin{aligned} S(t) &= T(t)Q'(t) \\ R(t) &= T(t)Q(t) \end{aligned}$$



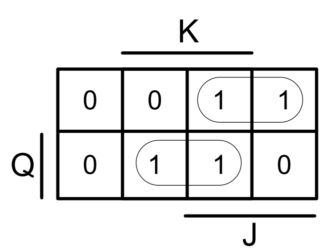
3. Create a JK flip-flop using a T flip-flop.

Solution The excitation table of a T flip-flop is:

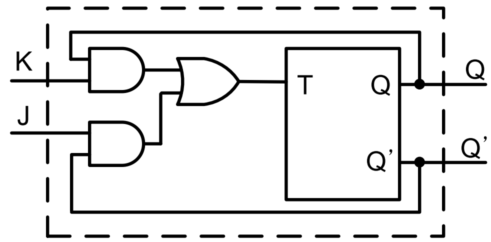
$Q(t)$	$Q(t+1)=0$	$Q(t+1)=1$
0	0	1
1	1	0
	$T(t)$	

Similarly, we can get:

$Q(t)$	$J(t)K(t)$				$J(t)K(t)$			
	00	01	10	11	00	01	10	11
0	0	0	1	1	0	0	1	1
1	1	0	1	0	0	1	0	1
	$Q(t+1)$				$T(t)$			

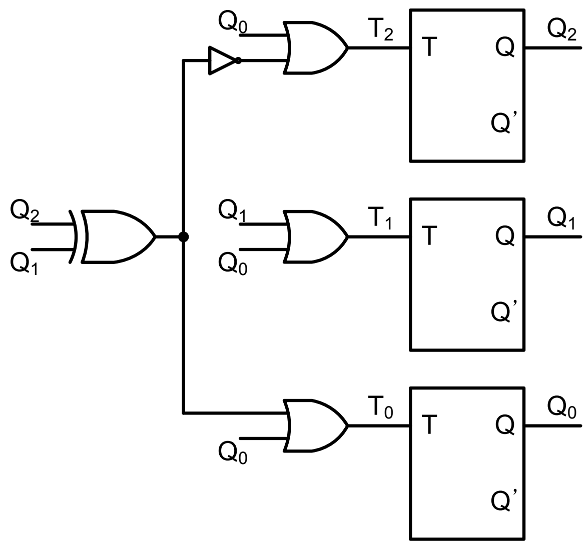


$$T(t) = Q(t)K(t) + Q'(t)J(t)$$



Problem 6 (5 points)

We would like to analyze the sequential system shown below. It is a autonomous counter which outputs a fixed string of numbers. The output changes at every clock cycle.



1. Write the expressions for T_2, T_1, and T_0.

   Solution Looking at the gate network we can write:

$$\begin{aligned} T_2 &= Q_0 + (Q_2 \oplus Q_1)' \\ &= Q_0 + Q_2'Q_1' + Q_2Q_1 \\ T_1 &= Q_1 + Q_0 \\ T_0 &= Q_0 + Q_2 \oplus Q_1 \\ &= Q_0 + Q_2'Q_1 + Q_2Q_1' \end{aligned}$$

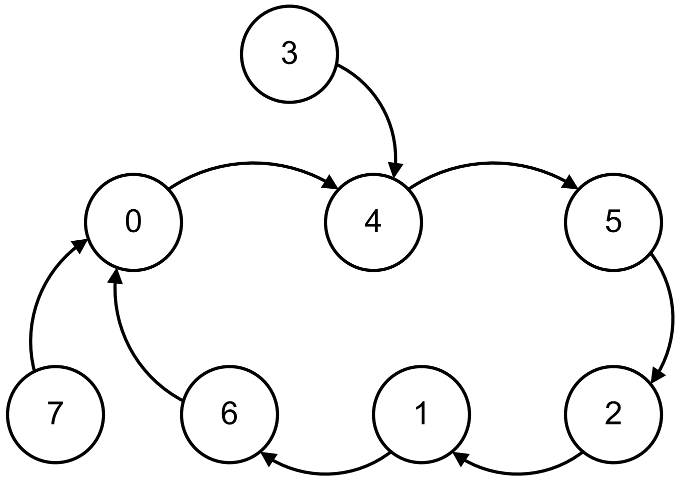
2. Write the table of T_2, T_1 and T_0. Using this table, show the state transition table.

   Solution

PS	T			NS		
$Q_2Q_1Q_0$	T_2	T_1	T_0	Q_2	Q_1	Q_0
000	1	0	0	1	0	0
001	1	1	1	1	1	0
010	0	1	1	0	0	1
011	1	1	1	1	0	0
100	0	0	1	1	0	1
101	1	1	1	0	1	0
110	1	1	0	0	0	0
111	1	1	1	0	0	0

3. Draw the state transition diagram of the system.

Solution Writing the state values in decimal numbers, the state diagram is as shown:



Problem 7 (10 points)

We want to design a cyclic counter which has an output sequence of period 8 as shown:

0000 → 0001 → 0011 → 0111 → 1111 → 1110 → 1100 → 1000 → 0000 → 0001 →...

The counter does not have an input signal, but moves to the appropriate next state at every clock. Code the states so that the output at each state will be the same as the state assignment, in other words, $z(t) = s(t)$. Assume that the counter will always start at 0000 and will never enter an unused state.

1. Design the counter using T flip-flops. Write the state transition table, show the table of flip-flop inputs, draw the K-maps, and write switching expressions for each state bit T_i.

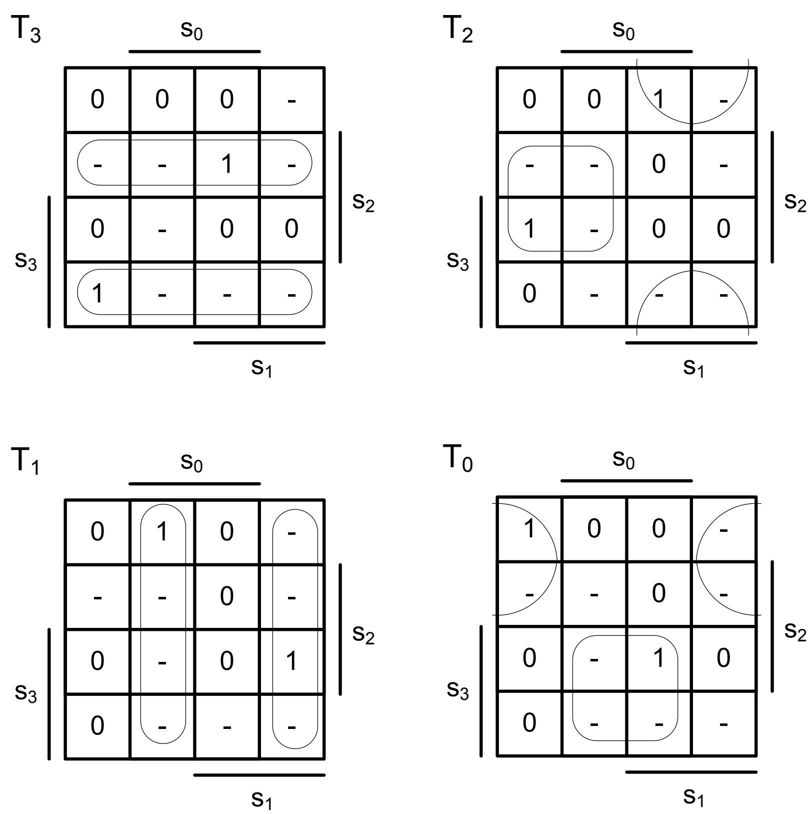
   Solution Since $z(t) = s(t)$, the state transition table is as shown:

PS				NS			
s_3	s_2	s_1	s_0	s_3	s_2	s_1	s_0
0	0	0	0	0	0	0	1
0	0	0	1	0	0	1	1
0	0	1	0	-	-	-	-
0	0	1	1	0	1	1	1
0	1	0	0	-	-	-	-
0	1	0	1	-	-	-	-
0	1	1	0	-	-	-	-
0	1	1	1	1	1	1	1
1	0	0	0	0	0	0	0
1	0	0	1	-	-	-	-
1	0	1	0	-	-	-	-
1	0	1	1	-	-	-	-
1	1	0	0	1	0	0	0
1	1	0	1	-	-	-	-
1	1	1	0	1	1	0	0
1	1	1	1	1	1	1	0

   Examining the state transitions in the table and using the excitation table of the T flip-flop, we can get:

	PS				T		
s_3	s_2	s_1	s_0	T_3	T_2	T_1	T_0
0	0	0	0	0	0	0	1
0	0	0	1	0	0	1	0
0	0	1	0	-	-	-	-
0	0	1	1	0	1	0	0
0	1	0	0	-	-	-	-
0	1	0	1	-	-	-	-
0	1	1	0	-	-	-	-
0	1	1	1	1	0	0	0
1	0	0	0	1	0	0	0
1	0	0	1	-	-	-	-
1	0	1	0	-	-	-	-
1	0	1	1	-	-	-	-
1	1	0	0	0	1	0	0
1	1	0	1	-	-	-	-
1	1	1	0	0	0	1	0
1	1	1	1	0	0	0	1

From here, we can get the following K-maps:



and the corresponding switching expressions would be:

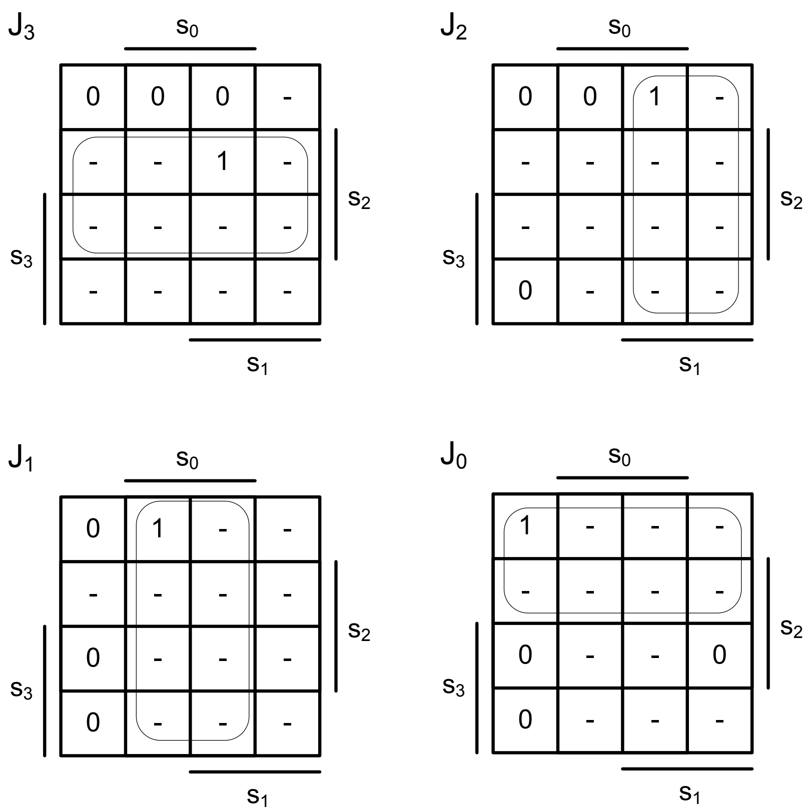
$$
\begin{aligned}
T_3 &= s_3 s_2{}' + s_3{}' s_2 \\
T_2 &= s_2 s_1{}' + s_2{}' s_1 \\
T_1 &= s_1 s_0{}' + s_1{}' s_0 \\
T_0 &= s_3 s_0 + s_3{}' s_0{}'
\end{aligned}
$$

2. Repeat the same process using JK flip-flops. The state transition table is the same as part 1. Show the table of flip-flop inputs, K-maps, and switching expressions for each J_i and K_i.

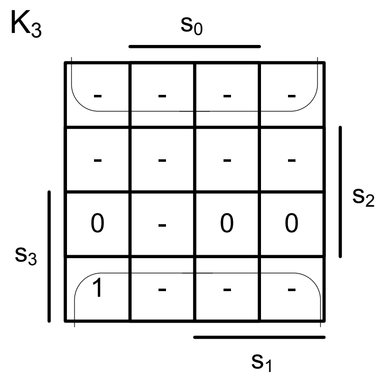
Solution Again, using the excitation table for JK flip-flops, we can write:

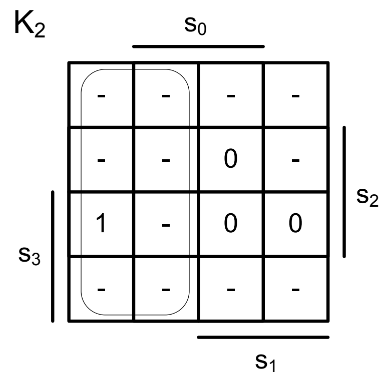
PS				JK			
s_3	s_2	s_1	s_0				
0	0	0	0	0-	0-	0-	1-
0	0	0	1	0-	0-	1-	-0
0	0	1	0	--	--	--	--
0	0	1	1	0-	1-	-0	-0
0	1	0	0	--	--	--	--
0	1	0	1	--	--	--	--
0	1	1	0	--	--	--	--
0	1	1	1	1-	-0	-0	-0
1	0	0	0	-1	0-	0-	0-
1	0	0	1	--	--	--	--
1	0	1	0	--	--	--	--
1	0	1	1	--	--	--	--
1	1	0	0	-0	-1	0-	0-
1	1	0	1	--	--	--	--
1	1	1	0	-0	-0	-1	0-
1	1	1	1	-0	-0	-0	-1

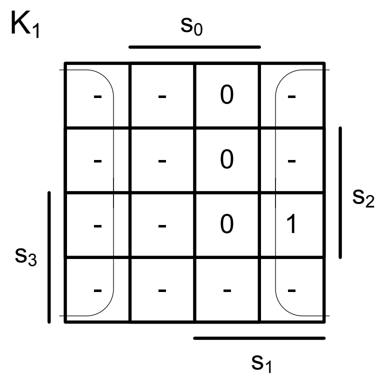
With this table, we can get the following K-maps for J:

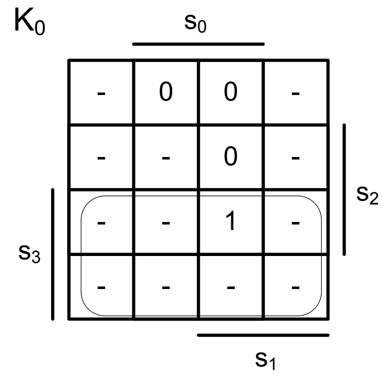


and K:









The switching expressions are:

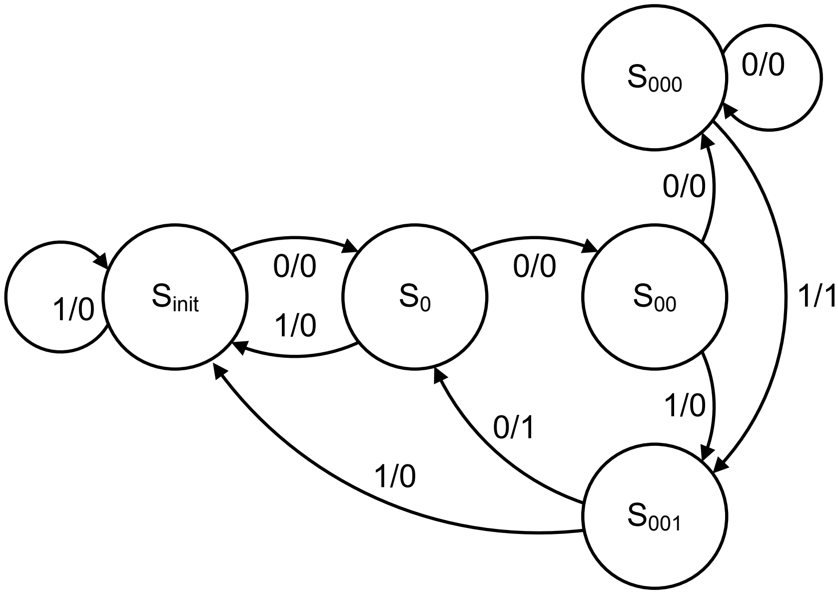
$$
\begin{aligned}
J_3 &= s_2 \\
J_2 &= s_1 \\
J_1 &= s_0 \\
J_0 &= {s_3}' \\
K_3 &= {s_2}' \\
K_2 &= {s_1}' \\
K_1 &= {s_0}' \\
K_0 &= s_3
\end{aligned}
$$

Problem 8 (10 points)

We would like to design a pattern recognizer with a binary stream as input. The system has a binary output bit, which is 1 whenever $x(t-3,t) = 0010$ or 0001 and 0 otherwise.

1. Draw the state transition diagram. Try to minimize the number of states. (*Hint: The system can be designed using only 5 states.*)

   Solution We can create a pattern recognizer by only creating states for the states necessary for identifying the patterns, and simply moving to one of the previous states when it becomes certain that the current string will not match any valid patterns. This gives us the following state diagram.



Alternatively, it is also possible to write a loose state description and do state minimization. It should also give you 5 states.

2. Encode the states into binary bits. From the encoding, write the state transition table and table of JK flip-flop inputs.

Solution Since we have 5 states, we need 3 state bits to represent them all. We shall use the following encoding.

	s_2	s_1	s_0
S_{init}	0	0	0
S_0	0	0	1
S_{00}	0	1	0
S_{000}	0	1	1
S_{001}	1	0	0

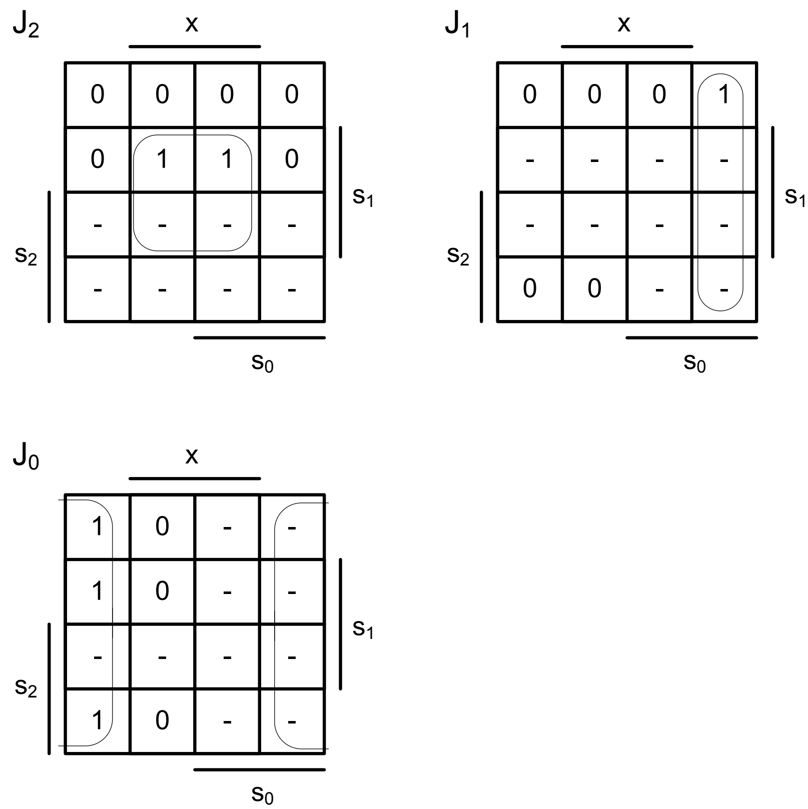
With this encoding we can get the following tables.

PS	NS		JK					
	$x=0$	$x=1$	$x=0$			$x=1$		
000	001,0	000,0	0-	0-	1-	0-	0-	0-
001	010,0	000,0	0-	1-	-1	0-	0-	-1
010	011,0	100,0	0-	-0	1-	1-	-1	0-
011	011,0	100,1	0-	-0	-0	1-	-1	-1
100	001,1	000,0	-1	0-	1-	-1	0-	0-

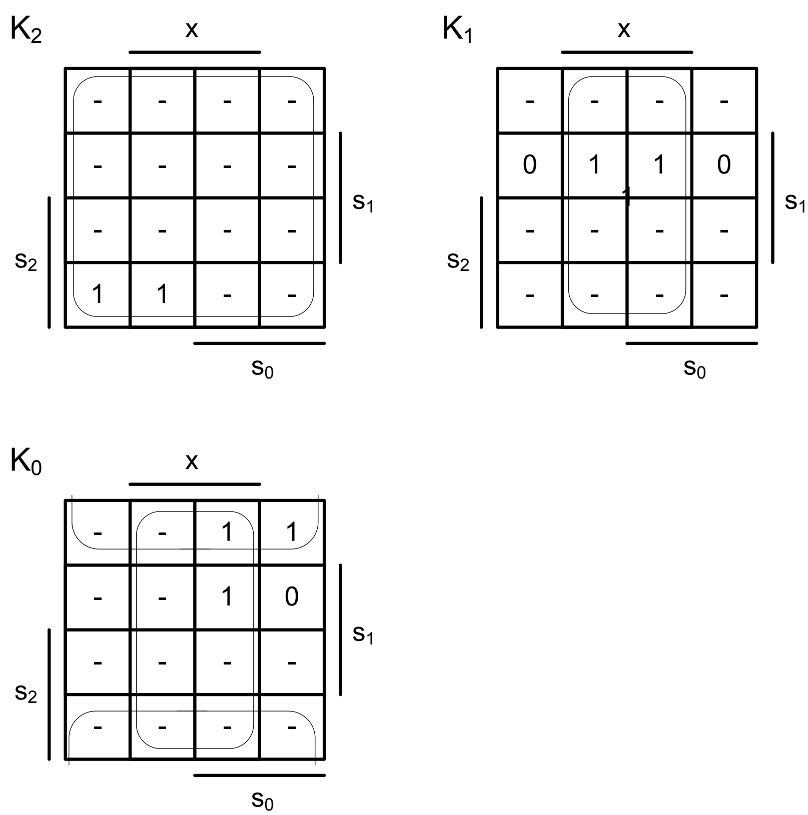
All the items not on the table are don't-cares.

3. Using K-maps, derive the switching expressions for each flip-flop input J_i, K_i, and the output bit z.

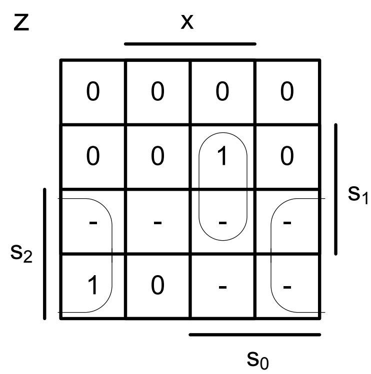
Solution K-maps for Js:


J2
x
s1
s2
s0
J1
x
s1
s2
s0
J0
x
s1
s2
s0

K-maps for Ks:


K2
x
s1
s2
s0
K1
x
s1
s2
s0
K0
x
s1
s2
s0

K-map for z:



The switching expressions are therefore:

$$
\begin{aligned}
J_2 &= xs_1 \\
J_1 &= x's_0 \\
J_0 &= x' \\
K_2 &= 1 \\
K_1 &= x \\
K_0 &= x + s_1' \\
z &= xs_1s_0 + x's_2
\end{aligned}
$$

4. Draw the sequential flip-flop network.

Solution