

[CS M51A FALL 18] HOMEWORK 2

Due: 10/19/18

Homework Problems (60 points total)

Problem 1 (5 Points)

Convert the following expression to Sum of Minterms and Product of Maxterms.

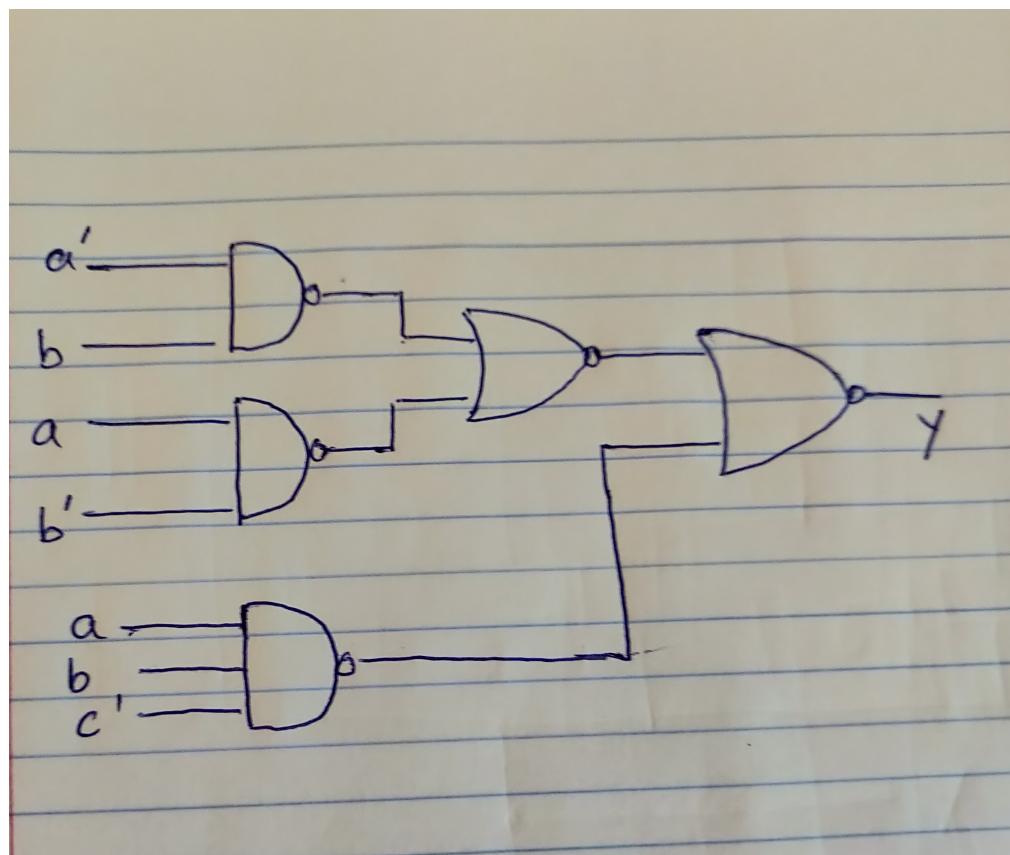
$$\text{Exp} = a + bc' + abc$$

problem 2 (15 points)

Given the expression $a + bc$. Show the expression using CMOS logic using only NAND gates and NOT gates
(Reduce the expression to NAND gate only logic and draw the CMOS diagram)

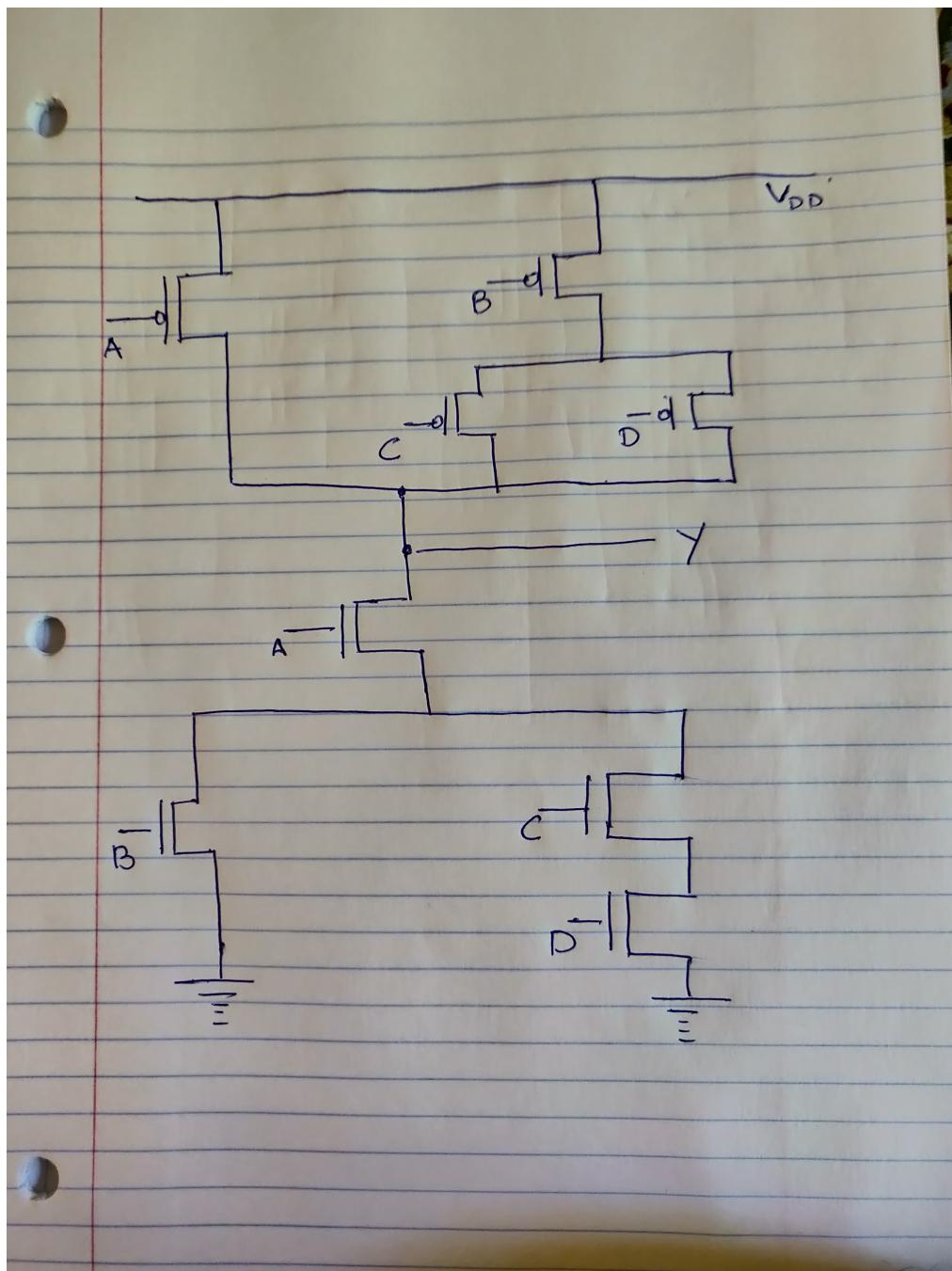
problem 3 (10 points)

Analyze the given gate logic and reduce the expression to sum of minterms form. (Hint: You can reduce the gates to simpler form)



problem 4 (15 points)

1. Analyse the given CMOS logic. Give the function/expression for it. (10 points)



2.Convert the result into SOP products form (5 Points)

problem 5 (15 points)

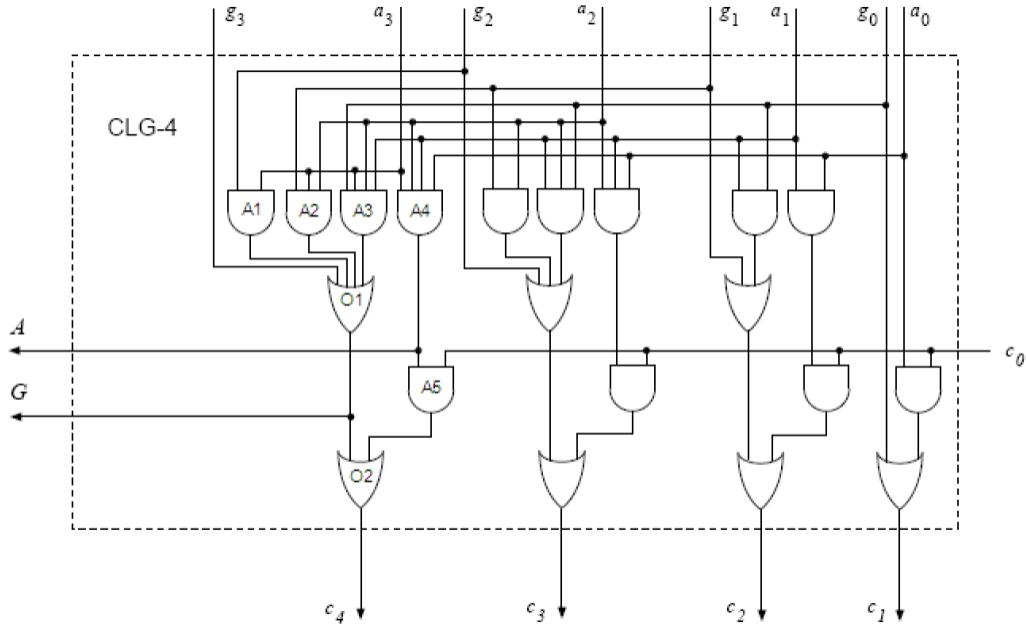
Analyze the following gate network with the output load value information and Table 4.1 from the textbook.

The output load values:

$$L_A = 2.0$$

$$L_G = 6.0$$

$$L_{c_4} = 4.0$$



1. (5 points) Calculate the total load of all the inputs ($g_3 \sim g_0$, $a_3 \sim a_0$, and c_0)

2. (10 points) Of the possible paths, which one likely has the worst case delay to the output signal c_4 ? Find the worst case value of $t_{pHL}(c_4)$?