Problem 1

Minimize the number of states for the following state transition table. Show all the intermediate steps.
Name the new minimized state with the first letter in the group. For example, if a group includes the old states $\{B, D, E\}$, then the name for the new state is B. Also, arrange the rows in the ascending order of state names.

PS	$x = a$	$x = b$	$x = c$
A	G, 1	H, 0	B, 1
B	C, 1	H, 0	B, 1
C	B, 0	D, 1	H, 0
D	C, 1	H, 0	E, 1
E	A, 0	C, 1	E, 0
F	B, 0	D, 1	H, 0
G	A, 0	D, 1	H, 0
H	G, 0	H, 0	F, 1
	NS,z		

Solution:

$$P_1 = (A, B, D), (C, E, F, G), (H)$$

	Group 1			Group 2				Group 3
	A	B	D	C	E	F	G	H
$x = a$	2	2	2	1	1	1	1	2
$x = b$	3	3	3	1	2	1	1	3
$x = c$	1	1	2	3	2	3	3	2

$$P_2 = (A, B), (D), (C, F, G), (E), (H)$$

	Group 1		Group 2	Group 3			Group 4	Group 5
	A	B	D	C	F	G	E	H
$x = a$	3	3	3	1	1	1	1	3
$x = b$	5	5	5	2	2	2	3	5
$x = c$	1	1	4	5	5	5	4	3

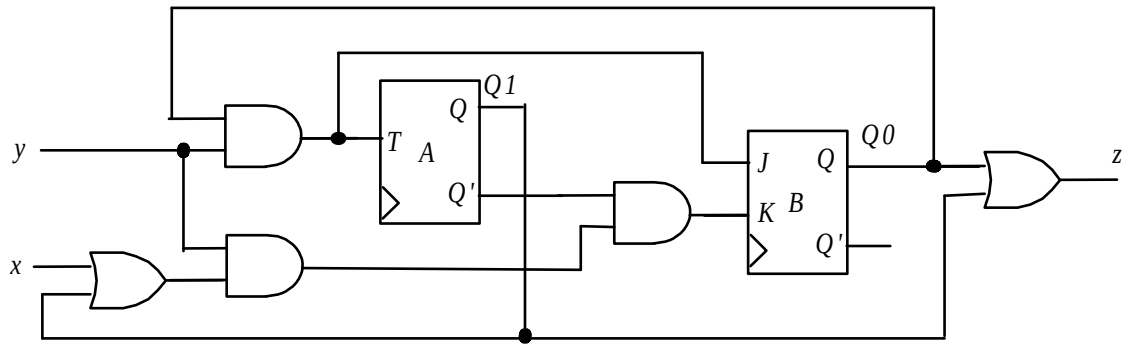
$$\Rightarrow P_3 = (A, B), (D), (C, F, G), (E), (H)$$

Now that $P_3 = P_2$, we stop here. The minimized table is then as follows:

PS	$x = a$	$x = b$	$x = c$
A	C, 1	H, 0	A, 1
C	A, 0	D, 1	H, 0
D	C, 1	H, 0	E, 1
E	A, 0	C, 1	E, 0
H	C, 0	H, 0	C, 1
		NS,z	

Problem 2

Given the following sequential network, complete its state transition table. You can use extra spaces to show your intermediate results.



$Q_1(t)Q_0(t)$	xy			
	00	01	10	11
00				
01				
10				
11				
	$Q_1(t+1)Q_0(t+1)$, z			

Solution: We construct truth tables for control signal T, JK and output z first. Note that $T = yQ_0$, $J = T = yQ_0$, $K = Q_1'y(x + Q_1) = xyQ_1'$, and $z = Q_0 + Q_1$.

$Q_1(t)Q_0(t)$	xy			
	00	01	10	11
00	0	0	0	0
01	0	1	0	1
10	0	0	0	0
11	0	1	0	1
	T			

$Q_1(t)Q_0(t)$	xy			
	00	01	10	11
00	00	00	00	01
01	00	10	00	11
10	00	00	00	00
11	00	10	00	10
	JK			

$Q_1(t)Q_0(t)$	xy			
	00	01	10	11
00	0	0	0	0
01	1	1	1	1
10	1	1	1	1
11	1	1	1	1
	z			

Together with T and JK flip flop's truth table, we have:

$Q_1(t)Q_0(t)$	xy			
	00	01	10	11
00	00,0	00,0	00,0	00,0
01	01,1	11,1	01,1	10,1
10	10,1	10,1	10,1	10,1
11	11,1	01,1	11,1	01,1
	$Q_1(t+1)Q_0(t+1)$, z			

Problem 3

Design a modulo-7 autonomous counter with the following output sequence:

$$0, 1, 2, 3, 6, 5, 4, 0, 1, 2, 3, 6, 5, 4, \cdots$$

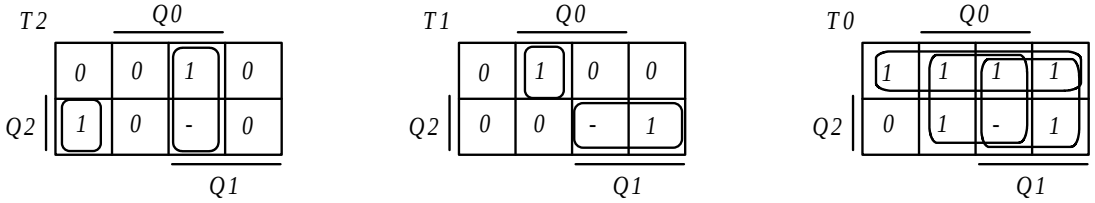
The initial state is 0 and the output of the counter is the current state, i.e. $z(t) = s(t)$.

1. Using the minimum number of T flip-flops and 2 and 3-input NAND gates to implement the counter. You can assume T flip-flops give both complemented and uncomplemented output variables.

2. Implement the above counter using a standard modulo-7 counter, a 3-input decoder and a 8-input encoder. Do not use any additional gates. *Solution:* We need 3 T flip-flops to implement the counter. The truth table for the control signals $T_2T_1T_0$ is as follows (by using T flip flop's excitation function):

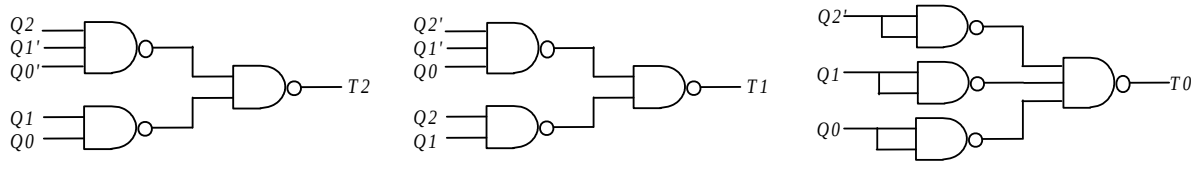
count	$PS(Q_2Q_1Q_0)$	$NS(Q_2Q_1Q_0)/z$	T_2	T_1	T_0
0	000	001	0	0	1
1	001	010	0	1	1
2	010	011	0	0	1
3	011	110	1	0	1
4	100	000	1	0	0
5	101	100	0	0	1
6	110	101	0	1	1
–	111	– – –	–	–	–

   The K-maps for $T_2T_1T_0$ are:



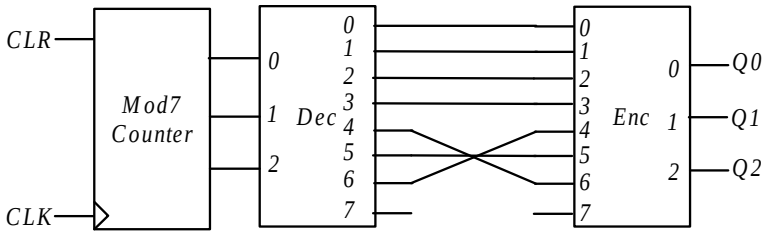
   Therefore the switching expressions are: $T_2 = Q_2Q_1'Q_0' + Q_1Q_0$, $T_1 = Q_2'Q_1'Q_0 + Q_2Q_1$, and $T_0 = Q_2' + Q_1 + Q_0$.

   And finally the combinational nets are:



3. Using a standard modulo-7 counter, a 3-input decoder and a 8-input encoder to implement the above counter. Do not use any additional gates.

Solution:


CLR
CLK
Mod7
Counter
0
1
2
Dec
0
1
2
3
4
5
6
7
0
1
2
3
4
5
6
7
Enc
0
1
2
Q0
Q1
Q2

Problem 4

1. Complete the following table. If you can not put an entry, explain the reason.

Number system	Number of bits	Signed integer x	Representation x_R	Binary vector X
2's compl.	5	-17		
2's compl.	6	-17		
2's compl.	7	-17		
2's compl.	5		17	
2's compl.	6		17	
1's compl.	5		17	
2's compl.	5			01101
2's compl.	6			111100

Solution:

Number system	Number of bits	Signed interger x	Representation x_R	Bit vector X
2's compl.	5	-17	(Not in range)	(Not in range)
2's compl.	6	-17	47	101111
2's compl.	7	-17	111	1101111
2's compl.	5	-15	17	10001
2's compl.	6	17	17	010001
1's compl.	5	-14	17	10001
2's compl.	5	13	13	01101
2's compl.	6	-4	60	111100

2. Compute $z = a - 2b + 2c$ in 2's complement for $a = 5$, $b = 6$, and $c = -13$. Perform calculations on bit-vectors representing a, b, and c and show every step of your work. Using the minimum number of bits to accommodate z without overflow.

   Solution: Since $z = 5 - 2 \times 6 + 2 \times (-13) = -33$, we should at least have 7 bits to represent z in 2's complement system.

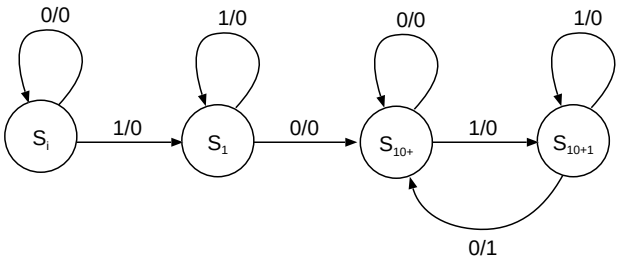
Variable value	Representation	Bit vector
$a = 5$	5	0000101
$b = 6$	6	0000110
$2b = 12$	12	0001100
$-2b = -12$	116	1110100
$c = -13$	115	1110011
$2c = -26$	102	1100110
$z = -33$	95	$0000101 + 1110100 + 1100110 = (1)1011111$

Problem 5

a (6 points) Draw a state diagram for a sequential system which outputs a 1 when it recognizes: a 1 followed by one or more 0s, followed by one or more 1s followed by a 0. Otherwise the system outputs 0. Below are some examples of input/output pairs for this pattern recognizer,

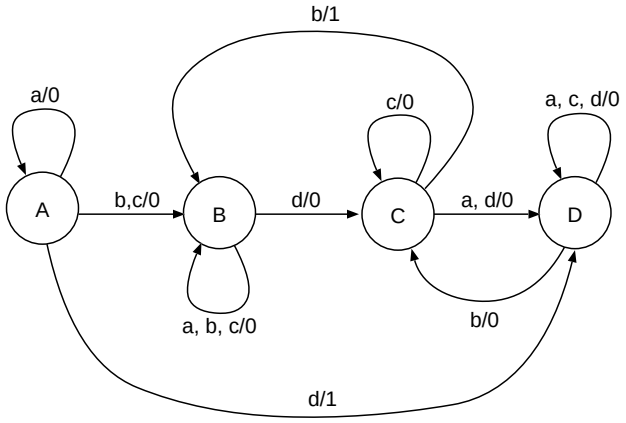
Examples,

- $x(t-5,t) = 110100$
  $z(t-5,t) = 000010$
- $x(t-7,t) = 10001110$
  $z(t-7,t) = 00000001$
- $x(t-9,t) = 1101010101$
  $z(t-9,t) = 0000101010$



b (9 points) Implement the state machine, whose state diagram is shown below, using T flip-flops and NOR gates.

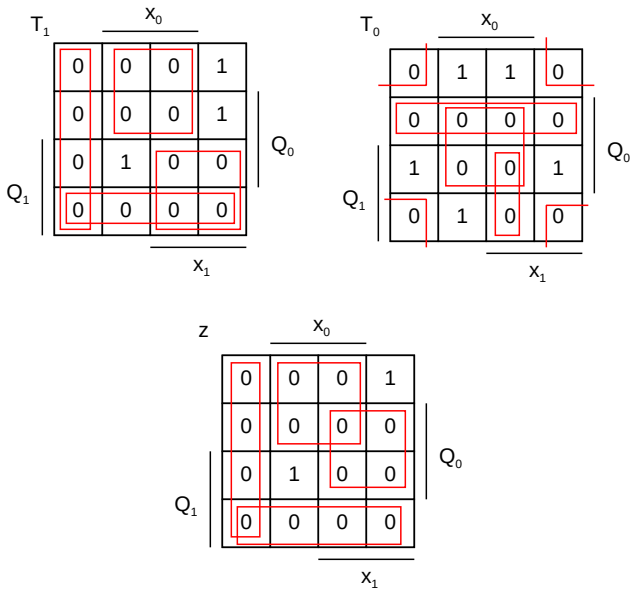
- Use a Gray-code encoding of your states, (i.e., A, B, C, D encoded as $Q_1Q_0 = (00, 01, 11, 10)$ respectively)
- Assume that inputs $x = (a, b, c, d)$ are encoded as $x_1x_0 = (00, 01, 11, 10)$ respectively.
- Assume a variable ordering $f(Q_1, Q_0, x_1, x_0)$ for any switching expressions you derive.
- Assume inverted inputs are available.
- Assume flip-flops provide Q'.
- Minimize combinational networks
- Draw the corresponding gate network.



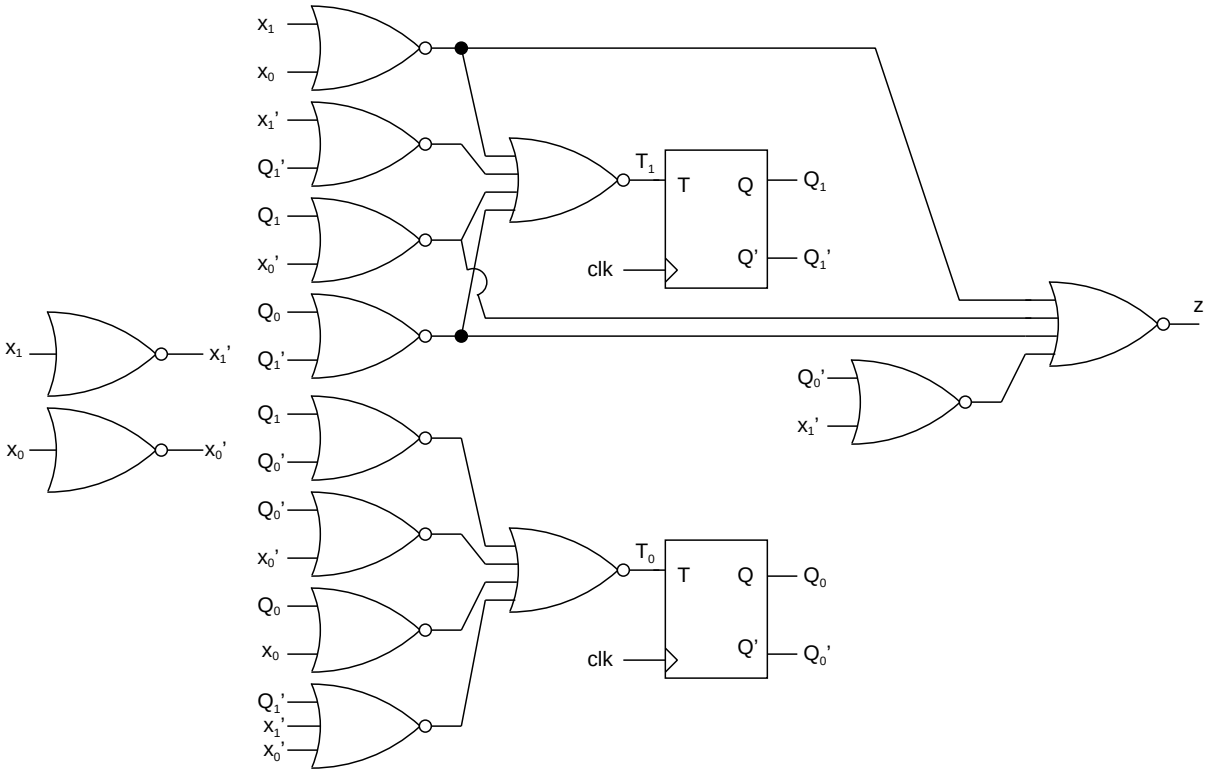
	x			
PS	a	b	c	d
A	$A,0$	$B,0$	$B,0$	$D,1$
B	$B,0$	$B,0$	$B,0$	$C,0$
C	$D,0$	$B,1$	$C,0$	$D,0$
D	$D,0$	$C,0$	$D,0$	$D,0$
	NS, z			

	x_1x_0			
$Q_1(t)Q_0(t)$	00	01	11	10
00	00,0	01,0	01,0	10,1
01	01,0	01,0	01,0	11,0
11	10,0	01,1	11,0	10,0
10	10,0	11,0	10,0	10,0
	$Q_1(t+1)Q_0(t+1), z$			

From these we can determine the switching expressions for T_1, T_0 and z using Karnaugh maps,

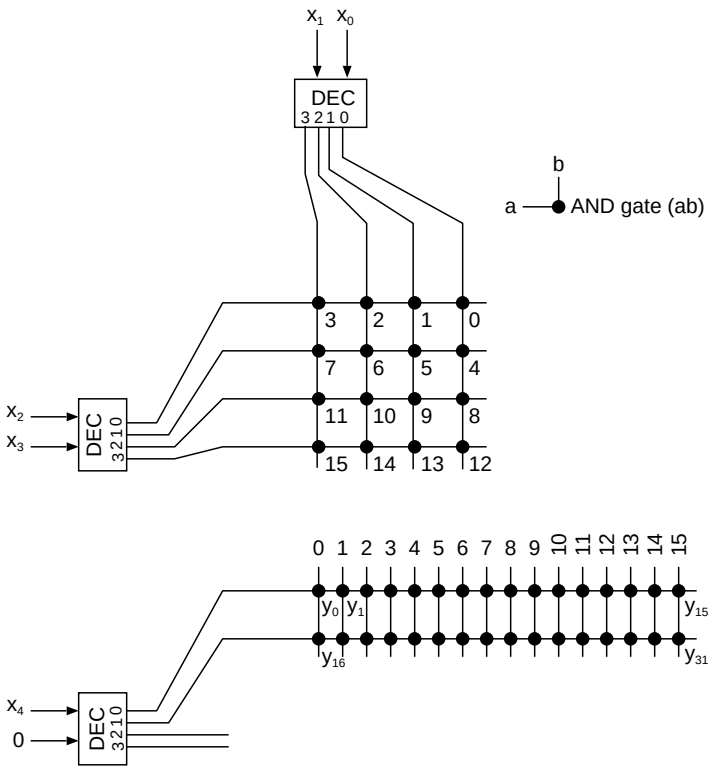


$$T_1 = (x_1 + x_0)(x_1' + Q_1')(Q_1 + x_0')(Q_0 + Q_1')$$
$$T_0 = (Q_1 + Q_0')(Q_0' + x_0')(x_0 + Q_0)(Q_1' + x_1' + x_0')$$
$$z = (Q_1' + Q_0)(x_1 + x_0)(Q_1 + x_0')(Q_0' + x_1')$$



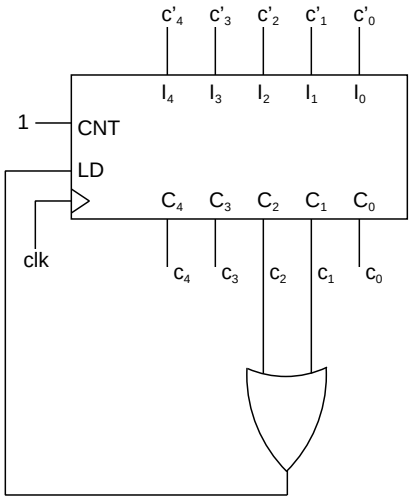
Problem 6

Using a coincident decoder scheme, design a 5-bit decoder module using 2-bit decoder modules and 2-input AND gates.



Problem 7

Show the count sequence for the following counter system, i.e., what will the count output be each clock cycle? Show enough of the sequence such that the pattern is evident. Assume the counter starts at $c_4c_3c_2c_1c_0 = 00000$.



Sequence: **0** (00000), **1** (00001), **2** (00010), **29** (11101), **2** (00010), **29** (11101), ...

Problem 8

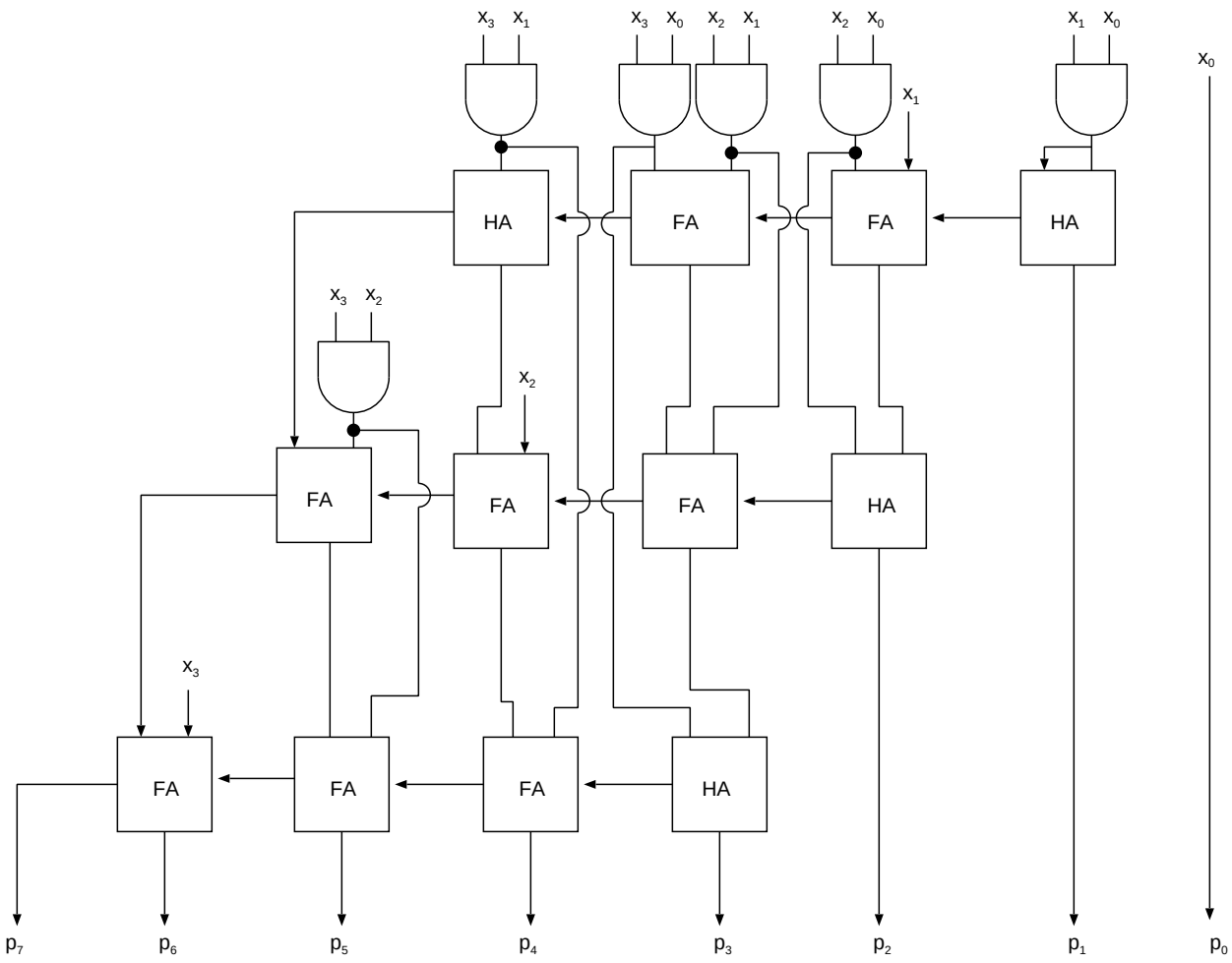
Design a combinational network which produces $z = x^2$, $x = (x_3, x_2, x_1, x_0)$ and $x \geq 0$. You have half-adders, full-adders, and 2-input AND gates available. Assume that the delays are $t_{HA} = 2t$, $t_{FA} = 3t$, and $t_{AND} = t$.

a (1 points) What is the minimum precision of z?

8 bits, $z = (z_7, z_6, \ldots, z_0)$

b (5 points) Show the bit matrix, the network, indicate all connections, and label all signals.

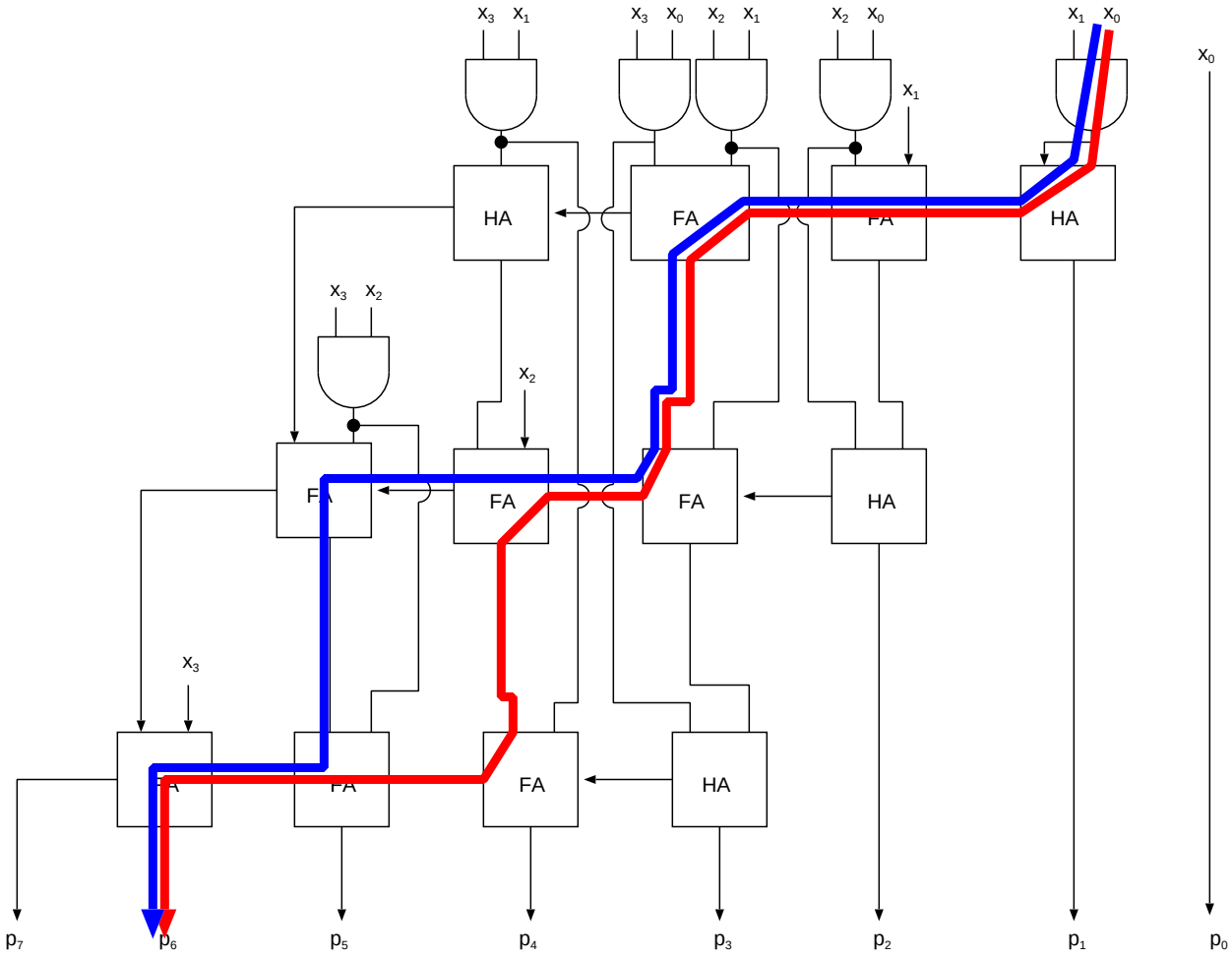
7	6	5	4	3	2	1	0
				x_3x_0	x_2x_0	x_1x_0	x_0
			x_3x_1	x_2x_1	x_1	x_0x_1	
		x_3x_2	x_2	x_1x_2	x_0x_2		
	x_3	x_2x_3	x_1x_3	x_0x_3			



c (2 points) Determine the delay T in the critical path (using the given t_{HA}, t_{FA}, and t_{AND}). Is the critical path unique?

The path is not unique, two are shown.

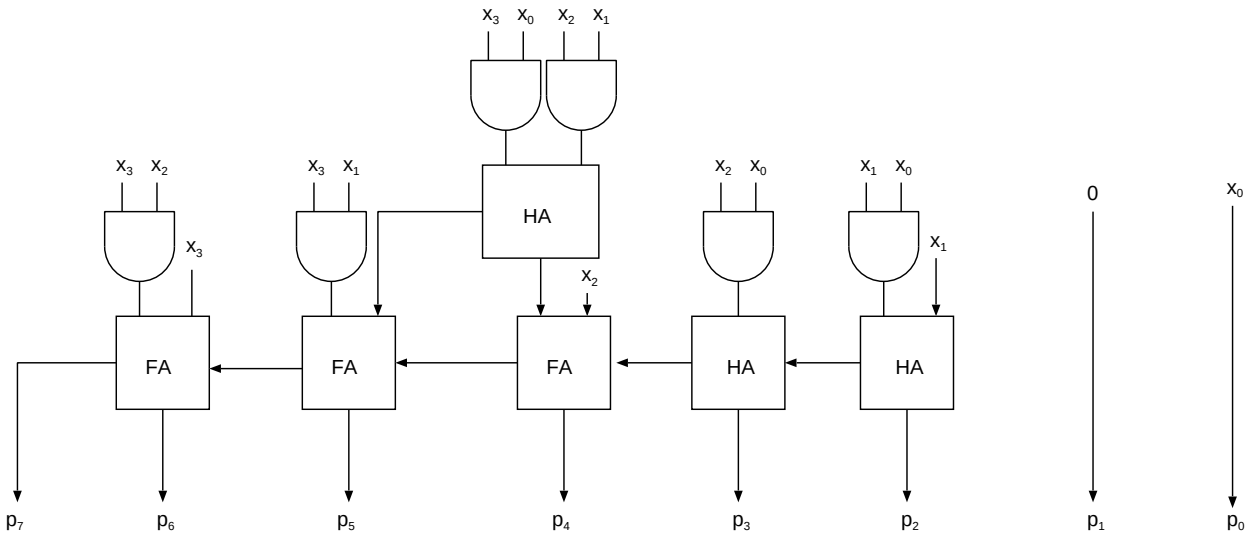
$$T = t_{AND} + t_{HA} + 7t_{FA} = 24t$$



d (7 points) Show how to improve your design so that it uses at most 6 AND gates, 3 half-adders, and 3 full-adders. Draw the corresponding network and determine its critical path delay (using the given t_{HA}, t_{FA}, and t_{AND}).

By observing that $x_i x_j = x_j x_i$ so that $x_i x_j + x_j x_i = 2x_i x_j$ we obtain a reduced bit-matrix after rearranging the row entries

7	6	5	4	3	2	1	0
	x_3x_2	x_3x_1	x_3x_0	x_2x_0	x_1x_0	0	x_0
	x_3		x_2x_1		x_1		
			x_2				



$$T_{improved} = t_{AND} + 2t_{HA} + 3t_{FA} = 14t$$