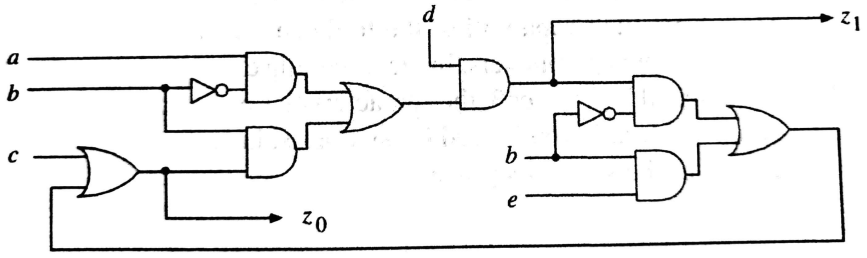
[CS M51A FALL 18] HOMEWORK 3

Due: 10/26/18

Homework Problems (80 points total)

Problem 1 (10 Points)

Show that the network in the figure below is combinational even though there is a physical loop.



Problem 2 (10 points)

For the following tabular description of a network, give its graphical description and determine whether the network is valid. If not valid, make modifications on the description so that it is valid.

From	To
R	A_1
S	A_2
A	B_1
A_2	C_1
T	C_2
X	C_3
C	D_1
Y	D_2
B	E_1
D	E_2
E	Z

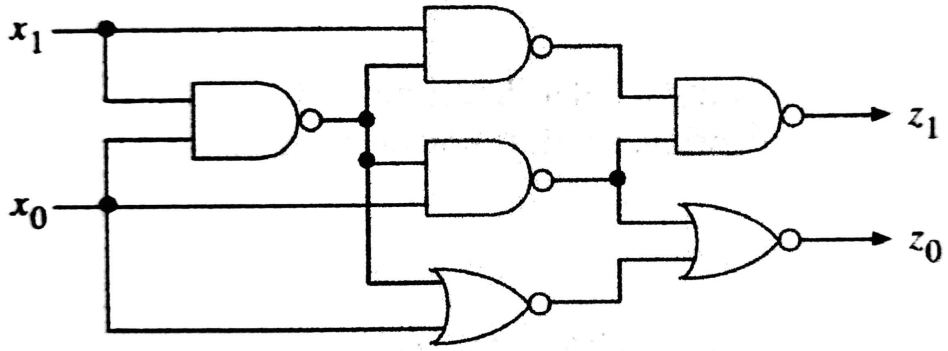
Gate	Type	Input	Output
A	AND2	A_1	A
		A_2	
B	NOT	B_1	B
C	AND3	C_1	C
		C_2	
		C_3	
D	OR2	D_1	D
		D_2	
E	OR2	E_1	E
		E_2	

Problem 3 (10 points)

Show that the set {XNOR,OR} is universal. You can use constant 0 or 1 (only one of them).

Problem 4 (10 points)

Analyze the NAND-NOR network shown in the figure below. Obtain switching expressions for the outputs.



Problem 5 (40 points)

Analyze the network as shown in the figure below. Obtain:

a. Switching expressions for each of the outputs.
b. A high-level description assuming that the bit-vector $\underline{s} = (s_2, s_1, s_0)$ represents an integer in the radix-2 representation.
c. For the gate characteristics given in Table 4.1, determine (decompose the gates not available in the table):

- the load factor of each input;
- the load for each gate output; and
- the delay of the network. Give this delay in terms of the load of the output.

d. Give a timing diagram showing the delays in the critical path.