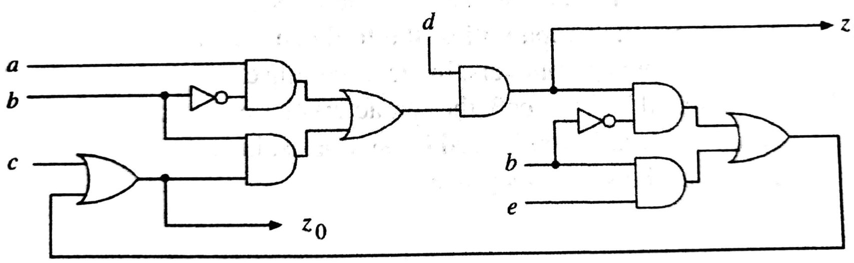
[CS M51A FALL 18] Solution to HOMEWORK 3

Due: 10/26/18

Homework Problems (80 points total)

Problem 1 (10 Points)

Show that the network in the figure below is combinational even though there is a physical loop.



Solution

z_1' = value of z_1 at a prev. point

$z_0 = z_1'\bar{b} + be + c$

$z_1 = (a\bar{b} + bz_0)d$

Replacing z_0 in z_1

$z_1 = [a\bar{b} + b(z_1'\bar{b} + be + c)]\, d$

$z_1 = [a\bar{b} + (\underline{\underline{b\bar{b}}}z_1' + be + bc)]\, d$

$z_1 = [a\bar{b} + 0 + be + be]\, d$

Hence z_1 does not depend on previous value of itself (or any other previous)

Hence, combinational

[$\because$ b interrupts the loop basically]

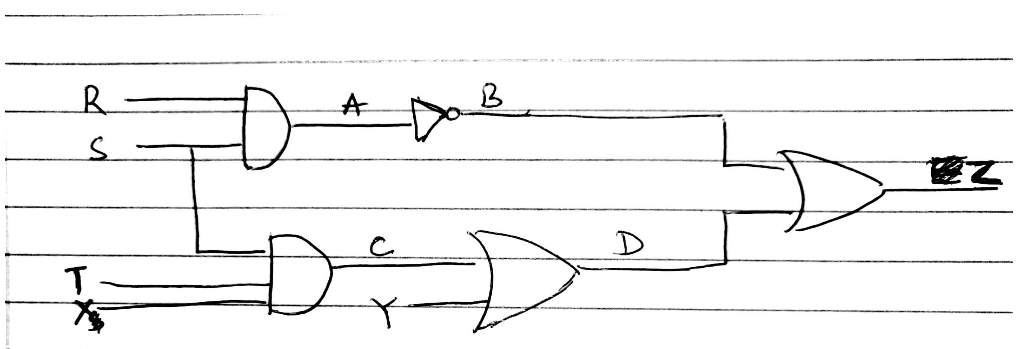
Problem 2 (10 points)

For the following tabular description of a network, give its graphical description and determine whether the network is valid. If not valid, make modifications on the description so that it is valid.

From	To
R	A_1
S	A_2
A	B_1
A_2	C_1
T	C_2
X	C_3
C	D_1
Y	D_2
B	E_1
D	E_2
E	Z

Gate	Type	Input	Output
A	AND2	A_1	A
		A_2	
B	NOT	B_1	B
C	AND3	C_1	C
		C_2	
		C_3	
D	OR2	D_1	D
		D_2	
E	OR2	E_1	E
		E_2	

Solution



The network is valid.

Problem 3 (10 points)

Show that the set {XNOR,OR} is universal. You can use constant 0 or 1 (only one of them).

Solution

If we show that NOT can be realized, then since {OR,NOT} is universal, we can say that {XNOR,OR} is universal.

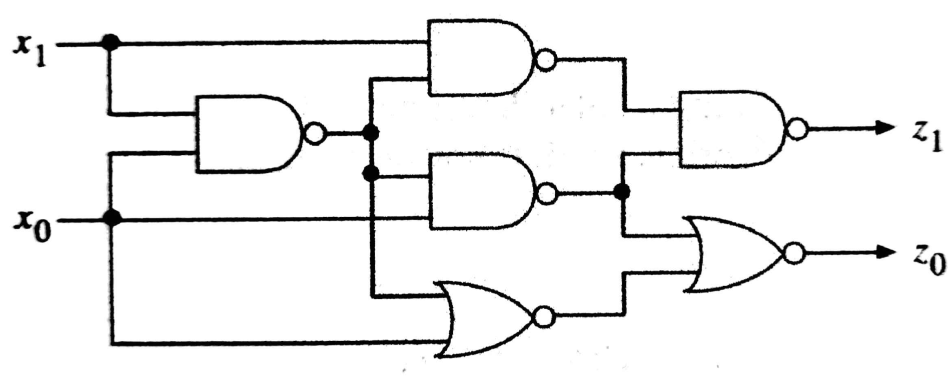
$$XNOR(x, y) = xy + x'y'$$

Since we can use the constant 0, it is clear that:

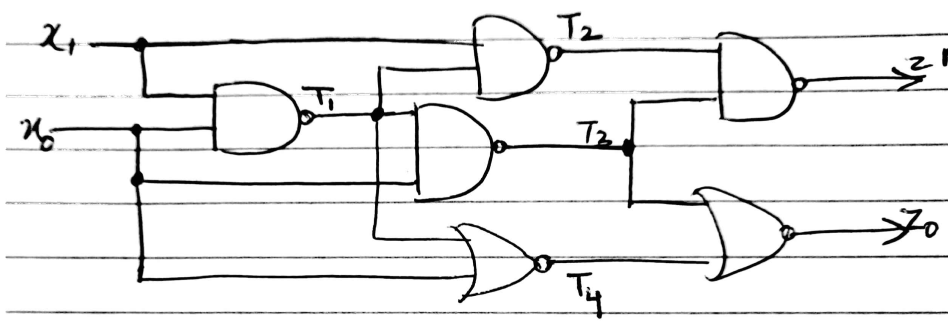
$$NOT(x) = XNOR(x, 0) = x.0 + x'.1 = x'$$

Problem 4 (10 points)

1.Analyze the NAND-NOR network shown in the figure below. Obtain switching expressions for the outputs.



Solution



$$
\begin{aligned}
Z_0 &= (T_3 + T_4)' \\
&= \left((x_0 T_1)' + (T_1 + x_0)'\right)' \\
&= (x_0' + T_1' + T_1' x_0')' \\
&= (x_0' + T_1')' \\
&= \left(x_0' + ((x_0 x_1)')'\right)' \\
&= (x_0' + x_0 x_1)' \\
&= x_0 (x_0' + x_1') \\
&= x_0 x_1'
\end{aligned}
$$

$$
\begin{aligned}
Z_1 &= (T_2 T_3)' \\
&= ((x_1 T_1)'(T_1 x_0)')' \\
&= x_1 T_1 + x_0 T_1 \\
&= (x_0 x_1)'(x_0 + x_1) \\
&= (x_0' + x_1')(x_0 + x_1) \\
&= x_0' x_1 + x_1' x_0 \\
&= x_0 \oplus x_1
\end{aligned}
$$

Can be done using mixed logic also. Will be simpler that way.

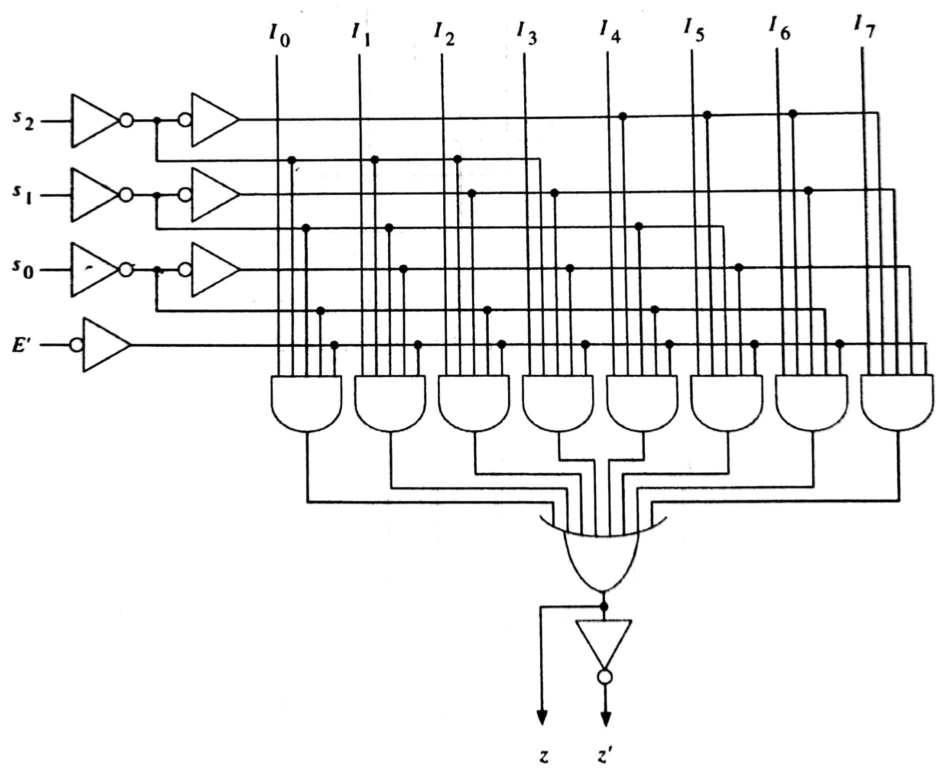
Problem 5 (40 points)

Analyze the network as shown in the figure below. Obtain:

a. Switching expressions for each of the outputs.
b. A high-level description assuming that the bit-vector $\underline{s} = (s_2, s_1, s_0)$ represents an integer in the radix-2 representation.
c. For the gate characteristics given in Table 4.1, determine (decompose the gates not available in the table):

- the load factor of each input;
- the load for each gate output; and
- the delay of the network. Give this delay in terms of the load of the output.

d. Give a timing diagram showing the delays in the critical path.



Solution a. The switching expression for output z is:

$$z = E(I_0 s_2' s_1' s_0' + I_1 s_2' s_1' s_0 + I_2 s_2' s_1 s_0' + I_3 s_2' s_1 s_0 + I_4 s_2 s_1' s_0' + I_5 s_2 s_1' s_0 + I_6 s_2 s_1 s_0' + I_7 s_2 s_1 s_0)$$

b. If n is the decimal representation of $\{s_2, s_1, s_0\}, then: If E = 1, z = I_n$
Else 0.
It is kind of like a 8 X 1 selector.
c. The load factor of each input is 1, since each input is connected to only one gate input.
Load for NOT connected to $E' = 8$
Load for first NOT gates connected to $s_i = 5$
Load for second NOT gates = 4
Load for AND gates = 1
Load for OR gate = L1 + 1
where L1 is load on output z

Load for last NOT gate = L2
where L2 is the Load on the output z'
For delay:

$$AND(x_4, x_3, x_2, x_1, x_0) = AND(AND(x_4, x_3, x_2), AND(x_1, x_0))$$

and

$$OR(x_7, x_6, \ldots, x_1, x_0) = OR(OR(x_7, x_6, x_5, x_4), OR(x_3, x_2, x_1, x_0)$$

Let :

$$\begin{aligned}
t_{pLH}(\text{AND-5}) &= T_1 \\
t_{pHL}(\text{AND-5}) &= T_2 \\
t_{pLH}(\text{OR-8}) &= T_3 \\
t_{pHL}(\text{OR-8}) &= T_4
\end{aligned}$$

Then :

$$\begin{aligned}
T_1 &= t_{pLH}(\text{AND-3}) + t_{pLH}(\text{AND-2}) = 0.2 + 0.038 + 0.15 + 0.037 = 0.43 \\
T_2 &= t_{pHL}(\text{AND-3}) + t_{pHL}(\text{AND-2}) = 0.18 + 0.018 + 0.16 + 0.017 = 0.38 \\
T_3 &= t_{pLH}(\text{OR-4}) + t_{pLH}(\text{OR-2}) = 0.13 + 0.038 + 0.12 + 0.037(L_1 + 1) = 0.33 + 0.037L_1 \\
T_4 &= t_{pHL}(\text{OR-4}) + t_{pHL}(\text{OR-2}) = 0.45 + 0.025 + 0.2 + 0.019(L_1 + 1) = 0.69 + 0.019L_1
\end{aligned}$$

The critical path delay is:

$$\begin{aligned}
t_{pLH}(s_2, z') &= t_{pLH}(\text{NOT}) + t_{pHL}(\text{NOT}) + t_{pHL}(\text{AND-5}) + t_{pHL}(\text{OR-8}) + t_{pLH}(\text{NOT}) \\
&= 0.02 + 0.038 \times 5 + 0.05 + 0.017 \times 4 + T_2 + T_4 + 0.02 + 0.038 \times L_2 \\
&= 0.35 + T_2 + T_4 + 0.038 \times L_2 \\
t_{pHL}(s_2, z') &= t_{pHL}(\text{NOT}) + t_{pLH}(\text{NOT}) + t_{pLH}(\text{AND-5}) + t_{pLH}(\text{OR-8}) + t_{pHL}(\text{NOT}) \\
&= 0.05 + 0.017 \times 5 + 0.02 + 0.038 \times 4 + T_1 + T_3 + 0.05 + 0.017 \times L_2 \\
&= 0.36 + T_1 + T_3 + 0.017 \times L_2
\end{aligned}$$

d.