# [CS M51A FALL 18] Solution to HOMEWORK 2

Due: 10/19/18

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## Homework Problems (60 points total)

### Problem 1 (5 Points)

Convert the following expression to Sum of Minterms and Product of Maxterms.

$$\text{Exp} = \text{a} + \text{bc'} + \text{abc}$$

***Solution***

Exp = a + bc' + abc
a = a(b+b')(c+c')
bc' = bc'(a+a')
So exp becomes:
= abc + ab'c' + abc' + ab'c + abc + abc' + a'bc'
= abc + ab'c' + abc' + ab'c + a'bc'
= $\text{m}_7 + m_4 + m_6 + m_5 + m_2$
= $\sum (2, 4, 5, 6, 7) = \prod (0, 1, 3)$

**problem 2 (15 points)**

Given the expression a + bc. Show the expression using CMOS logic using only NAND gates and NOT gates (Reduce the expression to NAND gate only logic and draw the CMOS diagram)

***Solution***

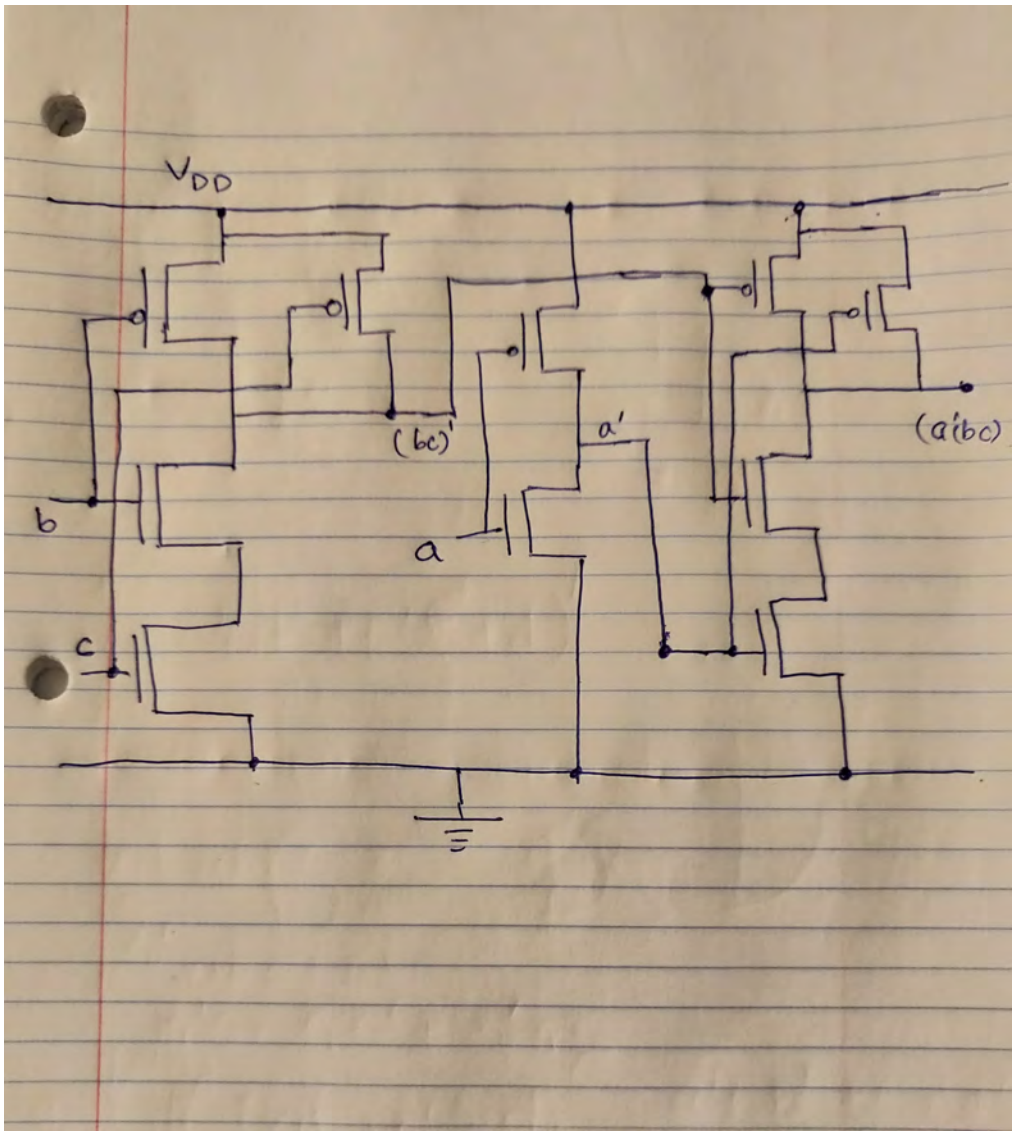
The given expression a + bc reduces to NAND only logic in the following way:

a + bc

= (a')' + ((bc)')'

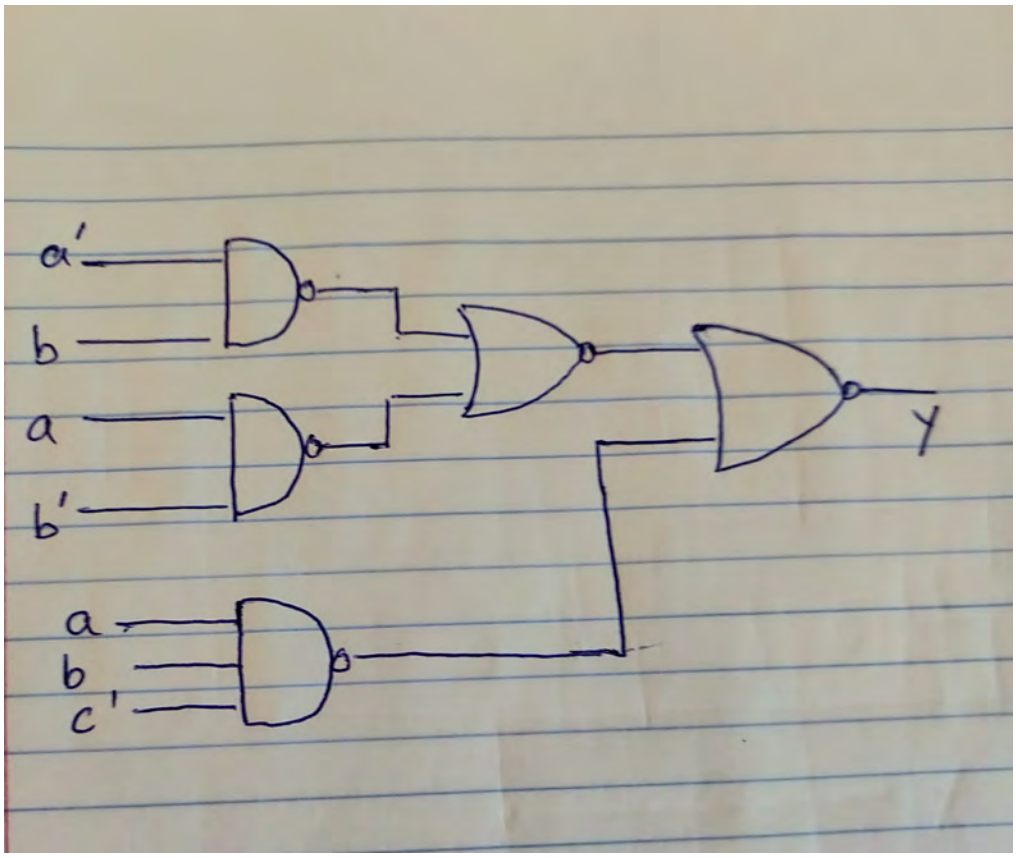
= (a'(bc)')'

The CMOS logic Diagram for the above expression would be:

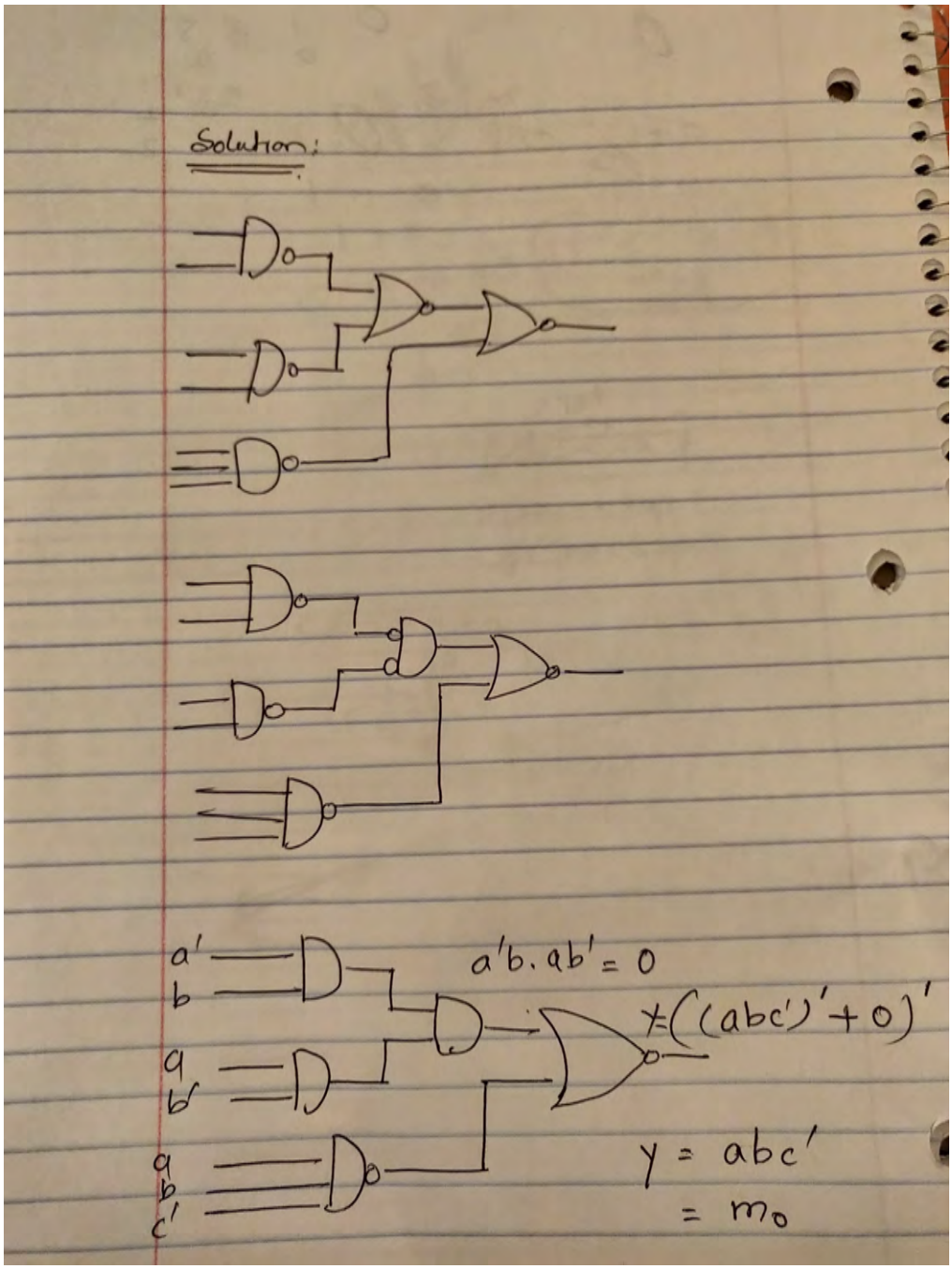


**problem 3 (10 points)**

Analyze the given gate logic and reduce the expression to sum of minterms form. (Hint: You can reduce the gates to simpler form)

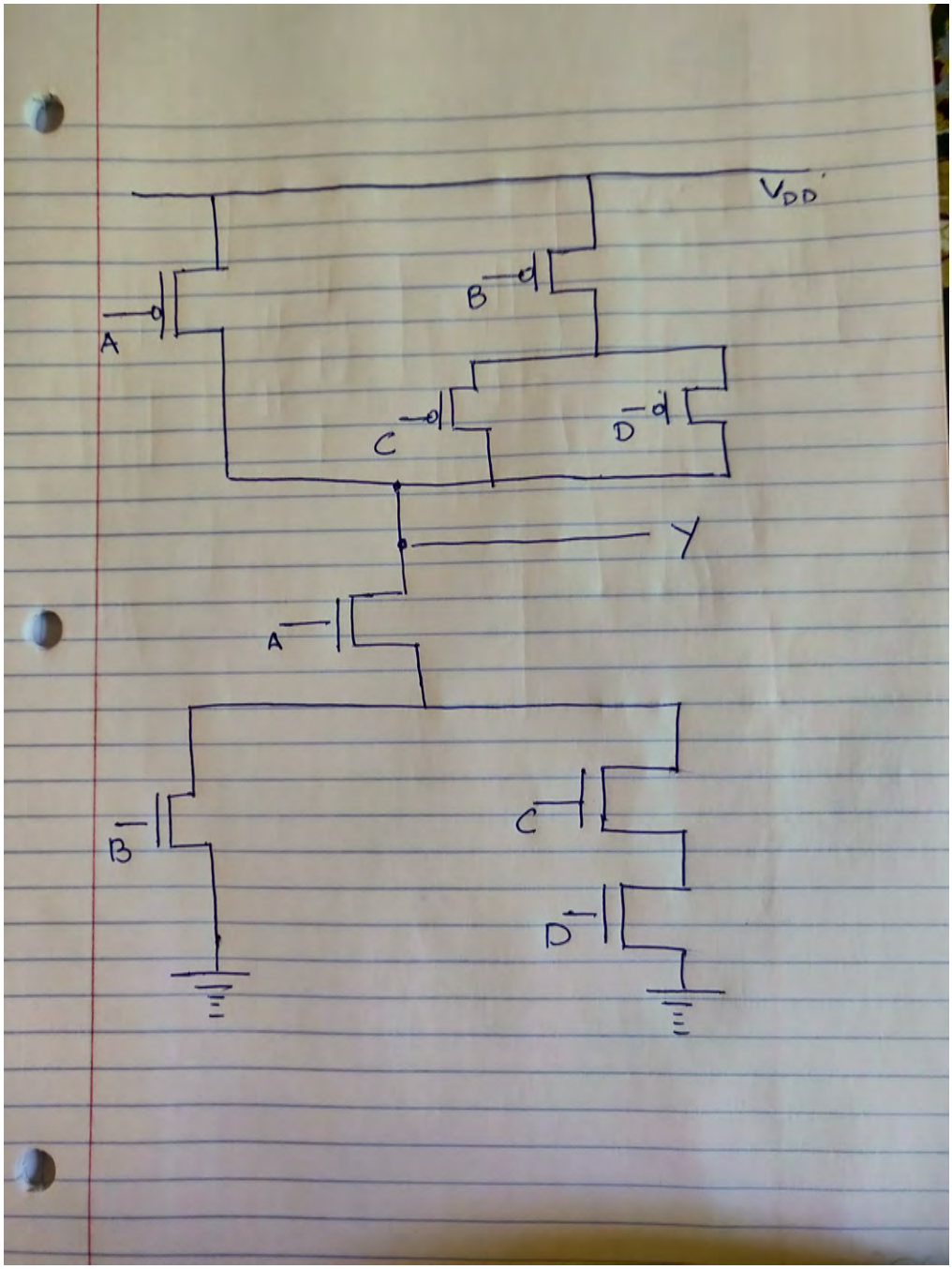


***Solution***



**problem 4 (15 points)**

1.Analyse the given CMOS logic. Give the function/expression for it. (10 points)




***Solution***

The CMOS circuit is a NAND logic since has the same NMOS in Series and it PMOS in Parallel.
So we can find the expresion would be of the form (xy)'
It is evident that x = A
For y, in the NMOS, C and D in series making it CD parallel with B making y = B + CD
So the circuit becomes (A(B+CD))'

2.Convert the result into SOP products form (5 Points)

***Solution***

By Applying DeMorgan's, we get:

(A(B+CD))'

=A' + (B+CD)'

=A' + B'.(CD)'

=A' + B'.(C'+D')

=A' + B'C' + B'D'

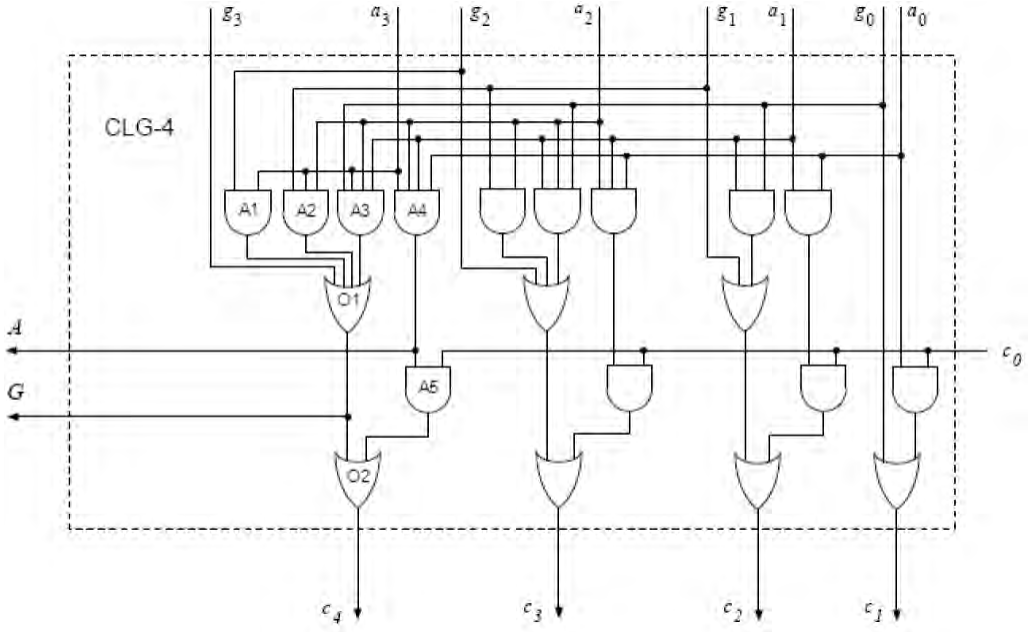
Since each term in the last expression is a product term. This is the final SOP form.

**problem 5 (15 points)**

Analyze the following gate network with the output load value information and Table 4.1 from the textbook.

The output load values:

$$L_A = 2.0$$
$$L_G = 6.0$$
$$L_{c_4} = 4.0$$




1. (5 points) Calculate the total load of all the inputs ($g_3 \sim g_0$, $a_3 \sim a_0$, and $c_0$)

***Solution*** All gates in the gate network have its load factor value at 1.0. Thus, calculating the total load of an input is equivalent to counting the number of gates it drives.

The load values are ($g_3 \sim g_0$, $a_3 \sim a_0$, and $c_0$): 1, 2, 3, 4, 4, 6, 6, 4, 4

2. (10 points) Of the possible paths, which one likely has the worst case delay to the output signal $c_4$? Find the worst case value of $t_{pHL}(c_4)$?

***Solution*** Looking at the circuit, the path with the worst delay would be either $A4 \rightarrow A5 \rightarrow O2$ or $A4 \rightarrow O1 \rightarrow O2$. The two gates, $A2$ and $A1$, have fewer inputs and equal or less load, thus the paths that go though these gates will be faster than the ones going through $A3$ or $A4$, and therefore do not need to be considered.

We calculate the delay of these two paths and compare them to find the worst case value of $t_{pLH}$. The total load values we need are $L_{A3} = 1$, $L_{A4} = L_A + 1 = 3$, $L_{O1} = L_G + 1 = 7$, $L_{A5} = 1$ and $L_{O2} = L_{c_4} = 4$.

$$\begin{aligned} t_{pHL}(c_4) &= t_{pHL}(O2) + t_{pHL}(A5) + t_{pHL}(A4) \\ &\text{or} \quad t_{pHL}(O2) + t_{pHL}(O1) + t_{pHL}(A3) \end{aligned}$$

$$\begin{aligned} & t_{pHL}(O2) + t_{pHL}(A5) + t_{pHL}(A4) \\ = \; & 0.20 + 0.019L_{O2} + 0.16 + 0.017L_{A5} + 0.21 + 0.019L_{A4} \\ = \; & 0.21 + 0.019 \cdot 4 + 0.16 + 0.017 + 0.20 + 0.019 \cdot 3 \\ = \; & 0.72 \text{ (ns)} \end{aligned}$$

$$\begin{aligned} & t_{pHL}(O2) + t_{pHL}(O1) + t_{pHL}(A3) \\ = \; & 0.20 + 0.019L_{O2} + 0.45 + 0.025L_{O1} + 0.21 + 0.019L_{A3} \\ = \; & 0.20 + 0.019 \cdot 4 + 0.45 + 0.025 \cdot 7 + 0.21 + 0.019 \\ = \; & 1.13 \text{ (ns)} \end{aligned}$$

We can see that the second path is the slower of the two. The worst $t_{pHL}$ delay path to $c_4$ is $A3 \rightarrow O1 \rightarrow O2$ and the delay value is 1.13 ns.