

Problem 1

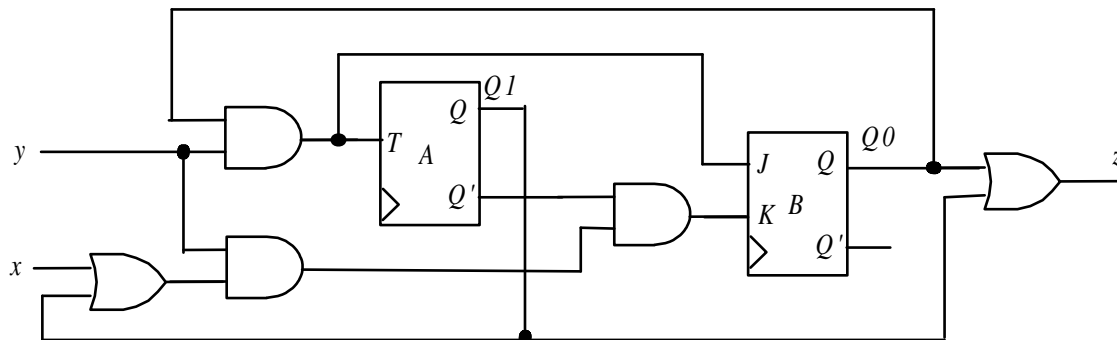
Minimize the number of states for the following state transition table. Show all the intermediate steps.

Name the new minimized state with the first letter in the group. For example, if a group includes the old states $\{B, D, E\}$, then the name for the new state is B . Also, arrange the rows in the ascending order of state names.

PS	$x = a$	$x = b$	$x = c$
A	$G, 1$	$H, 0$	$B, 1$
B	$C, 1$	$H, 0$	$B, 1$
C	$B, 0$	$D, 1$	$H, 0$
D	$C, 1$	$H, 0$	$E, 1$
E	$A, 0$	$C, 1$	$E, 0$
F	$B, 0$	$D, 1$	$H, 0$
G	$A, 0$	$D, 1$	$H, 0$
H	$G, 0$	$H, 0$	$F, 1$
	NS,z		

Problem 2

Given the following sequential network, complete its state transition table. You can use extra spaces to show your intermediate results.



$Q_1(t)Q_0(t)$	xy			
	00	01	10	11
00				
01				
10				
11				
	$Q_1(t+1)Q_0(t+1), z$			

Problem 3

Design a modulo-7 autonomous counter with the following output sequence:

$$0, 1, 2, 3, 6, 5, 4, 0, 1, 2, 3, 6, 5, 4, \dots$$

The initial state is 0 and the output of the counter is the current state, i.e. $z(t) = s(t)$.

1. Using the minimum number of T flip-flops and 2 and 3-input NAND gates to implement the counter. You can assume T flip-flops give both complemented and uncomplemented output variables.
2. Implement the above counter using a standard modulo-7 counter, a 3-input decoder and a 8-input encoder. Do not use any additional gates.

Problem 4

1. Complete the following table. If you can not put an entry, explain the reason.

Number system	Number of bits	Signed integer x	Representation x_R	Binary vector X
2's compl.	5	-17		
2's compl.	6	-17		
2's compl.	7	-17		
2's compl.	5		17	
2's compl.	6		17	
1's compl.	5		17	
2's compl.	5			01101
2's compl.	6			111100

2. Compute $z = a - 2b + 2c$ in 2's complement for $a = 5$, $b = 6$, and $c = -13$. Perform calculations on bit-vectors representing a , b , and c and show every step of your work. Using the minimum number of bits to accommodate z without overflow.

Problem 5

- a (6 points)** Draw a state diagram for a sequential system which outputs a 1 when it recognizes: a 1 followed by one or more 0s, followed by one or more 1s followed by a 0. Otherwise the system outputs 0. Below are some examples of input/output pairs for this pattern recognizer,

Examples,

•

$$x(t-5, t) = 110100$$

$$z(t-5, t) = 000010$$

•

$$x(t-7, t) = 10001110$$

$$z(t-7, t) = 00000001$$

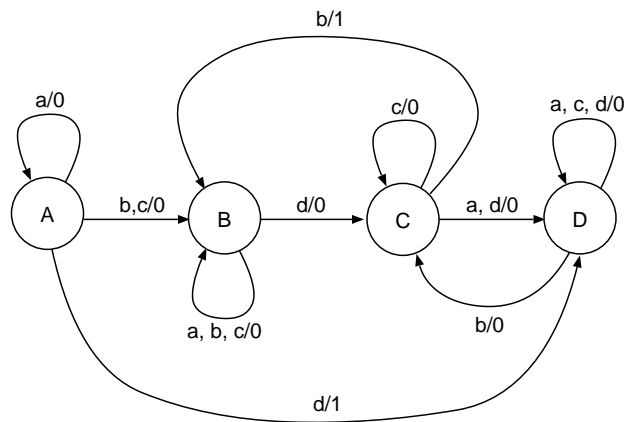
•

$$x(t-9, t) = 1101010101$$

$$z(t-9, t) = 0000101010$$

b (9 points) Implement the state machine, whose state diagram is shown below, using T flip-flops and NOR gates.

- Use a Gray-code encoding of your states, (i.e., A, B, C, D encoded as $Q_1Q_0 = (00, 01, 11, 10)$ respectively)
- Assume that inputs $x = (a, b, c, d)$ are encoded as $x_1x_0 = (00, 01, 11, 10)$ respectively.
- Assume a variable ordering $f(Q_1, Q_0, x_1, x_0)$ for any switching expressions you derive.
- Assume inverted inputs are available.
- Assume flip-flops provide Q' .
- Minimize combinational networks
- Draw the corresponding gate network.



Populate the state transition table given below,

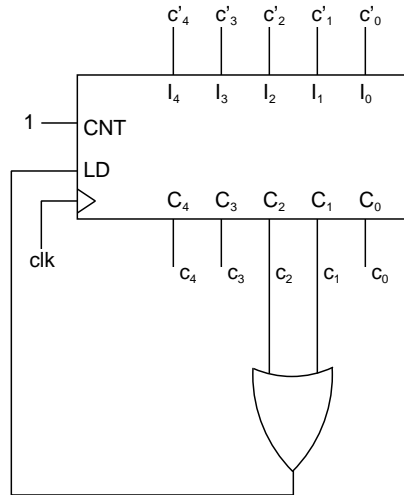
	x			
PS	a	b	c	d
A				
B				
C				
D				
	NS, z			

Problem 6

Using a coincident decoder scheme, design a 5-bit decoder module using 2-bit decoder modules and 2-input AND gates.

Problem 7

Show the count sequence for the following counter system, i.e., what will the count output be each clock cycle? Show enough of the sequence such that the pattern is evident. Assume the counter starts at $c_4c_3c_2c_1c_0 = 00000$.



Problem 8

Design a combinational network which produces $z = x^2$, $x = (x_3, x_2, x_1, x_0)$ and $x \geq 0$. You have half-adders, full-adders, and 2-input AND gates available. Assume that the delays are $t_{HA} = 2t$, $t_{FA} = 3t$, and $t_{AND} = t$.

a (1 points) What is the minimum precision of z ?

b (5 points) Show the bit matrix, the network, indicate all connections, and label all signals.

c (2 points) Determine the delay T in the critical path (using the given t_{HA} , t_{FA} , and t_{AND}). Is the critical path unique?

d (7 points) Show how to improve your design so that it uses at most 6 AND gates, 3 half-adders, and 3 full-adders. Draw the corresponding network and determine its critical path delay (using the given t_{HA} , t_{FA} , and t_{AND}).