NutsBoard
Pistachio Single Board Computer
Hardware Manual

Rev 1.1 09212017

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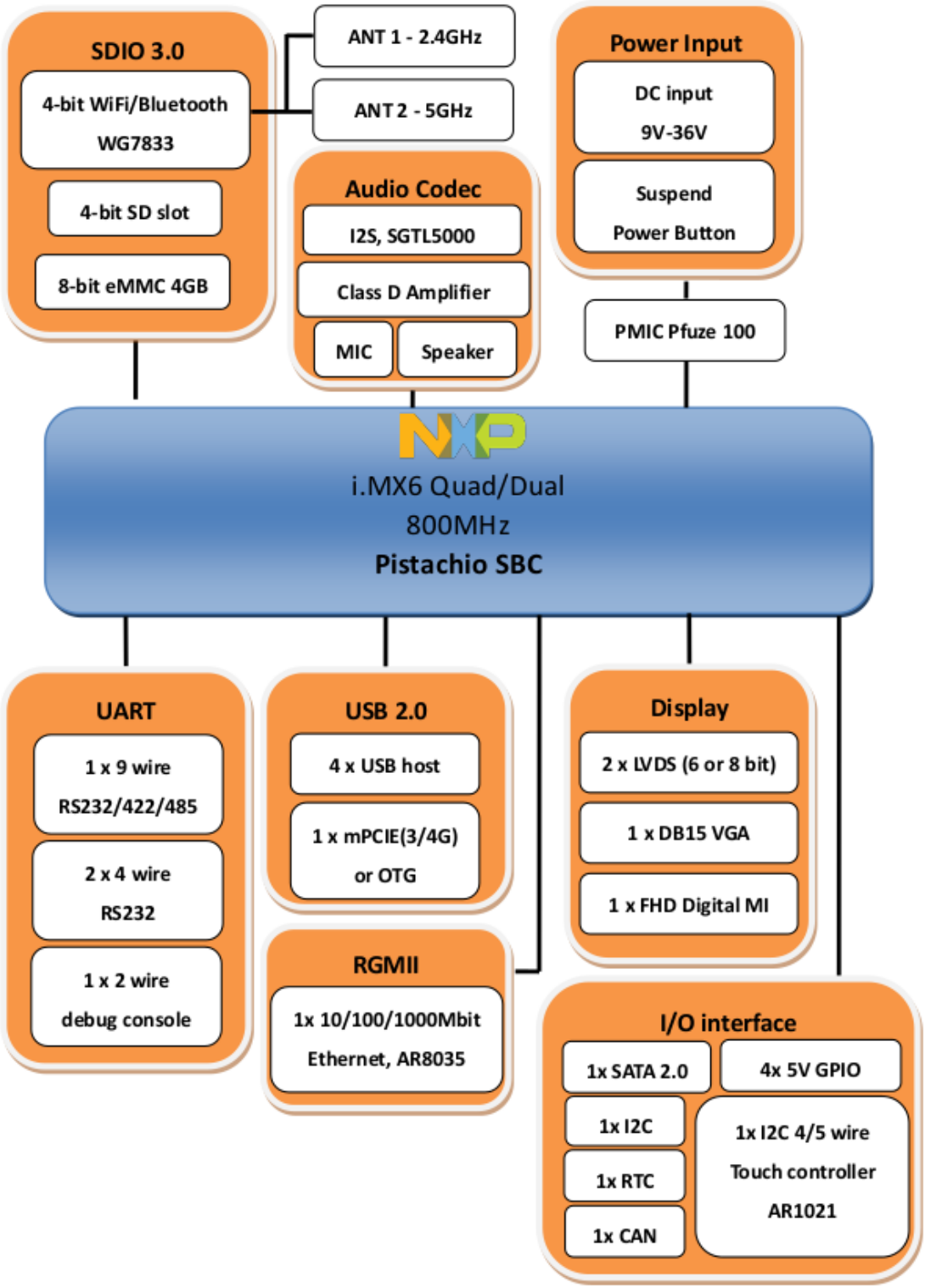
Revision History

Revision	Date	Author	Description
V1.0	05/25/2017	Victor	First Release
V1.1	08/15/2017	Wig	Change to NutsBoard style

Contents

1. Pistachio Overview

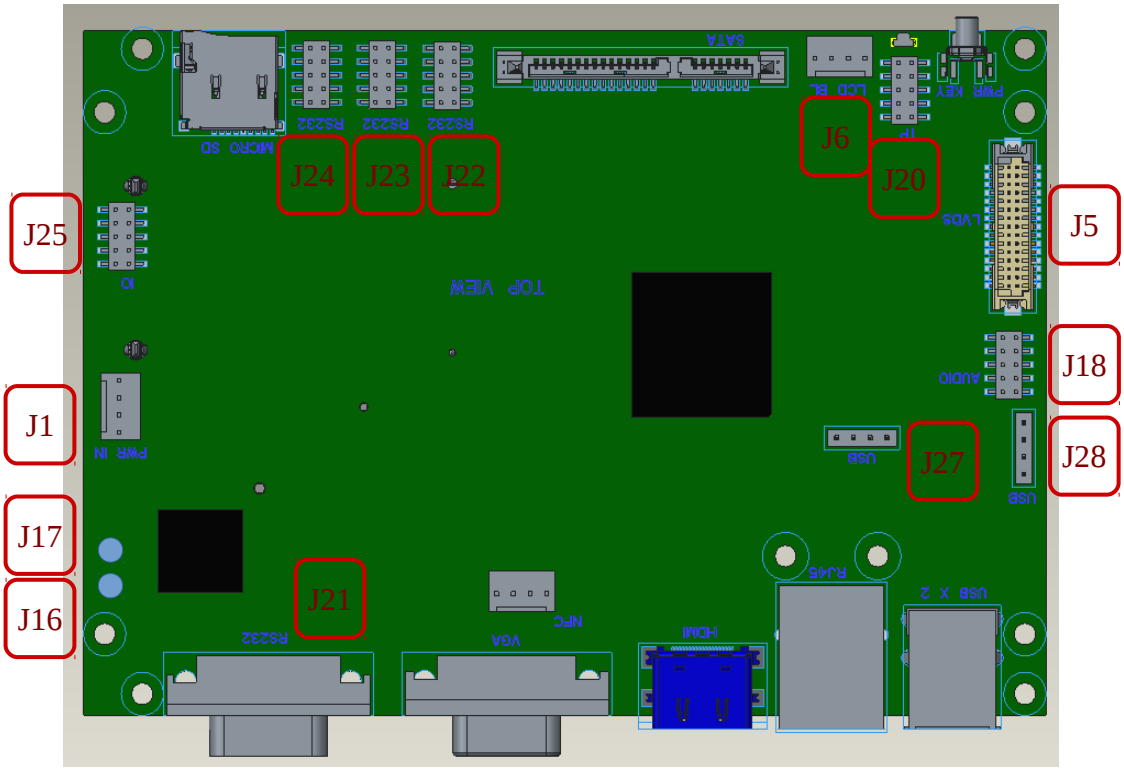


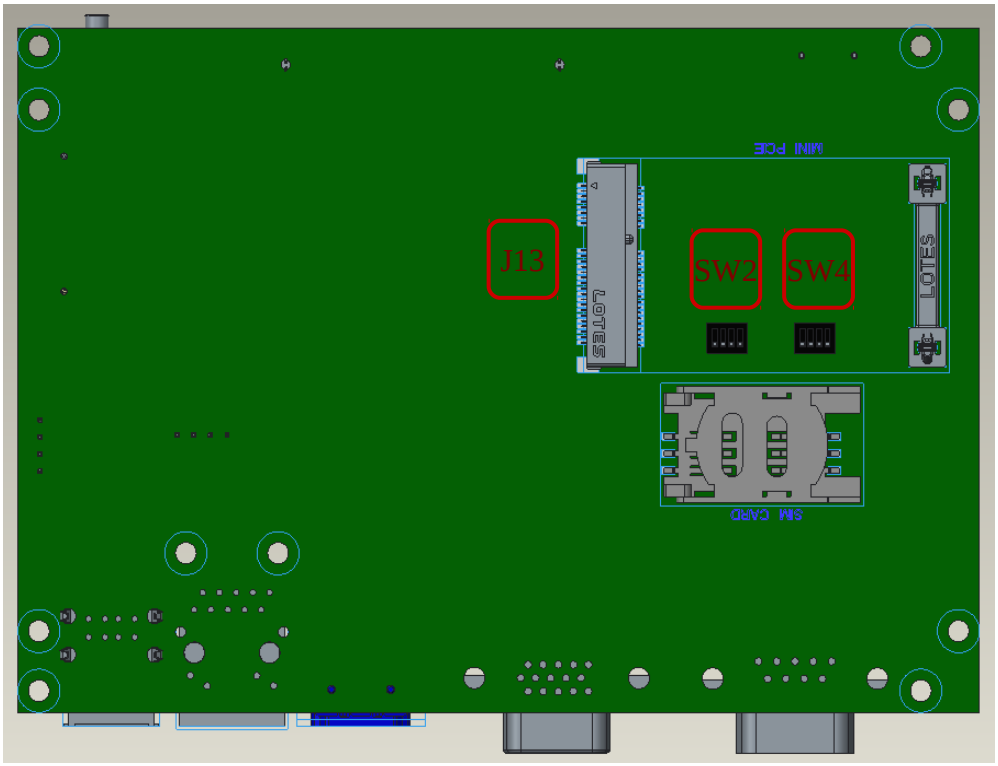
NutsBoard – Pistachio SBC block diagram

2. Hardware Specification

- CPU - NXP ARM Cortex-A9 Quad/Dual 800MHz
- Memory - 2GB DDR3
- Storage - 4GB eMMC
- PMIC - NXP PFUZE100
- WiFi - 802.11a/b/g/n 2.4GHz,5GHz
- Bluetooth - BT v4.2
- EEPROM - eFUSE
- RTC - x1
- Network - 10/100/1000Mb RGMII Ethernet
- USB Host/OTG - x4/x1(mPCIE connector)
- Serial - RS232/422/485 x1, RS232 x3 (one is debug console)
- CAN bus - x1
- I2C - x1
- PWM - x1
- Touch - I2C x1
- Audio - x1 with class D amplifier
- SD slot - x1
- GPIO - x4
- Display - LVDS x2, VGA x1, DMI x1
- SATA - x1
- mPCIE - x1, SIM card slot x1

3. Pin Header Definition





3-1. J27 USB header

Pin number	Pin name
1	+5V
2	D-
3	D+
4	GND

3-2. J28 USB header

Pin number	Pin name
1	+5V
2	D-
3	D+
4	GND

3-3. J29 CAN bus header

Pin number	Pin name
1	GND
2	CANH_B
3	CANL_B
4	GND

3-4. J18 speaker & microphone header

Pin number	Pin name
1	SPKLn
2	MICBIAS
3	SPKLp
4	MIC_IN
5	SPKRn
6	Microphone_DET
7	SPKRp
8	GND
9	Headphone_DET
10	NC

3-5. J5 LVDS connector

Pin number	Pin name	Pin number	Pin name
1	LV0_T0N	2	LV1_T0N
3	LV0_T0P	4	LV1_T0P
5	LV0_T1N	6	LV1_T1N
7	LV0_T1P	8	LV1_T1P
9	LV0_T2N	10	LV1_T2N
11	LV0_T2P	12	LV1_T2P
13	GND	14	GND
15	LV0_CKN	16	LV1_CKN
17	LV0_CKP	18	LV1_CKP
19	GND	20	GND
21	LV0_T3N	22	LV1_T3N
23	LV0_T3P	24	LV1_T3P
25	NC	26	NC
27	NC	28	NC
29	LCD_PWR	30	LCD_PWR

3-6. J20 Touch panel header (4/5-wire RTP & CTP)

Pin number	Pin name		
	CTP	4-Wire RTP	5-Wire RTP
1		RES_Y+	RES_Y+
2	TP_3V3		
3		RES_Y-	RES_Y-
4	TP_RST		
5	Ground(RP7 equipped)	NC(RP7 open)	RES_5W(RP7 open)
6	TP_INT		
7		RES_X+	RES_X+
8	TP_SCL		
9		RES_X-	RES_X-
10	TP_SDA		

3-7. J6 LCD backlight header 2.54mm

Pin number	Pin name
1	BL_PWR
2	GND
3	LCD_BL_ON
4	LCD_BL_PWM

3-8. J22 RS232 header

Pin number	Pin name
1	5VDC
2	RTS
3	5VDC
4	RX
5	GND
6	TX
7	GND
8	CTS
9	GND
10	GND

3-9. J23 RS232 header

Pin number	Pin name
1	5VDC
2	RTS
3	5VDC
4	RX
5	GND
6	TX
7	GND
8	CTS
9	GND
10	GND

3-10. J24 RS232 header

Default as console port, baud:115200, data: 8, parity: N, stop: 1

Pin number	Pin name
1	5VDC
2	RTS
3	5VDC
4	RX
5	GND
6	TX
7	GND
8	CTS
9	GND
10	GND

3-11. J25 Expansion header

Pin number	**Pin name**
1	GND
2	SDA
3	3.3V
4	SCL
5	GPIO_5V1
6	SAM_SHDNB
7	GPIO_5V2
8	SAM_SINTB
9	GPIO_5V3
10	GPIO_5V4

3-12. J1 DC input header 2.54mm

Pin number	Pin name
1	GND
2	DC_VIN
3	DC_VIN
4	GND

3-13. J17 WiFi/Bluetooth Antenna 2.4G

Pin number	Pin name
1	RF
2	GND

3-14. J16 WiFi/Bluetooth Antenna 5G

Pin number	Pin name
1	RF
2	GND

3-15. J21 RS232/422/485 DSUB-9 connector

Pin number	Pin name		
	RS232	**RS422**	**RS485 2w**
1	DCD	TX-	DATA-
2	RXD	TX+	DATA+
3	TXD	RX+	
4	DTR	RX-	
5	GND	GND	
6	DSR		
7	RTS		
8	CTS		
9	RI		

3-16. J13 mPCIE connector

Pin number	Pin name	Pin number	Pin name
1	RESERVED	2	VCC_3V3
3	RESERVED	4	GND
5	RESERVED	6	RESERVED
7	RESERVED	8	USIM_VDD
9	GND	10	USIM_DATA
11	NC	12	USIM_CLK
13	NC	14	USIM_RST
15	GND	16	RESERVED
17	NC	18	GND
19	NC	20	RESERVED
21	GND	22	3G_RST
23	NC	24	VCC_3V3
25	NC	26	GND
27	GND	28	RESERVED
29	GND	30	NC
31	NC	32	RESERVED
33	mPCIE_RST	34	GND
35	GND	36	USB_DM
37	GND	38	USB_DP
39	VCC_3V3	40	GND
41	VCC_3V3	42	RESERVED
43	GND	44	USB_ID
45	NC	46	NC
47	NC	48	NC
49	NC	50	GND
51	NC	52	VCC_3V3

4. Switch settings

4-1. SW2 Boot configuration

Pin number	Pin position	
	SD boot	eMMC boot
1	OFF	ON
2	OFF	ON
3	ON	OFF
4	ON	OFF

4-2. SW4 RS232/RS422/RS485 settings for J21

Pin 1	Pin 2	Pin 3	Pin 4	Mode
ON	OFF	X	X	RS232
ON	ON	ON	OFF	RS422
ON	ON	ON	ON	RS422 RXD +/- with 120 ohm termination
ON	ON	OFF	OFF	RS485 full duplex
ON	ON	OFF	ON	RS485 full duplex RXD +/- with 120 ohm termination
OFF	ON	OFF	OFF	RS485 half duplex without ECHO
OFF	ON	OFF	ON	RS485 half duplex without ECHO Data +/- with 120 ohm termination