CSE30320 Computer Architecture: MIPS Instruction Encoding Map Subset (others grayed out)

instruction bits [31:26]

opcode						
dec	hex	bin	op	descr	format	class
0	0	000000	*func*		R	alu, jump
1	1	000001	*func*		I	branch
2	2	000010	j	jump	J	jump
3	3	000011	jal	jump and link	J	jump
4	4	000100	beq	branch if equal	I	branch
5	5	000101	bne	branch not equal	I	branch
6	6	000110	blez		I	branch
7	7	000111	bgtz		I	branch
8	8	001000	addi	add immediate	I	alu
9	9	001001	addiu	add imm unsigned	I	alu
10	A	001010	slti	set less than imm	I	alu
11	B	001011	sltiu	slt imm unsigned	I	alu
12	C	001100	andi	and immediate	I	alu
13	D	001101	ori	or immediate	I	alu
14	E	001110	xori	xor immediate	I	alu
15	F	001111	lui	load upper immediate	I	alu
16	10	010000	*cop*			
17	11	010001	*cop*			
18	12	010010	*cop*			
19	13	010011				
20	14	010100	beql		I	branch
21	15	010101	bnel		I	branch
22	16	010110	blezl		I	branch
23	17	010111	bgtzl		I	branch
24	18	011000				
25	19	011001				
26	1A	011010				
27	1B	011011				
28	1C	011100	*func*		R	
29	1D	011101				
30	1E	011110				
31	1F	011111				
32	20	100000	lb	load byte	I	mem
33	21	100001	lh	load half	I	mem
34	22	100010	lwl		I	mem
35	23	100011	lw	load word	I	mem
36	24	100100	lbu	load byte unsigned	I	mem
37	25	100101	lhu	load half unsigned	I	mem
38	26	100110	lwr		I	mem
39	27	100111				
40	28	101000	sb	store byte	I	mem
41	29	101001	sh	store half	I	mem
42	2A	101010	swl		I	mem
43	2B	101011	sw	store word	I	mem
44	2C	101100				
45	2D	101101				
46	2E	101110	swr		I	mem
47	2F	101111	cache		I	
48	30	110000	ll		I	mem
49	31	110001	lwc1		I	cop
50	32	110010	lwc2		I	cop
51	33	110011	pref		I	
52	34	110100				
53	35	110101	ldc1		I	cop
54	36	110110	ldc2		I	
55	37	110111				
56	38	111000	sc		I	cop
57	39	111001	swc1		I	cop
58	3A	111010	swc2		I	cop
59	3B	111011				
60	3C	111100				
61	3D	111101	sdc1		I	cop
62	3E	111110	sdc2		I	cop
63	3F	111111				

bits [5:0] when [31:26] = 0

func					
dec	hex	bin	op	descr	class
0	0	000000	sll	shift left logical	alu
1	1	000001			
2	2	000010	srl	shift right logical	alu
3	3	000011	sra		alu
4	4	000100	sllv		alu
5	5	000101			
6	6	000110	srlv		alu
7	7	000111	srav		alu
8	8	001000	jr	jump register	jump
9	9	001001	jalr		jump
10	A	001010	movz		alu
11	B	001011	movn		alu
12	C	001100	syscall	system call	sys
13	D	001101	break		sys
14	E	001110			
15	F	001111	sync		alu
16	10	010000	mfhi		alu
17	11	010001	mthi		alu
18	12	010010	mflo		alu
19	13	010011	mtlo		alu
20	14	010100			
21	15	010101			
22	16	010110			
23	17	010111			
24	18	011000	mult		alu
25	19	011001	multu		alu
26	1A	011010	div		alu
27	1B	011011	divu		alu
28	1C	011100			
29	1D	011101			
30	1E	011110			
31	1F	011111			
32	20	100000	add	add	alu
33	21	100001	addu	add unsigned	alu
34	22	100010	sub	subtract	alu
35	23	100011	subu	sub unsigned	alu
36	24	100100	and	and	alu
37	25	100101	or	or	alu
38	26	100110	xor	xor	alu
39	27	100111	nor	nor	alu
40	28	101000			
41	29	101001			
42	2A	101010	slt	set less than	alu
43	2B	101011	sltu	set less than unsigned	alu
44	2C	101100			
45	2D	101101			
46	2E	101110			
47	2F	101111			
48	30	110000	tge		sys
49	31	110001	tgeu		sys
50	32	110010	tit		sys
51	33	110011	titu		sys
52	34	110100	teq		sys
53	35	110101			
54	36	110110	tne		sys
55	37	110111			
56	38	111000			
57	39	111001			
58	3A	111010			
59	3B	111011			
60	3C	111100			
61	3D	111101			
62	3E	111110			
63	3F	111111			