PRÁTICA 6

```
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;
use IEEE.STD_LOGIC_unsigned.ALL;

entity practica6 is
    Port ( P1 : in  STD_LOGIC;
           P0 : in  STD_LOGIC;
           D3 : in  STD_LOGIC;
           D2 : in  STD_LOGIC;
           D1 : in  STD_LOGIC;
           D0 : in  STD_LOGIC;
           F : out  STD_LOGIC;
           J1 : out STD_LOGIC_VECTOR(3 downto 0);
           J2 : out STD_LOGIC_VECTOR(3 downto 0));
end practica6;

architecture interior of practica6 is
           signal producto: std_logic_vector(1 downto 0);
           signal dinero_v: std_logic_vector(3 downto 0);
           signal dinero_int: integer range 0 to 15;
           signal precio: integer range 0 to 7;
           signal cambio: integer range 0 to 15;
begin



           producto <= P1&P0;
           dinero_v <= D3&D2&D1&D0;
           dinero_int <= conv_integer(dinero_v);



           precio <= 2 when producto = "00" else -- (Coca Cola)
                                    3 when producto = "01" else -- (Patatas)
                                    5 when producto = "10" else -- (Postre)
                                    6 when producto = "11"; -- (Albóndigas)
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```
        process(cambio, dinero_int, precio)
        begin

                if (dinero_int - precio) >= 0 then

                        cambio <= dinero_int - precio;
                        F <= '0';

                else

                        cambio <= precio - dinero_int;
                        F <= '1';
                end if;

                                case cambio is
                                when 0 => J2 <= "0011"; J1 <= "1111";
                                when 1 => J2 <= "0000"; J1 <= "0110";
                                when 2 => J2 <= "0101"; J1 <= "1011";
                                when 3 => J2 <= "0100"; J1 <= "1111";
                                when 4 => J2 <= "0110"; J1 <= "0110";
                                when 5 => J2 <= "0110"; J1 <= "1101";
                                when 6 => J2 <= "0111"; J1 <= "1101";
                                when 7 => J2 <= "0000"; J1 <= "0111";
                                when 8 => J2 <= "0111"; J1 <= "1111";
                                when 9 => J2 <= "0110"; J1 <= "1111";

                                when others => J2 <= "0000"; J1 <= "0000";
                        end case;
                end process;

end interior;
```