Practica 5

```
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;

entity Modulo is
    Port ( G3 : in  STD_LOGIC;
           G2 : in  STD_LOGIC;
           G1 : in  STD_LOGIC;
           G0 : in  STD_LOGIC;
           P : out  STD_LOGIC;
           S : out  STD_LOGIC;
           T : out  STD_LOGIC;
           C : out  STD_LOGIC);
end Modulo;

architecture Behavioral of Modulo is

           signal entrada: std_logic_vector (3 downto 0);
begin

           entrada <= G3 & G2 & G1 & G0;
           --Declaro P



           P <= '1' when entrada = "0000" else
                        '1' when entrada = "0001" else
                        '1' when entrada = "0011" else
                        '1' when entrada = "0010" else
                        '0';

           --Declaro S
           with entrada select
                    S <= '1' when "0110",
                                 '1' when "0111",
                                 '1' when "0101",
                                 '1' when "0100",
                                 '0' when others;
```

```
--Declaro T
        process (entrada)
                begin

        if entrada = "1100" then T <= '1';
        elsif entrada = "1101" then T <= '1';
        elsif entrada = "1111" then T <= '1';
        elsif entrada = "1110" then T <= '1';
        else T <='0' ; end if;
        end process;

        -- Declaro C

        process (entrada)
                begin

        case entrada is

                                                when "1010" => C <= '1' ;
                                                when "1011" => C <= '1' ;
                                                when "1001" => C <= '1' ;
                                                when "1000" => C <= '1' ;
                                                when others => C <= '0' ;
                                                end case;
end process;

end Behavioral;
```