

PRACTICA 7 - C1

```
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;

entity Practica_3xilinx is
  Port ( E : in STD_LOGIC;
        CK : in STD_LOGIC;
        RS : in STD_LOGIC;
        Q : out STD_LOGIC_VECTOR (2 downto 0);
        S : out STD_LOGIC);
end Practica_3xilinx;

architecture MOORE of Practica_3xilinx is
  subtype mis_estados is std_logic_vector(2 downto 0);
  constant E0 : mis_estados := "000";
  constant E1 : mis_estados := "001";
  constant E2 : mis_estados := "010";
  constant E3 : mis_estados := "011";
  constant E4 : mis_estados := "100";
  constant E5 : mis_estados := "101";
  signal estado : mis_estados;
begin
  EVOLUCION: process
    begin
      wait until CK = '1';
      if (RS = '1') then estado <= E0;
      else case estado is
        when E0 => if (E = '1') then estado <= E1; end if;
        when E1 => if (E = '1') then estado <= E2; else estado <= E0;
        end if;
        when E2 => if (E = '1') then estado <= E3; else estado <= E0;
        end if;
        when E3 => if (E = '0') then estado <= E4; end if;
        when E4 => if (E = '0') then estado <= E5; end if;
        when E5 => if (E = '0') then estado <= E0; end if;
        when others =>
          end case;
        end if;
      end process;
end;
```

```
process (estado)
begin
    case estado is
        when E0 => S <='0';
        when E1 => S <='0';
        when E2 => S <='0';
        when E3 => S <='1';
        when E4 => S <='1';
        when E5 => S <='1';
        when others => S <='0';
    end case;

    end process;
    Q<=estado;

end MOORE;
```