PRÁCTICA 7 - SISTEMA COMPLETO

```
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;

entity Sistema_Completo is
    Port ( RESET : in  STD_LOGIC;
           CLK_50MHZ : in  STD_LOGIC;
           CLK_CR : in  STD_LOGIC;
           E : in  STD_LOGIC;
           Q : out  STD_LOGIC_VECTOR (2 downto 0);
           S : out  STD_LOGIC);
end Sistema_Completo;

architecture Behavioral of Sistema_Completo is

component ANTIRREBOTES IS
          GENERIC (SIMULAR: STD_LOGIC := '1');
          PORT (CLK_50MHZ, E: IN STD_LOGIC; S: OUT STD_LOGIC);
END component;



component Practica_3xilinx is
    Port ( E  : in  STD_LOGIC;
           CK : in  STD_LOGIC;
                        RS : in  STD_LOGIC;
                        Q  : out  STD_LOGIC_VECTOR (2 downto 0);
           S  : out STD_LOGIC);
end component;

SIGNAL CLK_SR: std_logic;

begin

C1: Practica_3xilinx PORT MAP (
                    E => E,
                    CK => CLK_SR,
                    RS => RESET,
                    Q => Q,
                    S => S
          );

end Behavioral;
```