RF Solid State Driver for Argonne Light Source

Branko Popovic
Lee Teng Internship
University of Iowa
Goeff Waldschmidt
Argonne National Laboratory
Argonne, IL
August 13, 2010

Abstract

Currently, power to the APS storage ring and Booster cavities is provided from klystrons with a eventual goal to move to a solid state RF system. A modular design centered around a 1 kW amplifier has been decided on. The driver amplifier was created for this module system using Agilent's ADS circuit simulation software and then built and tested.

Introduction

Currently, power to the APS storage ring and Booster cavities is provided from 1.1 MW continuous wave (CW) klystrons. Two klystrons provide RF power to the 16 storage ring cavities and a third supplies power to the Booster cavities. Vendors are becoming increasingly difficult to find for replacement klystrons, as a result they are difficult and expensive to replace. The eventual goal is to replace the klystrons and to use a CW 200 kW solid state RF system that consists of 1 KW modules to provide RF to each of the 16 cavities instead.

A similar setup is in use at SOLEIL synchrotron outside of Paris, France though the modules are combined to produce 200kW are 330 W each instead of 1kW. APS has chosen to use the Freescale MRF6VP41KHR6 device which produces 1kW CW per module at 352 MHz. The reason for 1kW modules is the available floor space in the RF building, Bldg. 420 at Argonne Laboratory. A larger output power density(W/m^2) is required as a result of the space requirements.

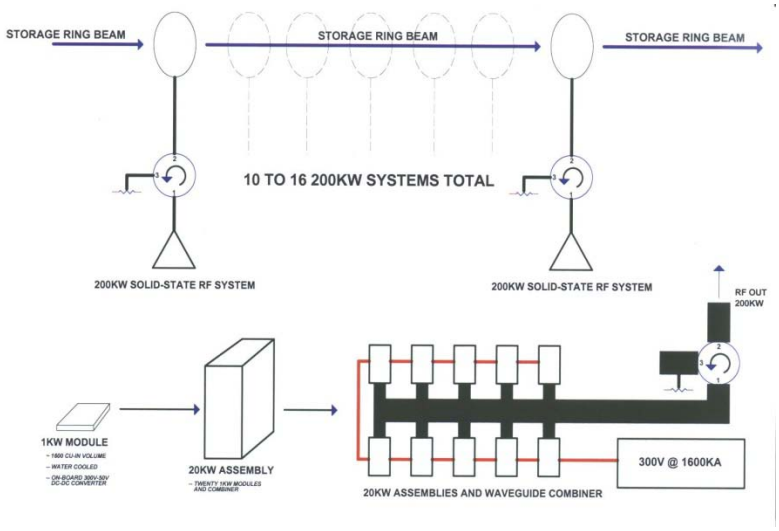

Figure 1: Proposed Solid State Amplifier System using 1kW Modules

1kW Amplifier Module Design

Typically amplifiers consist of multiple stages; in this case the solid state amplifier system will consist of a pre-driver, driver and a final push pull amplifier producing 1kW peak power. Since noise is amplified as well as the desired signal. Low-noise transistors are needed in early stages of amplification

The pre-driver consists of a general purpose amplifier based around Freescale's MMG3014NT1 producing about 20 dBm power output at 1 dB compression. While the driver, the focus of this project and paper, is Freescale's MRF6V2010N, an N-Channel enhancement MOSFET which will output the 10W. Finally, as stated previously, Freescale's MRF6VP41KHR6 push-pull amplifier provides the 1kW output.

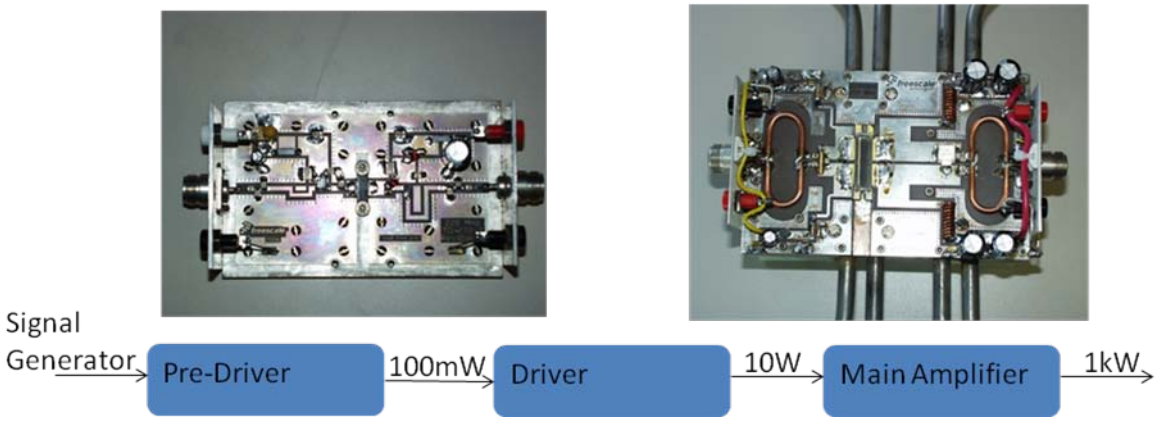

Figure 2: The 1kW Amplifier design with the driver(left) and main amplifier(right) boards pictured.

1kW Main Amplifier Design

The main component of this amplifier system is Freescale's MRF6VP41KHR6 device, which is capable of 1kW peak power at 450MHz. This is currently cutting edge technology and thus they are various issues with the device that need to be overcome. Especially important is efficiency and the heat output occurring during day to day operation. It is also important that the solid state replacement of the klystrons have at least the same reliability as the present system. Reliability is directly related to the temperature of the transistor, as show in the figure 4, which is comparing junction temperature and mean time to failure (MTTF). Water cooling is required for day to day operation of the 1kW amplifier as a result of the required power output and efficiency. The expected efficiency of this amplifier system is >62%.

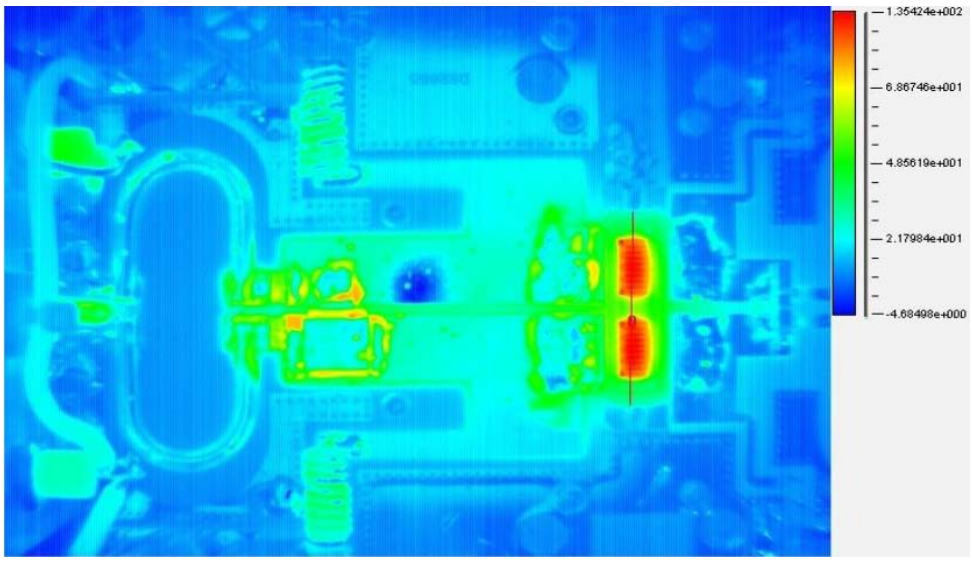

Figure 3: IR image of the Freescale MRF6VP41KHR6 test board

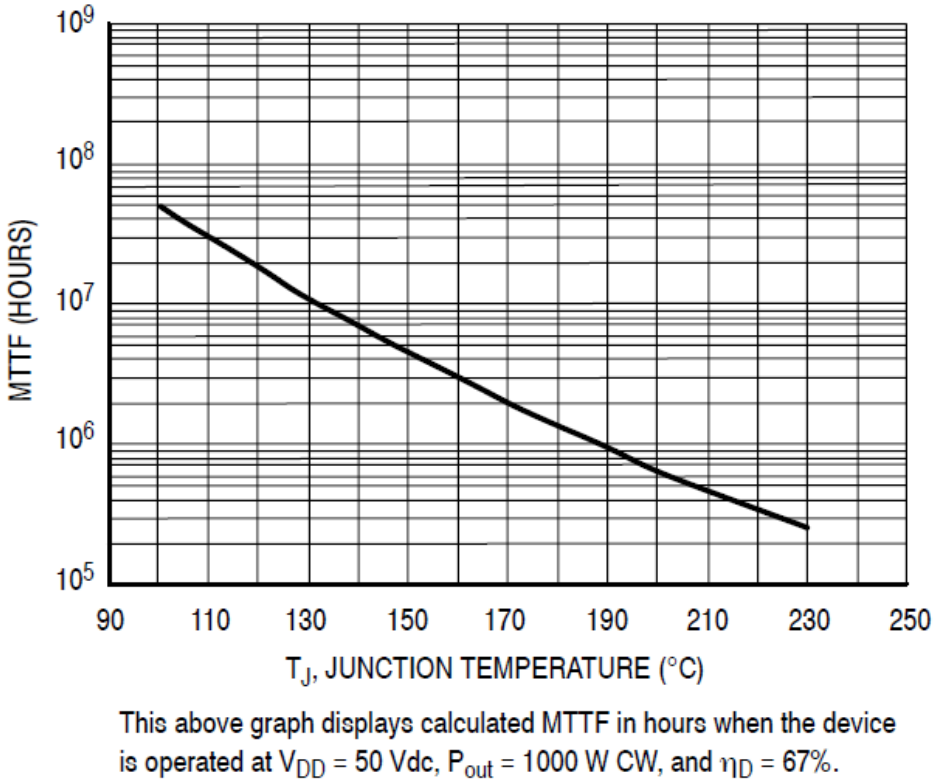

Figure 4: MTTF vs. Junction Temperature graph take from Freescale MRF6VP41KHR6 datasheet

Driver Amplifier Design

The focus of much of the work done over this past summer is the driver amplifier design. The rest of this paper will detail the different stages and procedures of the design.

DC Bias Network

The transistor requires a DC source to bias it. The value for the gate quiescent voltage (V_{GSQ}) is measured from DC curves or just taken from the datasheet for the transistor. While the voltage supply (V_{DD}) value is also listed on the datasheet for the transistor. Usually the DC bias network is just a voltage divider. APS will use a temperature dependent bias circuit using an LM723 integrated circuit to control the gate bias to prevent variation of the device gain. As the temperature increases, the integrated circuit decreases the gate bias, thus reducing the power output and as a result the temperature of the transistor.

Inductors are used as RF blockers to separate the DC bias network from the RF portion of the circuit. Then decoupling capacitors remove any RF signals that are not blocked by the inductors. Finally Ferrite beads remove any RF noise that may have been included with the DC source.

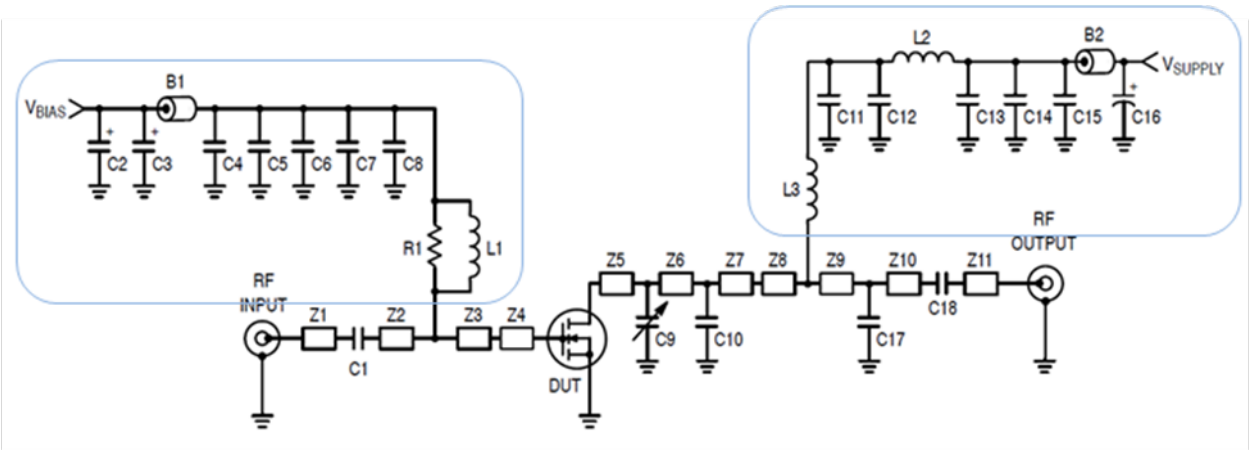

Figure 5: Driver circuit shown with DC networks circled.

In figure 5 the RF blockers are L1, L2 and L3. While the ferrite beads are B1 and B2. The decoupling capacitors are all of the capacitors in the DC network.

Determining Driver Stability with the Agilent ADS Software

Ideally the transistor and overall circuit are unconditionally stable across a wide frequency band. The fact there could be noise at frequencies other than the fundament frequency, in this case 352 MHz, that could trigger oscillation and possible destruction of the transistor is the reason for desiring stability across a wide frequency band. The following equations[1] use S-parameters to check for stability:

$$\mu = \frac{1-|S_{11}|^2}{|S_{22}-\Delta(S_{11}^*)|+|S_{21}S_{12}|} \geq 1 \qquad K = \frac{1-|S_{11}|^2-|S_{22}|^2+|\Delta|^2}{2|S_{12}S_{21}|} \geq 1$$

$$\mu_{prime} = \frac{1-|S_{22}|^2}{|S_{11}-\Delta(S_{22}^*)|+|S_{21}S_{12}|} \geq 1 \qquad |\Delta| = |S_{11}S_{22}-S_{21}S_{12}| < 1$$

Stability is achieved when either μ or μ_{prime} are greater than one, or K is greater than one and $|\Delta|$ is less than one.

Included in ADS are simulation components related to the S-parameters to graph the K-factor and μ's.

The chart for μ in figure 7 shows possible instability below 200 MHz. After contacting Freescale it was discovered that the model is not accurate below this frequency because of the range of their test setup. As a result of their own construction and testing of prototype boards, Freescale has included in their design a 120ohm resistor as a feedback to provide stability at lower frequencies, though its effects are unseen in the graph for μ.

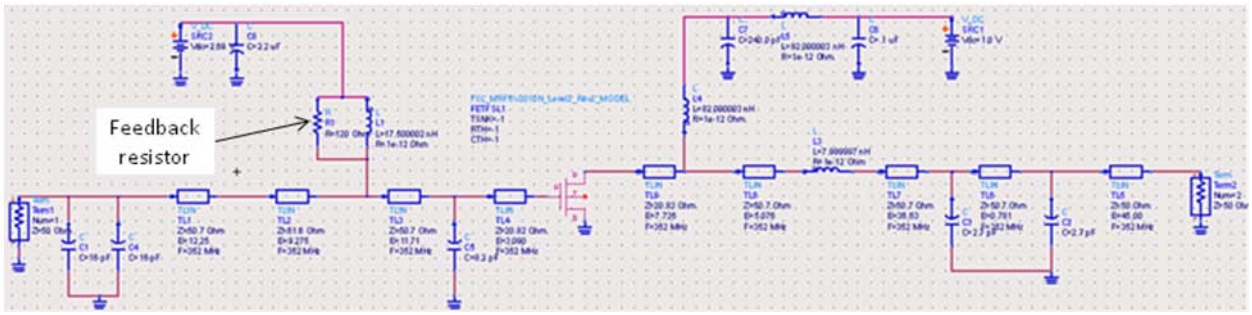

Figure 6 : Driver circuit with the feedback resistor.

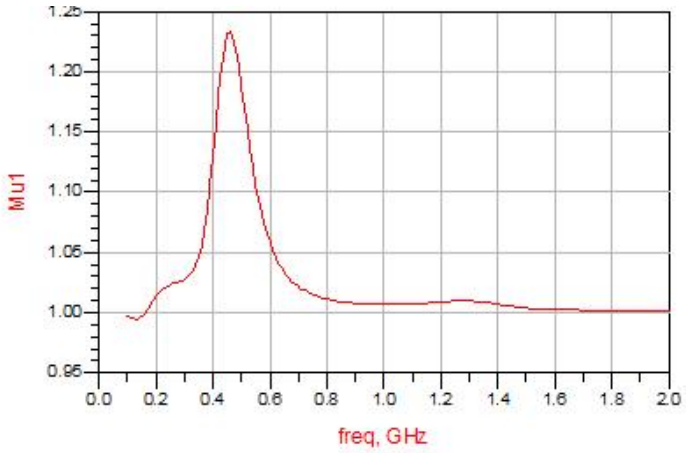

Figure 7: Plot of μ vs freq. Showing instability below 200MHz.

Harmonic Balance

The transistor is a non-linear device and as a result could produce harmonics at frequencies other then the operating frequency. The rest of the components, such as inductors, capacitors, resisters and microstrip lines are linear elements. Since there are non-linear and linear elements in the circuit harmonic balance simulation is used, specifically in the load pull and source pull operations.

The following describes the procedure for harmonic balance analysis.

In harmonic balance simulation the linear circuit's currents are measured in the frequency domain, since simulation time is much less than in the time domain. This is possible because they are linear devices. While the nonlinear circuit voltages are also measured in the frequency domain but then are transformed into the time domain using the inverse Fourier transform. In the time domain the nonlinear currents are calculated and then Fourier transformed into the frequency domain. In the frequency domain Kirchhoff's current law(KCL), that the total current at each node is zero, is verified for the linear and nonlinear currents. If it is not verified the simulation is run again with an increased number of harmonics until convergence using KCL is satisfied. When it is satisfied, the major harmonics are accounted for. This is summarized in figure 8.

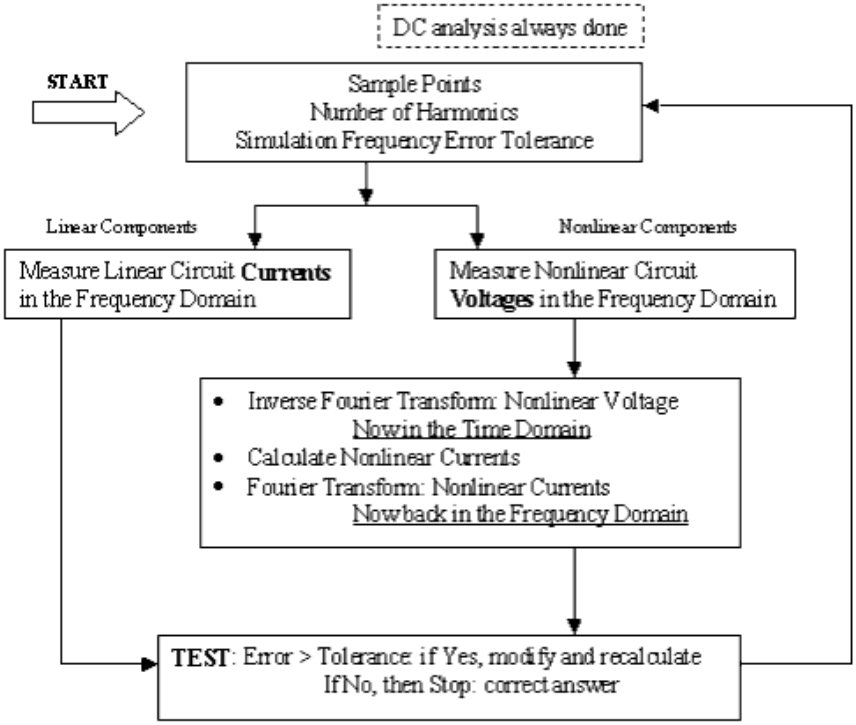

Figure 8: Flowchart of the harmonic balance procedure [2]

Source & Load Pull Analysis

When designing the matching networks it is usually desired to maximize power added efficiency (PAE), power delivered or gain. Thus the particular impedances to match the input and output to in order to maximize one of these parameters are determined from load and source pull methods.

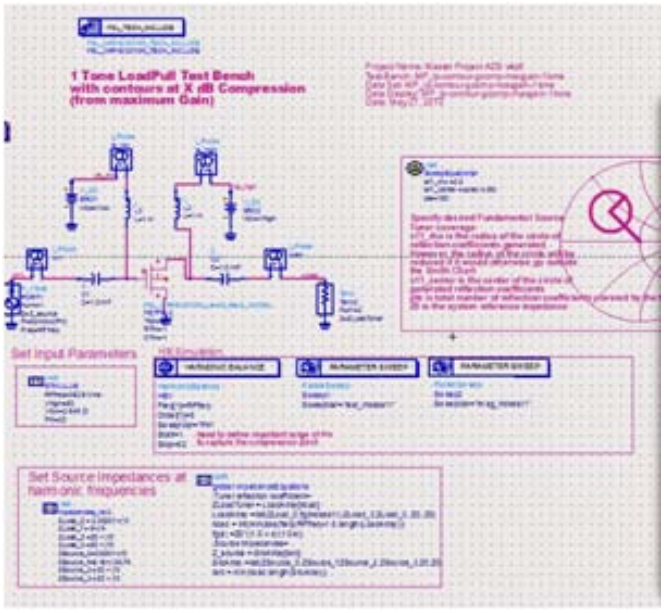

Figure 9: Load Pull for the driver transistor in ADS

The procedure employed is to start with a source pull with the load impedance is set to the respective impedances from the prototype board from the datasheet. Then the source reflection is varied to produce circles of constant values on the Smith Chart. The center of these circles is the given impedance. After the desired circle and point on the circle is chosen, this will be the source impedance for the load pull. The same procedure is followed for the load pull, where the center of circles is the load impedance of the transistor. This complete procedure is usually iterated three times to find the ideal source and load impedances for maximum PAE, power delivered or gain.

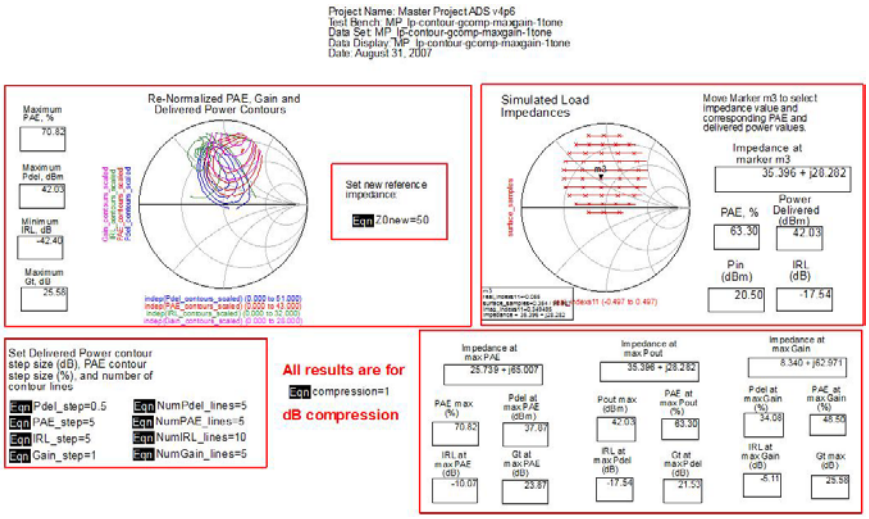

Figure 10: Results of Load pull with PAE and delivered power constant circles in the upper left box and summary of peak PAE, gain and power output in the lower right box.

Creating Matching Networks

Matching networks are created based on the results from the Load/Source Pull analysis, in the case of the driver amplifier: Z_{source}= 6.2 + j28.8; Z_{load} = 35.4 + j28.3. Lumped element inductors and capacitors are then used for matching elements. In addition to the lumped elements, distributed elements such as the microstrip transmission lines must be incorporated into the matching network. Matching networks may be created visually on the Smith chart, with ADS providing a Smith chart tool. Various topologies may be investigated.

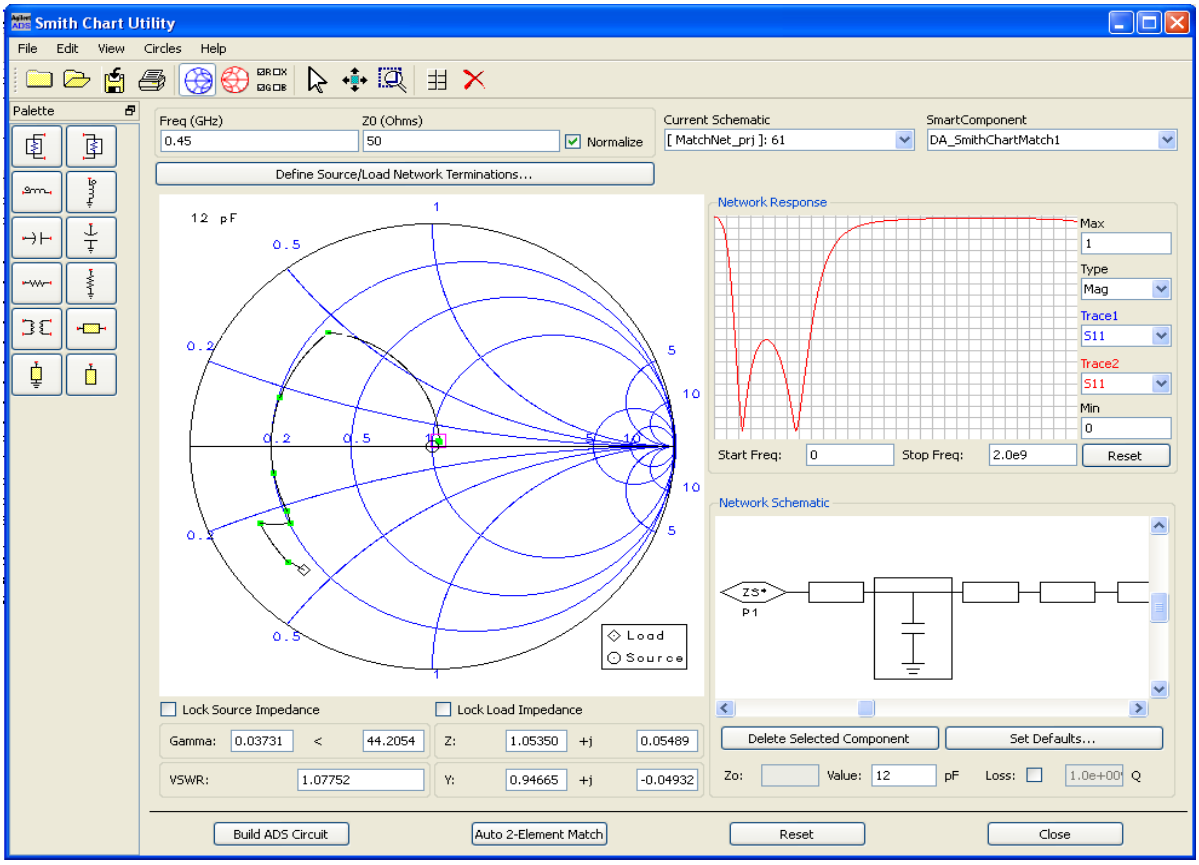

Figure 11: ADS Smith Chart Utility with matching network created

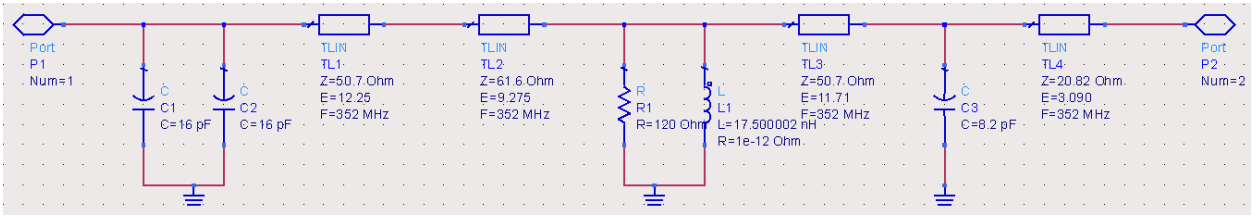

Figure 12 : Input Matching Network for 450 MHz MRF6V2010N Driver

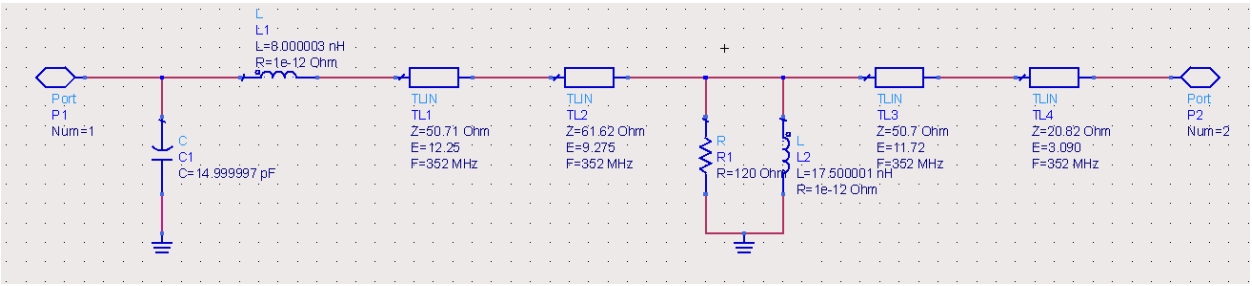

Figure 13: Output Matching Network for 450 MHz MRF6V2010N Driver

Parasitic Effects of Distributed Elements

Due to distribute element geometry, there are parasitic capacitances and inductances. Though for this particular design at 352MHz, the frequencies are low enough that they are negligible. For higher frequencies, mostly above the 1 GHz, these geometries need to be accounted for in simulations. The trace geometries can be created in ADS and then inserted into the schematic along with the lumped elements.

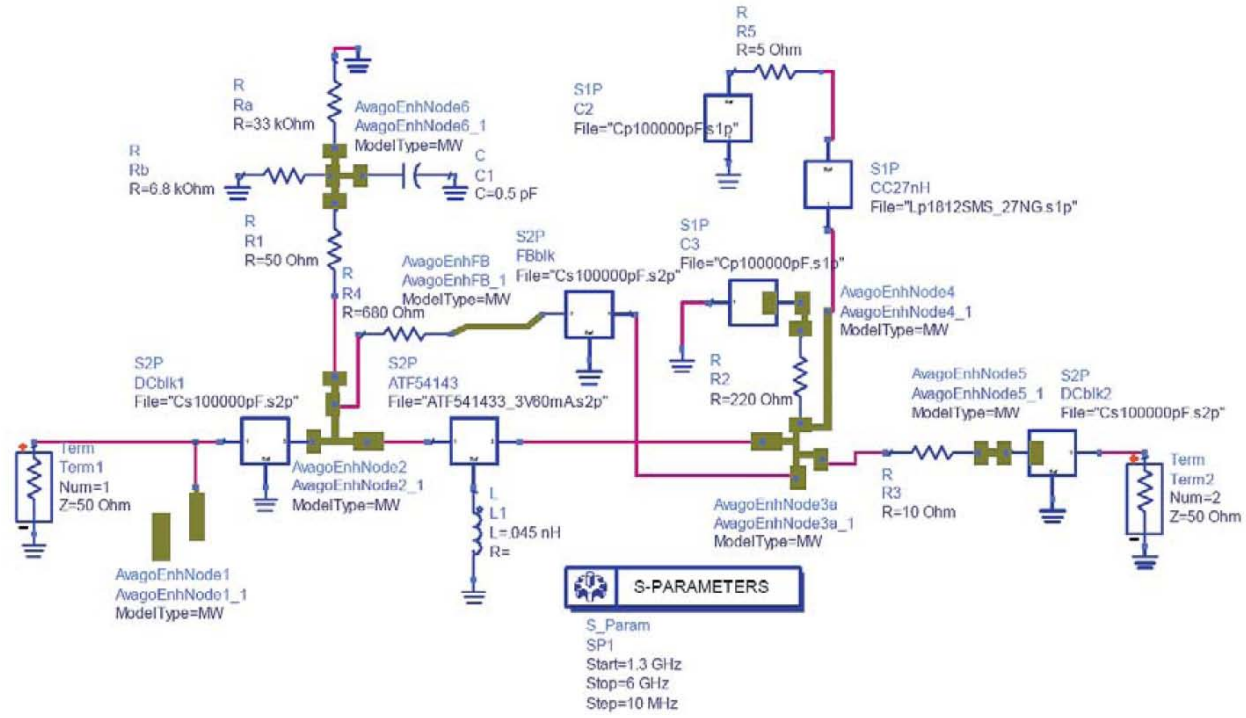

Figure 14: LNA design at 2.4GHz with geometries of trace lines accounted for [3]

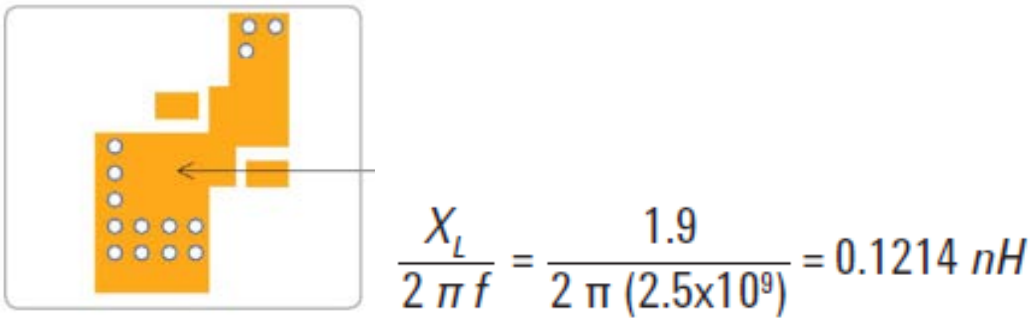

Figure 15: Parasitic inductance at the transistor source lead [3]

Handwound Inductors

During the construction of the driver amplifier there was an issue with part availability. The RF blocking inductors in the DC power supply section of the board were unattainable and a suitable substitute could not be found in time. As a result the inductors were hand-wound using the following simple air-core inductor equation:

$$L\,(\mu H) = \frac{d^2\,n^2}{18\,d + 40\,\ell}$$

L = inductance in microhenrys,
d = coil diameter in inches (from wire center to wire center),
ℓ = coil length in inches, and
n = number of turns.

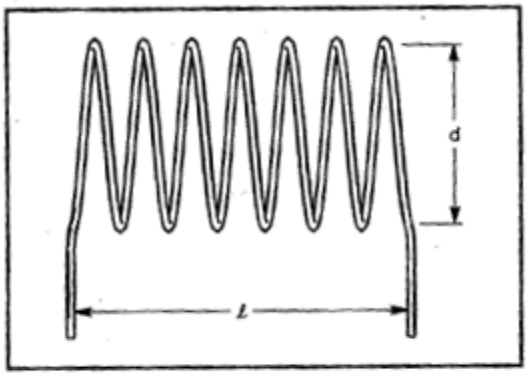

Fig 6.39 — Coil dimensions used in the inductance formula for air-core inductors.

Figure 16: Equation for hand-wound air-core inductor[4]

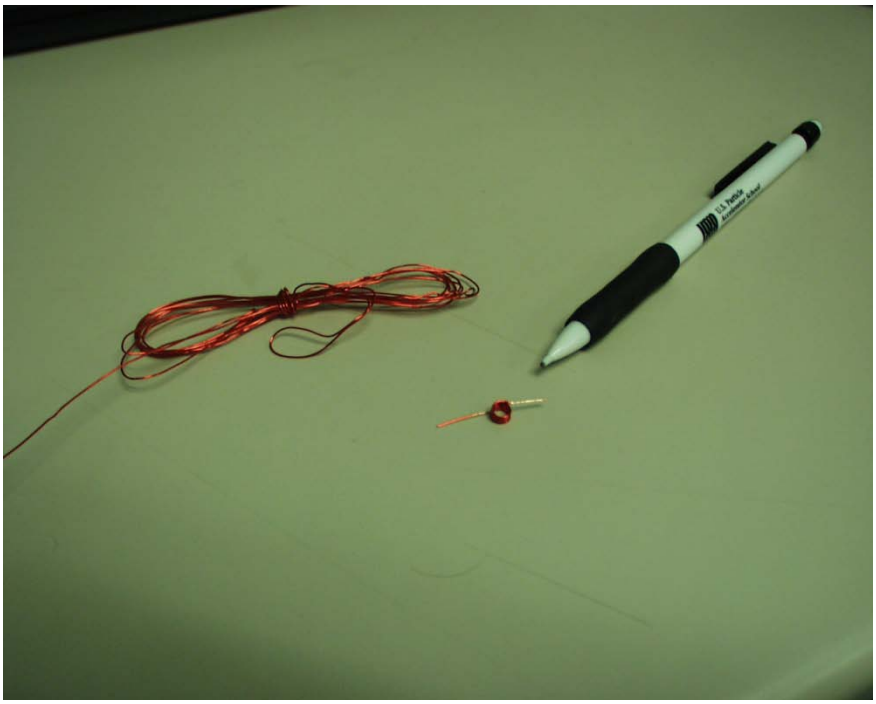

Figure 17: Hand-wound inductor

The necessary dimensions were taken from the data sheet of the unattainable inductor and were used to calculate the number of turns necessary. A drill bit of the required diameter size was used to wind the wire around to create the inductor. The desired value was 82 nH and the measured value of the hand-wound inductor was around 90nH, which should perform satisfactorily.

Circuit Board Prototyping

A prototype of the driver PCB was etched using the circuit prototype, Quick Circuit 3000, available to the RF group. IsoPro software is used to load the CAD drawings and then modify them to program the prototyper. The files include the placement and sizing of the traces, vias and screw holes.

Figure 18: Quick Circuit 3000 prototyper

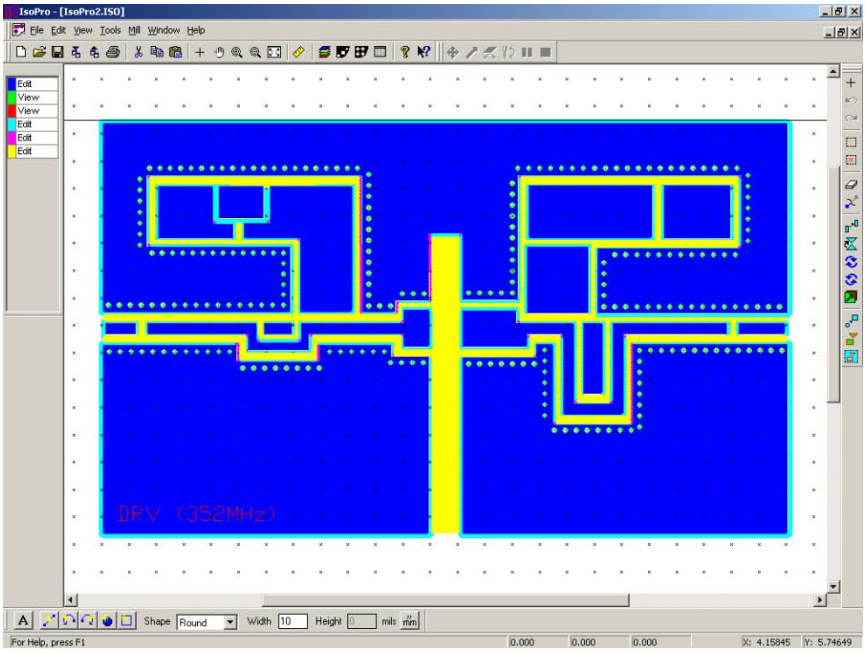

Figure 19: ISOPRO screenshot with driver geometry with isolation and rubout areas highlighted

The PCB board itself consists of a substrate sandwiched between to copper layers. The prototyper uses various bits to drill the vias and screw holes. It then etches the traces by removing the copper layer of

the board using a specialized bit. Finally it cuts the specific PCB board's shape out of the larger PCB. Then the vias are filled with bailbars in order to connect the top and bottom ground planes electrically.

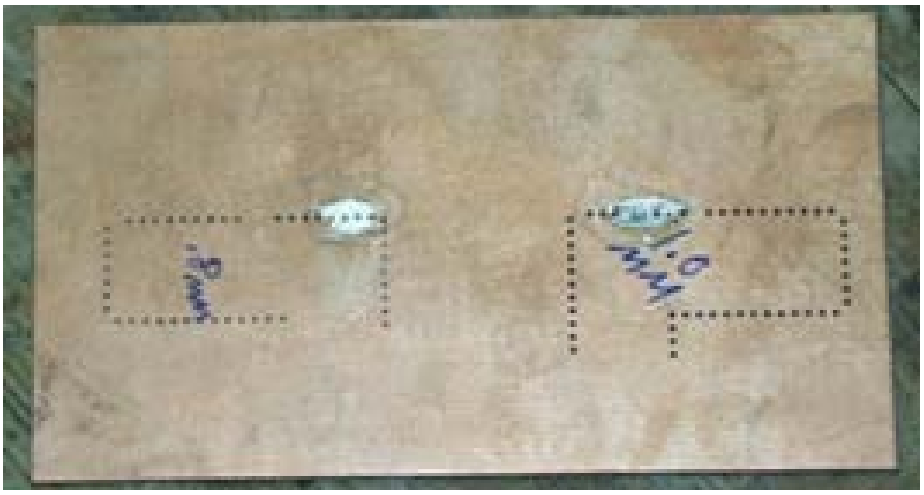

Figure 20: Vias drilled by Quick Circuit with bailbars

Driver Prototype

Freescale sent a PCB for 220MHz model of the driver and it was determined that this would perform satisfactorily. This was the PCB that was used for the actual driver prototype.

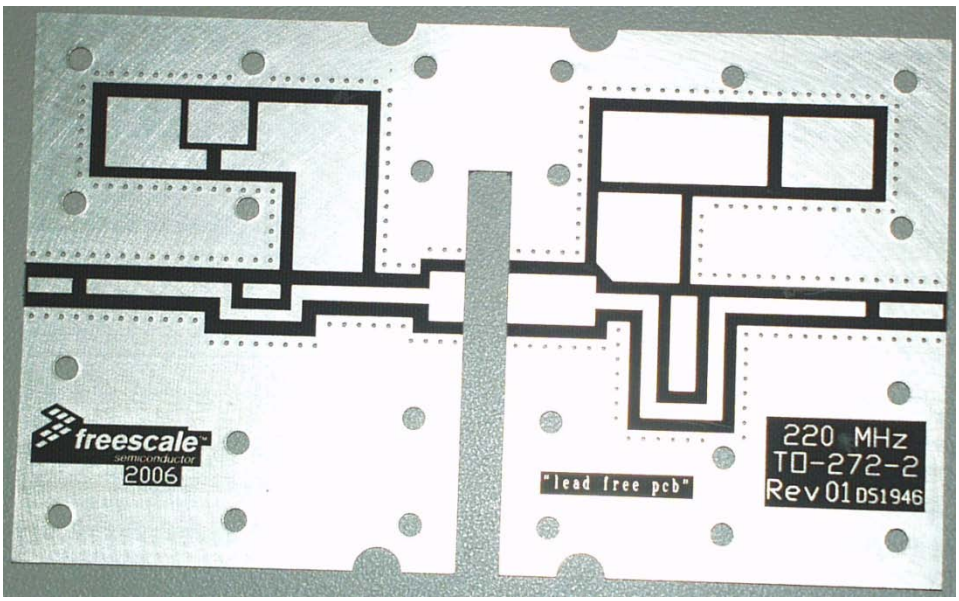

Figure 21: Freescale's PCB

The board was brazed to a copper carrier for thermal conductivity and also to enlarge the ground plane. The lumped elements were then soldered on and then finally the transistor. The transistor is thermally connected to the copper carrier with thermal grease. After successful operation it will be soldered to the

carrier for improved thermal contact, along with better DC contact between the transistor source and ground.

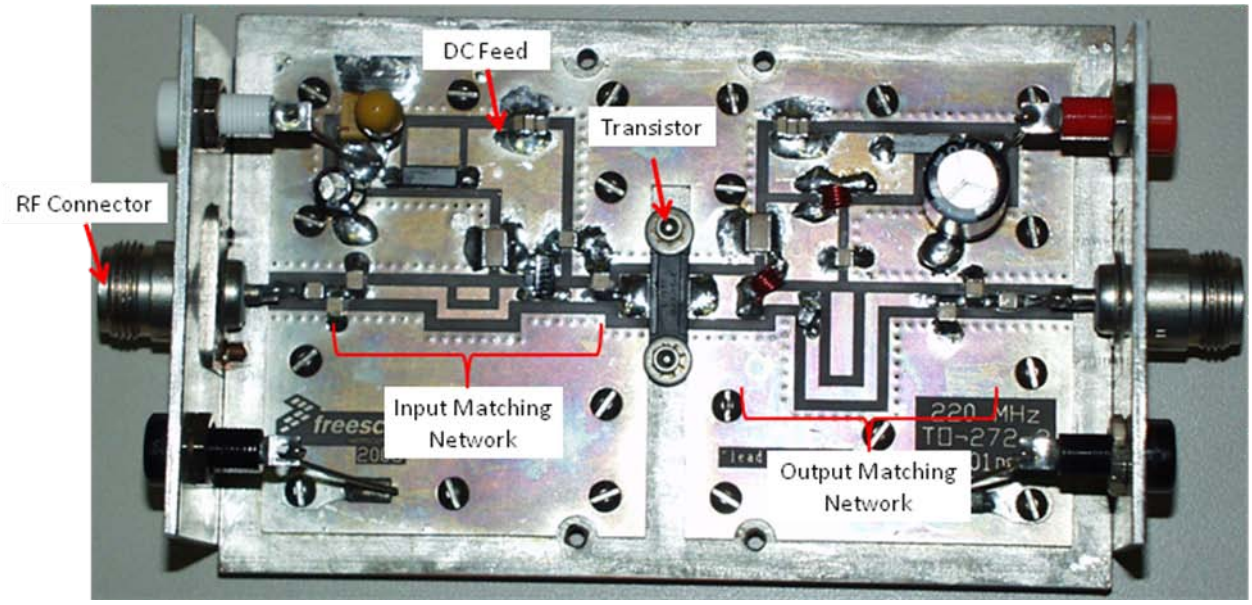

Figure 22: Completed prototype driver amplifier

Test and Measurement

A function generator at 352 MHz was used for the RF input. While a 30dB commercial amplifier was used to amplify the signal from the function generator to 20 dBm into the driver amplifier. Separate DC supplies were used for the gate and drain voltages. A power meter was used to measure the output power.

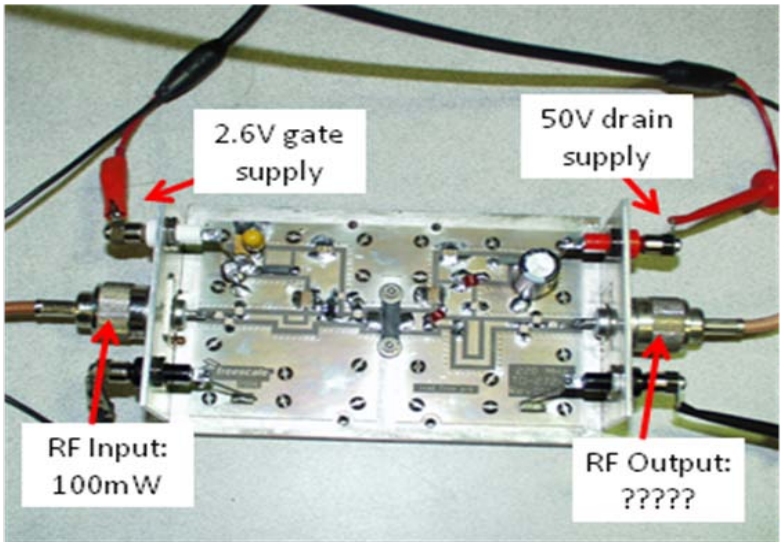

Figure 23: Driver amplifier connected to the test setup

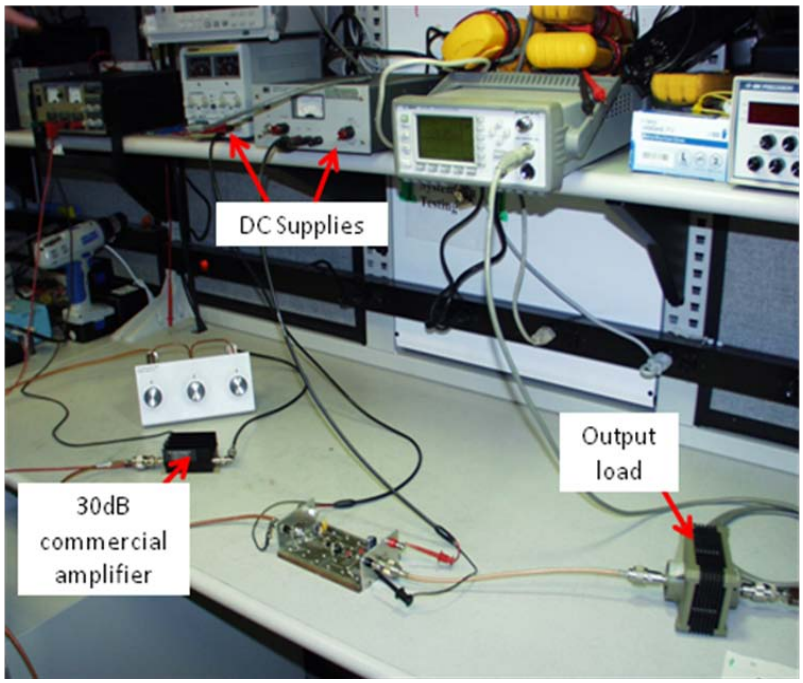

Figure 24: Driver amplifier test setup

Measurement Results

The driver amplifier was measured from 100 mW to 10 W output. While the gain was measured to be 19.3 dB compared with the simulated value of 20.1 dB. Finally the driver efficiency was measured to be 48.9% at 10.4W output power with the simulated drain efficiency at 50.1%. These are preliminary results, with more performance possible as a result of fine tuning the input and output networks. The capacitor positions on the microstrip can be adjusted to possibly provide even more gain. Also there are alternate matching networks that have been simulated that could be employed to further optimize the circuit

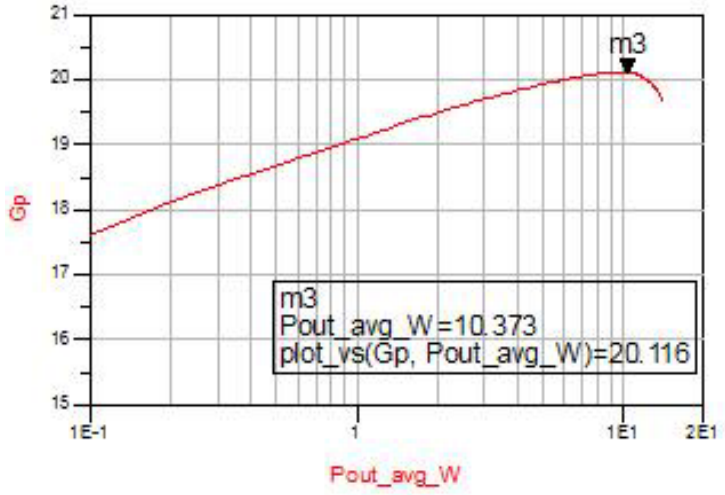

Figure 25: Simulated driver amplifier gain

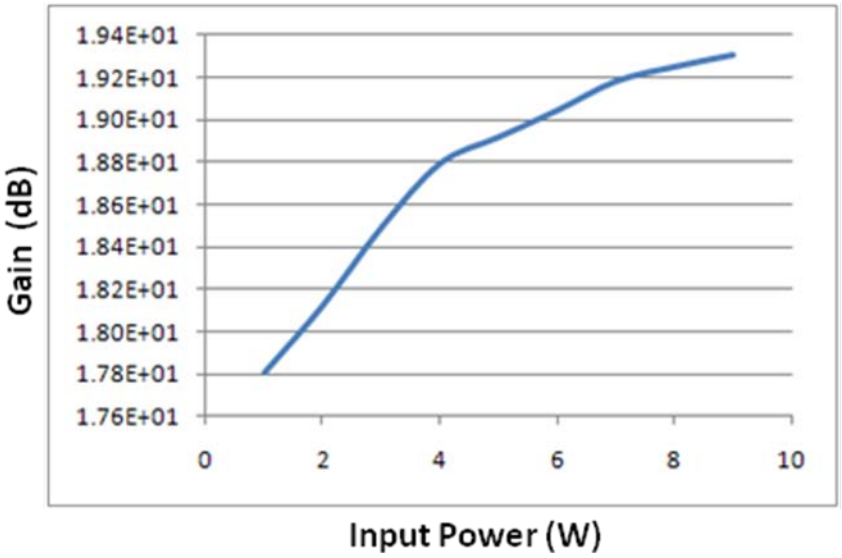

Figure 26: Measured gain of driver amplifier

Acknowledgements

I would like to thank my mentor, Geoff Waldschmidt, along with Doug Horan and Bruce Epperson for their guidance and help with technical issues and the assembly of the board.

Sources

[1] G. Gonzalez. *Microwave Transistor Amplifiers: Analysis and Design*, 2nd ed. Upper Saddle River, NJ: Prentice Hall, 1997. Print.

[2]“Harmonic Balance Background”. [Online]. Available: http://edocs.soco.agilent.com/display/ads2009/Harmonic+Balance+Background. [Accessed: Aug. 12, 2010].

[3] K. Payne “Practical RF Amplifier Design using the Available Gain Procedure and the Advanced Design System EM/Circuit Co-Simulation Capability,” Agilent Technologies, USA, 2009.

[4]“The Arrl Handbook for Radio Communications 2007” Newington, CT: American Radio Relay League, 2006. Print.