Contents

Carfield Block Diagram

Figure 1: Carfield Block Diagram

1 Carfield Documentation

2 Architecture

Carfield is organized in *domains*. As a mixed-criticality system (MCS), each domain serves different purposes in terms of functional safety and reliability, security, and computation capabilities.

Carfield relies on Cheshire as its host domain, and extends its minimal SoC with additional interconnect ports and interrupts.

The above block diagram depicts a fully-featured Carfield SoC, which currently provides:

- **Domains**:
  - *Host domain* (Cheshire), a Linux-capable RV64 system based on dual-core CVA6 processors with self-invalidation coherency mechanism
  - *Safe domain*, a Triple-Core-Lockstep (TCLS) RV32 microcontroller system based on CV32E40P, with fast interrupt handling through the RISC-V CLIC
  - *Secure domain*, a Dual-Core-Lockstep (DCLS) RV32 Hardware Root of Trust (HW RoT) systems that ensures the secure boot for the whole platform, serves as secure monitor for the entire system, and provides crypto acceleration services through various crypto-accelerators
  - *Accelerator domain*, comprises two programmable multi-core accelerators (PMCAs), an 12-cores integer cluster with Hybrid Modular Redundancy (HMR) capabilities oriented to compute intensive integer workloads such as AI, and a vectorial cluster with floating point vector processing capabilities to accelerate intensive control tasks
- **On-chip and off-chip memory endpoints**:
  - *Dynamic SPM*: dynamically configurable scratchpad memory (SPM) for *interleaved* or *contiguous* accesses aiming at reducing systematic bus conflicts to improve the time-predictability of the on-chip communication
  - *Partitionable hybrid LLC SPM*: the last-level cache (*host domain*) can be configured as SPM at runtime, as described in Cheshire's Architecture
  - *External DRAM*: off-chip HyperRAM (Infineon) interfaced with in-house, open-source AXI4 Hyberbus memory controller and digital PHY connected to Cheshire's LLC

- **Mailbox unit**
  - Main communication vehicle among domains, based on an interrupt notification mechanism
- **Platform control registers (PCRs)**
  - Management and control registers for the entire platform, control clock sources assignments, clock gating, isolation.
- **Interconnect** (as in Cheshire):
  - A last level cache (LLC) configurable as a scratchpad memory (SPM) per-way
  - Up to 16 external AXI4 manager ports and 16 AXI and Regbus subordinate ports
  - Per-manager AXI4 traffic regulators for real-time applications
  - Per-manager AXI4 bus error units (UNBENT) for interconnect error handling
- **Interrupts** (as in Cheshire):
  - Core-local (CLINT *and* CLIC) and platform (PLIC) interrupt controllers
  - Dynamic interrupt routing from and to internal and external targets.
- **Peripherals**:
  - Generic timers
  - PWM timers
  - Watchdog timer
  - Ethernet
  - CAN

2.1 Memory Map

This section shows Carfield's memory map. The group `Internal to Cheshire` in the table below only recalls the memory map described in the dedicatd documentation for Cheshire and is explicitely shown here for clarity.

Start Address	End Address (excl.)	Length	Size	Permissions	Cacheable	Atomics	Region	Device
Internal to Cheshire								
`0x0000_0000`	`0x0004_0000`	`0x04_0000`	256 KiB	(debug)			Debug	Debug CVA6
`0x0004_0000`	`0x0100_0000`							*Reserved*
`0x0100_0000`	`0x0100_1000`	`0x00_1000`	4 KiB	rw			Config	AXI_DMA_Config
`0x0100_1000`	`0x0200_0000`							*Reserved*
`0x0200_0000`	`0x0204_0000`	`0x04_0000`	256 KiB	rx			Memory	Boot ROM

Start Address	End Address (excl.)	Length	Size	Permissions	Cacheable	Atomics	Region	Device
0x0204_0000	0x0208_0000	0x04_0000	256 KiB	rw			Irq	CLINT
0x0208_0000	0x020c_0000	0x04_0000	256 KiB	rw			Irq	IRQ_Routing
0x020c_0000	0x0210_0000	0x04_0000	256 KiB	rw			Irq	AXI_REALM_unit
0x020c_0000	0x0300_0000						*Reserved*	
0x0300_0000	0x0300_1000	0x00_1000	4 KiB	rw			Config	Cheshire_PCRs
0x0300_1000	0x0300_2000	0x00_1000	4 KiB	rw			Config	LLC
0x0300_2000	0x0300_3000	0x00_1000	4 KiB	rw			I/O	UART
0x0300_3000	0x0300_4000	0x00_1000	4 KiB	rw			I/O	I2C
0x0300_4000	0x0300_5000	0x00_1000	4 KiB	rw			I/O	SPIM
0x0300_5000	0x0300_6000	0x00_1000	4 KiB	rw			I/O	GPIO
0x0300_6000	0x0300_7000	0x00_1000	4 KiB	rw			Config	Serial_Link
0x0300_7000	0x0300_8000	0x00_1000	4 KiB	rw			Config	VGA
0x0300_8000	0x0300_A000	0x00_1000	8 KiB	rw			Config	UNBENT (bus error unit)
0x0300_A000	0x0300_B000	0x00_1000	4 KiB	rw			Config	Tagger (LLC partitioning)
0x0300_8000	0x0400_0000						*Reserved*	
0x0400_0000	0x1000_0000	0x40_0000	64 MiB	rw			Irq	PLIC
0x0800_0000	0x0C00_0000	0x40_0000	64 MiB	rw			Irq	CLIC_INT, CLIC_TV, CLIC_VS, MCLIC
0x1000_0000	0x1400_0000	0x40_0000	64 MiB	rwx	yes	yes	Memory	LLC_Scratchpad
0x1400_0000	0x1800_0000	0x40_0000	64 MiB	rwx		yes	Memory	LLC_Scratchpad
0x1800_0000	0x2000_0000						*Reserved*	
External to Cheshire				rw				
0x2000_0000	0x2000_1000	0x00_1000	4 KiB	rw			I/O	Ethernet
0x2000_1000	0x2000_2000	0x00_1000	4 KiB	rw			I/O	CAN_BUS

Start Address	End Address (excl.)	Length	Size	Permissions	Cacheable	Atomics	Region	Device
0x2000_2000	0x2000_3000	0x00_1000	4 KiB	rw			I/O	(empty)
0x2000_3000	0x2000_4000	0x00_1000	4 KiB	rw			I/O	(empty)
0x2000_4000	0x2000_5000	0x00_1000	4 KiB	rw			I/O	GP_timer_1 (System timer)
0x2000_5000	0x2000_6000	0x00_1000	4 KiB	rw			I/O	GP_timer_2 (Advanced timer)
0x2000_6000	0x2000_7000	0x00_1000	4 KiB	rw			I/O	GP timer 3
0x2000_7000	0x2000_8000	0x00_1000	4 KiB	rw			I/O	Watchdog_time
0x2000_8000	0x2000_9000	0x00_1000	4 KiB	rw			I/O	(empty)
0x2000_9000	0x2000_a000	0x00_1000	4 KiB	rw			I/O	HyperBUS
0x2000_a000	0x2000_b000	0x00_1000	4 KiB	rw			I/O	Pad Config
0x2000_b000	0x2000_c000	0x00_1000	4 KiB	rw			I/O	L2_ECC_Config
0x2001_0000	0x2001_1000	0x00_1000	4 KiB	rw			I/O	Carfield_Control_and_Status
0x2002_0000	0x2002_1000	0x00_1000	4 KiB	rw			I/O	(if any) PLL/CLOCK
0x2800_1000	0x4000_0000						*Reserved*	
0x4000_0000	0x4000_1000	0x00_1000	4 KiB	rw			Irq	Mailboxes
0x4000_1000	0x5000_0000						*Reserved*	
0x5000_0000	0x5080_0000	0x80_0000	8 MiB	rw			Accelerators	Integer_Cluster
0x5080_0000	0x5100_0000						*Reserved*	
0x5100_0000	0x5180_0000	0x80_0000	8 MiB	rw			Accelerators	FP_Cluster
0x5100_0000	0x6000_0000						*Reserved*	
0x6000_0000	0x6002_0000	0x02_0000	128 KiB	rw		yes	Safe domain	Safety Island Memory
0x6002_0000	0x6020_0000	0x1e_0000		rw			Safe domain	reserved
0x6020_0000	0x6030_0000	0x10_0000	1 MiB	rw		yes	Safe domain	Safety_Island_Peripherals

Start Address	End Address (excl.)	Length	Size	Permissions	Cacheable	Atomics	Region	Device
0x6030_0000	0x6080_0000	0x50_0000		rw			Safe domain	reserved
0x6080_0000	0x7000_0000						*Reserved*	
0x7000_0000	0x7002_0000	0x02_0000	128 KiB	rwx	yes	yes	Memory	LLC Scratchpad
0x7800_0000	0x7810_0000	0x10_0000	1 MiB	rwx	yes	yes	Memory	L2 Scratchpad (Port 1, interleaved)
0x7810_0000	0x7820_0000	0x10_0000	1 MiB	rwx	yes	yes	Memory	L2 Scratchpad (Port 1, non-interleaved)
0x7820_0000	0x7830_0000	0x10_0000	1 MiB	rwx	yes	yes	Memory	L2 Scratchpad (Port 2, interleaved)
0x7830_0000	0x7840_0000	0x10_0000	1 MiB	rwx	yes	yes	Memory	L2 Scratchpad (Port 2, non-interleaved)
0x8000_0000	0x20_8000_0000	0x20_0000_0000	128 GiB	rwx	yes	yes	Memory	LLC/DRAM

2.2 Interrupt map

Carfield's interrupt components are exhaustivly described in the dedicated section of the documentation for Cheshire. This section describes Carfield's interrupt map.

Interrupt Source	Interrupt sink	Bitwidth	Connection	Type	Comment
Carfield peripherals					
`intr_wkup_timer_expired_o`		1	`car_wdt_intrs[0]`	level-sensitive	
`intr_wdog_timer_bark_o`		1	`car_wdt_intrs[1]`	level-sensitive	
`nmi_wdog_timer_bark_o`		1	`car_wdt_intrs[2]`	level-sensitive	
`wkup_req_o`		1	`car_wdt_intrs[3]`	level-sensitive	
`aon_timer_rst_req_o`		1	`car_wdt_intrs[4]`	level-sensitive	
`irq`		1	`car_can_intr`	level-sensitive	
`ch_0_o[0]`		1	`car_adv_timer_ch0`	edge-sensitive	
`ch_0_o[1]`		1	`car_adv_timer_ch1`	edge-sensitive	

Interrupt Source	Interrupt sink	Bitwidth	Connection	Type	Comment
ch_0_o[2]		1	car_adv_timer_ch2	edge-sensitive	
ch_0_o[3]		1	car_adv_timer_ch3	edge-sensitive	
events_o[0]		1	car_adv_timer_events[0]	edge-sensitive	
events_o[1]		1	car_adv_timer_events[1]	edge-sensitive	
events_o[2]		1	car_adv_timer_events[2]	edge-sensitive	
events_o[3]		1	car_adv_timer_events[3]	edge-sensitive	
irq_lo_o		1	car_sys_timer_lo	edge-sensitive	
irq_hi_o		1	car_sys_timer_hi	edge-sensitive	
Cheshire peripherals					
zero		1	zero	level-sensitive	
uart		1	uart	level-sensitive	
i2c_fmt_threshold		1	i2c_fmt_threshold	level-sensitive	
i2c_rx_threshold		1	i2c_rx_threshold	level-sensitive	
i2c_fmt_overflow		1	i2c_fmt_overflow	level-sensitive	
i2c_rx_overflow		1	i2c_rx_overflow	level-sensitive	
i2c_nak		1	i2c_nak	level-sensitive	
i2c_scl_interference		1	i2c_scl_interference	level-sensitive	
i2c_sda_interference		1	i2c_sda_interference	level-sensitive	
i2c_stretch_timeout		1	i2c_stretch_timeout	level-sensitive	
i2c_sda_unstable		1	i2c_sda_unstable	level-sensitive	
i2c_cmd_complete		1	i2c_cmd_complete	level-sensitive	
i2c_tx_stretch		1	i2c_tx_stretch	level-sensitive	

Interrupt Source	Interrupt sink	Bitwidth	Connection	Type	Comment
i2c_tx_overflow		1	i2c_tx_overflow	level-sensitive	
i2c_acq_full		1	i2c_acq_full	level-sensitive	
i2c_unexp_stop		1	i2c_unexp_stop	level-sensitive	
i2c_host_timeout		1	i2c_host_timeout	level-sensitive	
spih_error		1	spih_error	level-sensitive	
spih_spi_event		1	spih_spi_event	level-sensitive	
gpio		32	gpio	level-sensitive	
Spatz cluster					
	msip_i[0]	1	(hostd_spatzcl_mb_intr_ored[0] | safed_spatzcl_intr_mb[0])	level-sensitive	Snitch core #0
	msip_i[1]	1	(hostd_spatzcl_mb_intr_ored[1] | safed_spatzcl_intr_mb[1])	level-sensitive	Snitch core #1
	mtip_i[0]	1	chs_mti[0]	level-sensitive	Snitch core #0
	mtip_i[1]	1	chs_mti[1]	level-sensitive	Snitch core #1
	meip_i	2	\-		unconnected
	seip_i	2	\-		unconnected
HRM integer cluster					
eoc_o		1	pulpcl_eoc	level-sensitive	
	mbox_irq_i	1	(hostd_pulpcl_mb_intr_ored | safed_pulpcl_intr_mb)	level-sensitive	to offload binaries
Secure domain					
	irq_ibex_i	1	(hostd_secd_mb_intr_ored | safed_secd_intr_mb)	level-sensitive	to wake-up Ibex core
Safe domain					
	irqs_i[0]	1	hostd_safed_mbox_intr[0]	level-sensitive	from host domain CVA6#0

Interrupt Source	Interrupt sink	Bitwidth	Connection	Type	Comment
	irqs_i[1]	1	hostd_safed_mbox_intr[1]	level-sensitive	from host domain CVA6#1
	irqs_i[2]	1	secd_safed_mbox_intr	level-sensitive	from secure domain
	irqs_i[3]	1	pulpcl_safed_mbox_intr	level-sensitive	from HMR custer
	irqs_i[4]	1	spatzcl_safed_mbox_intr	level-sensitive	from vectorial cluster
	irqs[5]	1	irqs_distributed_249	level-sensitive	tied to 0
	irqs[6]	1	irqs_distributed_250	level-sensitive	host domain UART
	irqs[7]	1	irqs_distributed_251	level-sensitive	i2c_fmt_threshold
	irqs[8]	1	irqs_distributed_252	level-sensitive	i2c_rx_threshold
	irqs[9]	1	irqs_distributed_253	level-sensitive	i2c_fmt_overview
	irqs[10]	1	irqs_distributed_254	level-sensitive	i2c_rx_overflow
	irqs[11]	1	irqs_distributed_255	level-sensitive	i2c_nak
	irqs[12]	1	irqs_distributed_256	level-sensitive	i2c_scl_interference
	irqs[13]	1	irqs_distributed_257	level-sensitive	i2c_sda_interference
	irqs[14]	1	irqs_distributed_258	level-sensitive	i2c_stret h_timeout
	irqs[15]	1	irqs_distributed_259	level-sensitive	i2c_sda_unstable
	irqs[16]	1	irqs_distributed_260	level-sensitive	i2c_cmd_complete
	irqs[17]	1	irqs_distributed_261	level-sensitive	i2c_tx_stretch
	irqs[18]	1	irqs_distributed_262	level-sensitive	i2c_tx_overflow
	irqs[19]	1	irqs_distributed_263	level-sensitive	i2c_acq_full
	irqs[20]	1	irqs_distributed_264	level-sensitive	i2c_unexp_stop
	irqs[21]	1	irqs_distributed_265	level-sensitive	i2c_host_timeout

Interrupt Source	Interrupt sink	Bitwidth	Connection	Type	Comment
	irqs[22]	1	irqs_distributed_266	level-sensitive	spih_error
	irqs[23]	1	irqs_distributed_267	level-sensitive	spih_spi_event
	irqs[55:24]	32	irqs_distributed_299:268	level-sensitive	gpio
	irqs_i[56]	1	irqs_distributed_300	level-sensitive	pulpcl_eoc
	irqs_i[57]	1	irqs_distributed_309	level-sensitive	car_wdt_intrs[0]
	irqs_i[58]	1	irqs_distributed_310	level-sensitive	car_wdt_intrs[1]
	irqs_i[59]	1	irqs_distributed_311	level-sensitive	car_wdt_intrs[2]
	irqs_i[60]	1	irqs_distributed_312	level-sensitive	car_wdt_intrs[3]
	irqs_i[61]	1	irqs_distributed_313	level-sensitive	car_wdt_intrs[4]
	irqs_i[62]	1	irqs_distributed_314	level-sensitive	car_can_intr
	irqs_i[63]	1	irqs_distributed_315	edge-sensitive	car_adv_timer_ch0
	irqs_i[64]	1	irqs_distributed_316	edge-sensitive	car_adv_timer_ch1
	irqs_i[65]	1	irqs_distributed_317	edge-sensitive	car_adv_timer_ch2
	irqs_i[66]	1	irqs_distributed_318	edge-sensitive	car_adv_timer_ch3
	irqs_i[67]	1	irqs_distributed_319	edge-sensitive	car_adv_timer_events[0]
	irqs_i[68]	1	irqs_distributed_320	edge-sensitive	car_adv_timer_events[1]
	irqs_i[69]	1	irqs_distributed_321	edge-sensitive	car_adv_timer_events[2]
	irqs_i[70]	1	irqs_distributed_322	edge-sensitive	car_adv_timer_events[0]
	irqs_i[71]	1	irqs_distributed_323	edge-sensitive	car_sys_timer_lo
	irqs_i[72]	1	irqs_distributed_324	edge-sensitive	car_sys_timer_hi
	irqs_i[127:74]	54	irqs_distributed_331:325	-	tied to 0
Cheshire					
	intr_ext_i[0]	1	pulpcl_eoc	level-sensitive	from HMR cluster

Interrupt Source	Interrupt sink	Bitwidth	Connection	Type	Comment
	intr_ext_i	[2:1]	pulpcl_hostd_mbox_intr	level-sensitive	from HMR cluster
	intr_ext_i	[4:3]	spatzcl_hostd_mbox_intr	level-sensitive	from vectorial cluster
	intr_ext_i	[6:5]	safed_hostd_mbox_intr	level-sensitive	from safe domain
	intr_ext_i	[8:7]	secd_hostd_mbox_intr	level-sensitive	from secure domain
	intr_ext_i	[9]	car_wdt_intrs[0]	level-sensitive	from carfield peripherals
	intr_ext_i	[10]	car_wdt_intrs[1]	level-sensitive	from carfield peripherals
	intr_ext_i	[11]	car_wdt_intrs[2]	level-sensitive	from carfield peripherals
	intr_ext_i	[12]	car_wdt_intrs[3]	level-sensitive	from carfield peripherals
	intr_ext_i	[13]	car_wdt_intrs[4]	level-sensitive	from carfield peripherals
	intr_ext_i	[14]	car_can_intr	level-sensitive	from carfield peripherals
	intr_ext_i	[15]	car_adv_timer_ch0	edge-sensitive	from carfield peripherals
	intr_ext_i	[16]	car_adv_timer_ch1	edge-sensitive	from carfield peripherals
	intr_ext_i	[17]	car_adv_timer_ch2	edge-sensitive	from carfield peripherals
	intr_ext_i	[18]	car_adv_timer_ch3	edge-sensitive	from carfield peripherals
	intr_ext_i	[19]	car_adv_timer_events[0]	edge-sensitive	from carfield peripherals
	intr_ext_i	[20]	car_adv_timer_events[1]	edge-sensitive	from carfield peripherals
	intr_ext_i	[21]	car_adv_timer_events[2]	edge-sensitive	from carfield peripherals
	intr_ext_i	[22]	car_adv_timer_events[3]	edge-sensitive	from carfield peripherals
	intr_ext_i	[23]	car_sys_timer_lo	edge-sensitive	from carfield peripherals
	intr_ext_i	[24]	car_sys_timer_hi	edge-sensitive	from carfield peripherals
	intr_ext_i	[31:25]	0		tied to 0
meip_ext_o[0]	-			level-sensitive	unconnected

Interrupt Source	Interrupt sink	Bitwidth	Connection	Type	Comment
`meip_ext_o[1]`		-		level-sensitive	unconnected
`meip_ext_o[2]`		-		level-sensitive	unconnected
`seip_ext_o[0]`		-		level-sensitive	unconnected
`seip_ext_o[1]`		-		level-sensitive	unconnected
`seip_ext_o[2]`		-		level-sensitive	unconnected
`msip_ext_o[0]`		-		level-sensitive	unconnected
`msip_ext_o[1]`		-		level-sensitive	unconnected
`msip_ext_o[2]`		-		level-sensitive	unconnected
`mtip_ext_o[0]`		-		level-sensitive	Snitch core #0
`mtip_ext_o[1]`		-		level-sensitive	Snitch core #1
`mtip_ext_o[2]`		-		level-sensitive	unconnected

2.3 Domains

The total number of domains is 7: *host domain*, *safe domain*, *secure domain*, *integer PMCA domain*, *vectorial PMCA domain*, *peripheral domain*, *dynamic SPM*.

Carfield's domains live in dedicated repositories. We therefore invite the reader to consult the documentation of each domain.

For more information about domains' memory requirements, visit Synthesis and physical implementation.

Below, we focus on domains' parameterization within Carfield.

2.3.1 Host domain (Cheshire)

The *host domain* (Cheshire) embeds all the necessary components required to run OSs such as embedded Linux. It has two orthogonal *operation modes*.

1. *Untrusted mode*: in this operation mode, the host domain is tasked to run untrusted services, i.e. non time- and non safety-critical applications. For example, this could be the case of infotainment on a modern car. In this mode, as in traditional automotive platforms, safety and resiliency features are deferred to a dedicated 32-bit microcontroller-like system, called `safe domain` in Carfield.

2. *Hybrid trusted/untrusted mode*: in this operation mode, the host domain is in charge of both critical and non-critical applications. Key features supported to achieve this are:

- A virtualization layer, which allows the system to accommodate the execution of multiple OSs, including rich, Unix-like OSs and Real-Time OSs (RTOS), coexisting on the same HW.
- Spatial and temporal partitioning of resources: AXI matrix crossbar (AXI-REALM), LLC, TLB, and a `physical tagger` in front of the cores to mark partitions by acting directly on the physical address space
- Runtime configurable data/instruction cache and SPM
- Fast interrupt handling, with optional interrupt routing through the RISC-V fast interrupt controller CLIC,
- Configurable dual core setup between *lockstep* or *SMP* mode.

Hybrid operation mode is currently experimental, and mostly for research purposes. We advise of relying on a combination of host ad safe domain for a more traditional approach.

Cheshire is configured as follows:

- Two 64-bit, RISC-V CVA6 cores, with lightweight self-invalidation cache coherency, fast interrupt and virtualization support.
- 8 external AXI manager ports (`AxiNumExtSlv`) added to the matrix crossbar:
  - Dynamic SPM port 0
  - Dynamic SPM port 1
  - Safe domain
  - HMR cluster
  - Vectorial cluster
  - Mailbox unit
  - Ethernet
  - Peripherals
- 4 external AXI subordinate ports (`AxiNumExtMst`) added to the matrix crossbar:
  - Safe domain
  - Secure domain
  - HMR cluster
  - Vectorial cluster
- 4 external regbus subordinate ports (`NumTotalRegSlv`):
  - PCRs: control domains enable, clock gate, isolation
  - PLL control registers: for ASIC top-levels, leave unconnected otherwise
  - Padmux control registers: for ASIC top-levels, leave unconnected otherwise
  - Dynamic SPM ECC control registers
- AXI-REALM unit for bandwidth regulation and monitoring integrated in front of each AXI matrix crossbar manager
- Last-level cache (LLC) with HW spatial partitioning
- 32 *external* input interrupts (`CarfieldNumExtIntrs`), see Interrupt map in addition to Cheshire's own internal interrupts. Unused are tied to 0 (currently 9/32)

- 2 external interruptible harts (`CarfieldNumInterruptibleHarts`). The interruptible harts are Snitch core #0 and #1 in the vectorial cluster.
- An interrupt router with 1 external target (`CarfieldNUmRouterTargets`), tasked to distribute N input interrupts to M targets. In Carfield, the external target is the `safe domain`.
- All Cheshire peripherals, except for VGA

By default, Cheshire hosts 128KiB of hybrid LLC/SPM, user-configurable.

2.3.2 Safe domain

The *safe domain* is a simple MCU-like domain that comprises three 32-bit real-time CV32E40P (CV32RT) RISC-V cores operating in triple-core-lockstep mode (TCLS).

These cores, enhanced with the RISC-V CLIC controller and optimized for fast interrupt handling and context switch, run RTOSs and safety-critical applications, embodying a core tenet of the platform reliability.

The *safe domain* is essential when the *host domain* is operated in *untrusted* mode.

The *safe domain* is configured as follows:

- 1 RISC-V debug module prividing indipendent JTAG interface off-Carfield
- 1 AXI manager and 1 AXI subordinate ports, 32-bit data and 32-bit address wide, to and from the *host domain*, respectively. AXI datawidth conversion with the host domain is handled internally to the safe domain.
- 1 generic timer, essential for periodic ticks common in RTOSs. The generic timer in the *safe domain* is the same integrated in Carfield's *peripheral domain*.
- CLIC RISC-V interrupt controller; as opposed to Cheshire, currently the CLIC is configured to run run in M-mode.
- 128 *external* input interrupts. Unused are tied to 0.
- Fast interrupt extension that extends CV32 with additional logic to accelerate context switching. From here, the name CV32RT
- 1 32-bit per-core FPU with down to float-16 precision, totaling 3 FPUs

By default, the processing elements share access to 128KiB of SPM for instructions and data, user-configurable.

2.3.3 Secure domain

The secure domain, based on the OpenTitan project, serves as the Hardware Root-of-Trust (HWRoT) of the platform. It handles *secure boot* and system integrity monitoring fully in HW through cryptographic acceleration services.

Compared to vanilla OpenTitan, the secure domain integrated in Carfield is modified/configured as follows:

- 1 AXI4 manager interface to Carfield, with a bridge between AXI4 and TileLink Uncached Lightweight (TL-UL) internally used by OpenTitan. By only exposing a manager port, unwanted access to the secure domain is prevented.

- Embedded flash memory replaced with an SRAM preloaded before secure boot procedure from an external SPI flash through OpenTitan private SPI peripheral. Once preload is over, the OpenTitan secure boot framework is unchanged compared to the vanilla version.
- Finally, a *boot manager* module has been designed and integrated to manage the two available bootmodes. In **Secure** mode, the systems executes the secure boot framework as soon as the reset is asserted, loading code from the external SPI and performing the signature check on its content. Otherwise, in **Non-secure** mode, the *secure domain* is clock gated and must be clocked and woken-up by an external entity (e.g., *host domain*)

By default, the secure domain hosts 512KiB of main SPM, and 16KiB of OTP memory, user-configurable.

2.3.4 Accelerator domain

To augment computational capabilities, Carfield incorporates two PMCAs, described below. Both PMCAs integrate DMA engines to independently fetch data from the on-chip SPM or external DRAM.

2.3.4.1 HMR integer PMCA The hybrid modular redundancy (HMR) *integer PMCA* is specialized in accelerating the inference of Deep Learning and Machine Learning models. The multicore accelerator is built around 12 32-bit RISC-V cores empowered with ISA extensions, enabling integer arithmetic from 32-bit down to 2-bit precision.

The integer PMCA does not integrate a fully-fledged FPU co-processor. Nevertheless, it features a highly specialized domain specific accelerator (DSA), RedMulE, which enables fast and energy-efficient floating-point GEMM on 16-bit and 8-bit data formats. This makes the PMCA capable of on-chip training of generalized Deep Learning models.

As part of a MCS, the integer PMCA's general-purpose cores can be reconfigured for *redundant execution*. A Hybrid Modular Redundancy (HMR) unit allows the split/lock of the available cores in different redundant configurations during runtime, trading off the computing performance and the fault resilience capability according to the criticality of the application.

The PMCA can be configured in multiple redundant modes: * **Independent:** All cores act independently with no redundancy mechanism. This configuration allows higher performance but has no reliability. * **Dual Modular Redundancy (DMR)**: The cores are grouped in lock-stepped pairs and rely on a specialized hardware extension for fast fault recovery in less than 30 clock cycles in case of fault detection. The PMCA provides the best trade-off between performance and fault recovery in this configuration. * **Triple Modular Redundancy (TMR)**: The cores are grouped in lock-stepped triplets and rely on either hardware extension or software mechanisms to recover from incurring faults. The PMCA provides the highest fault resilience in this configuration, at the cost of reduced performance.

By default, the integer PMCA's processing elements and tensor accelerator share access to 256KiB of L1 SPM, user-configurable.

2.3.4.2 Vectorial PMCA

The *vectorial PMCA*, or Spatz PMCA handles vectorizable multi-format floating-point workloads.

A Spatz vector unit acts as a coprocessor of the Snitch core, a tiny RV32IMA core which decodes and forwards vector instructions to the vector unit.

A Snitch core and a Spatz vector unit are together referred to as *Core Complex (CC)*. The vectorial PMCA is composed by two CCs, each with the following configuration:

- 2 KiB of latch-based VRF
- 4 transprecision FPUs
- 1 integer processing unit (IPU)

Each FPU supports *FP8*, *FP16*, *FP32*, and *FP64* computation, while the IPU supports 8, 16, 32, and 64-bit integer computation.

By default, the CCs share access to 128KiB of L1 SPM, user-configurable.

2.4 On-chip and off-chip memory endpoints

2.4.1 Dynamic scratchpad memory (SPM)

The dynamic SPM features dynamically switching address mapping policy. It manages the following features:

- Two AXI subordinate ports
- Two address mapping modes: *interleaved* and *contiguous*
- 4 address spaces, 2 for each port. The address space is used to select the AXI port to use, and the mapping mode
- Every address space points to the same physical SRAM through a low-latency matrix crossbar
- ECC-equipped memory banks

By default, Carfield hosts 1MiB of dynamic SPM, user-configurable.

2.4.2 Partitionable hybrid LLC/SPM

Carfield hosts a LLC optionaly reconfigurable as SPM during runtime. In addition, the LLC supports HW-based partitioning to exploit intra-process or inter-processes isolation, improving the system's predictability. The LLC is described in detail in Cheshire's Architecture.

2.4.3 HyperBus off-chip link

Carfield integrates a in-house, open-source implementation of Infineon' HyperBus off-chip controller to connect to external HyperRAM modules.

It manages the following features:

- An AXI interface that attaches to Cheshire's partitionable hybrid LLC/SPM

- A configurable number of physical HyperRAM chips it can be attached to; by default, support for 2 physical chips is provided
- Support for HyperRAM chips with different densities (from 8MiB to 64MiB per chip aligned with specs).

2.5 System bus interconnect

The interconnect is composed of a main AXI4 matrix (or crossbar) with AXI5 atomic operations (ATOPs) support. The crossbar extends Cheshire's with additional external AXI manager and subordinate ports.

Cheshire's auxiliary Regbus demultiplexer is extended with additional peripheral configuration ports for external PLL/FLL and padmux configuration, which are specific of ASIC wrappers.

An additional peripheral subsystem based on APB hosts Carfield-specific peripherals.

2.6 Mailbox unit

The mailbox unit consists in a number of configurable mailboxes. Each mailbox is the preferred communication vehicle between *domains*. It can be used to wake-up certain domains, notify an *offloader* (e.g., Cheshire) that a *target device* (e.g., the integer PMCA) has reached execution completion, dispatch *entry points* to a *target device* to jump-start its execution, and many others.

It manages the following features:

- Interrupt based signaling receiver and sender
- A shared memory space common to all the mailboxes, implemented as a single register file. Currently, Carfield implements 25 mailboxes.
- Support for 32-bit word aligned read/write access.
- A convenience AXI-Lite wrapper for the configuration port.

Assuming each mailbox is identified with id `i`, the register file map reads:

Offset	Register	Width (bit)	Note
`0x00 + i * 0x100`	`INT_SND_STAT`	1	current irq status
`0x04 + i * 0x100`	`INT_SND_SET`	1	set irq
`0x08 + i * 0x100`	`INT_SND_CLR`	1	clear irq
`0x0C + i * 0x100`	`INT_SND_EN`	1	enable irq
`0x40 + i * 0x100`	`INT_RCV_STAT`	1	current irq status
`0x44 + i * 0x100`	`INT_RCV_SET`	1	set irq
`0x48 + i * 0x100`	`INT_RCV_CLR`	1	clear irq
`0x4C + i * 0x100`	`INT_RCV_EN`	1	enable irq
`0x80 + i * 0x100`	`LETTER0`	32	message
`0x8C + i * 0x100`	`LETTER1`	32	message

The above register map can be found in the dedicated repository and is reported here for convenience.

2.7 Platform control registers

PCRs provide basic system information, and control clock, reset and other functionalities of Carfield's *domains*.

A more detailed overview of each PCR (register subfields and description) can be found here. PCR base address is listed in the Memory Map as for the other devices.

Name	Offset	Length	Description
VERSION0	0x0	4	Cheshire sha256 commit
VERSION1	0x4	4	Safety Island sha256 commit
VERSION2	0x8	4	Security Island sha256 commit
VERSION3	0xc	4	PULP Cluster sha256 commit
VERSION4	0x10	4	Spatz CLuster sha256 commit
JEDEC_IDCODE	0x14	4	JEDEC ID CODE
GENERIC_SCRATCH0	0x18	4	Scratch
GENERIC_SCRATCH1	0x1c	4	Scratch
HOST_RST	0x20	4	Host Domain reset -active high, inverted in HW-
PERIPH_RST	0x24	4	Periph Domain reset -active high, inverted in HW-
SAFETY_ISLAND_RST	0x28	4	Safety Island reset -active high, inverted in HW-
SECURITY_ISLAND_RST	0x2c	4	Security Island reset -active high, inverted in HW-
PULP_CLUSTER_RST	0x30	4	PULP Cluster reset -active high, inverted in HW-
SPATZ_CLUSTER_RST	0x34	4	Spatz Cluster reset -active high, inverted in HW-
L2_RST	0x38	4	L2 reset -active high, inverted in HW-
PERIPH_ISOLATE	0x3c	4	Periph Domain AXI isolate
SAFETY_ISLAND_ISOLATE	0x40	4	Safety Island AXI isolate
SECURITY_ISLAND_ISOLATE	0x44	4	Security Island AXI isolate
PULP_CLUSTER_ISOLATE	0x48	4	PULP Cluster AXI isolate
SPATZ_CLUSTER_ISOLATE	0x4c	4	Spatz Cluster AXI isolate
L2_ISOLATE	0x50	4	L2 AXI isolate
PERIPH_ISOLATE_STATUS	0x54	4	Periph Domain AXI isolate status
SAFETY_ISLAND_ISOLATE_STATUS	0x58	4	Safety Island AXI isolate status
SECURITY_ISLAND_ISOLATE_STATUS	0x5c	4	Security Island AXI isolate status
PULP_CLUSTER_ISOLATE_STATUS	0x60	4	PULP Cluster AXI isolate status
SPATZ_CLUSTER_ISOLATE_STATUS	0x64	4	Spatz Cluster AXI isolate status
L2_ISOLATE_STATUS	0x68	4	L2 AXI isolate status
PERIPH_CLK_EN	0x6c	4	Periph Domain clk gate enable
SAFETY_ISLAND_CLK_EN	0x70	4	Safety Island clk gate enable
SECURITY_ISLAND_CLK_EN	0x74	4	Security Island clk gate enable
PULP_CLUSTER_CLK_EN	0x78	4	PULP Cluster clk gate enable
SPATZ_CLUSTER_CLK_EN	0x7c	4	Spatz Cluster clk gate enable
L2_CLK_EN	0x80	4	Shared L2 memory clk gate enable
PERIPH_CLK_SEL	0x84	4	Periph Domain pll select (0 -> host pll, 1 -> alt PLL, 2 -> per pll)
SAFETY_ISLAND_CLK_SEL	0x88	4	Safety Island pll select (0 -> host pll, 1 -> alt PLL, 2 -> per pll)

Name	Offset	Length	Description
SECURITY_ISLAND_CLK_SEL	0x8c	4	Security Island pll select (0 -> host pll, 1 -> alt PLL, 2 -> per pll)
PULP_CLUSTER_CLK_SEL	0x90	4	PULP Cluster pll select (0 -> host pll, 1 -> alt PLL, 2 -> per pll)
SPATZ_CLUSTER_CLK_SEL	0x94	4	Spatz Cluster pll select (0 -> host pll, 1 -> alt PLL, 2 -> per pll)
L2_CLK_SEL	0x98	4	L2 Memory pll select (0 -> host pll, 1 -> alt PLL, 2 -> per pll)
PERIPH_CLK_DIV_VALUE	0x9c	4	Periph Domain clk divider value
SAFETY_ISLAND_CLK_DIV_VALUE	0xa0	4	Safety Island clk divider value
SECURITY_ISLAND_CLK_DIV_VALUE	0xa4	4	Security Island clk divider value
PULP_CLUSTER_CLK_DIV_VALUE	0xa8	4	PULP Cluster clk divider value
SPATZ_CLUSTER_CLK_DIV_VALUE	0xac	4	Spatz Cluster clk divider value
L2_CLK_DIV_VALUE	0xb0	4	L2 Memory clk divider value
HOST_FETCH_ENABLE	0xb4	4	Host Domain fetch enable
SAFETY_ISLAND_FETCH_ENABLE	0xb8	4	Safety Island fetch enable
SECURITY_ISLAND_FETCH_ENABLE	0xbc	4	Security Island fetch enable
PULP_CLUSTER_FETCH_ENABLE	0xc0	4	PULP Cluster fetch enable
SPATZ_CLUSTER_DEBUG_REQ	0xc4	4	Spatz Cluster debug req
HOST_BOOT_ADDR	0xc8	4	Host boot address
SAFETY_ISLAND_BOOT_ADDR	0xcc	4	Safety Island boot address
SECURITY_ISLAND_BOOT_ADDR	0xd0	4	Security Island boot address
PULP_CLUSTER_BOOT_ADDR	0xd4	4	PULP Cluster boot address
SPATZ_CLUSTER_BOOT_ADDR	0xd8	4	Spatz Cluster boot address
PULP_CLUSTER_BOOT_ENABLE	0xdc	4	PULP Cluster boot enable
SPATZ_CLUSTER_BUSY	0xe0	4	Spatz Cluster busy
PULP_CLUSTER_BUSY	0xe4	4	PULP Cluster busy
PULP_CLUSTER_EOC	0xe8	4	PULP Cluster end of computation
ETH_RGMII_PHY_CLK_DIV_EN	0xec	4	Ethernet RGMII PHY clock divider enable bit
ETH_RGMII_PHY_CLK_DIV_VALUE	0xf0	4	Ethernet RGMII PHY clock divider value
ETH_MDIO_CLK_DIV_EN	0xf4	4	Ethernet MDIO clock divider enable bit
ETH_MDIO_CLK_DIV_VALUE	0xf8	4	Ethernet MDIO clock divider value

2.8 Peripherals

Carfield enhances Cheshire's peripheral subsystem with additional capabilities.

An external AXI manager port is attached to the matrix crossbar. The 64-bit data, 48-bit address AXI protocol is converted to the slower, 32-bit data and address APB protocol. An APB demultiplexer allows attaching several peripherals, described below.

2.8.1 Generic and advanced timer

Carfield integrates a generic timer and an advanced timer.

The *generic timer* manages the following features:

- 2 general purpose 32-bit up counter timers
- Input trigger sources:
  - FLL/PLL clock
  - FLL/PLL clock + Prescaler
  - Real-time clock (RTC) at crystal frequency (32kHz) or higher
  - External event
- 8-bit programmable prescaler to FLL/PLL clock
- Counting modes:
  - One shot mode: timer is stopped after first comparison match
  - Continuous mode: timer continues counting after comparison match
  - Cycle mode: timer resets to 0 after comparison match and continues counting
  - 64 bit cascaded mode
- Interrupt request generation on comparison match

For more information, read the dedicated documentation.

The *advanced timer* manages the following features:

- 4 timers with 4 output signal channels each
- PWM generation functionality
- Multiple trigger input sources:
  - output signal channels of all timers
  - 32 GPIOs
  - Real-time clock (RTC) at crystal frequency (32kHz) or higher
  - FLL/PLL clock In Carfield, we rely on a RTC.
- Configurable input trigger modes
- Configurable prescaler for each timer
- Configurable counting mode for each timer
- Configurable channel threshold action for each timer
- 4 configurable output events
- Configurable clock gating of each timer

For more information, read the dedicated documentation.

2.8.2 Watchdog timer

We employ the watchdog timer developed by the OpenTitan project project. It manages the following features:

- Two 32-bit upcounting timers: one timer functions as a wakeup timer, one as a watchdog timer
- 2 thresholds: *bark* (generates an interrupt) and *bite* (resets core)
- A 12 bit pre-scaler for the wakeup timer to enable very long timeouts

For more information, read the dedicated documentation.

Reset and Clock Distribution for a domain X

Figure 2: Reset and Clock Distribution for a domain X

Isolation for a domain X

Figure 3: Isolation for a domain X

2.8.3 CAN

We employ a CAN device developed by the Czech Technical University in Prague. It manages the following features:

- CAN 2.0, CAN FD 1.0 and ISO CAN FD
- Avalon memory bus
- Timestamping and transmission at given time
- Optional event and error logging
- Fault confinement state manipulation
- Transceiver delay measurement
- Variety of interrupt sources
- Filtering of received frame
- Listen-only mode, Self-test mode, Acknowledge forbidden mode
- Up to 14 Mbit in "Data" bit-rate (with 100 Mhz Core clock)

For more information, read the dedicated documentation

2.8.4 Ethernet

We employ Ethernet IPs developed by Alex Forencich and assemble them with a high-performant DMA, the same used in Cheshire.

We use Reduced gigabit media-independent interface (RGMII) that supports speed up to 1000Mbit/s (1GHz).

For more information, read the dedicated documentation of Ethernet components from its original repository.

2.9 Clock and reset

The two figures above show the clock, reset and isolation distribution for a *domain* `X` in Carfield, and their relationship. A more detailed description is provided below.

2.9.1 Clock distribution scheme, clock gating and isolation

Carfield is provided with 3 clocks sources. They can be fully asynchronous and not bound to any phase relationship, since dual-clock FIFOs are placed between domains to allow clock domain crossing (CDC):

- `host_clk_i`: preferably, clock of the *host domain*
- `alt_clk_i`: preferably, clock of *alternate* domains, namely *safe domain*, *secure domain*, *accelerator domain*
- `per_clk_i`: preferably, clock of *peripheral domain*

In addition, a real-time clock (RTC, `rt_clk_i`) is provided externally, at crystal frequency (32kHz) or higher.

These clocks are supplied externally, by a dedicated PLL per clock source or by a single PLL that supplies all three clock sources. The configuration of the clock source can be handled by the external PLL wrapper configuration registers, e.g. in a ASIC top level

Regardless of the specific name used for the clock signals in HW, Carfield has a flexible clock distribution that allows each of the 3 clock sources to be assigned to a *domain*, as explained below.

As the top figure shows, out of the 7 *domains* described in Domains, 6 can be clock gated and *isolated*: *safe domain*, *secure domain*, *accelerator domain*, *peripheral domain*, *dynamic SPM*.

When *isolation* for a domain `X` is enabled, data transfers towards a domain are terminated and never reach it. To achieve this, an AXI4 compliant *isolation* module is placed in front of each domain. The bottom figure shows in detail the architecture of the isolation scheme between the *host domain* and a generic `X` domain, highlighting its relationship with the domain's reset and cloc signals.

For each of the 6 clock gateable domains, the following clock distribution scheme applies:

1. The user selects one of the 3 different clock sources
2. The selected clock source for the domain is fed into a default-bypassed arbitrary integer clock divider with 50% duty cycle. This allows to use different integer clock divisions for every target domain to use different clock frequencies
3. The internal clock gate of the clock divider is used to provide clock gating for the domain.

HW resources for the clock distribution (steps 1., 2., and 3.) and isolation of a domain `X`, are SW-controlled via dedicated PCRs. Refer to Platform Control Registers in this page for more information.

The only domain that is always-on and de-isolated is the *host domain* (Cheshire). If required, clock gating and/or isolation of it can be handled at higher levels of hierarchy, e.g. in a dedicated ASIC wrapper.

2.9.2 Startup behavior after Power-on reset (POR)

The user can decide whether *secure boot* must be performed on the executing code before runtime. If so, the *secure domain* must be active after POR, i.e., clocked and de-isolated. This behavior is regulated by the input pin `secure_boot_i` according to the following table:

secure_boot_i	Secure Boot	System status after POR
0	OFF	*secure domain* gated and isolated as the other 5 domains, *host domain* always-on and idle
1	ON	*host domain* always-on and idle, *secure domain* active, takes over *secure boot* and can't be warm reset-ed; other 5 domains gated and isolated

Regardless of the value of `secure_boot_i`, since by default some domains are clock gated and isolated after POR, SW or external physical interfaces (JTAG/Serial Link) must handle their wake-up process. Routines are provided in the Software Stack.

2.9.3 Reset distribution scheme

Carfield is provided with one POR (active-low), `pwr_on_rst_ni`, responsible for the platform's *cold reset*.

The POR is synchronized with the clock of each domain, user-selected as explained above, and propagated to the domain.

In addition, a *warm reset* can be initiated from SW through the PCRs for each domain. Exceptions to this are the *host domain* (always-on), and the *secure domain* when `secure_boot_i` is asserted.

2.10 axi_dma_config / doc / idma_desc64_frontend_doc.md

2.11 Summary

Name	Offset	Length	Description
idma_desc64.desc_addr	0x0	8	This register specifies the bus address at which the first transfer
idma_desc64.status	0x8	8	This register contains status information for the DMA.

2.12 desc_addr

This register specifies the bus address at which the first transfer descriptor can be found. A write to this register starts the transfer. - Offset: `0x0` - Reset default: `0xffffffffffffffff` - Reset mask: `0xffffffffffffffff`

2.12.1 Fields

{"reg": [{"name": "desc_addr", "bits": 64, "attr": ["wo"], "rotate": 0}], "config": {"lanes":

Bits	Type	Reset	Name	Description
63:0	wo	0xffffffffffffffff	desc_addr	

2.13 status

This register contains status information for the DMA. - Offset: `0x8` - Reset default: `0x0` - Reset mask: `0x3`

2.13.1 Fields


```
{"reg": [{"name": "busy", "bits": 1, "attr": ["ro"], "rotate": -90}, {"name": "fifo_full", "bi
```


Bits	Type	Reset	Name	Description
63:2				Reserved
1	ro	0x0	fifo_full	If this bit is set, the buffers of the DMA are full. Any further submissions via the desc_addr register may overwrite previously submitted jobs or get lost.
0	ro	0x0	busy	The DMA is busy

2.14 axi_dma_config / doc / idma_reg32_2d_frontend_doc.md

2.15 Summary

Name	Offset	Length	Description
idma_reg32_2d_frontend.src_addr	0x0	4	Source Address
idma_reg32_2d_frontend.dst_addr	0x4	4	Destination Address
idma_reg32_2d_frontend.num_bytes	0x8	4	Number of bytes
idma_reg32_2d_frontend.conf	0xc	4	Configuration Register for DMA settings
idma_reg32_2d_frontend.stride_src	0x10	4	Source Stride
idma_reg32_2d_frontend.stride_dst	0x14	4	Destination Stride
idma_reg32_2d_frontend.num_repetitions	0x18	4	Number of 2D repetitions
idma_reg32_2d_frontend.status	0x1c	4	DMA Status
idma_reg32_2d_frontend.next_id	0x20	4	Next ID, launches transfer, returns 0 if transfer not set up properly.
idma_reg32_2d_frontend.done	0x24	4	Get ID of finished transactions.

2.16 src_addr

Source Address - Offset: `0x0` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.16.1 Fields

{"reg": [{"name": "src_addr", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1

Bits	Type	Reset	Name	Description
31:0	rw	0x0	src_addr	Source Address

2.17 dst_addr

Destination Address - Offset: `0x4` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.17.1 Fields

{"reg": [{"name": "dst_addr", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1

Bits	Type	Reset	Name	Description
31:0	rw	0x0	dst_addr	Destination Address

2.18 num_bytes

Number of bytes - Offset: `0x8` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.18.1 Fields

{"reg": [{"name": "num_bytes", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes":

Bits	Type	Reset	Name	Description
31:0	rw	0x0	num_bytes	Number of bytes

2.19 conf

Configuration Register for DMA settings - Offset: `0xc` - Reset default: `0x0` - Reset mask: `0xf`

2.19.1 Fields

{"reg": [{"name": "decouple", "bits": 1, "attr": ["rw"], "rotate": -90}, {"name": "deburst", "

Bits	Type	Reset	Name	Description
31:4				Reserved
3	rw	0x0	twod	2D transfer
2	rw	0x0	serialize	Serialize enable
1	rw	0x0	deburst	Deburst enable
0	rw	0x0	decouple	Decouple enable

2.20 stride_src

Source Stride - Offset: `0x10` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.20.1 Fields

{"reg": [{"name": "stride_src", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes":

Bits	Type	Reset	Name	Description
31:0	rw	0x0	stride_src	Source Stride

2.21 stride_dst

Destination Stride - Offset: `0x14` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.21.1 Fields

{"reg": [{"name": "stride_dst", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes":

Bits	Type	Reset	Name	Description
31:0	rw	0x0	stride_dst	Destination Stride

2.22 num_repetitions

Number of 2D repetitions - Offset: `0x18` - Reset default: `0x1` - Reset mask: `0xffffffff`

2.22.1 Fields

{"reg": [{"name": "num_repetitions", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"la

Bits	Type	Reset	Name	Description
31:0	rw	0x1	num_repetitions	Number of 2D repetitions

2.23 status

DMA Status - Offset: `0x1c` - Reset default: `0x0` - Reset mask: `0xffff`

2.23.1 Fields


```
{"reg": [{"name": "busy", "bits": 16, "attr": ["ro"], "rotate": 0}, {"bits": 16}], "config": {"
```


Bits	Type	Reset	Name	Description
31:16				Reserved
15:0	ro	x	busy	DMA busy

2.24 next_id

Next ID, launches transfer, returns 0 if transfer not set up properly. - Offset: `0x20` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.24.1 Fields


```
{"reg": [{"name": "next_id", "bits": 32, "attr": ["ro"], "rotate": 0}], "config": {"lanes": 1,
```


Bits	Type	Reset	Name	Description
31:0	ro	x	next_id	Next ID, launches transfer, returns 0 if transfer not set up properly.

2.25 done

Get ID of finished transactions. - Offset: `0x24` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.25.1 Fields


```
{"reg": [{"name": "done", "bits": 32, "attr": ["ro"], "rotate": 0}], "config": {"lanes": 1, "f
```


Bits	Type	Reset	Name	Description
31:0	ro	x	done	Get ID of finished transactions.

2.26 axi_dma_config / doc / idma_reg64_2d_frontend_doc.md

2.27 Summary

Name	Offset	Length	Description
idma_reg64_2d_frontend.src_addr	0x0	8	Source Address
idma_reg64_2d_frontend.dst_addr	0x8	8	Destination Address
idma_reg64_2d_frontend.num_bytes	0x10	8	Number of bytes
idma_reg64_2d_frontend.conf	0x18	8	Configuration Register for DMA settings
idma_reg64_2d_frontend.status	0x20	8	DMA Status
idma_reg64_2d_frontend.next_id	0x28	8	Next ID, launches transfer, returns 0 if transfer not set up properly.
idma_reg64_2d_frontend.done	0x30	8	Get ID of finished transactions.
idma_reg64_2d_frontend.stride_src	0x38	8	Source Stride
idma_reg64_2d_frontend.stride_dst	0x40	8	Destination Stride
idma_reg64_2d_frontend.num_repetitions	0x48	8	Number of 2D repetitions

2.28 src_addr

Source Address - Offset: `0x0` - Reset default: `0x0` - Reset mask: `0xffffffffffffffff`

2.28.1 Fields


```
{"reg": [{"name": "src_addr", "bits": 64, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1
```


Bits	Type	Reset	Name	Description
63:0	rw	0x0	src_addr	Source Address

2.29 dst_addr

Destination Address - Offset: `0x8` - Reset default: `0x0` - Reset mask: `0xffffffffffffffff`

2.29.1 Fields


```
{"reg": [{"name": "dst_addr", "bits": 64, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1
```


Bits	Type	Reset	Name	Description
63:0	rw	0x0	dst_addr	Destination Address

2.30 num_bytes

Number of bytes - Offset: `0x10` - Reset default: `0x0` - Reset mask: `0xffffffffffffffff`

2.30.1 Fields

{"reg": [{"name": "num_bytes", "bits": 64, "attr": ["rw"], "rotate": 0}], "config": {"lanes":

Bits	Type	Reset	Name	Description
63:0	rw	0x0	num_bytes	Number of bytes

2.31 conf

Configuration Register for DMA settings - Offset: `0x18` - Reset default: `0x0` - Reset mask: `0x7`

2.31.1 Fields

{"reg": [{"name": "decouple", "bits": 1, "attr": ["rw"], "rotate": -90}, {"name": "deburst", "

Bits	Type	Reset	Name	Description
63:3				Reserved
2	rw	0x0	serialize	Serialize enable
1	rw	0x0	deburst	Deburst enable
0	rw	0x0	decouple	Decouple enable

2.32 status

DMA Status - Offset: `0x20` - Reset default: `0x0` - Reset mask: `0x1`

2.32.1 Fields

{"reg": [{"name": "busy", "bits": 1, "attr": ["ro"], "rotate": -90}, {"bits": 63}], "config":

Bits	Type	Reset	Name	Description
63:1				Reserved
0	ro	x	busy	DMA busy

2.33 next_id

Next ID, launches transfer, returns 0 if transfer not set up properly. - Offset: `0x28` - Reset default: `0x0` - Reset mask: `0xffffffffffffffff`

2.33.1 Fields

{"reg": [{"name": "next_id", "bits": 64, "attr": ["ro"], "rotate": 0}], "config": {"lanes": 1,

Bits	Type	Reset	Name	Description
63:0	ro	x	next_id	Next ID, launches transfer, returns 0 if transfer not set up properly.

2.34 done

Get ID of finished transactions. - Offset: `0x30` - Reset default: `0x0` - Reset mask: `0xffffffffffffffff`

2.34.1 Fields

{"reg": [{"name": "done", "bits": 64, "attr": ["ro"], "rotate": 0}], "config": {"lanes": 1, "f

Bits	Type	Reset	Name	Description
63:0	ro	x	done	Get ID of finished transactions.

2.35 stride_src

Source Stride - Offset: `0x38` - Reset default: `0x0` - Reset mask: `0xffffffffffffffff`

2.35.1 Fields

{"reg": [{"name": "stride_src", "bits": 64, "attr": ["rw"], "rotate": 0}], "config": {"lanes":

Bits	Type	Reset	Name	Description
63:0	rw	0x0	stride_src	Source Stride

2.36 stride_dst

Destination Stride - Offset: `0x40` - Reset default: `0x0` - Reset mask: `0xffffffffffffffff`

2.36.1 Fields

{"reg": [{"name": "stride_dst", "bits": 64, "attr": ["rw"], "rotate": 0}], "config": {"lanes":

Bits	Type	Reset	Name	Description
63:0	rw	0x0	stride_dst	Destination Stride

2.37 num_repetitions

Number of 2D repetitions - Offset: `0x48` - Reset default: `0x0` - Reset mask: `0xffffffffffffffff`

2.37.1 Fields

{"reg": [{"name": "num_repetitions", "bits": 64, "attr": ["rw"], "rotate": 0}], "config": {"la

Bits	Type	Reset	Name	Description
63:0	rw	0x0	num_repetitions	Number of 2D repetitions

2.38 axi_dma_config / doc / idma_reg64_frontend_doc.md

2.39 Summary

Name	Offset	Length	Description
idma_reg64_frontend.src_addr	0x0	8	Source Address
idma_reg64_frontend.dst_addr	0x8	8	Destination Address
idma_reg64_frontend.num_bytes	0x10	8	Number of bytes
idma_reg64_frontend.conf	0x18	8	Configuration Register for DMA settings
idma_reg64_frontend.status	0x20	8	DMA Status
idma_reg64_frontend.next_id	0x28	8	Next ID, launches transfer, returns 0 if transfer not set up properly.
idma_reg64_frontend.done	0x30	8	Get ID of finished transactions.

2.40 src_addr

Source Address - Offset: `0x0` - Reset default: `0x0` - Reset mask: `0xffffffffffffffff`

2.40.1 Fields

{"reg": [{"name": "src_addr", "bits": 64, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1

Bits	Type	Reset	Name	Description
63:0	rw	0x0	src_addr	Source Address

2.41 dst_addr

Destination Address - Offset: `0x8` - Reset default: `0x0` - Reset mask: `0xffffffffffffffff`

2.41.1 Fields

{"reg": [{"name": "dst_addr", "bits": 64, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1

Bits	Type	Reset	Name	Description
63:0	rw	0x0	dst_addr	Destination Address

2.42 num_bytes

Number of bytes - Offset: `0x10` - Reset default: `0x0` - Reset mask: `0xffffffffffffffff`

2.42.1 Fields

{"reg": [{"name": "num_bytes", "bits": 64, "attr": ["rw"], "rotate": 0}], "config": {"lanes":

Bits	Type	Reset	Name	Description
63:0	rw	0x0	num_bytes	Number of bytes

2.43 conf

Configuration Register for DMA settings - Offset: `0x18` - Reset default: `0x0` - Reset mask: `0x7`

2.43.1 Fields

{"reg": [{"name": "decouple", "bits": 1, "attr": ["rw"], "rotate": -90}, {"name": "deburst", "

Bits	Type	Reset	Name	Description
63:3				Reserved
2	rw	0x0	serialize	Serialize enable
1	rw	0x0	deburst	Deburst enable
0	rw	0x0	decouple	Decouple enable

2.44 status

DMA Status - Offset: `0x20` - Reset default: `0x0` - Reset mask: `0x1`

2.44.1 Fields

`{"reg": [{"name": "busy", "bits": 1, "attr": ["ro"], "rotate": -90}, {"bits": 63}], "config": `

Bits	Type	Reset	Name	Description
63:1				Reserved
0	ro	x	busy	DMA busy

2.45 next_id

Next ID, launches transfer, returns 0 if transfer not set up properly. - Offset: `0x28` - Reset default: `0x0` - Reset mask: `0xffffffffffffffff`

2.45.1 Fields

`{"reg": [{"name": "next_id", "bits": 64, "attr": ["ro"], "rotate": 0}], "config": {"lanes": 1,`

Bits	Type	Reset	Name	Description
63:0	ro	x	next_id	Next ID, launches transfer, returns 0 if transfer not set up properly.

2.46 done

Get ID of finished transactions. - Offset: `0x30` - Reset default: `0x0` - Reset mask: `0xffffffffffffffff`

2.46.1 Fields

{"reg": [{"name": "done", "bits": 64, "attr": ["ro"], "rotate": 0}], "config": {"lanes": 1, "f

Bits	Type	Reset	Name	Description
63:0	ro	x	done	Get ID of finished transactions.

2.47 axi_llc / doc / registers.md

2.48 Summary

Name	Offset	Length	Description
axi_llc.CFG_SPM_LOW	0x0	4	SPM Configuration (lower 32 bit)
axi_llc.CFG_SPM_HIGH	0x4	4	SPM Configuration (upper 32 bit)
axi_llc.CFG_FLUSH_LOW	0x8	4	Flush Configuration (lower 32 bit)
axi_llc.CFG_FLUSH_HIGH	0xc	4	Flush Configuration (upper 32 bit)
axi_llc.COMMIT_CFG	0x10	4	Commit the configuration
axi_llc.FLUSHED_LOW	0x18	4	Flushed Flag (lower 32 bit)
axi_llc.FLUSHED_HIGH	0x1c	4	Flushed Flag (upper 32 bit)
axi_llc.BIST_OUT_LOW	0x20	4	Tag Storage BIST Result (lower 32 bit)
axi_llc.BIST_OUT_HIGH	0x24	4	Tag Storage BIST Result (upper 32 bit)
axi_llc.SET_ASSO_LOW	0x28	4	Instantiated Set-Associativity (lower 32 bit)
axi_llc.SET_ASSO_HIGH	0x2c	4	Instantiated Set-Associativity (upper 32 bit)
axi_llc.NUM_LINES_LOW	0x30	4	Instantiated Number of Cache-Lines (lower 32 bit)
axi_llc.NUM_LINES_HIGH	0x34	4	Instantiated Number of Cache-Lines (upper 32 bit)
axi_llc.NUM_BLOCKS_LOW	0x38	4	Instantiated Number of Blocks (lower 32 bit)
axi_llc.NUM_BLOCKS_HIGH	0x3c	4	Instantiated Number of Blocks (upper 32 bit)
axi_llc.VERSION_LOW	0x40	4	AXI LLC Version (lower 32 bit)
axi_llc.VERSION_HIGH	0x44	4	AXI LLC Version (upper 32 bit)
axi_llc.BIST_STATUS	0x48	4	Status register of the BIST

2.49 CFG_SPM_LOW

SPM Configuration (lower 32 bit) - Offset: `0x0` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.49.1 Fields

{"reg": [{"name": "low", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "fo

Bits	Type	Reset	Name	Description
31:0	rw	0x0	low	lower 32 bit

2.50 CFG_SPM_HIGH

SPM Configuration (upper 32 bit) - Offset: `0x4` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.50.1 Fields

{"reg": [{"name": "high", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "f

Bits	Type	Reset	Name	Description
31:0	rw	0x0	high	upper 32 bit

2.51 CFG_FLUSH_LOW

Flush Configuration (lower 32 bit) - Offset: `0x8` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.51.1 Fields

{"reg": [{"name": "low", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "fo

Bits	Type	Reset	Name	Description
31:0	rw	0x0	low	lower 32 bit

2.52 CFG_FLUSH_HIGH

Flush Configuration (upper 32 bit) - Offset: `0xc` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.52.1 Fields

{"reg": [{"name": "high", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "f

Bits	Type	Reset	Name	Description
31:0	rw	0x0	high	upper 32 bit

2.53 COMMIT_CFG

Commit the configuration - Offset: `0x10` - Reset default: `0x0` - Reset mask: `0x1`

2.53.1 Fields


```
{"reg": [{"name": "commit", "bits": 1, "attr": ["rw1s"], "rotate": -90}, {"bits": 31}], "confi
```


Bits	Type	Reset	Name	Description
31:1				Reserved
0	rw1s	0x0	commit	commit configuration

2.54 FLUSHED_LOW

Flushed Flag (lower 32 bit) - Offset: `0x18` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.54.1 Fields


```
{"reg": [{"name": "low", "bits": 32, "attr": ["ro"], "rotate": 0}], "config": {"lanes": 1, "fo
```


Bits	Type	Reset	Name	Description
31:0	ro	0x0	low	lower 32 bit

2.55 FLUSHED_HIGH

Flushed Flag (upper 32 bit) - Offset: `0x1c` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.55.1 Fields


```
{"reg": [{"name": "high", "bits": 32, "attr": ["ro"], "rotate": 0}], "config": {"lanes": 1, "f
```


Bits	Type	Reset	Name	Description
31:0	ro	0x0	high	upper 32 bit

2.56 BIST_OUT_LOW

Tag Storage BIST Result (lower 32 bit) - Offset: `0x20` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.56.1 Fields

{"reg": [{"name": "low", "bits": 32, "attr": ["ro"], "rotate": 0}], "config": {"lanes": 1, "fo

Bits	Type	Reset	Name	Description
31:0	ro	0x0	low	lower 32 bit

2.57 BIST_OUT_HIGH

Tag Storage BIST Result (upper 32 bit) - Offset: `0x24` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.57.1 Fields

{"reg": [{"name": "high", "bits": 32, "attr": ["ro"], "rotate": 0}], "config": {"lanes": 1, "f

Bits	Type	Reset	Name	Description
31:0	ro	0x0	high	upper 32 bit

2.58 SET_ASSO_LOW

Instantiated Set-Associativity (lower 32 bit) - Offset: `0x28` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.58.1 Fields

{"reg": [{"name": "low", "bits": 32, "attr": ["ro"], "rotate": 0}], "config": {"lanes": 1, "fo

Bits	Type	Reset	Name	Description
31:0	ro	0x0	low	lower 32 bit

2.59 SET_ASSO_HIGH

Instantiated Set-Associativity (upper 32 bit) - Offset: `0x2c` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.59.1 Fields

{"reg": [{"name": "high", "bits": 32, "attr": ["ro"], "rotate": 0}], "config": {"lanes": 1, "f

Bits	Type	Reset	Name	Description
31:0	ro	0x0	high	upper 32 bit

2.60 NUM_LINES_LOW

Instantiated Number of Cache-Lines (lower 32 bit) - Offset: `0x30` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.60.1 Fields

{"reg": [{"name": "low", "bits": 32, "attr": ["ro"], "rotate": 0}], "config": {"lanes": 1, "fo

Bits	Type	Reset	Name	Description
31:0	ro	0x0	low	lower 32 bit

2.61 NUM_LINES_HIGH

Instantiated Number of Cache-Lines (upper 32 bit) - Offset: `0x34` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.61.1 Fields

{"reg": [{"name": "high", "bits": 32, "attr": ["ro"], "rotate": 0}], "config": {"lanes": 1, "f

Bits	Type	Reset	Name	Description
31:0	ro	0x0	high	upper 32 bit

2.62 NUM_BLOCKS_LOW

Instantiated Number of Blocks (lower 32 bit) - Offset: `0x38` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.62.1 Fields

{"reg": [{"name": "low", "bits": 32, "attr": ["ro"], "rotate": 0}], "config": {"lanes": 1, "fo

Bits	Type	Reset	Name	Description
31:0	ro	0x0	low	lower 32 bit

2.63 NUM_BLOCKS_HIGH

Instantiated Number of Blocks (upper 32 bit) - Offset: `0x3c` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.63.1 Fields

{"reg": [{"name": "high", "bits": 32, "attr": ["ro"], "rotate": 0}], "config": {"lanes": 1, "f

Bits	Type	Reset	Name	Description
31:0	ro	0x0	high	upper 32 bit

2.64 VERSION_LOW

AXI LLC Version (lower 32 bit) - Offset: `0x40` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.64.1 Fields

{"reg": [{"name": "low", "bits": 32, "attr": ["ro"], "rotate": 0}], "config": {"lanes": 1, "fo

Bits	Type	Reset	Name	Description
31:0	ro	0x0	low	lower 32 bit

2.65 VERSION_HIGH

AXI LLC Version (upper 32 bit) - Offset: `0x44` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.65.1 Fields

{"reg": [{"name": "high", "bits": 32, "attr": ["ro"], "rotate": 0}], "config": {"lanes": 1, "f

Bits	Type	Reset	Name	Description
31:0	ro	0x0	high	upper 32 bit

2.66 BIST_STATUS

Status register of the BIST - Offset: `0x48` - Reset default: `0x0` - Reset mask: `0x1`

2.66.1 Fields


```
{"reg": [{"name": "done", "bits": 1, "attr": ["ro"], "rotate": -90}, {"bits": 31}], "config": +
```


Bits	Type	Reset	Name	Description
31:1				Reserved
0	ro	0x0	done	BIST successfully completed

2.67 axi_realm / doc / registers.md

2.68 Summary

Name	Offset	Length	Description
axi_rt.major_version	0x0	4	Value of the major_version.
axi_rt.minor_version	0x4	4	Value of the minor_version.
axi_rt.patch_version	0x8	4	Value of the patch_version.
axi_rt.rt_enable	0xc	4	Enable RT feature on master
axi_rt.rt_bypassed	0x10	4	Is the RT inactive?
axi_rt.len_limit_0	0x14	4	Fragmentation of the bursts in beats.
axi_rt.len_limit_1	0x18	4	Fragmentation of the bursts in beats.
axi_rt.imtu_enable	0x1c	4	Enables the IMTU.
axi_rt.imtu_abort	0x20	4	Resets both the period and the budget.
axi_rt.start_addr_sub_low_0	0x24	4	The lower 32bit of the start address.
axi_rt.start_addr_sub_low_1	0x28	4	The lower 32bit of the start address.
axi_rt.start_addr_sub_low_2	0x2c	4	The lower 32bit of the start address.
axi_rt.start_addr_sub_low_3	0x30	4	The lower 32bit of the start address.
axi_rt.start_addr_sub_low_4	0x34	4	The lower 32bit of the start address.

Name	Offset	Length	Description
axi_rt.start_addr_sub_low_5	0x38	4	The lower 32bit of the start address.
axi_rt.start_addr_sub_low_6	0x3c	4	The lower 32bit of the start address.
axi_rt.start_addr_sub_low_7	0x40	4	The lower 32bit of the start address.
axi_rt.start_addr_sub_low_8	0x44	4	The lower 32bit of the start address.
axi_rt.start_addr_sub_low_9	0x48	4	The lower 32bit of the start address.
axi_rt.start_addr_sub_low_10	0x4c	4	The lower 32bit of the start address.
axi_rt.start_addr_sub_low_11	0x50	4	The lower 32bit of the start address.
axi_rt.start_addr_sub_low_12	0x54	4	The lower 32bit of the start address.
axi_rt.start_addr_sub_low_13	0x58	4	The lower 32bit of the start address.
axi_rt.start_addr_sub_low_14	0x5c	4	The lower 32bit of the start address.
axi_rt.start_addr_sub_low_15	0x60	4	The lower 32bit of the start address.
axi_rt.start_addr_sub_high_0	0x64	4	The higher 32bit of the start address.
axi_rt.start_addr_sub_high_1	0x68	4	The higher 32bit of the start address.
axi_rt.start_addr_sub_high_2	0x6c	4	The higher 32bit of the start address.
axi_rt.start_addr_sub_high_3	0x70	4	The higher 32bit of the start address.
axi_rt.start_addr_sub_high_4	0x74	4	The higher 32bit of the start address.
axi_rt.start_addr_sub_high_5	0x78	4	The higher 32bit of the start address.
axi_rt.start_addr_sub_high_6	0x7c	4	The higher 32bit of the start address.
axi_rt.start_addr_sub_high_7	0x80	4	The higher 32bit of the start address.
axi_rt.start_addr_sub_high_8	0x84	4	The higher 32bit of the start address.
axi_rt.start_addr_sub_high_9	0x88	4	The higher 32bit of the start address.
axi_rt.start_addr_sub_high_10	0x8c	4	The higher 32bit of the start address.
axi_rt.start_addr_sub_high_11	0x90	4	The higher 32bit of the start address.

Name	Offset	Length	Description
axi_rt.start_addr_sub_high_12	0x94	4	The higher 32bit of the start address.
axi_rt.start_addr_sub_high_13	0x98	4	The higher 32bit of the start address.
axi_rt.start_addr_sub_high_14	0x9c	4	The higher 32bit of the start address.
axi_rt.start_addr_sub_high_15	0xa0	4	The higher 32bit of the start address.
axi_rt.end_addr_sub_low_0	0xa4	4	The lower 32bit of the end address.
axi_rt.end_addr_sub_low_1	0xa8	4	The lower 32bit of the end address.
axi_rt.end_addr_sub_low_2	0xac	4	The lower 32bit of the end address.
axi_rt.end_addr_sub_low_3	0xb0	4	The lower 32bit of the end address.
axi_rt.end_addr_sub_low_4	0xb4	4	The lower 32bit of the end address.
axi_rt.end_addr_sub_low_5	0xb8	4	The lower 32bit of the end address.
axi_rt.end_addr_sub_low_6	0xbc	4	The lower 32bit of the end address.
axi_rt.end_addr_sub_low_7	0xc0	4	The lower 32bit of the end address.
axi_rt.end_addr_sub_low_8	0xc4	4	The lower 32bit of the end address.
axi_rt.end_addr_sub_low_9	0xc8	4	The lower 32bit of the end address.
axi_rt.end_addr_sub_low_10	0xcc	4	The lower 32bit of the end address.
axi_rt.end_addr_sub_low_11	0xd0	4	The lower 32bit of the end address.
axi_rt.end_addr_sub_low_12	0xd4	4	The lower 32bit of the end address.
axi_rt.end_addr_sub_low_13	0xd8	4	The lower 32bit of the end address.
axi_rt.end_addr_sub_low_14	0xdc	4	The lower 32bit of the end address.
axi_rt.end_addr_sub_low_15	0xe0	4	The lower 32bit of the end address.
axi_rt.end_addr_sub_high_0	0xe4	4	The higher 32bit of the end address.
axi_rt.end_addr_sub_high_1	0xe8	4	The higher 32bit of the end address.
axi_rt.end_addr_sub_high_2	0xec	4	The higher 32bit of the end address.

Name	Offset	Length	Description
axi_rt.end_addr_sub_high_3	0xf0	4	The higher 32bit of the end address.
axi_rt.end_addr_sub_high_4	0xf4	4	The higher 32bit of the end address.
axi_rt.end_addr_sub_high_5	0xf8	4	The higher 32bit of the end address.
axi_rt.end_addr_sub_high_6	0xfc	4	The higher 32bit of the end address.
axi_rt.end_addr_sub_high_7	0x100	4	The higher 32bit of the end address.
axi_rt.end_addr_sub_high_8	0x104	4	The higher 32bit of the end address.
axi_rt.end_addr_sub_high_9	0x108	4	The higher 32bit of the end address.
axi_rt.end_addr_sub_high_10	0x10c	4	The higher 32bit of the end address.
axi_rt.end_addr_sub_high_11	0x110	4	The higher 32bit of the end address.
axi_rt.end_addr_sub_high_12	0x114	4	The higher 32bit of the end address.
axi_rt.end_addr_sub_high_13	0x118	4	The higher 32bit of the end address.
axi_rt.end_addr_sub_high_14	0x11c	4	The higher 32bit of the end address.
axi_rt.end_addr_sub_high_15	0x120	4	The higher 32bit of the end address.
axi_rt.write_budget_0	0x124	4	The budget for writes.
axi_rt.write_budget_1	0x128	4	The budget for writes.
axi_rt.write_budget_2	0x12c	4	The budget for writes.
axi_rt.write_budget_3	0x130	4	The budget for writes.
axi_rt.write_budget_4	0x134	4	The budget for writes.
axi_rt.write_budget_5	0x138	4	The budget for writes.
axi_rt.write_budget_6	0x13c	4	The budget for writes.
axi_rt.write_budget_7	0x140	4	The budget for writes.
axi_rt.write_budget_8	0x144	4	The budget for writes.
axi_rt.write_budget_9	0x148	4	The budget for writes.
axi_rt.write_budget_10	0x14c	4	The budget for writes.
axi_rt.write_budget_11	0x150	4	The budget for writes.
axi_rt.write_budget_12	0x154	4	The budget for writes.
axi_rt.write_budget_13	0x158	4	The budget for writes.
axi_rt.write_budget_14	0x15c	4	The budget for writes.
axi_rt.write_budget_15	0x160	4	The budget for writes.
axi_rt.read_budget_0	0x164	4	The budget for reads.
axi_rt.read_budget_1	0x168	4	The budget for reads.
axi_rt.read_budget_2	0x16c	4	The budget for reads.
axi_rt.read_budget_3	0x170	4	The budget for reads.

Name	Offset	Length	Description
axi_rt.read_budget_4	0x174	4	The budget for reads.
axi_rt.read_budget_5	0x178	4	The budget for reads.
axi_rt.read_budget_6	0x17c	4	The budget for reads.
axi_rt.read_budget_7	0x180	4	The budget for reads.
axi_rt.read_budget_8	0x184	4	The budget for reads.
axi_rt.read_budget_9	0x188	4	The budget for reads.
axi_rt.read_budget_10	0x18c	4	The budget for reads.
axi_rt.read_budget_11	0x190	4	The budget for reads.
axi_rt.read_budget_12	0x194	4	The budget for reads.
axi_rt.read_budget_13	0x198	4	The budget for reads.
axi_rt.read_budget_14	0x19c	4	The budget for reads.
axi_rt.read_budget_15	0x1a0	4	The budget for reads.
axi_rt.write_period_0	0x1a4	4	The period for writes.
axi_rt.write_period_1	0x1a8	4	The period for writes.
axi_rt.write_period_2	0x1ac	4	The period for writes.
axi_rt.write_period_3	0x1b0	4	The period for writes.
axi_rt.write_period_4	0x1b4	4	The period for writes.
axi_rt.write_period_5	0x1b8	4	The period for writes.
axi_rt.write_period_6	0x1bc	4	The period for writes.
axi_rt.write_period_7	0x1c0	4	The period for writes.
axi_rt.write_period_8	0x1c4	4	The period for writes.
axi_rt.write_period_9	0x1c8	4	The period for writes.
axi_rt.write_period_10	0x1cc	4	The period for writes.
axi_rt.write_period_11	0x1d0	4	The period for writes.
axi_rt.write_period_12	0x1d4	4	The period for writes.
axi_rt.write_period_13	0x1d8	4	The period for writes.
axi_rt.write_period_14	0x1dc	4	The period for writes.
axi_rt.write_period_15	0x1e0	4	The period for writes.
axi_rt.read_period_0	0x1e4	4	The period for reads.
axi_rt.read_period_1	0x1e8	4	The period for reads.
axi_rt.read_period_2	0x1ec	4	The period for reads.
axi_rt.read_period_3	0x1f0	4	The period for reads.
axi_rt.read_period_4	0x1f4	4	The period for reads.
axi_rt.read_period_5	0x1f8	4	The period for reads.
axi_rt.read_period_6	0x1fc	4	The period for reads.
axi_rt.read_period_7	0x200	4	The period for reads.
axi_rt.read_period_8	0x204	4	The period for reads.
axi_rt.read_period_9	0x208	4	The period for reads.
axi_rt.read_period_10	0x20c	4	The period for reads.
axi_rt.read_period_11	0x210	4	The period for reads.
axi_rt.read_period_12	0x214	4	The period for reads.
axi_rt.read_period_13	0x218	4	The period for reads.
axi_rt.read_period_14	0x21c	4	The period for reads.
axi_rt.read_period_15	0x220	4	The period for reads.
axi_rt.write_budget_left_0	0x224	4	The budget left for writes.
axi_rt.write_budget_left_1	0x228	4	The budget left for writes.

Name	Offset	Length	Description
axi_rt.write_budget_left_2	0x22c	4	The budget left for writes.
axi_rt.write_budget_left_3	0x230	4	The budget left for writes.
axi_rt.write_budget_left_4	0x234	4	The budget left for writes.
axi_rt.write_budget_left_5	0x238	4	The budget left for writes.
axi_rt.write_budget_left_6	0x23c	4	The budget left for writes.
axi_rt.write_budget_left_7	0x240	4	The budget left for writes.
axi_rt.write_budget_left_8	0x244	4	The budget left for writes.
axi_rt.write_budget_left_9	0x248	4	The budget left for writes.
axi_rt.write_budget_left_10	0x24c	4	The budget left for writes.
axi_rt.write_budget_left_11	0x250	4	The budget left for writes.
axi_rt.write_budget_left_12	0x254	4	The budget left for writes.
axi_rt.write_budget_left_13	0x258	4	The budget left for writes.
axi_rt.write_budget_left_14	0x25c	4	The budget left for writes.
axi_rt.write_budget_left_15	0x260	4	The budget left for writes.
axi_rt.read_budget_left_0	0x264	4	The budget left for reads.
axi_rt.read_budget_left_1	0x268	4	The budget left for reads.
axi_rt.read_budget_left_2	0x26c	4	The budget left for reads.
axi_rt.read_budget_left_3	0x270	4	The budget left for reads.
axi_rt.read_budget_left_4	0x274	4	The budget left for reads.
axi_rt.read_budget_left_5	0x278	4	The budget left for reads.
axi_rt.read_budget_left_6	0x27c	4	The budget left for reads.
axi_rt.read_budget_left_7	0x280	4	The budget left for reads.
axi_rt.read_budget_left_8	0x284	4	The budget left for reads.
axi_rt.read_budget_left_9	0x288	4	The budget left for reads.
axi_rt.read_budget_left_10	0x28c	4	The budget left for reads.
axi_rt.read_budget_left_11	0x290	4	The budget left for reads.
axi_rt.read_budget_left_12	0x294	4	The budget left for reads.
axi_rt.read_budget_left_13	0x298	4	The budget left for reads.
axi_rt.read_budget_left_14	0x29c	4	The budget left for reads.
axi_rt.read_budget_left_15	0x2a0	4	The budget left for reads.
axi_rt.write_period_left_0	0x2a4	4	The period left for writes.
axi_rt.write_period_left_1	0x2a8	4	The period left for writes.
axi_rt.write_period_left_2	0x2ac	4	The period left for writes.
axi_rt.write_period_left_3	0x2b0	4	The period left for writes.
axi_rt.write_period_left_4	0x2b4	4	The period left for writes.
axi_rt.write_period_left_5	0x2b8	4	The period left for writes.
axi_rt.write_period_left_6	0x2bc	4	The period left for writes.
axi_rt.write_period_left_7	0x2c0	4	The period left for writes.
axi_rt.write_period_left_8	0x2c4	4	The period left for writes.
axi_rt.write_period_left_9	0x2c8	4	The period left for writes.
axi_rt.write_period_left_10	0x2cc	4	The period left for writes.
axi_rt.write_period_left_11	0x2d0	4	The period left for writes.
axi_rt.write_period_left_12	0x2d4	4	The period left for writes.
axi_rt.write_period_left_13	0x2d8	4	The period left for writes.
axi_rt.write_period_left_14	0x2dc	4	The period left for writes.
axi_rt.write_period_left_15	0x2e0	4	The period left for writes.

Name	Offset	Length	Description
axi_rt.read_period_left_0	0x2e4	4	The period left for reads.
axi_rt.read_period_left_1	0x2e8	4	The period left for reads.
axi_rt.read_period_left_2	0x2ec	4	The period left for reads.
axi_rt.read_period_left_3	0x2f0	4	The period left for reads.
axi_rt.read_period_left_4	0x2f4	4	The period left for reads.
axi_rt.read_period_left_5	0x2f8	4	The period left for reads.
axi_rt.read_period_left_6	0x2fc	4	The period left for reads.
axi_rt.read_period_left_7	0x300	4	The period left for reads.
axi_rt.read_period_left_8	0x304	4	The period left for reads.
axi_rt.read_period_left_9	0x308	4	The period left for reads.
axi_rt.read_period_left_10	0x30c	4	The period left for reads.
axi_rt.read_period_left_11	0x310	4	The period left for reads.
axi_rt.read_period_left_12	0x314	4	The period left for reads.
axi_rt.read_period_left_13	0x318	4	The period left for reads.
axi_rt.read_period_left_14	0x31c	4	The period left for reads.
axi_rt.read_period_left_15	0x320	4	The period left for reads.
axi_rt.isolate	0x324	4	Is the interface requested to be isolated?
axi_rt.isolated	0x328	4	Is the interface isolated?
axi_rt.num_managers	0x32c	4	Value of the num_managers parameter.
axi_rt.addr_width	0x330	4	Value of the addr_width parameter.
axi_rt.data_width	0x334	4	Value of the data_width parameter.
axi_rt.id_width	0x338	4	Value of the id_width parameter.
axi_rt.user_width	0x33c	4	Value of the user_width parameter.
axi_rt.num_pending	0x340	4	Value of the num_pending parameter.
axi_rt.w_buffer_depth	0x344	4	Value of the w_buffer_depth parameter.
axi_rt.num_addr_regions	0x348	4	Value of the num_addr_regions parameter.
axi_rt.period_width	0x34c	4	Value of the period_width parameter.
axi_rt.budget_width	0x350	4	Value of the budget_width parameter.
axi_rt.max_num_managers	0x354	4	Value of the max_num_managers parameter.

2.69 major_version

Value of the major_version. - Offset: `0x0` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.69.1 Fields

{"reg": [{"name": "major_version", "bits": 32, "attr": ["ro"], "rotate": 0}], "config": {"lanes

Bits	Type	Reset	Name	Description
31:0	ro	0x0	major_version	Value of the major_version.

2.70 minor_version

Value of the minor_version. - Offset: `0x4` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.70.1 Fields

{"reg": [{"name": "minor_version", "bits": 32, "attr": ["ro"], "rotate": 0}], "config": {"lanes

Bits	Type	Reset	Name	Description
31:0	ro	0x0	minor_version	Value of the minor_version.

2.71 patch_version

Value of the patch_version. - Offset: `0x8` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.71.1 Fields

{"reg": [{"name": "patch_version", "bits": 32, "attr": ["ro"], "rotate": 0}], "config": {"lanes

Bits	Type	Reset	Name	Description
31:0	ro	0x0	patch_version	Value of the patch_version.

2.72 rt_enable

Enable RT feature on master - Offset: `0xc` - Reset default: `0x0` - Reset mask: `0xff`

2.72.1 Fields

{"reg": [{"name": "enable_0", "bits": 1, "attr": ["wo"], "rotate": -90}, {"name": "enable_1", "

Bits	Type	Reset	Name	Description
31:8				Reserved
7	wo	0x0	enable_7	Enable RT feature on master
6	wo	0x0	enable_6	Enable RT feature on master
5	wo	0x0	enable_5	Enable RT feature on master
4	wo	0x0	enable_4	Enable RT feature on master
3	wo	0x0	enable_3	Enable RT feature on master
2	wo	0x0	enable_2	Enable RT feature on master
1	wo	0x0	enable_1	Enable RT feature on master
0	wo	0x0	enable_0	Enable RT feature on master

2.73 rt_bypassed

Is the RT inactive? - Offset: `0x10` - Reset default: `0x0` - Reset mask: `0xff`

2.73.1 Fields

{"reg": [{"name": "bypassed_0", "bits": 1, "attr": ["ro"], "rotate": -90}, {"name": "bypassed_

Bits	Type	Reset	Name	Description
31:8				Reserved
7	ro	x	bypassed_7	Is the RT inactive?
6	ro	x	bypassed_6	Is the RT inactive?
5	ro	x	bypassed_5	Is the RT inactive?
4	ro	x	bypassed_4	Is the RT inactive?
3	ro	x	bypassed_3	Is the RT inactive?
2	ro	x	bypassed_2	Is the RT inactive?
1	ro	x	bypassed_1	Is the RT inactive?
0	ro	x	bypassed_0	Is the RT inactive?

2.74 len_limit_0

Fragmentation of the bursts in beats. - Offset: `0x14` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.74.1 Fields

{"reg": [{"name": "len_0", "bits": 8, "attr": ["wo"], "rotate": 0}, {"name": "len_1", "bits": 8

Bits	Type	Reset	Name	Description
31:24	wo	0x0	len_3	Fragmentation of the bursts in beats.
23:16	wo	0x0	len_2	Fragmentation of the bursts in beats.
15:8	wo	0x0	len_1	Fragmentation of the bursts in beats.
7:0	wo	0x0	len_0	Fragmentation of the bursts in beats.

2.75 len_limit_1

Fragmentation of the bursts in beats. - Offset: `0x18` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.75.1 Fields

`{"reg": [{"name": "len_4", "bits": 8, "attr": ["wo"], "rotate": 0}, {"name": "len_5", "bits": 8`

Bits	Type	Reset	Name	Description
31:24	wo	0x0	len_7	For len_limit1
23:16	wo	0x0	len_6	For len_limit1
15:8	wo	0x0	len_5	For len_limit1
7:0	wo	0x0	len_4	For len_limit1

2.76 imtu_enable

Enables the IMTU. - Offset: `0x1c` - Reset default: `0x0` - Reset mask: `0xff`

2.76.1 Fields

`{"reg": [{"name": "enable_0", "bits": 1, "attr": ["wo"], "rotate": -90}, {"name": "enable_1",`

Bits	Type	Reset	Name	Description
31:8				Reserved
7	wo	0x0	enable_7	Enables the IMTU.
6	wo	0x0	enable_6	Enables the IMTU.
5	wo	0x0	enable_5	Enables the IMTU.
4	wo	0x0	enable_4	Enables the IMTU.
3	wo	0x0	enable_3	Enables the IMTU.
2	wo	0x0	enable_2	Enables the IMTU.
1	wo	0x0	enable_1	Enables the IMTU.
0	wo	0x0	enable_0	Enables the IMTU.

2.77 imtu_abort

Resets both the period and the budget. - Offset: `0x20` - Reset default: `0x0` - Reset mask: `0xff`

2.77.1 Fields

{"reg": [{"name": "abort_0", "bits": 1, "attr": ["wo"], "rotate": -90}, {"name": "abort_1", "bi

Bits	Type	Reset	Name	Description
31:8				Reserved
7	wo	0x0	abort_7	Resets both the period and the budget.
6	wo	0x0	abort_6	Resets both the period and the budget.
5	wo	0x0	abort_5	Resets both the period and the budget.
4	wo	0x0	abort_4	Resets both the period and the budget.
3	wo	0x0	abort_3	Resets both the period and the budget.
2	wo	0x0	abort_2	Resets both the period and the budget.
1	wo	0x0	abort_1	Resets both the period and the budget.
0	wo	0x0	abort_0	Resets both the period and the budget.

2.78 start_addr_sub_low

The lower 32bit of the start address. - Reset default: `0x0` - Reset mask: `0xffffffff`

2.78.1 Instances

Name	Offset
start_addr_sub_low_0	0x24
start_addr_sub_low_1	0x28
start_addr_sub_low_2	0x2c
start_addr_sub_low_3	0x30
start_addr_sub_low_4	0x34
start_addr_sub_low_5	0x38
start_addr_sub_low_6	0x3c
start_addr_sub_low_7	0x40
start_addr_sub_low_8	0x44
start_addr_sub_low_9	0x48
start_addr_sub_low_10	0x4c
start_addr_sub_low_11	0x50
start_addr_sub_low_12	0x54
start_addr_sub_low_13	0x58
start_addr_sub_low_14	0x5c
start_addr_sub_low_15	0x60

2.78.2 Fields

{"reg": [{"name": "write_budget", "bits": 32, "attr": ["wo"], "rotate": 0}], "config": {"lanes"

Bits	Type	Reset	Name	Description
31:0	wo	0x0	write_budget	The lower 32bit of the start address.

2.79 start_addr_sub_high

The higher 32bit of the start address. - Reset default: `0x0` - Reset mask: `0xffffffff`

2.79.1 Instances

Name	Offset
start_addr_sub_high_0	0x64
start_addr_sub_high_1	0x68
start_addr_sub_high_2	0x6c
start_addr_sub_high_3	0x70
start_addr_sub_high_4	0x74
start_addr_sub_high_5	0x78
start_addr_sub_high_6	0x7c
start_addr_sub_high_7	0x80
start_addr_sub_high_8	0x84
start_addr_sub_high_9	0x88
start_addr_sub_high_10	0x8c
start_addr_sub_high_11	0x90
start_addr_sub_high_12	0x94
start_addr_sub_high_13	0x98
start_addr_sub_high_14	0x9c
start_addr_sub_high_15	0xa0

2.79.2 Fields

{"reg": [{"name": "write_budget", "bits": 32, "attr": ["wo"], "rotate": 0}], "config": {"lanes"

Bits	Type	Reset	Name	Description
31:0	wo	0x0	write_budget	The higher 32bit of the start address.

2.80 end_addr_sub_low

The lower 32bit of the end address. - Reset default: `0x0` - Reset mask: `0xffffffff`

2.80.1 Instances

Name	Offset
end_addr_sub_low_0	0xa4
end_addr_sub_low_1	0xa8
end_addr_sub_low_2	0xac
end_addr_sub_low_3	0xb0
end_addr_sub_low_4	0xb4
end_addr_sub_low_5	0xb8
end_addr_sub_low_6	0xbc
end_addr_sub_low_7	0xc0
end_addr_sub_low_8	0xc4
end_addr_sub_low_9	0xc8
end_addr_sub_low_10	0xcc
end_addr_sub_low_11	0xd0
end_addr_sub_low_12	0xd4
end_addr_sub_low_13	0xd8
end_addr_sub_low_14	0xdc
end_addr_sub_low_15	0xe0

2.80.2 Fields

{"reg": [{"name": "write_budget", "bits": 32, "attr": ["wo"], "rotate": 0}], "config": {"lanes"

Bits	Type	Reset	Name	Description
31:0	wo	0x0	write_budget	The lower 32bit of the end address.

2.81 end_addr_sub_high

The higher 32bit of the end address. - Reset default: `0x0` - Reset mask: `0xffffffff`

2.81.1 Instances

Name	Offset
end_addr_sub_high_0	0xe4
end_addr_sub_high_1	0xe8
end_addr_sub_high_2	0xec
end_addr_sub_high_3	0xf0
end_addr_sub_high_4	0xf4
end_addr_sub_high_5	0xf8
end_addr_sub_high_6	0xfc
end_addr_sub_high_7	0x100
end_addr_sub_high_8	0x104
end_addr_sub_high_9	0x108

Name	Offset
end_addr_sub_high_10	0x10c
end_addr_sub_high_11	0x110
end_addr_sub_high_12	0x114
end_addr_sub_high_13	0x118
end_addr_sub_high_14	0x11c
end_addr_sub_high_15	0x120

2.81.2 Fields

{"reg": [{"name": "write_budget", "bits": 32, "attr": ["wo"], "rotate": 0}], "config": {"lanes"

Bits	Type	Reset	Name	Description
31:0	wo	0x0	write_budget	The higher 32bit of the end address.

2.82 write_budget

The budget for writes. - Reset default: `0x0` - Reset mask: `0xffffffff`

2.82.1 Instances

Name	Offset
write_budget_0	0x124
write_budget_1	0x128
write_budget_2	0x12c
write_budget_3	0x130
write_budget_4	0x134
write_budget_5	0x138
write_budget_6	0x13c
write_budget_7	0x140
write_budget_8	0x144
write_budget_9	0x148
write_budget_10	0x14c
write_budget_11	0x150
write_budget_12	0x154
write_budget_13	0x158
write_budget_14	0x15c
write_budget_15	0x160

2.82.2 Fields

{"reg": [{"name": "write_budget", "bits": 32, "attr": ["wo"], "rotate": 0}], "config": {"lanes"

Bits	Type	Reset	Name	Description
31:0	wo	0x0	write_budget	The budget for writes.

2.83 read_budget

The budget for reads. - Reset default: `0x0` - Reset mask: `0xffffffff`

2.83.1 Instances

Name	Offset
read_budget_0	0x164
read_budget_1	0x168
read_budget_2	0x16c
read_budget_3	0x170
read_budget_4	0x174
read_budget_5	0x178
read_budget_6	0x17c
read_budget_7	0x180
read_budget_8	0x184
read_budget_9	0x188
read_budget_10	0x18c
read_budget_11	0x190
read_budget_12	0x194
read_budget_13	0x198
read_budget_14	0x19c
read_budget_15	0x1a0

2.83.2 Fields

`{"reg": [{"name": "read_budget", "bits": 32, "attr": ["wo"], "rotate": 0}], "config": {"lanes"`

Bits	Type	Reset	Name	Description
31:0	wo	0x0	read_budget	The budget for reads.

2.84 write_period

The period for writes. - Reset default: `0x0` - Reset mask: `0xffffffff`

2.84.1 Instances

Name	Offset
write_period_0	0x1a4
write_period_1	0x1a8
write_period_2	0x1ac
write_period_3	0x1b0
write_period_4	0x1b4
write_period_5	0x1b8
write_period_6	0x1bc
write_period_7	0x1c0
write_period_8	0x1c4
write_period_9	0x1c8
write_period_10	0x1cc
write_period_11	0x1d0
write_period_12	0x1d4
write_period_13	0x1d8
write_period_14	0x1dc
write_period_15	0x1e0

2.84.2 Fields

{"reg": [{"name": "write_period", "bits": 32, "attr": ["wo"], "rotate": 0}], "config": {"lanes"

Bits	Type	Reset	Name	Description
31:0	wo	0x0	write_period	The period for writes.

2.85 read_period

The period for reads. - Reset default: `0x0` - Reset mask: `0xffffffff`

2.85.1 Instances

Name	Offset
read_period_0	0x1e4
read_period_1	0x1e8
read_period_2	0x1ec
read_period_3	0x1f0
read_period_4	0x1f4
read_period_5	0x1f8
read_period_6	0x1fc
read_period_7	0x200
read_period_8	0x204
read_period_9	0x208

Name	Offset
read_period_10	0x20c
read_period_11	0x210
read_period_12	0x214
read_period_13	0x218
read_period_14	0x21c
read_period_15	0x220

2.85.2 Fields

{"reg": [{"name": "read_period", "bits": 32, "attr": ["wo"], "rotate": 0}], "config": {"lanes"

Bits	Type	Reset	Name	Description
31:0	wo	0x0	read_period	The period for reads.

2.86 write_budget_left

The budget left for writes. - Reset default: `0x0` - Reset mask: `0xffffffff`

2.86.1 Instances

Name	Offset
write_budget_left_0	0x224
write_budget_left_1	0x228
write_budget_left_2	0x22c
write_budget_left_3	0x230
write_budget_left_4	0x234
write_budget_left_5	0x238
write_budget_left_6	0x23c
write_budget_left_7	0x240
write_budget_left_8	0x244
write_budget_left_9	0x248
write_budget_left_10	0x24c
write_budget_left_11	0x250
write_budget_left_12	0x254
write_budget_left_13	0x258
write_budget_left_14	0x25c
write_budget_left_15	0x260

2.86.2 Fields

{"reg": [{"name": "write_budget_left", "bits": 32, "attr": ["ro"], "rotate": 0}], "config": {"

Bits	Type	Reset	Name	Description
31:0	ro	0x0	write_budget_left	The budget left for writes.

2.87 read_budget_left

The budget left for reads. - Reset default: `0x0` - Reset mask: `0xffffffff`

2.87.1 Instances

Name	Offset
read_budget_left_0	0x264
read_budget_left_1	0x268
read_budget_left_2	0x26c
read_budget_left_3	0x270
read_budget_left_4	0x274
read_budget_left_5	0x278
read_budget_left_6	0x27c
read_budget_left_7	0x280
read_budget_left_8	0x284
read_budget_left_9	0x288
read_budget_left_10	0x28c
read_budget_left_11	0x290
read_budget_left_12	0x294
read_budget_left_13	0x298
read_budget_left_14	0x29c
read_budget_left_15	0x2a0

2.87.2 Fields

{"reg": [{"name": "read_budget_left", "bits": 32, "attr": ["ro"], "rotate": 0}], "config": {"la

Bits	Type	Reset	Name	Description
31:0	ro	0x0	read_budget_left	The budget left for reads.

2.88 write_period_left

The period left for writes. - Reset default: `0x0` - Reset mask: `0xffffffff`

2.88.1 Instances

Name	Offset
write_period_left_0	0x2a4
write_period_left_1	0x2a8
write_period_left_2	0x2ac
write_period_left_3	0x2b0
write_period_left_4	0x2b4
write_period_left_5	0x2b8
write_period_left_6	0x2bc
write_period_left_7	0x2c0
write_period_left_8	0x2c4
write_period_left_9	0x2c8
write_period_left_10	0x2cc
write_period_left_11	0x2d0
write_period_left_12	0x2d4
write_period_left_13	0x2d8
write_period_left_14	0x2dc
write_period_left_15	0x2e0

2.88.2 Fields

{"reg": [{"name": "write_period_left", "bits": 32, "attr": ["ro"], "rotate": 0}], "config": {"

Bits	Type	Reset	Name	Description
31:0	ro	0x0	write_period_left	The period left for writes.

2.89 read_period_left

The period left for reads. - Reset default: `0x0` - Reset mask: `0xffffffff`

2.89.1 Instances

Name	Offset
read_period_left_0	0x2e4
read_period_left_1	0x2e8
read_period_left_2	0x2ec
read_period_left_3	0x2f0
read_period_left_4	0x2f4
read_period_left_5	0x2f8
read_period_left_6	0x2fc
read_period_left_7	0x300
read_period_left_8	0x304
read_period_left_9	0x308

Name	Offset
read_period_left_10	0x30c
read_period_left_11	0x310
read_period_left_12	0x314
read_period_left_13	0x318
read_period_left_14	0x31c
read_period_left_15	0x320

2.89.2 Fields

{"reg": [{"name": "read_period_left", "bits": 32, "attr": ["ro"], "rotate": 0}], "config": {"la

Bits	Type	Reset	Name	Description
31:0	ro	0x0	read_period_left	The period left for reads.

2.90 isolate

Is the interface requested to be isolated? - Offset: `0x324` - Reset default: `0x0` - Reset mask: `0xff`

2.90.1 Fields

{"reg": [{"name": "isolate_0", "bits": 1, "attr": ["ro"], "rotate": -90}, {"name": "isolate_1"

Bits	Type	Reset	Name	Description
31:8				Reserved
7	ro	x	isolate_7	Is the interface requested to be isolated?
6	ro	x	isolate_6	Is the interface requested to be isolated?
5	ro	x	isolate_5	Is the interface requested to be isolated?
4	ro	x	isolate_4	Is the interface requested to be isolated?
3	ro	x	isolate_3	Is the interface requested to be isolated?
2	ro	x	isolate_2	Is the interface requested to be isolated?
1	ro	x	isolate_1	Is the interface requested to be isolated?
0	ro	x	isolate_0	Is the interface requested to be isolated?

2.91 isolated

Is the interface isolated? - Offset: `0x328` - Reset default: `0x0` - Reset mask: `0xff`

2.91.1 Fields

{"reg": [{"name": "isolated_0", "bits": 1, "attr": ["ro"], "rotate": -90}, {"name": "isolated_

Bits	Type	Reset	Name	Description
31:8				Reserved
7	ro	x	isolated_7	Is the interface isolated?
6	ro	x	isolated_6	Is the interface isolated?
5	ro	x	isolated_5	Is the interface isolated?
4	ro	x	isolated_4	Is the interface isolated?
3	ro	x	isolated_3	Is the interface isolated?
2	ro	x	isolated_2	Is the interface isolated?
1	ro	x	isolated_1	Is the interface isolated?
0	ro	x	isolated_0	Is the interface isolated?

2.92 num_managers

Value of the num_managers parameter. - Offset: `0x32c` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.92.1 Fields

{"reg": [{"name": "num_managers", "bits": 32, "attr": ["ro"], "rotate": 0}], "config": {"lanes"

Bits	Type	Reset	Name	Description
31:0	ro	x	num_managers	Value of the num_managers parameter.

2.93 addr_width

Value of the addr_width parameter. - Offset: `0x330` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.93.1 Fields

{"reg": [{"name": "addr_width", "bits": 32, "attr": ["ro"], "rotate": 0}], "config": {"lanes":

Bits	Type	Reset	Name	Description
31:0	ro	x	addr_width	Value of the addr_width parameter.

2.94 data_width

Value of the data_width parameter. - Offset: `0x334` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.94.1 Fields

{"reg": [{"name": "data_width", "bits": 32, "attr": ["ro"], "rotate": 0}], "config": {"lanes":

Bits	Type	Reset	Name	Description
31:0	ro	x	data_width	Value of the data_width parameter.

2.95 id_width

Value of the id_width parameter. - Offset: `0x338` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.95.1 Fields

{"reg": [{"name": "id_width", "bits": 32, "attr": ["ro"], "rotate": 0}], "config": {"lanes": 1

Bits	Type	Reset	Name	Description
31:0	ro	x	id_width	Value of the id_width parameter.

2.96 user_width

Value of the user_width parameter. - Offset: `0x33c` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.96.1 Fields

{"reg": [{"name": "user_width", "bits": 32, "attr": ["ro"], "rotate": 0}], "config": {"lanes":

Bits	Type	Reset	Name	Description
31:0	ro	x	user_width	Value of the user_width parameter.

2.97 num_pending

Value of the num_pending parameter. - Offset: `0x340` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.97.1 Fields

{"reg": [{"name": "num_pending", "bits": 32, "attr": ["ro"], "rotate": 0}], "config": {"lanes"

Bits	Type	Reset	Name	Description
31:0	ro	x	num_pending	Value of the num_pending parameter.

2.98 w_buffer_depth

Value of the w_buffer_depth parameter. - Offset: `0x344` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.98.1 Fields

`{"reg": [{"name": "w_buffer_depth", "bits": 32, "attr": ["ro"], "rotate": 0}], "config": {"lane`

Bits	Type	Reset	Name	Description
31:0	ro	x	w_buffer_depth	Value of the w_buffer_depth parameter.

2.99 num_addr_regions

Value of the num_addr_regions parameter. - Offset: `0x348` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.99.1 Fields

`{"reg": [{"name": "num_addr_regions", "bits": 32, "attr": ["ro"], "rotate": 0}], "config": {"la`

Bits	Type	Reset	Name	Description
31:0	ro	x	num_addr_regions	Value of the num_addr_regions parameter.

2.100 period_width

Value of the period_width parameter. - Offset: `0x34c` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.100.1 Fields

`{"reg": [{"name": "period_width", "bits": 32, "attr": ["ro"], "rotate": 0}], "config": {"lanes"`

Bits	Type	Reset	Name	Description
31:0	ro	x	period_width	Value of the period_width parameter.

2.101 budget_width

Value of the budget_width parameter. - Offset: `0x350` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.101.1 Fields

`{"reg": [{"name": "budget_width", "bits": 32, "attr": ["ro"], "rotate": 0}], "config": {"lanes"`

Bits	Type	Reset	Name	Description
31:0	ro	x	budget_width	Value of the budget_width parameter.

2.102 max_num_managers

Value of the max_num_managers parameter. - Offset: `0x354` - Reset default: `0x8` - Reset mask: `0xffffffff`

2.102.1 Fields

`{"reg": [{"name": "max_num_managers", "bits": 32, "attr": ["ro"], "rotate": 0}], "config": {"la`

Bits	Type	Reset	Name	Description
31:0	ro	0x8	max_num_managers	Value of the max_num_managers parameter.

2.103 can_bus / doc / registers.md

2.104 Summary

Name	Offset	Length	Description
can_bus.ahb_ifc_hsel_valid	0x0	4	Auto-extracted signal hsel_valid from ahb_ifc.vhd
can_bus.ahb_ifc_write_acc_d	0x4	4	Auto-extracted signal write_acc_d from ahb_ifc.vhd
can_bus.ahb_ifc_write_acc_q	0x8	4	Auto-extracted signal write_acc_q from ahb_ifc.vhd
can_bus.ahb_ifc_haddr_q	0xc	4	Auto-extracted signal haddr_q from ahb_ifc.vhd
can_bus.ahb_ifc_h_ready_raw	0x10	4	Auto-extracted signal h_ready_raw from ahb_ifc.vhd

Name	Offset	Length	Description
can_bus.ahb_ifc_sbe_d	0x14	4	Auto-extracted signal sbe_d from ahb_ifc.vhd
can_bus.ahb_ifc_sbe_q	0x18	4	Auto-extracted signal sbe_q from ahb_ifc.vhd
can_bus.ahb_ifc_swr_i	0x1c	4	Auto-extracted signal swr_i from ahb_ifc.vhd
can_bus.ahb_ifc_srd_i	0x20	4	Auto-extracted signal srd_i from ahb_ifc.vhd
can_bus.bit_destuffing_discard_stuff_bit	0x24	4	Auto-extracted signal discard_stuff_bit from bit_destuffing.vhd
can_bus.bit_destuffing_non_fix_to_fix_chng	0x28	4	Auto-extracted signal non_fix_to_fix_chng from bit_destuffing.vhd
can_bus.bit_destuffing_stuff_lvl_reached	0x2c	4	Auto-extracted signal stuff_lvl_reached from bit_destuffing.vhd
can_bus.bit_destuffing_stuff_rule_violate	0x30	4	Auto-extracted signal stuff_rule_violate from bit_destuffing.vhd
can_bus.bit_destuffing_enable_prev	0x34	4	Auto-extracted signal enable_prev from bit_destuffing.vhd
can_bus.bit_destuffing_fixed_prev_q	0x38	4	Auto-extracted signal fixed_prev_q from bit_destuffing.vhd
can_bus.bit_destuffing_fixed_prev_d	0x3c	4	Auto-extracted signal fixed_prev_d from bit_destuffing.vhd
can_bus.bit_destuffing_same_bits_erase	0x40	4	Auto-extracted signal same_bits_erase from bit_destuffing.vhd
can_bus.bit_destuffing_destuffed_q	0x44	4	Auto-extracted signal destuffed_q from bit_destuffing.vhd
can_bus.bit_destuffing_destuffed_d	0x48	4	Auto-extracted signal destuffed_d from bit_destuffing.vhd
can_bus.bit_destuffing_stuff_err_q	0x4c	4	Auto-extracted signal stuff_err_q from bit_destuffing.vhd
can_bus.bit_destuffing_stuff_err_d	0x50	4	Auto-extracted signal stuff_err_d from bit_destuffing.vhd
can_bus.bit_destuffing_prev_val_q	0x54	4	Auto-extracted signal prev_val_q from bit_destuffing.vhd
can_bus.bit_destuffing_prev_val_d	0x58	4	Auto-extracted signal prev_val_d from bit_destuffing.vhd
can_bus.bit_err_detector_bit_err_d	0x5c	4	Auto-extracted signal bit_err_d from bit_err_detector.vhd

Name	Offset	Length	Description
can_bus.bit_err_detector_bit_err_q	0x60	4	Auto-extracted signal bit_err_q from bit_err_detector.vhd
can_bus.bit_err_detector_bit_err_ssp_capt_d	0x64	4	Auto-extracted signal bit_err_ssp_capt_d from bit_err_detector.vhd
can_bus.bit_err_detector_bit_err_ssp_capt_q	0x68	4	Auto-extracted signal bit_err_ssp_capt_q from bit_err_detector.vhd
can_bus.bit_err_detector_bit_err_ssp_valid	0x6c	4	Auto-extracted signal bit_err_ssp_valid from bit_err_detector.vhd
can_bus.bit_err_detector_bit_err_ssp_condition	0x70	4	Auto-extracted signal bit_err_ssp_condition from bit_err_detector.vhd
can_bus.bit_err_detector_bit_err_norm_valid	0x74	4	Auto-extracted signal bit_err_norm_valid from bit_err_detector.vhd
can_bus.bit_filter_masked_input	0x78	4	Auto-extracted signal masked_input from bit_filter.vhd
can_bus.bit_filter_masked_value	0x7c	4	Auto-extracted signal masked_value from bit_filter.vhd
can_bus.bit_segment_meter_sel_tseg1	0x80	4	Auto-extracted signal sel_tseg1 from bit_segment_meter.vhd
can_bus.bit_segment_meter_exp_seg_length_ce	0x84	4	Auto-extracted signal exp_seg_length_ce from bit_segment_meter.vhd
can_bus.bit_segment_meter_phase_err_mt_sjw	0x88	4	Auto-extracted signal phase_err_mt_sjw from bit_segment_meter.vhd
can_bus.bit_segment_meter_phase_err_eq_sjw	0x8c	4	Auto-extracted signal phase_err_eq_sjw from bit_segment_meter.vhd
can_bus.bit_segment_meter_exit_ph2_immediate	0x90	4	Auto-extracted signal exit_ph2_immediate from bit_segment_meter.vhd
can_bus.bit_segment_meter_exit_segm_regular	0x94	4	Auto-extracted signal exit_segm_regular from bit_segment_meter.vhd
can_bus.bit_segment_meter_exit_segm_regular_tseg1	0x98	4	Auto-extracted signal exit_segm_regular_tseg1 from bit_segment_meter.vhd
can_bus.bit_segment_meter_exit_segm_regular_tseg2	0x9c	4	Auto-extracted signal exit_segm_regular_tseg2 from bit_segment_meter.vhd

Name	Offset	Length	Description
can_bus.bit_segment_meter_sjw_mt_zero	0xa0	4	Auto-extracted signal sjw_mt_zero from bit_segment_meter.vhd
can_bus.bit_segment_meter_use_basic_segm_length	0xa4	4	Auto-extracted signal use_basic_segm_length from bit_segment_meter.vhd
can_bus.bit_segment_meter_phase_err_sjw_by_one	0xa8	4	Auto-extracted signal phase_err_sjw_by_one from bit_segment_meter.vhd
can_bus.bit_segment_meter_shorten_tseg1_after_tseg2	0xac	4	Auto-extracted signal shorten_tseg1_after_tseg2 from bit_segment_meter.vhd
can_bus.bit_stuffing_data_out_i	0xb0	4	Auto-extracted signal data_out_i from bit_stuffing.vhd
can_bus.bit_stuffing_data_halt_q	0xb4	4	Auto-extracted signal data_halt_q from bit_stuffing.vhd
can_bus.bit_stuffing_data_halt_d	0xb8	4	Auto-extracted signal data_halt_d from bit_stuffing.vhd
can_bus.bit_stuffing_fixed_reg_q	0xbc	4	Auto-extracted signal fixed_reg_q from bit_stuffing.vhd
can_bus.bit_stuffing_fixed_reg_d	0xc0	4	Auto-extracted signal fixed_reg_d from bit_stuffing.vhd
can_bus.bit_stuffing_enable_prev	0xc4	4	Auto-extracted signal enable_prev from bit_stuffing.vhd
can_bus.bit_stuffing_non_fix_to_fix_chng	0xc8	4	Auto-extracted signal non_fix_to_fix_chng from bit_stuffing.vhd
can_bus.bit_stuffing_stuff_lvl_reached	0xcc	4	Auto-extracted signal stuff_lvl_reached from bit_stuffing.vhd
can_bus.bit_stuffing_same_bits_rst_trig	0xd0	4	Auto-extracted signal same_bits_rst_trig from bit_stuffing.vhd
can_bus.bit_stuffing_same_bits_rst	0xd4	4	Auto-extracted signal same_bits_rst from bit_stuffing.vhd
can_bus.bit_stuffing_insert_stuff_bit	0xd8	4	Auto-extracted signal insert_stuff_bit from bit_stuffing.vhd

Name	Offset	Length	Description
can_bus.bit_stuffing_data_out_d_ena	0xdc	4	Auto-extracted signal data_out_d_ena from bit_stuffing.vhd
can_bus.bit_stuffing_data_out_d	0xe0	4	Auto-extracted signal data_out_d from bit_stuffing.vhd
can_bus.bit_stuffing_data_out_ce	0xe4	4	Auto-extracted signal data_out_ce from bit_stuffing.vhd
can_bus.bit_time_cfg_capture_drv_tq_nbt	0xe8	4	Auto-extracted signal drv_tq_nbt from bit_time_cfg_capture.vhd
can_bus.bit_time_cfg_capture_drv_prs_nbt	0xec	4	Auto-extracted signal drv_prs_nbt from bit_time_cfg_capture.vhd
can_bus.bit_time_cfg_capture_drv_ph1_nbt	0xf0	4	Auto-extracted signal drv_ph1_nbt from bit_time_cfg_capture.vhd
can_bus.bit_time_cfg_capture_drv_ph2_nbt	0xf4	4	Auto-extracted signal drv_ph2_nbt from bit_time_cfg_capture.vhd
can_bus.bit_time_cfg_capture_drv_sjw_nbt	0xf8	4	Auto-extracted signal drv_sjw_nbt from bit_time_cfg_capture.vhd
can_bus.bit_time_cfg_capture_drv_tq_dbt	0xfc	4	Auto-extracted signal drv_tq_dbt from bit_time_cfg_capture.vhd
can_bus.bit_time_cfg_capture_drv_prs_dbt	0x100	4	Auto-extracted signal drv_prs_dbt from bit_time_cfg_capture.vhd
can_bus.bit_time_cfg_capture_drv_ph1_dbt	0x104	4	Auto-extracted signal drv_ph1_dbt from bit_time_cfg_capture.vhd
can_bus.bit_time_cfg_capture_drv_ph2_dbt	0x108	4	Auto-extracted signal drv_ph2_dbt from bit_time_cfg_capture.vhd
can_bus.bit_time_cfg_capture_drv_sjw_dbt	0x10c	4	Auto-extracted signal drv_sjw_dbt from bit_time_cfg_capture.vhd
can_bus.bit_time_cfg_capture_tseg1_nbt_d	0x110	4	Auto-extracted signal tseg1_nbt_d from bit_time_cfg_capture.vhd
can_bus.bit_time_cfg_capture_tseg1_dbt_d	0x114	4	Auto-extracted signal tseg1_dbt_d from bit_time_cfg_capture.vhd

Name	Offset	Length	Description
can_bus.bit_time_cfg_capture_drv_ena	0x118	4	Auto-extracted signal drv_ena from bit_time_cfg_capture.vhd
can_bus.bit_time_cfg_capture_drv_ena_reg	0x11c	4	Auto-extracted signal drv_ena_reg from bit_time_cfg_capture.vhd
can_bus.bit_time_cfg_capture_drv_ena_reg_2	0x120	4	Auto-extracted signal drv_ena_reg_2 from bit_time_cfg_capture.vhd
can_bus.bit_time_cfg_capture_capture	0x124	4	Auto-extracted signal capture from bit_time_cfg_capture.vhd
can_bus.bit_time_counters_tq_counter_d	0x128	4	Auto-extracted signal tq_counter_d from bit_time_counters.vhd
can_bus.bit_time_counters_tq_counter_q	0x12c	4	Auto-extracted signal tq_counter_q from bit_time_counters.vhd
can_bus.bit_time_counters_tq_counter_ce	0x130	4	Auto-extracted signal tq_counter_ce from bit_time_counters.vhd
can_bus.bit_time_counters_tq_counter_allow	0x134	4	Auto-extracted signal tq_counter_allow from bit_time_counters.vhd
can_bus.bit_time_counters_tq_edge_i	0x138	4	Auto-extracted signal tq_edge_i from bit_time_counters.vhd
can_bus.bit_time_counters_segm_counter_d	0x13c	4	Auto-extracted signal segm_counter_d from bit_time_counters.vhd
can_bus.bit_time_counters_segm_counter_q	0x140	4	Auto-extracted signal segm_counter_q from bit_time_counters.vhd
can_bus.bit_time_counters_segm_counter_ce	0x144	4	Auto-extracted signal segm_counter_ce from bit_time_counters.vhd
can_bus.bit_time_fsm_bt_fsm_ce	0x148	4	Auto-extracted signal bt_fsm_ce from bit_time_fsm.vhd
can_bus.bus_sampling_drv_ena	0x14c	4	Auto-extracted signal drv_ena from bus_sampling.vhd
can_bus.bus_sampling_drv_ssp_offset	0x150	4	Auto-extracted signal drv_ssp_offset from bus_sampling.vhd
can_bus.bus_sampling_drv_ssp_delay_select	0x154	4	Auto-extracted signal drv_ssp_delay_select from bus_sampling.vhd
can_bus.bus_sampling_data_rx_synced	0x158	4	Auto-extracted signal data_rx_synced from bus_sampling.vhd

Name	Offset	Length	Description
can_bus.bus_sampling_prev_Sample	0x15c	4	Auto-extracted signal prev_Sample from bus_sampling.vhd
can_bus.bus_sampling_sample_sec_i	0x160	4	Auto-extracted signal sample_sec_i from bus_sampling.vhd
can_bus.bus_sampling_data_tx_delayed	0x164	4	Auto-extracted signal data_tx_delayed from bus_sampling.vhd
can_bus.bus_sampling_edge_rx_valid	0x168	4	Auto-extracted signal edge_rx_valid from bus_sampling.vhd
can_bus.bus_sampling_edge_tx_valid	0x16c	4	Auto-extracted signal edge_tx_valid from bus_sampling.vhd
can_bus.bus_sampling_ssp_delay	0x170	4	Auto-extracted signal ssp_delay from bus_sampling.vhd
can_bus.bus_sampling_tx_trigger_q	0x174	4	Auto-extracted signal tx_trigger_q from bus_sampling.vhd
can_bus.bus_sampling_tx_trigger_ssp	0x178	4	Auto-extracted signal tx_trigger_ssp from bus_sampling.vhd
can_bus.bus_sampling_shift_regs_res_d	0x17c	4	Auto-extracted signal shift_regs_res_d from bus_sampling.vhd
can_bus.bus_sampling_shift_regs_res_q	0x180	4	Auto-extracted signal shift_regs_res_q from bus_sampling.vhd
can_bus.bus_sampling_shift_regs_res_q_scan	0x184	4	Auto-extracted signal shift_regs_res_q_scan from bus_sampling.vhd
can_bus.bus_sampling_ssp_enable	0x188	4	Auto-extracted signal ssp_enable from bus_sampling.vhd
can_bus.bus_traffic_counters_tx_ctr_i	0x18c	4	Auto-extracted signal tx_ctr_i from bus_traffic_counters.vhd
can_bus.bus_traffic_counters_rx_ctr_i	0x190	4	Auto-extracted signal rx_ctr_i from bus_traffic_counters.vhd
can_bus.bus_traffic_counters_tx_ctr_rst_n_d	0x194	4	Auto-extracted signal tx_ctr_rst_n_d from bus_traffic_counters.vhd
can_bus.bus_traffic_counters_tx_ctr_rst_n_q	0x198	4	Auto-extracted signal tx_ctr_rst_n_q from bus_traffic_counters.vhd

Name	Offset	Length	Description
can_bus.bus_traffic_counters_tx_ctr_rst_n_q_scan	0x19c	4	Auto-extracted signal tx_ctr_rst_n_q_scan from bus_traffic_counters.vhd
can_bus.bus_traffic_counters_rx_ctr_rst_n_d	0x1a0	4	Auto-extracted signal rx_ctr_rst_n_d from bus_traffic_counters.vhd
can_bus.bus_traffic_counters_rx_ctr_rst_n_q	0x1a4	4	Auto-extracted signal rx_ctr_rst_n_q from bus_traffic_counters.vhd
can_bus.bus_traffic_counters_rx_ctr_rst_n_q_scan	0x1a8	4	Auto-extracted signal rx_ctr_rst_n_q_scan from bus_traffic_counters.vhd
can_bus.can_apb_tb_s_apb_paddr	0x1ac	4	Auto-extracted signal s_apb_paddr from can_apb_tb.vhd
can_bus.can_apb_tb_s_apb_penable	0x1b0	4	Auto-extracted signal s_apb_penable from can_apb_tb.vhd
can_bus.can_apb_tb_s_apb_pprot	0x1b4	4	Auto-extracted signal s_apb_pprot from can_apb_tb.vhd
can_bus.can_apb_tb_s_apb_prdata	0x1b8	4	Auto-extracted signal s_apb_prdata from can_apb_tb.vhd
can_bus.can_apb_tb_s_apb_pready	0x1bc	4	Auto-extracted signal s_apb_pready from can_apb_tb.vhd
can_bus.can_apb_tb_s_apb_psel	0x1c0	4	Auto-extracted signal s_apb_psel from can_apb_tb.vhd
can_bus.can_apb_tb_s_apb_pslverr	0x1c4	4	Auto-extracted signal s_apb_pslverr from can_apb_tb.vhd
can_bus.can_apb_tb_s_apb_pstrb	0x1c8	4	Auto-extracted signal s_apb_pstrb from can_apb_tb.vhd
can_bus.can_apb_tb_s_apb_pwdata	0x1cc	4	Auto-extracted signal s_apb_pwdata from can_apb_tb.vhd
can_bus.can_apb_tb_s_apb_pwrite	0x1d0	4	Auto-extracted signal s_apb_pwrite from can_apb_tb.vhd
can_bus.can_core_drv_clr_rx_ctr	0x1d4	4	Auto-extracted signal drv_clr_rx_ctr from can_core.vhd

Name	Offset	Length	Description
can_bus.can_core_drv_clr_tx_ctr	0x1d8	4	Auto-extracted signal drv_clr_tx_ctr from can_core.vhd
can_bus.can_core_drv_bus_mon_ena	0x1dc	4	Auto-extracted signal drv_bus_mon_ena from can_core.vhd
can_bus.can_core_drv_ena	0x1e0	4	Auto-extracted signal drv_ena from can_core.vhd
can_bus.can_core_rec_ident_i	0x1e4	4	Auto-extracted signal rec_ident_i from can_core.vhd
can_bus.can_core_rec_dlc_i	0x1e8	4	Auto-extracted signal rec_dlc_i from can_core.vhd
can_bus.can_core_rec_ident_type_i	0x1ec	4	Auto-extracted signal rec_ident_type_i from can_core.vhd
can_bus.can_core_rec_frame_type_i	0x1f0	4	Auto-extracted signal rec_frame_type_i from can_core.vhd
can_bus.can_core_rec_is_rtr_i	0x1f4	4	Auto-extracted signal rec_is_rtr_i from can_core.vhd
can_bus.can_core_rec_brs_i	0x1f8	4	Auto-extracted signal rec_brs_i from can_core.vhd
can_bus.can_core_rec_esi_i	0x1fc	4	Auto-extracted signal rec_esi_i from can_core.vhd
can_bus.can_core_alc	0x200	4	Auto-extracted signal alc from can_core.vhd
can_bus.can_core_erc_capture	0x204	4	Auto-extracted signal erc_capture from can_core.vhd
can_bus.can_core_is_transmitter	0x208	4	Auto-extracted signal is_transmitter from can_core.vhd
can_bus.can_core_is_receiver	0x20c	4	Auto-extracted signal is_receiver from can_core.vhd
can_bus.can_core_is_idle	0x210	4	Auto-extracted signal is_idle from can_core.vhd
can_bus.can_core_arbitration_lost_i	0x214	4	Auto-extracted signal arbitration_lost_i from can_core.vhd
can_bus.can_core_set_transmitter	0x218	4	Auto-extracted signal set_transmitter from can_core.vhd
can_bus.can_core_set_receiver	0x21c	4	Auto-extracted signal set_receiver from can_core.vhd
can_bus.can_core_set_idle	0x220	4	Auto-extracted signal set_idle from can_core.vhd
can_bus.can_core_is_err_active	0x224	4	Auto-extracted signal is_err_active from can_core.vhd

Name	Offset	Length	Description
can_bus.can_core_is_err_passive	0x228	4	Auto-extracted signal is_err_passive from can_core.vhd
can_bus.can_core_is_bus_off_i	0x22c	4	Auto-extracted signal is_bus_off_i from can_core.vhd
can_bus.can_core_err_detected_i	0x230	4	Auto-extracted signal err_detected_i from can_core.vhd
can_bus.can_core_primary_err	0x234	4	Auto-extracted signal primary_err from can_core.vhd
can_bus.can_core_act_err_ovr_flag	0x238	4	Auto-extracted signal act_err_ovr_flag from can_core.vhd
can_bus.can_core_err_delim_late	0x23c	4	Auto-extracted signal err_delim_late from can_core.vhd
can_bus.can_core_set_err_active	0x240	4	Auto-extracted signal set_err_active from can_core.vhd
can_bus.can_core_err_ctrs_unchanged	0x244	4	Auto-extracted signal err_ctrs_unchanged from can_core.vhd
can_bus.can_core_stuff_enable	0x248	4	Auto-extracted signal stuff_enable from can_core.vhd
can_bus.can_core_destuff_enable	0x24c	4	Auto-extracted signal destuff_enable from can_core.vhd
can_bus.can_core_fixed_stuff	0x250	4	Auto-extracted signal fixed_stuff from can_core.vhd
can_bus.can_core_tx_frame_no_sof	0x254	4	Auto-extracted signal tx_frame_no_sof from can_core.vhd
can_bus.can_core_stuff_length	0x258	4	Auto-extracted signal stuff_length from can_core.vhd
can_bus.can_core_dst_ctr	0x25c	4	Auto-extracted signal dst_ctr from can_core.vhd
can_bus.can_core_bst_ctr	0x260	4	Auto-extracted signal bst_ctr from can_core.vhd
can_bus.can_core_stuff_err	0x264	4	Auto-extracted signal stuff_err from can_core.vhd
can_bus.can_core_crc_enable	0x268	4	Auto-extracted signal crc_enable from can_core.vhd
can_bus.can_core_crc_spec_enable	0x26c	4	Auto-extracted signal crc_spec_enable from can_core.vhd

Name	Offset	Length	Description
can_bus.can_core_crc_calc_from_rx	0x270	4	Auto-extracted signal crc_calc_from_rx from can_core.vhd
can_bus.can_core_crc_15	0x274	4	Auto-extracted signal crc_15 from can_core.vhd
can_bus.can_core_crc_17	0x278	4	Auto-extracted signal crc_17 from can_core.vhd
can_bus.can_core_crc_21	0x27c	4	Auto-extracted signal crc_21 from can_core.vhd
can_bus.can_core_sp_control_i	0x280	4	Auto-extracted signal sp_control_i from can_core.vhd
can_bus.can_core_sp_control_q	0x284	4	Auto-extracted signal sp_control_q from can_core.vhd
can_bus.can_core_sync_control_i	0x288	4	Auto-extracted signal sync_control_i from can_core.vhd
can_bus.can_core_ssp_reset_i	0x28c	4	Auto-extracted signal ssp_reset_i from can_core.vhd
can_bus.can_core_tran_delay_meas_i	0x290	4	Auto-extracted signal tran_delay_meas_i from can_core.vhd
can_bus.can_core_tran_valid_i	0x294	4	Auto-extracted signal tran_valid_i from can_core.vhd
can_bus.can_core_rec_valid_i	0x298	4	Auto-extracted signal rec_valid_i from can_core.vhd
can_bus.can_core_br_shifted_i	0x29c	4	Auto-extracted signal br_shifted_i from can_core.vhd
can_bus.can_core_fcs_changed_i	0x2a0	4	Auto-extracted signal fcs_changed_i from can_core.vhd
can_bus.can_core_err_warning_limit_i	0x2a4	4	Auto-extracted signal err_warning_limit_i from can_core.vhd
can_bus.can_core_tx_err_ctr	0x2a8	4	Auto-extracted signal tx_err_ctr from can_core.vhd
can_bus.can_core_rx_err_ctr	0x2ac	4	Auto-extracted signal rx_err_ctr from can_core.vhd
can_bus.can_core_norm_err_ctr	0x2b0	4	Auto-extracted signal norm_err_ctr from can_core.vhd
can_bus.can_core_data_err_ctr	0x2b4	4	Auto-extracted signal data_err_ctr from can_core.vhd
can_bus.can_core_pc_tx_trigger	0x2b8	4	Auto-extracted signal pc_tx_trigger from can_core.vhd
can_bus.can_core_pc_rx_trigger	0x2bc	4	Auto-extracted signal pc_rx_trigger from can_core.vhd

Name	Offset	Length	Description
can_bus.can_core_pc_tx_data_nbs	0x2c0	4	Auto-extracted signal pc_tx_data_nbs from can_core.vhd
can_bus.can_core_pc_rx_data_nbs	0x2c4	4	Auto-extracted signal pc_rx_data_nbs from can_core.vhd
can_bus.can_core_crc_data_tx_wbs	0x2c8	4	Auto-extracted signal crc_data_tx_wbs from can_core.vhd
can_bus.can_core_crc_data_tx_nbs	0x2cc	4	Auto-extracted signal crc_data_tx_nbs from can_core.vhd
can_bus.can_core_crc_data_rx_wbs	0x2d0	4	Auto-extracted signal crc_data_rx_wbs from can_core.vhd
can_bus.can_core_crc_data_rx_nbs	0x2d4	4	Auto-extracted signal crc_data_rx_nbs from can_core.vhd
can_bus.can_core_crc_trig_tx_wbs	0x2d8	4	Auto-extracted signal crc_trig_tx_wbs from can_core.vhd
can_bus.can_core_crc_trig_tx_nbs	0x2dc	4	Auto-extracted signal crc_trig_tx_nbs from can_core.vhd
can_bus.can_core_crc_trig_rx_wbs	0x2e0	4	Auto-extracted signal crc_trig_rx_wbs from can_core.vhd
can_bus.can_core_crc_trig_rx_nbs	0x2e4	4	Auto-extracted signal crc_trig_rx_nbs from can_core.vhd
can_bus.can_core_bst_data_in	0x2e8	4	Auto-extracted signal bst_data_in from can_core.vhd
can_bus.can_core_bst_data_out	0x2ec	4	Auto-extracted signal bst_data_out from can_core.vhd
can_bus.can_core_bst_trigger	0x2f0	4	Auto-extracted signal bst_trigger from can_core.vhd
can_bus.can_core_data_halt	0x2f4	4	Auto-extracted signal data_halt from can_core.vhd
can_bus.can_core_bds_data_in	0x2f8	4	Auto-extracted signal bds_data_in from can_core.vhd
can_bus.can_core_bds_data_out	0x2fc	4	Auto-extracted signal bds_data_out from can_core.vhd
can_bus.can_core_bds_trigger	0x300	4	Auto-extracted signal bds_trigger from can_core.vhd
can_bus.can_core_destuffed	0x304	4	Auto-extracted signal destuffed from can_core.vhd

Name	Offset	Length	Description
can_bus.can_core_tx_ctr	0x308	4	Auto-extracted signal tx_ctr from can_core.vhd
can_bus.can_core_rx_ctr	0x30c	4	Auto-extracted signal rx_ctr from can_core.vhd
can_bus.can_core_tx_data_wbs_i	0x310	4	Auto-extracted signal tx_data_wbs_i from can_core.vhd
can_bus.can_core_lpb_dominant	0x314	4	Auto-extracted signal lpb_dominant from can_core.vhd
can_bus.can_core_form_err	0x318	4	Auto-extracted signal form_err from can_core.vhd
can_bus.can_core_ack_err	0x31c	4	Auto-extracted signal ack_err from can_core.vhd
can_bus.can_core_crc_err	0x320	4	Auto-extracted signal crc_err from can_core.vhd
can_bus.can_core_is_arbitration	0x324	4	Auto-extracted signal is_arbitration from can_core.vhd
can_bus.can_core_is_control	0x328	4	Auto-extracted signal is_control from can_core.vhd
can_bus.can_core_is_data	0x32c	4	Auto-extracted signal is_data from can_core.vhd
can_bus.can_core_is_stuff_count	0x330	4	Auto-extracted signal is_stuff_count from can_core.vhd
can_bus.can_core_is_crc	0x334	4	Auto-extracted signal is_crc from can_core.vhd
can_bus.can_core_is_crc_delim	0x338	4	Auto-extracted signal is_crc_delim from can_core.vhd
can_bus.can_core_is_ack_field	0x33c	4	Auto-extracted signal is_ack_field from can_core.vhd
can_bus.can_core_is_ack_delim	0x340	4	Auto-extracted signal is_ack_delim from can_core.vhd
can_bus.can_core_is_eof	0x344	4	Auto-extracted signal is_eof from can_core.vhd
can_bus.can_core_is_err_frm	0x348	4	Auto-extracted signal is_err_frm from can_core.vhd
can_bus.can_core_is_intermission	0x34c	4	Auto-extracted signal is_intermission from can_core.vhd
can_bus.can_core_is_suspend	0x350	4	Auto-extracted signal is_suspend from can_core.vhd
can_bus.can_core_is_overload_i	0x354	4	Auto-extracted signal is_overload_i from can_core.vhd
can_bus.can_core_is_sof	0x358	4	Auto-extracted signal is_sof from can_core.vhd

Name	Offset	Length	Description
can_bus.can_core_sof_pulse_i	0x35c	4	Auto-extracted signal sof_pulse_i from can_core.vhd
can_bus.can_core_load_init_vect	0x360	4	Auto-extracted signal load_init_vect from can_core.vhd
can_bus.can_core_retr_ctr_i	0x364	4	Auto-extracted signal retr_ctr_i from can_core.vhd
can_bus.can_core_decrement_rec	0x368	4	Auto-extracted signal decrement_rec from can_core.vhd
can_bus.can_core_bit_err_after_ack_err	0x36c	4	Auto-extracted signal bit_err_after_ack_err from can_core.vhd
can_bus.can_core_is_pexs	0x370	4	Auto-extracted signal is_pexs from can_core.vhd
can_bus.can_crc_drv_fd_type	0x374	4	Auto-extracted signal drv_fd_type from can_crc.vhd
can_bus.can_crc_init_vect_15	0x378	4	Auto-extracted signal init_vect_15 from can_crc.vhd
can_bus.can_crc_init_vect_17	0x37c	4	Auto-extracted signal init_vect_17 from can_crc.vhd
can_bus.can_crc_init_vect_21	0x380	4	Auto-extracted signal init_vect_21 from can_crc.vhd
can_bus.can_crc_crc_17_21_data_in	0x384	4	Auto-extracted signal crc_17_21_data_in from can_crc.vhd
can_bus.can_crc_crc_17_21_trigger	0x388	4	Auto-extracted signal crc_17_21_trigger from can_crc.vhd
can_bus.can_crc_crc_15_data_in	0x38c	4	Auto-extracted signal crc_15_data_in from can_crc.vhd
can_bus.can_crc_crc_15_trigger	0x390	4	Auto-extracted signal crc_15_trigger from can_crc.vhd
can_bus.can_crc_crc_ena_15	0x394	4	Auto-extracted signal crc_ena_15 from can_crc.vhd
can_bus.can_crc_crc_ena_17_21	0x398	4	Auto-extracted signal crc_ena_17_21 from can_crc.vhd
can_bus.can_top_ahb_ctu_can_data_in	0x39c	4	Auto-extracted signal ctu_can_data_in from can_top_ahb.vhd
can_bus.can_top_ahb_ctu_can_data_out	0x3a0	4	Auto-extracted signal ctu_can_data_out from can_top_ahb.vhd

Name	Offset	Length	Description
can_bus.can_top_ahb_ctu_can_adress	0x3a4	4	Auto-extracted signal ctu_can_adress from can_top_ahb.vhd
can_bus.can_top_ahb_ctu_can_scs	0x3a8	4	Auto-extracted signal ctu_can_scs from can_top_ahb.vhd
can_bus.can_top_ahb_ctu_can_srd	0x3ac	4	Auto-extracted signal ctu_can_srd from can_top_ahb.vhd
can_bus.can_top_ahb_ctu_can_swr	0x3b0	4	Auto-extracted signal ctu_can_swr from can_top_ahb.vhd
can_bus.can_top_ahb_ctu_can_sbe	0x3b4	4	Auto-extracted signal ctu_can_sbe from can_top_ahb.vhd
can_bus.can_top_ahb_res_n_out_i	0x3b8	4	Auto-extracted signal res_n_out_i from can_top_ahb.vhd
can_bus.can_top_apb_reg_data_in	0x3bc	4	Auto-extracted signal reg_data_in from can_top_apb.vhd
can_bus.can_top_apb_reg_data_out	0x3c0	4	Auto-extracted signal reg_data_out from can_top_apb.vhd
can_bus.can_top_apb_reg_addr	0x3c4	4	Auto-extracted signal reg_addr from can_top_apb.vhd
can_bus.can_top_apb_reg_be	0x3c8	4	Auto-extracted signal reg_be from can_top_apb.vhd
can_bus.can_top_apb_reg_rden	0x3cc	4	Auto-extracted signal reg_rden from can_top_apb.vhd
can_bus.can_top_apb_reg_wren	0x3d0	4	Auto-extracted signal reg_wren from can_top_apb.vhd
can_bus.can_top_level_drv_bus	0x3d4	4	Auto-extracted signal drv_bus from can_top_level.vhd
can_bus.can_top_level_stat_bus	0x3d8	4	Auto-extracted signal stat_bus from can_top_level.vhd
can_bus.can_top_level_res_n_sync	0x3dc	4	Auto-extracted signal res_n_sync from can_top_level.vhd
can_bus.can_top_level_res_core_n	0x3e0	4	Auto-extracted signal res_core_n from can_top_level.vhd
can_bus.can_top_level_res_soft_n	0x3e4	4	Auto-extracted signal res_soft_n from can_top_level.vhd
can_bus.can_top_level_sp_control	0x3e8	4	Auto-extracted signal sp_control from can_top_level.vhd

Name	Offset	Length	Description
can_bus.can_top_level_rx_buf_size	0x3ec	4	Auto-extracted signal rx_buf_size from can_top_level.vhd
can_bus.can_top_level_rx_full	0x3f0	4	Auto-extracted signal rx_full from can_top_level.vhd
can_bus.can_top_level_rx_empty	0x3f4	4	Auto-extracted signal rx_empty from can_top_level.vhd
can_bus.can_top_level_rx_frame_count	0x3f8	4	Auto-extracted signal rx_frame_count from can_top_level.vhd
can_bus.can_top_level_rx_mem_free	0x3fc	4	Auto-extracted signal rx_mem_free from can_top_level.vhd
can_bus.can_top_level_rx_read_pointer	0x400	4	Auto-extracted signal rx_read_pointer from can_top_level.vhd
can_bus.can_top_level_rx_write_pointer	0x404	4	Auto-extracted signal rx_write_pointer from can_top_level.vhd
can_bus.can_top_level_rx_data_overrun	0x408	4	Auto-extracted signal rx_data_overrun from can_top_level.vhd
can_bus.can_top_level_rx_read_buff	0x40c	4	Auto-extracted signal rx_read_buff from can_top_level.vhd
can_bus.can_top_level_rx_mof	0x410	4	Auto-extracted signal rx_mof from can_top_level.vhd
can_bus.can_top_level_txtb_port_a_data	0x414	4	Auto-extracted signal txtb_port_a_data from can_top_level.vhd
can_bus.can_top_level_txtb_port_a_address	0x418	4	Auto-extracted signal txtb_port_a_address from can_top_level.vhd
can_bus.can_top_level_txtb_port_a_cs	0x41c	4	Auto-extracted signal txtb_port_a_cs from can_top_level.vhd
can_bus.can_top_level_txtb_port_a_be	0x420	4	Auto-extracted signal txtb_port_a_be from can_top_level.vhd
can_bus.can_top_level_txtb_sw_cmd_index	0x424	4	Auto-extracted signal txtb_sw_cmd_index from can_top_level.vhd
can_bus.can_top_level_txt_buf_failed_bof	0x428	4	Auto-extracted signal txt_buf_failed_bof from can_top_level.vhd

Name	Offset	Length	Description
can_bus.can_top_level_int_vector	0x42c	4	Auto-extracted signal int_vector from can_top_level.vhd
can_bus.can_top_level_int_ena	0x430	4	Auto-extracted signal int_ena from can_top_level.vhd
can_bus.can_top_level_int_mask	0x434	4	Auto-extracted signal int_mask from can_top_level.vhd
can_bus.can_top_level_rec_ident	0x438	4	Auto-extracted signal rec_ident from can_top_level.vhd
can_bus.can_top_level_rec_dlc	0x43c	4	Auto-extracted signal rec_dlc from can_top_level.vhd
can_bus.can_top_level_rec_ident_type	0x440	4	Auto-extracted signal rec_ident_type from can_top_level.vhd
can_bus.can_top_level_rec_frame_type	0x444	4	Auto-extracted signal rec_frame_type from can_top_level.vhd
can_bus.can_top_level_rec_is_rtr	0x448	4	Auto-extracted signal rec_is_rtr from can_top_level.vhd
can_bus.can_top_level_rec_brs	0x44c	4	Auto-extracted signal rec_brs from can_top_level.vhd
can_bus.can_top_level_rec_esi	0x450	4	Auto-extracted signal rec_esi from can_top_level.vhd
can_bus.can_top_level_store_data_word	0x454	4	Auto-extracted signal store_data_word from can_top_level.vhd
can_bus.can_top_level_sof_pulse	0x458	4	Auto-extracted signal sof_pulse from can_top_level.vhd
can_bus.can_top_level_store_metadata	0x45c	4	Auto-extracted signal store_metadata from can_top_level.vhd
can_bus.can_top_level_store_data	0x460	4	Auto-extracted signal store_data from can_top_level.vhd
can_bus.can_top_level_rec_valid	0x464	4	Auto-extracted signal rec_valid from can_top_level.vhd
can_bus.can_top_level_rec_abort	0x468	4	Auto-extracted signal rec_abort from can_top_level.vhd
can_bus.can_top_level_store_metadata_f	0x46c	4	Auto-extracted signal store_metadata_f from can_top_level.vhd
can_bus.can_top_level_store_data_f	0x470	4	Auto-extracted signal store_data_f from can_top_level.vhd
can_bus.can_top_level_rec_valid_f	0x474	4	Auto-extracted signal rec_valid_f from can_top_level.vhd

Name	Offset	Length	Description
can_bus.can_top_level_rec_abort_f	0x478	4	Auto-extracted signal rec_abort_f from can_top_level.vhd
can_bus.can_top_level_txtb_hw_cmd_int	0x47c	4	Auto-extracted signal txtb_hw_cmd_int from can_top_level.vhd
can_bus.can_top_level_is_bus_off	0x480	4	Auto-extracted signal is_bus_off from can_top_level.vhd
can_bus.can_top_level_txtb_available	0x484	4	Auto-extracted signal txtb_available from can_top_level.vhd
can_bus.can_top_level_txtb_port_b_clk_en	0x488	4	Auto-extracted signal txtb_port_b_clk_en from can_top_level.vhd
can_bus.can_top_level_tran_dlc	0x48c	4	Auto-extracted signal tran_dlc from can_top_level.vhd
can_bus.can_top_level_tran_is_rtr	0x490	4	Auto-extracted signal tran_is_rtr from can_top_level.vhd
can_bus.can_top_level_tran_ident_type	0x494	4	Auto-extracted signal tran_ident_type from can_top_level.vhd
can_bus.can_top_level_tran_frame_type	0x498	4	Auto-extracted signal tran_frame_type from can_top_level.vhd
can_bus.can_top_level_tran_brs	0x49c	4	Auto-extracted signal tran_brs from can_top_level.vhd
can_bus.can_top_level_tran_identifier	0x4a0	4	Auto-extracted signal tran_identifier from can_top_level.vhd
can_bus.can_top_level_tran_word	0x4a4	4	Auto-extracted signal tran_word from can_top_level.vhd
can_bus.can_top_level_tran_frame_valid	0x4a8	4	Auto-extracted signal tran_frame_valid from can_top_level.vhd
can_bus.can_top_level_txtb_changed	0x4ac	4	Auto-extracted signal txtb_changed from can_top_level.vhd
can_bus.can_top_level_txtb_clk_en	0x4b0	4	Auto-extracted signal txtb_clk_en from can_top_level.vhd
can_bus.can_top_level_err_detected	0x4b4	4	Auto-extracted signal err_detected from can_top_level.vhd
can_bus.can_top_level_fcs_changed	0x4b8	4	Auto-extracted signal fcs_changed from can_top_level.vhd

Name	Offset	Length	Description
can_bus.can_top_level_err_warning_limit	0x4bc	4	Auto-extracted signal err_warning_limit from can_top_level.vhd
can_bus.can_top_level_arbitration_lost	0x4c0	4	Auto-extracted signal arbitration_lost from can_top_level.vhd
can_bus.can_top_level_tran_valid	0x4c4	4	Auto-extracted signal tran_valid from can_top_level.vhd
can_bus.can_top_level_br_shifted	0x4c8	4	Auto-extracted signal br_shifted from can_top_level.vhd
can_bus.can_top_level_is_overload	0x4cc	4	Auto-extracted signal is_overload from can_top_level.vhd
can_bus.can_top_level_rx_triggers	0x4d0	4	Auto-extracted signal rx_triggers from can_top_level.vhd
can_bus.can_top_level_tx_trigger	0x4d4	4	Auto-extracted signal tx_trigger from can_top_level.vhd
can_bus.can_top_level_sync_control	0x4d8	4	Auto-extracted signal sync_control from can_top_level.vhd
can_bus.can_top_level_no_pos_resync	0x4dc	4	Auto-extracted signal no_pos_resync from can_top_level.vhd
can_bus.can_top_level_nbt_ctrs_en	0x4e0	4	Auto-extracted signal nbt_ctrs_en from can_top_level.vhd
can_bus.can_top_level_dbt_ctrs_en	0x4e4	4	Auto-extracted signal dbt_ctrs_en from can_top_level.vhd
can_bus.can_top_level_trv_delay	0x4e8	4	Auto-extracted signal trv_delay from can_top_level.vhd
can_bus.can_top_level_rx_data_wbs	0x4ec	4	Auto-extracted signal rx_data_wbs from can_top_level.vhd
can_bus.can_top_level_tx_data_wbs	0x4f0	4	Auto-extracted signal tx_data_wbs from can_top_level.vhd
can_bus.can_top_level_ssp_reset	0x4f4	4	Auto-extracted signal ssp_reset from can_top_level.vhd
can_bus.can_top_level_tran_delay_meas	0x4f8	4	Auto-extracted signal tran_delay_meas from can_top_level.vhd
can_bus.can_top_level_bit_err	0x4fc	4	Auto-extracted signal bit_err from can_top_level.vhd
can_bus.can_top_level_sample_sec	0x500	4	Auto-extracted signal sample_sec from can_top_level.vhd

Name	Offset	Length	Description
can_bus.can_top_level_btmc_reset	0x504	4	Auto-extracted signal btmc_reset from can_top_level.vhd
can_bus.can_top_level_dbt_measure_start	0x508	4	Auto-extracted signal dbt_measure_start from can_top_level.vhd
can_bus.can_top_level_gen_first_ssp	0x50c	4	Auto-extracted signal gen_first_ssp from can_top_level.vhd
can_bus.can_top_level_sync_edge	0x510	4	Auto-extracted signal sync_edge from can_top_level.vhd
can_bus.can_top_level_tq_edge	0x514	4	Auto-extracted signal tq_edge from can_top_level.vhd
can_bus.can_top_level_tst_rdata_rx_buf	0x518	4	Auto-extracted signal tst_rdata_rx_buf from can_top_level.vhd
can_bus.clk_gate_clk_en_q	0x51c	4	Auto-extracted signal clk_en_q from clk_gate.vhd
can_bus.control_counter_ctrl_ctr_ce	0x520	4	Auto-extracted signal ctrl_ctr_ce from control_counter.vhd
can_bus.control_counter_compl_ctr_ce	0x524	4	Auto-extracted signal compl_ctr_ce from control_counter.vhd
can_bus.control_registers_reg_map_reg_sel	0x528	4	Auto-extracted signal reg_sel from control_registers_reg_map.vhd
can_bus.control_registers_reg_map_read_data_mux_in	0x52c	4	Auto-extracted signal read_data_mux_in from control_registers_reg_map.vhd
can_bus.control_registers_reg_map_read_data_mask_n	0x530	4	Auto-extracted signal read_data_mask_n from control_registers_reg_map.vhd
can_bus.control_registers_reg_map_read_mux_ena	0x534	4	Auto-extracted signal read_mux_ena from control_registers_reg_map.vhd
can_bus.crc_calc_crc_q	0x538	4	Auto-extracted signal crc_q from crc_calc.vhd
can_bus.crc_calc_crc_nxt	0x53c	4	Auto-extracted signal crc_nxt from crc_calc.vhd
can_bus.crc_calc_crc_shift	0x540	4	Auto-extracted signal crc_shift from crc_calc.vhd
can_bus.crc_calc_crc_shift_n_xor	0x544	4	Auto-extracted signal crc_shift_n_xor from crc_calc.vhd
can_bus.crc_calc_crc_d	0x548	4	Auto-extracted signal crc_d from crc_calc.vhd

Name	Offset	Length	Description
can_bus.crc_calc_crc_ce	0x54c	4	Auto-extracted signal crc_ce from crc_calc.vhd
can_bus.data_edge_detector_rx_data_prev	0x550	4	Auto-extracted signal rx_data_prev from data_edge_detector.vhd
can_bus.data_edge_detector_tx_data_prev	0x554	4	Auto-extracted signal tx_data_prev from data_edge_detector.vhd
can_bus.data_edge_detector_rx_data_sync_prev	0x558	4	Auto-extracted signal rx_data_sync_prev from data_edge_detector.vhd
can_bus.data_edge_detector_rx_edge_i	0x55c	4	Auto-extracted signal rx_edge_i from data_edge_detector.vhd
can_bus.data_edge_detector_tx_edge_i	0x560	4	Auto-extracted signal tx_edge_i from data_edge_detector.vhd
can_bus.data_mux_sel_data	0x564	4	Auto-extracted signal sel_data from data_mux.vhd
can_bus.data_mux_saturated_data	0x568	4	Auto-extracted signal saturated_data from data_mux.vhd
can_bus.data_mux_masked_data	0x56c	4	Auto-extracted signal masked_data from data_mux.vhd
can_bus.dlc_decoder_data_len_8_to_64	0x570	4	Auto-extracted signal data_len_8_to_64 from dlc_decoder.vhd
can_bus.dlc_decoder_data_len_can_2_0	0x574	4	Auto-extracted signal data_len_can_2_0 from dlc_decoder.vhd
can_bus.dlc_decoder_data_len_can_fd	0x578	4	Auto-extracted signal data_len_can_fd from dlc_decoder.vhd
can_bus.endian_swapper_swapped	0x57c	4	Auto-extracted signal swapped from endian_swapper.vhd
can_bus.err_counters_tx_err_ctr_ce	0x580	4	Auto-extracted signal tx_err_ctr_ce from err_counters.vhd
can_bus.err_counters_rx_err_ctr_ce	0x584	4	Auto-extracted signal rx_err_ctr_ce from err_counters.vhd
can_bus.err_counters_modif_tx_ctr	0x588	4	Auto-extracted signal modif_tx_ctr from err_counters.vhd
can_bus.err_counters_modif_rx_ctr	0x58c	4	Auto-extracted signal modif_rx_ctr from err_counters.vhd

Name	Offset	Length	Description
can_bus.err_counters_nom_err_ctr_ce	0x590	4	Auto-extracted signal nom_err_ctr_ce from err_counters.vhd
can_bus.err_counters_data_err_ctr_ce	0x594	4	Auto-extracted signal data_err_ctr_ce from err_counters.vhd
can_bus.err_counters_res_err_ctrs_d	0x598	4	Auto-extracted signal res_err_ctrs_d from err_counters.vhd
can_bus.err_counters_res_err_ctrs_q	0x59c	4	Auto-extracted signal res_err_ctrs_q from err_counters.vhd
can_bus.err_counters_res_err_ctrs_q_scan	0x5a0	4	Auto-extracted signal res_err_ctrs_q_scan from err_counters.vhd
can_bus.err_detector_err_frm_req_i	0x5a4	4	Auto-extracted signal err_frm_req_i from err_detector.vhd
can_bus.err_detector_err_type_d	0x5a8	4	Auto-extracted signal err_type_d from err_detector.vhd
can_bus.err_detector_err_type_q	0x5ac	4	Auto-extracted signal err_type_q from err_detector.vhd
can_bus.err_detector_err_pos_q	0x5b0	4	Auto-extracted signal err_pos_q from err_detector.vhd
can_bus.err_detector_form_err_i	0x5b4	4	Auto-extracted signal form_err_i from err_detector.vhd
can_bus.err_detector_crc_match_c	0x5b8	4	Auto-extracted signal crc_match_c from err_detector.vhd
can_bus.err_detector_crc_match_d	0x5bc	4	Auto-extracted signal crc_match_d from err_detector.vhd
can_bus.err_detector_crc_match_q	0x5c0	4	Auto-extracted signal crc_match_q from err_detector.vhd
can_bus.err_detector_dst_ctr_grey	0x5c4	4	Auto-extracted signal dst_ctr_grey from err_detector.vhd
can_bus.err_detector_dst_parity	0x5c8	4	Auto-extracted signal dst_parity from err_detector.vhd
can_bus.err_detector_stuff_count_check	0x5cc	4	Auto-extracted signal stuff_count_check from err_detector.vhd
can_bus.err_detector_crc_15_ok	0x5d0	4	Auto-extracted signal crc_15_ok from err_detector.vhd

Name	Offset	Length	Description
can_bus.err_detector_crc_17_ok	0x5d4	4	Auto-extracted signal crc_17_ok from err_detector.vhd
can_bus.err_detector_crc_21_ok	0x5d8	4	Auto-extracted signal crc_21_ok from err_detector.vhd
can_bus.err_detector_stuff_count_ok	0x5dc	4	Auto-extracted signal stuff_count_ok from err_detector.vhd
can_bus.err_detector_rx_crc_15	0x5e0	4	Auto-extracted signal rx_crc_15 from err_detector.vhd
can_bus.err_detector_rx_crc_17	0x5e4	4	Auto-extracted signal rx_crc_17 from err_detector.vhd
can_bus.err_detector_rx_crc_21	0x5e8	4	Auto-extracted signal rx_crc_21 from err_detector.vhd
can_bus.fault_confinement_drv_ewl	0x5ec	4	Auto-extracted signal drv_ewl from fault_confinement.vhd
can_bus.fault_confinement_drv_erp	0x5f0	4	Auto-extracted signal drv_erp from fault_confinement.vhd
can_bus.fault_confinement_drv_ctr_val	0x5f4	4	Auto-extracted signal drv_ctr_val from fault_confinement.vhd
can_bus.fault_confinement_drv_ctr_sel	0x5f8	4	Auto-extracted signal drv_ctr_sel from fault_confinement.vhd
can_bus.fault_confinement_drv_ena	0x5fc	4	Auto-extracted signal drv_ena from fault_confinement.vhd
can_bus.fault_confinement_tx_err_ctr_i	0x600	4	Auto-extracted signal tx_err_ctr_i from fault_confinement.vhd
can_bus.fault_confinement_rx_err_ctr_i	0x604	4	Auto-extracted signal rx_err_ctr_i from fault_confinement.vhd
can_bus.fault_confinement_inc_one	0x608	4	Auto-extracted signal inc_one from fault_confinement.vhd
can_bus.fault_confinement_inc_eight	0x60c	4	Auto-extracted signal inc_eight from fault_confinement.vhd
can_bus.fault_confinement_dec_one	0x610	4	Auto-extracted signal dec_one from fault_confinement.vhd
can_bus.fault_confinement_drv_rom_ena	0x614	4	Auto-extracted signal drv_rom_ena from fault_confinement.vhd
can_bus.fault_confinement_fsm_tx_err_ctr_mt_erp	0x618	4	Auto-extracted signal tx_err_ctr_mt_erp from fault_confinement_fsm.vhd
can_bus.fault_confinement_fsm_rx_err_ctr_mt_erp	0x61c	4	Auto-extracted signal rx_err_ctr_mt_erp from fault_confinement_fsm.vhd

Name	Offset	Length	Description
can_bus.fault_confinement_fsm_tx_err_ctr_mt_ewl	0x620	4	Auto-extracted signal tx_err_ctr_mt_ewl from fault_confinement_fsm.vhd
can_bus.fault_confinement_fsm_rx_err_ctr_mt_ewl	0x624	4	Auto-extracted signal rx_err_ctr_mt_ewl from fault_confinement_fsm.vhd
can_bus.fault_confinement_fsm_tx_err_ctr_mt_255	0x628	4	Auto-extracted signal tx_err_ctr_mt_255 from fault_confinement_fsm.vhd
can_bus.fault_confinement_fsm_err_warning_limit_d	0x62c	4	Auto-extracted signal err_warning_limit_d from fault_confinement_fsm.vhd
can_bus.fault_confinement_fsm_err_warning_limit_q	0x630	4	Auto-extracted signal err_warning_limit_q from fault_confinement_fsm.vhd
can_bus.fault_confinement_fsm_fc_fsm_res_d	0x634	4	Auto-extracted signal fc_fsm_res_d from fault_confinement_fsm.vhd
can_bus.fault_confinement_fsm_fc_fsm_res_q	0x638	4	Auto-extracted signal fc_fsm_res_q from fault_confinement_fsm.vhd
can_bus.fault_confinement_rules_inc_one_i	0x63c	4	Auto-extracted signal inc_one_i from fault_confinement_rules.vhd
can_bus.fault_confinement_rules_inc_eight_i	0x640	4	Auto-extracted signal inc_eight_i from fault_confinement_rules.vhd
can_bus.frame_filters_drv_filter_A_mask	0x644	4	Auto-extracted signal drv_filter_A_mask from frame_filters.vhd
can_bus.frame_filters_drv_filter_A_ctrl	0x648	4	Auto-extracted signal drv_filter_A_ctrl from frame_filters.vhd
can_bus.frame_filters_drv_filter_A_bits	0x64c	4	Auto-extracted signal drv_filter_A_bits from frame_filters.vhd
can_bus.frame_filters_int_filter_A_valid	0x650	4	Auto-extracted signal int_filter_A_valid from frame_filters.vhd
can_bus.frame_filters_drv_filter_B_mask	0x654	4	Auto-extracted signal drv_filter_B_mask from frame_filters.vhd
can_bus.frame_filters_drv_filter_B_ctrl	0x658	4	Auto-extracted signal drv_filter_B_ctrl from frame_filters.vhd

Name	Offset	Length	Description
can_bus.frame_filters_drv_filter_B_bits	0x65c	4	Auto-extracted signal drv_filter_B_bits from frame_filters.vhd
can_bus.frame_filters_int_filter_B_valid	0x660	4	Auto-extracted signal int_filter_B_valid from frame_filters.vhd
can_bus.frame_filters_drv_filter_C_mask	0x664	4	Auto-extracted signal drv_filter_C_mask from frame_filters.vhd
can_bus.frame_filters_drv_filter_C_ctrl	0x668	4	Auto-extracted signal drv_filter_C_ctrl from frame_filters.vhd
can_bus.frame_filters_drv_filter_C_bits	0x66c	4	Auto-extracted signal drv_filter_C_bits from frame_filters.vhd
can_bus.frame_filters_int_filter_C_valid	0x670	4	Auto-extracted signal int_filter_C_valid from frame_filters.vhd
can_bus.frame_filters_drv_filter_ran_ctrl	0x674	4	Auto-extracted signal drv_filter_ran_ctrl from frame_filters.vhd
can_bus.frame_filters_drv_filter_ran_lo_th	0x678	4	Auto-extracted signal drv_filter_ran_lo_th from frame_filters.vhd
can_bus.frame_filters_drv_filter_ran_hi_th	0x67c	4	Auto-extracted signal drv_filter_ran_hi_th from frame_filters.vhd
can_bus.frame_filters_int_filter_ran_valid	0x680	4	Auto-extracted signal int_filter_ran_valid from frame_filters.vhd
can_bus.frame_filters_drv_filters_ena	0x684	4	Auto-extracted signal drv_filters_ena from frame_filters.vhd
can_bus.frame_filters_int_data_type	0x688	4	Auto-extracted signal int_data_type from frame_filters.vhd
can_bus.frame_filters_int_data_ctrl	0x68c	4	Auto-extracted signal int_data_ctrl from frame_filters.vhd
can_bus.frame_filters_filter_A_enable	0x690	4	Auto-extracted signal filter_A_enable from frame_filters.vhd
can_bus.frame_filters_filter_B_enable	0x694	4	Auto-extracted signal filter_B_enable from frame_filters.vhd

Name	Offset	Length	Description
can_bus.frame_filters_filter_C_enable	0x698	4	Auto-extracted signal filter_C_enable from frame_filters.vhd
can_bus.frame_filters_filter_range_enable	0x69c	4	Auto-extracted signal filter_range_enable from frame_filters.vhd
can_bus.frame_filters_filter_result	0x6a0	4	Auto-extracted signal filter_result from frame_filters.vhd
can_bus.frame_filters_ident_valid_d	0x6a4	4	Auto-extracted signal ident_valid_d from frame_filters.vhd
can_bus.frame_filters_ident_valid_q	0x6a8	4	Auto-extracted signal ident_valid_q from frame_filters.vhd
can_bus.frame_filters_drv_drop_remote_frames	0x6ac	4	Auto-extracted signal drv_drop_remote_frames from frame_filters.vhd
can_bus.frame_filters_drop_rtr_frame	0x6b0	4	Auto-extracted signal drop_rtr_frame from frame_filters.vhd
can_bus.inf_ram_wrapper_int_read_data	0x6b4	4	Auto-extracted signal int_read_data from inf_ram_wrapper.vhd
can_bus.inf_ram_wrapper_byte_we	0x6b8	4	Auto-extracted signal byte_we from inf_ram_wrapper.vhd
can_bus.int_manager_drv_int_vect_clr	0x6bc	4	Auto-extracted signal drv_int_vect_clr from int_manager.vhd
can_bus.int_manager_drv_int_ena_set	0x6c0	4	Auto-extracted signal drv_int_ena_set from int_manager.vhd
can_bus.int_manager_drv_int_ena_clr	0x6c4	4	Auto-extracted signal drv_int_ena_clr from int_manager.vhd
can_bus.int_manager_drv_int_mask_set	0x6c8	4	Auto-extracted signal drv_int_mask_set from int_manager.vhd
can_bus.int_manager_drv_int_mask_clr	0x6cc	4	Auto-extracted signal drv_int_mask_clr from int_manager.vhd
can_bus.int_manager_int_ena_i	0x6d0	4	Auto-extracted signal int_ena_i from int_manager.vhd
can_bus.int_manager_int_mask_i	0x6d4	4	Auto-extracted signal int_mask_i from int_manager.vhd
can_bus.int_manager_int_vect_i	0x6d8	4	Auto-extracted signal int_vect_i from int_manager.vhd

Name	Offset	Length	Description
can_bus.int_manager_int_input_active	0x6dc	4	Auto-extracted signal int_input_active from int_manager.vhd
can_bus.int_manager_int_i	0x6e0	4	Auto-extracted signal int_i from int_manager.vhd
can_bus.int_module_int_mask_i	0x6e4	4	Auto-extracted signal int_mask_i from int_module.vhd
can_bus.int_module_int_ena_i	0x6e8	4	Auto-extracted signal int_ena_i from int_module.vhd
can_bus.int_module_int_mask_load	0x6ec	4	Auto-extracted signal int_mask_load from int_module.vhd
can_bus.int_module_int_mask_next	0x6f0	4	Auto-extracted signal int_mask_next from int_module.vhd
can_bus.memory_reg_reg_value_r	0x6f4	4	Auto-extracted signal reg_value_r from memory_reg.vhd
can_bus.memory_reg_wr_select	0x6f8	4	Auto-extracted signal wr_select from memory_reg.vhd
can_bus.memory_reg_wr_select_expanded	0x6fc	4	Auto-extracted signal wr_select_expanded from memory_reg.vhd
can_bus.memory_registers_status_comb	0x700	4	Auto-extracted signal status_comb from memory_registers.vhd
can_bus.memory_registers_can_core_cs	0x704	4	Auto-extracted signal can_core_cs from memory_registers.vhd
can_bus.memory_registers_control_registers_cs	0x708	4	Auto-extracted signal control_registers_cs from memory_registers.vhd
can_bus.memory_registers_control_registers_cs_reg	0x70c	4	Auto-extracted signal control_registers_cs_reg from memory_registers.vhd
can_bus.memory_registers_test_registers_cs	0x710	4	Auto-extracted signal test_registers_cs from memory_registers.vhd
can_bus.memory_registers_test_registers_cs_reg	0x714	4	Auto-extracted signal test_registers_cs_reg from memory_registers.vhd
can_bus.memory_registers_control_registers_rdata	0x718	4	Auto-extracted signal control_registers_rdata from memory_registers.vhd

Name	Offset	Length	Description
can_bus.memory_registers_test_registers_rdata	0x71c	4	Auto-extracted signal test_registers_rdata from memory_registers.vhd
can_bus.memory_registers_is_err_active	0x720	4	Auto-extracted signal is_err_active from memory_registers.vhd
can_bus.memory_registers_is_err_passive	0x724	4	Auto-extracted signal is_err_passive from memory_registers.vhd
can_bus.memory_registers_is_bus_off	0x728	4	Auto-extracted signal is_bus_off from memory_registers.vhd
can_bus.memory_registers_is_transmitter	0x72c	4	Auto-extracted signal is_transmitter from memory_registers.vhd
can_bus.memory_registers_is_receiver	0x730	4	Auto-extracted signal is_receiver from memory_registers.vhd
can_bus.memory_registers_is_idle	0x734	4	Auto-extracted signal is_idle from memory_registers.vhd
can_bus.memory_registers_reg_lock_1_active	0x738	4	Auto-extracted signal reg_lock_1_active from memory_registers.vhd
can_bus.memory_registers_reg_lock_2_active	0x73c	4	Auto-extracted signal reg_lock_2_active from memory_registers.vhd
can_bus.memory_registers_soft_res_q_n	0x740	4	Auto-extracted signal soft_res_q_n from memory_registers.vhd
can_bus.memory_registers_ewl_padded	0x744	4	Auto-extracted signal ewl_padded from memory_registers.vhd
can_bus.memory_registers_control_regs_clk_en	0x748	4	Auto-extracted signal control_regs_clk_en from memory_registers.vhd
can_bus.memory_registers_test_regs_clk_en	0x74c	4	Auto-extracted signal test_regs_clk_en from memory_registers.vhd
can_bus.memory_registers_clk_control_regs	0x750	4	Auto-extracted signal clk_control_regs from memory_registers.vhd
can_bus.memory_registers_clk_test_regs	0x754	4	Auto-extracted signal clk_test_regs from memory_registers.vhd
can_bus.memory_registers_rx_buf_mode	0x758	4	Auto-extracted signal rx_buf_mode from memory_registers.vhd

Name	Offset	Length	Description
can_bus.memory_registers_rx_move_cmd	0x75c	4	Auto-extracted signal rx_move_cmd from memory_registers.vhd
can_bus.memory_registers_ctr_pres_sel_q	0x760	4	Auto-extracted signal ctr_pres_sel_q from memory_registers.vhd
can_bus.operation_control_drv_ena	0x764	4	Auto-extracted signal drv_ena from operation_control.vhd
can_bus.operation_control_go_to_off	0x768	4	Auto-extracted signal go_to_off from operation_control.vhd
can_bus.prescaler_drv_ena	0x76c	4	Auto-extracted signal drv_ena from prescaler.vhd
can_bus.prescaler_tseg1_nbt	0x770	4	Auto-extracted signal tseg1_nbt from prescaler.vhd
can_bus.prescaler_tseg2_nbt	0x774	4	Auto-extracted signal tseg2_nbt from prescaler.vhd
can_bus.prescaler_brp_nbt	0x778	4	Auto-extracted signal brp_nbt from prescaler.vhd
can_bus.prescaler_sjw_nbt	0x77c	4	Auto-extracted signal sjw_nbt from prescaler.vhd
can_bus.prescaler_tseg1_dbt	0x780	4	Auto-extracted signal tseg1_dbt from prescaler.vhd
can_bus.prescaler_tseg2_dbt	0x784	4	Auto-extracted signal tseg2_dbt from prescaler.vhd
can_bus.prescaler_brp_dbt	0x788	4	Auto-extracted signal brp_dbt from prescaler.vhd
can_bus.prescaler_sjw_dbt	0x78c	4	Auto-extracted signal sjw_dbt from prescaler.vhd
can_bus.prescaler_segment_end	0x790	4	Auto-extracted signal segment_end from prescaler.vhd
can_bus.prescaler_h_sync_valid	0x794	4	Auto-extracted signal h_sync_valid from prescaler.vhd
can_bus.prescaler_is_tseg1	0x798	4	Auto-extracted signal is_tseg1 from prescaler.vhd
can_bus.prescaler_is_tseg2	0x79c	4	Auto-extracted signal is_tseg2 from prescaler.vhd
can_bus.prescaler_resync_edge_valid	0x7a0	4	Auto-extracted signal resync_edge_valid from prescaler.vhd
can_bus.prescaler_h_sync_edge_valid	0x7a4	4	Auto-extracted signal h_sync_edge_valid from prescaler.vhd
can_bus.prescaler_segm_counter_nbt	0x7a8	4	Auto-extracted signal segm_counter_nbt from prescaler.vhd

Name	Offset	Length	Description
can_bus.prescaler_segm_counter_dbt	0x7ac	4	Auto-extracted signal segm_counter_dbt from prescaler.vhd
can_bus.prescaler_exit_segm_req_nbt	0x7b0	4	Auto-extracted signal exit_segm_req_nbt from prescaler.vhd
can_bus.prescaler_exit_segm_req_dbt	0x7b4	4	Auto-extracted signal exit_segm_req_dbt from prescaler.vhd
can_bus.prescaler_tq_edge_nbt	0x7b8	4	Auto-extracted signal tq_edge_nbt from prescaler.vhd
can_bus.prescaler_tq_edge_dbt	0x7bc	4	Auto-extracted signal tq_edge_dbt from prescaler.vhd
can_bus.prescaler_rx_trig_req	0x7c0	4	Auto-extracted signal rx_trig_req from prescaler.vhd
can_bus.prescaler_tx_trig_req	0x7c4	4	Auto-extracted signal tx_trig_req from prescaler.vhd
can_bus.prescaler_start_edge	0x7c8	4	Auto-extracted signal start_edge from prescaler.vhd
can_bus.prescaler_bt_ctr_clear	0x7cc	4	Auto-extracted signal bt_ctr_clear from prescaler.vhd
can_bus.priority_decoder_l0_valid	0x7d0	4	Auto-extracted signal l0_valid from priority_decoder.vhd
can_bus.priority_decoder_l1_valid	0x7d4	4	Auto-extracted signal l1_valid from priority_decoder.vhd
can_bus.priority_decoder_l1_winner	0x7d8	4	Auto-extracted signal l1_winner from priority_decoder.vhd
can_bus.priority_decoder_l2_valid	0x7dc	4	Auto-extracted signal l2_valid from priority_decoder.vhd
can_bus.priority_decoder_l2_winner	0x7e0	4	Auto-extracted signal l2_winner from priority_decoder.vhd
can_bus.priority_decoder_l3_valid	0x7e4	4	Auto-extracted signal l3_valid from priority_decoder.vhd
can_bus.priority_decoder_l3_winner	0x7e8	4	Auto-extracted signal l3_winner from priority_decoder.vhd
can_bus.protocol_control_drv_can_fd_ena	0x7ec	4	Auto-extracted signal drv_can_fd_ena from protocol_control.vhd
can_bus.protocol_control_drv_bus_mon_ena	0x7f0	4	Auto-extracted signal drv_bus_mon_ena from protocol_control.vhd
can_bus.protocol_control_drv_retr_lim_ena	0x7f4	4	Auto-extracted signal drv_retr_lim_ena from protocol_control.vhd

Name	Offset	Length	Description
can_bus.protocol_control_drv_retr_th	0x7f8	4	Auto-extracted signal drv_retr_th from protocol_control.vhd
can_bus.protocol_control_drv_self_test_ena	0x7fc	4	Auto-extracted signal drv_self_test_ena from protocol_control.vhd
can_bus.protocol_control_drv_ack_forb	0x800	4	Auto-extracted signal drv_ack_forb from protocol_control.vhd
can_bus.protocol_control_drv_ena	0x804	4	Auto-extracted signal drv_ena from protocol_control.vhd
can_bus.protocol_control_drv_fd_type	0x808	4	Auto-extracted signal drv_fd_type from protocol_control.vhd
can_bus.protocol_control_drv_int_loopback_ena	0x80c	4	Auto-extracted signal drv_int_loopback_ena from protocol_control.vhd
can_bus.protocol_control_drv_bus_off_reset	0x810	4	Auto-extracted signal drv_bus_off_reset from protocol_control.vhd
can_bus.protocol_control_drv_ssp_delay_select	0x814	4	Auto-extracted signal drv_ssp_delay_select from protocol_control.vhd
can_bus.protocol_control_drv_pex	0x818	4	Auto-extracted signal drv_pex from protocol_control.vhd
can_bus.protocol_control_drv_cpexs	0x81c	4	Auto-extracted signal drv_cpexs from protocol_control.vhd
can_bus.protocol_control_tran_word_swapped	0x820	4	Auto-extracted signal tran_word_swapped from protocol_control.vhd
can_bus.protocol_control_err_frm_req	0x824	4	Auto-extracted signal err_frm_req from protocol_control.vhd
can_bus.protocol_control_tx_load_base_id	0x828	4	Auto-extracted signal tx_load_base_id from protocol_control.vhd
can_bus.protocol_control_tx_load_ext_id	0x82c	4	Auto-extracted signal tx_load_ext_id from protocol_control.vhd
can_bus.protocol_control_tx_load_dlc	0x830	4	Auto-extracted signal tx_load_dlc from protocol_control.vhd
can_bus.protocol_control_tx_load_data_word	0x834	4	Auto-extracted signal tx_load_data_word from protocol_control.vhd

Name	Offset	Length	Description
can_bus.protocol_control_tx_load_stuff_count	0x838	4	Auto-extracted signal tx_load_stuff_count from protocol_control.vhd
can_bus.protocol_control_tx_load_crc	0x83c	4	Auto-extracted signal tx_load_crc from protocol_control.vhd
can_bus.protocol_control_tx_shift_ena	0x840	4	Auto-extracted signal tx_shift_ena from protocol_control.vhd
can_bus.protocol_control_tx_dominant	0x844	4	Auto-extracted signal tx_dominant from protocol_control.vhd
can_bus.protocol_control_rx_clear	0x848	4	Auto-extracted signal rx_clear from protocol_control.vhd
can_bus.protocol_control_rx_store_base_id	0x84c	4	Auto-extracted signal rx_store_base_id from protocol_control.vhd
can_bus.protocol_control_rx_store_ext_id	0x850	4	Auto-extracted signal rx_store_ext_id from protocol_control.vhd
can_bus.protocol_control_rx_store_ide	0x854	4	Auto-extracted signal rx_store_ide from protocol_control.vhd
can_bus.protocol_control_rx_store_rtr	0x858	4	Auto-extracted signal rx_store_rtr from protocol_control.vhd
can_bus.protocol_control_rx_store_edl	0x85c	4	Auto-extracted signal rx_store_edl from protocol_control.vhd
can_bus.protocol_control_rx_store_dlc	0x860	4	Auto-extracted signal rx_store_dlc from protocol_control.vhd
can_bus.protocol_control_rx_store_esi	0x864	4	Auto-extracted signal rx_store_esi from protocol_control.vhd
can_bus.protocol_control_rx_store_brs	0x868	4	Auto-extracted signal rx_store_brs from protocol_control.vhd
can_bus.protocol_control_rx_store_stuff_count	0x86c	4	Auto-extracted signal rx_store_stuff_count from protocol_control.vhd
can_bus.protocol_control_rx_shift_ena	0x870	4	Auto-extracted signal rx_shift_ena from protocol_control.vhd

Name	Offset	Length	Description
can_bus.protocol_control_rx_shift_in_sel	0x874	4	Auto-extracted signal rx_shift_in_sel from protocol_control.vhd
can_bus.protocol_control_rec_is_rtr_i	0x878	4	Auto-extracted signal rec_is_rtr_i from protocol_control.vhd
can_bus.protocol_control_rec_dlc_d	0x87c	4	Auto-extracted signal rec_dlc_d from protocol_control.vhd
can_bus.protocol_control_rec_dlc_q	0x880	4	Auto-extracted signal rec_dlc_q from protocol_control.vhd
can_bus.protocol_control_rec_frame_type_i	0x884	4	Auto-extracted signal rec_frame_type_i from protocol_control.vhd
can_bus.protocol_control_ctrl_ctr_pload	0x888	4	Auto-extracted signal ctrl_ctr_pload from protocol_control.vhd
can_bus.protocol_control_ctrl_ctr_pload_val	0x88c	4	Auto-extracted signal ctrl_ctr_pload_val from protocol_control.vhd
can_bus.protocol_control_ctrl_ctr_ena	0x890	4	Auto-extracted signal ctrl_ctr_ena from protocol_control.vhd
can_bus.protocol_control_ctrl_ctr_zero	0x894	4	Auto-extracted signal ctrl_ctr_zero from protocol_control.vhd
can_bus.protocol_control_ctrl_ctr_one	0x898	4	Auto-extracted signal ctrl_ctr_one from protocol_control.vhd
can_bus.protocol_control_ctrl_counted_byte	0x89c	4	Auto-extracted signal ctrl_counted_byte from protocol_control.vhd
can_bus.protocol_control_ctrl_counted_byte_index	0x8a0	4	Auto-extracted signal ctrl_counted_byte_index from protocol_control.vhd
can_bus.protocol_control_ctrl_ctr_mem_index	0x8a4	4	Auto-extracted signal ctrl_ctr_mem_index from protocol_control.vhd
can_bus.protocol_control_compl_ctr_ena	0x8a8	4	Auto-extracted signal compl_ctr_ena from protocol_control.vhd
can_bus.protocol_control_reinteg_ctr_clr	0x8ac	4	Auto-extracted signal reinteg_ctr_clr from protocol_control.vhd
can_bus.protocol_control_reinteg_ctr_enable	0x8b0	4	Auto-extracted signal reinteg_ctr_enable from protocol_control.vhd

Name	Offset	Length	Description
can_bus.protocol_control_reinteg_ctr_expired	0x8b4	4	Auto-extracted signal reinteg_ctr_expired from protocol_control.vhd
can_bus.protocol_control_retr_ctr_clear	0x8b8	4	Auto-extracted signal retr_ctr_clear from protocol_control.vhd
can_bus.protocol_control_retr_ctr_add	0x8bc	4	Auto-extracted signal retr_ctr_add from protocol_control.vhd
can_bus.protocol_control_retr_limit_reached	0x8c0	4	Auto-extracted signal retr_limit_reached from protocol_control.vhd
can_bus.protocol_control_form_err_i	0x8c4	4	Auto-extracted signal form_err_i from protocol_control.vhd
can_bus.protocol_control_ack_err_i	0x8c8	4	Auto-extracted signal ack_err_i from protocol_control.vhd
can_bus.protocol_control_crc_check	0x8cc	4	Auto-extracted signal crc_check from protocol_control.vhd
can_bus.protocol_control_bit_err_arb	0x8d0	4	Auto-extracted signal bit_err_arb from protocol_control.vhd
can_bus.protocol_control_crc_match	0x8d4	4	Auto-extracted signal crc_match from protocol_control.vhd
can_bus.protocol_control_crc_err_i	0x8d8	4	Auto-extracted signal crc_err_i from protocol_control.vhd
can_bus.protocol_control_crc_clear_match_flag	0x8dc	4	Auto-extracted signal crc_clear_match_flag from protocol_control.vhd
can_bus.protocol_control_crc_src	0x8e0	4	Auto-extracted signal crc_src from protocol_control.vhd
can_bus.protocol_control_err_pos	0x8e4	4	Auto-extracted signal err_pos from protocol_control.vhd
can_bus.protocol_control_is_arbitration_i	0x8e8	4	Auto-extracted signal is_arbitration_i from protocol_control.vhd
can_bus.protocol_control_bit_err_enable	0x8ec	4	Auto-extracted signal bit_err_enable from protocol_control.vhd
can_bus.protocol_control_tx_data_nbs_i	0x8f0	4	Auto-extracted signal tx_data_nbs_i from protocol_control.vhd
can_bus.protocol_control_rx_crc	0x8f4	4	Auto-extracted signal rx_crc from protocol_control.vhd
can_bus.protocol_control_rx_stuff_count	0x8f8	4	Auto-extracted signal rx_stuff_count from protocol_control.vhd

Name	Offset	Length	Description
can_bus.protocol_control_fixed_stuff_i	0x8fc	4	Auto-extracted signal fixed_stuff_i from protocol_control.vhd
can_bus.protocol_control_arbitration_lost_i	0x900	4	Auto-extracted signal arbitration_lost_i from protocol_control.vhd
can_bus.protocol_control_alc_id_field	0x904	4	Auto-extracted signal alc_id_field from protocol_control.vhd
can_bus.protocol_control_drv_rom_ena	0x908	4	Auto-extracted signal drv_rom_ena from protocol_control.vhd
can_bus.protocol_control_fsm_state_reg_ce	0x90c	4	Auto-extracted signal state_reg_ce from protocol_control_fsm.vhd
can_bus.protocol_control_fsm_no_data_transmitter	0x910	4	Auto-extracted signal no_data_transmitter from protocol_control_fsm.vhd
can_bus.protocol_control_fsm_no_data_receiver	0x914	4	Auto-extracted signal no_data_receiver from protocol_control_fsm.vhd
can_bus.protocol_control_fsm_no_data_field	0x918	4	Auto-extracted signal no_data_field from protocol_control_fsm.vhd
can_bus.protocol_control_fsm_ctrl_ctr_pload_i	0x91c	4	Auto-extracted signal ctrl_ctr_pload_i from protocol_control_fsm.vhd
can_bus.protocol_control_fsm_ctrl_ctr_pload_unaliged	0x920	4	Auto-extracted signal ctrl_ctr_pload_unaliged from protocol_control_fsm.vhd
can_bus.protocol_control_fsm_crc_use_21	0x924	4	Auto-extracted signal crc_use_21 from protocol_control_fsm.vhd
can_bus.protocol_control_fsm_crc_use_17	0x928	4	Auto-extracted signal crc_use_17 from protocol_control_fsm.vhd
can_bus.protocol_control_fsm_crc_src_i	0x92c	4	Auto-extracted signal crc_src_i from protocol_control_fsm.vhd
can_bus.protocol_control_fsm_crc_length_i	0x930	4	Auto-extracted signal crc_length_i from protocol_control_fsm.vhd
can_bus.protocol_control_fsm_tran_data_length	0x934	4	Auto-extracted signal tran_data_length from protocol_control_fsm.vhd
can_bus.protocol_control_fsm_rec_data_length	0x938	4	Auto-extracted signal rec_data_length from protocol_control_fsm.vhd

Name	Offset	Length	Description
can_bus.protocol_control_fsm_rec_data_length_c	0x93c	4	Auto-extracted signal rec_data_length_c from protocol_control_fsm.vhd
can_bus.protocol_control_fsm_data_length_c	0x940	4	Auto-extracted signal data_length_c from protocol_control_fsm.vhd
can_bus.protocol_control_fsm_data_length_shifted_c	0x944	4	Auto-extracted signal data_length_shifted_c from protocol_control_fsm.vhd
can_bus.protocol_control_fsm_data_length_bits_c	0x948	4	Auto-extracted signal data_length_bits_c from protocol_control_fsm.vhd
can_bus.protocol_control_fsm_is_fd_frame	0x94c	4	Auto-extracted signal is_fd_frame from protocol_control_fsm.vhd
can_bus.protocol_control_fsm_frame_start	0x950	4	Auto-extracted signal frame_start from protocol_control_fsm.vhd
can_bus.protocol_control_fsm_tx_frame_ready	0x954	4	Auto-extracted signal tx_frame_ready from protocol_control_fsm.vhd
can_bus.protocol_control_fsm_ide_is_arbitration	0x958	4	Auto-extracted signal ide_is_arbitration from protocol_control_fsm.vhd
can_bus.protocol_control_fsm_arbitration_lost_condition	0x95c	4	Auto-extracted signal arbitration_lost_condition from protocol_control_fsm.vhd
can_bus.protocol_control_fsm_arbitration_lost_i	0x960	4	Auto-extracted signal arbitration_lost_i from protocol_control_fsm.vhd
can_bus.protocol_control_fsm_tx_failed	0x964	4	Auto-extracted signal tx_failed from protocol_control_fsm.vhd
can_bus.protocol_control_fsm_store_metadata_d	0x968	4	Auto-extracted signal store_metadata_d from protocol_control_fsm.vhd
can_bus.protocol_control_fsm_store_data_d	0x96c	4	Auto-extracted signal store_data_d from protocol_control_fsm.vhd
can_bus.protocol_control_fsm_rec_valid_d	0x970	4	Auto-extracted signal rec_valid_d from protocol_control_fsm.vhd
can_bus.protocol_control_fsm_rec_abort_d	0x974	4	Auto-extracted signal rec_abort_d from protocol_control_fsm.vhd
can_bus.protocol_control_fsm_go_to_suspend	0x978	4	Auto-extracted signal go_to_suspend from protocol_control_fsm.vhd

Name	Offset	Length	Description
can_bus.protocol_control_fsm_go_to_stuff_count_i	0x97c	4	Auto-extracted signal go_to_stuff_count from protocol_control_fsm.vhd
can_bus.protocol_control_fsm_rx_store_base_id_i	0x980	4	Auto-extracted signal rx_store_base_id_i from protocol_control_fsm.vhd
can_bus.protocol_control_fsm_rx_store_ext_id_i	0x984	4	Auto-extracted signal rx_store_ext_id_i from protocol_control_fsm.vhd
can_bus.protocol_control_fsm_rx_store_ide_i	0x988	4	Auto-extracted signal rx_store_ide_i from protocol_control_fsm.vhd
can_bus.protocol_control_fsm_rx_store_rtr_i	0x98c	4	Auto-extracted signal rx_store_rtr_i from protocol_control_fsm.vhd
can_bus.protocol_control_fsm_rx_store_edl_i	0x990	4	Auto-extracted signal rx_store_edl_i from protocol_control_fsm.vhd
can_bus.protocol_control_fsm_rx_store_dlc_i	0x994	4	Auto-extracted signal rx_store_dlc_i from protocol_control_fsm.vhd
can_bus.protocol_control_fsm_rx_store_esi_i	0x998	4	Auto-extracted signal rx_store_esi_i from protocol_control_fsm.vhd
can_bus.protocol_control_fsm_rx_store_brs_i	0x99c	4	Auto-extracted signal rx_store_brs_i from protocol_control_fsm.vhd
can_bus.protocol_control_fsm_rx_store_stuff_count_i	0x9a0	4	Auto-extracted signal rx_store_stuff_count_i from protocol_control_fsm.vhd
can_bus.protocol_control_fsm_rx_clear_i	0x9a4	4	Auto-extracted signal rx_clear_i from protocol_control_fsm.vhd
can_bus.protocol_control_fsm_tx_load_base_id_i	0x9a8	4	Auto-extracted signal tx_load_base_id_i from protocol_control_fsm.vhd
can_bus.protocol_control_fsm_tx_load_ext_id_i	0x9ac	4	Auto-extracted signal tx_load_ext_id_i from protocol_control_fsm.vhd
can_bus.protocol_control_fsm_tx_load_dlc_i	0x9b0	4	Auto-extracted signal tx_load_dlc_i from protocol_control_fsm.vhd
can_bus.protocol_control_fsm_tx_load_data_word_i	0x9b4	4	Auto-extracted signal tx_load_data_word_i from protocol_control_fsm.vhd

Name	Offset	Length	Description
can_bus.protocol_control_fsm_tx_load_stuff_count_i	0x9b8	4	Auto-extracted signal tx_load_stuff_count_i from protocol_control_fsm.vhd
can_bus.protocol_control_fsm_tx_load_crc_i	0x9bc	4	Auto-extracted signal tx_load_crc_i from protocol_control_fsm.vhd
can_bus.protocol_control_fsm_tx_shift_ena_i	0x9c0	4	Auto-extracted signal tx_shift_ena_i from protocol_control_fsm.vhd
can_bus.protocol_control_fsm_form_err_i	0x9c4	4	Auto-extracted signal form_err_i from protocol_control_fsm.vhd
can_bus.protocol_control_fsm_ack_err_i	0x9c8	4	Auto-extracted signal ack_err_i from protocol_control_fsm.vhd
can_bus.protocol_control_fsm_ack_err_flag	0x9cc	4	Auto-extracted signal ack_err_flag from protocol_control_fsm.vhd
can_bus.protocol_control_fsm_ack_err_flag_clr	0x9d0	4	Auto-extracted signal ack_err_flag_clr from protocol_control_fsm.vhd
can_bus.protocol_control_fsm_crc_err_i	0x9d4	4	Auto-extracted signal crc_err_i from protocol_control_fsm.vhd
can_bus.protocol_control_fsm_bit_err_arb_i	0x9d8	4	Auto-extracted signal bit_err_arb_i from protocol_control_fsm.vhd
can_bus.protocol_control_fsm_sp_control_switch_data	0x9dc	4	Auto-extracted signal sp_control_switch_data from protocol_control_fsm.vhd
can_bus.protocol_control_fsm_sp_control_switch_nominal	0x9e0	4	Auto-extracted signal sp_control_switch_nominal from protocol_control_fsm.vhd
can_bus.protocol_control_fsm_switch_to_ssp	0x9e4	4	Auto-extracted signal switch_to_ssp from protocol_control_fsm.vhd
can_bus.protocol_control_fsm_sp_control_ce	0x9e8	4	Auto-extracted signal sp_control_ce from protocol_control_fsm.vhd
can_bus.protocol_control_fsm_sp_control_d	0x9ec	4	Auto-extracted signal sp_control_d from protocol_control_fsm.vhd
can_bus.protocol_control_fsm_sp_control_q_i	0x9f0	4	Auto-extracted signal sp_control_q_i from protocol_control_fsm.vhd
can_bus.protocol_control_fsm_ssp_reset_i	0x9f4	4	Auto-extracted signal ssp_reset_i from protocol_control_fsm.vhd

Name	Offset	Length	Description
can_bus.protocol_control_fsm_sync_control_d	0x9f8	4	Auto-extracted signal sync_control_d from protocol_control_fsm.vhd
can_bus.protocol_control_fsm_sync_control_q	0x9fc	4	Auto-extracted signal sync_control_q from protocol_control_fsm.vhd
can_bus.protocol_control_fsm_perform_hsync	0xa00	4	Auto-extracted signal perform_hsync from protocol_control_fsm.vhd
can_bus.protocol_control_fsm_primary_err_i	0xa04	4	Auto-extracted signal primary_err_i from protocol_control_fsm.vhd
can_bus.protocol_control_fsm_err_delim_late_i	0xa08	4	Auto-extracted signal err_delim_late_i from protocol_control_fsm.vhd
can_bus.protocol_control_fsm_set_err_active_i	0xa0c	4	Auto-extracted signal set_err_active_i from protocol_control_fsm.vhd
can_bus.protocol_control_fsm_set_transmitter_i	0xa10	4	Auto-extracted signal set_transmitter_i from protocol_control_fsm.vhd
can_bus.protocol_control_fsm_set_receiver_i	0xa14	4	Auto-extracted signal set_receiver_i from protocol_control_fsm.vhd
can_bus.protocol_control_fsm_set_idle_i	0xa18	4	Auto-extracted signal set_idle_i from protocol_control_fsm.vhd
can_bus.protocol_control_fsm_first_err_delim_d	0xa1c	4	Auto-extracted signal first_err_delim_d from protocol_control_fsm.vhd
can_bus.protocol_control_fsm_first_err_delim_q	0xa20	4	Auto-extracted signal first_err_delim_q from protocol_control_fsm.vhd
can_bus.protocol_control_fsm_stuff_enable_set	0xa24	4	Auto-extracted signal stuff_enable_set from protocol_control_fsm.vhd
can_bus.protocol_control_fsm_stuff_enable_clear	0xa28	4	Auto-extracted signal stuff_enable_clear from protocol_control_fsm.vhd
can_bus.protocol_control_fsm_destuff_enable_set	0xa2c	4	Auto-extracted signal destuff_enable_set from protocol_control_fsm.vhd
can_bus.protocol_control_fsm_destuff_enable_clear	0xa30	4	Auto-extracted signal destuff_enable_clear from protocol_control_fsm.vhd

Name	Offset	Length	Description
can_bus.protocol_control_fsm_bit_err_disable	0xa34	4	Auto-extracted signal bit_err_disable from protocol_control_fsm.vhd
can_bus.protocol_control_fsm_bit_err_disable_receiver	0xa38	4	Auto-extracted signal bit_err_disable_receiver from protocol_control_fsm.vhd
can_bus.protocol_control_fsm_sof_pulse_i	0xa3c	4	Auto-extracted signal sof_pulse_i from protocol_control_fsm.vhd
can_bus.protocol_control_fsm_compl_ctr_ena_i	0xa40	4	Auto-extracted signal compl_ctr_ena_i from protocol_control_fsm.vhd
can_bus.protocol_control_fsm_tick_state_reg	0xa44	4	Auto-extracted signal tick_state_reg from protocol_control_fsm.vhd
can_bus.protocol_control_fsm_br_shifted_i	0xa48	4	Auto-extracted signal br_shifted_i from protocol_control_fsm.vhd
can_bus.protocol_control_fsm_is_arbitration_i	0xa4c	4	Auto-extracted signal is_arbitration_i from protocol_control_fsm.vhd
can_bus.protocol_control_fsm_crc_spec_enable_i	0xa50	4	Auto-extracted signal crc_spec_enable_i from protocol_control_fsm.vhd
can_bus.protocol_control_fsm_load_init_vect_i	0xa54	4	Auto-extracted signal load_init_vect_i from protocol_control_fsm.vhd
can_bus.protocol_control_fsm_drv_bus_off_reset_q	0xa58	4	Auto-extracted signal drv_bus_off_reset_q from protocol_control_fsm.vhd
can_bus.protocol_control_fsm_retr_ctr_clear_i	0xa5c	4	Auto-extracted signal retr_ctr_clear_i from protocol_control_fsm.vhd
can_bus.protocol_control_fsm_retr_ctr_add_i	0xa60	4	Auto-extracted signal retr_ctr_add_i from protocol_control_fsm.vhd
can_bus.protocol_control_fsm_decrement_rec_i	0xa64	4	Auto-extracted signal decrement_rec_i from protocol_control_fsm.vhd
can_bus.protocol_control_fsm_retr_ctr_add_block	0xa68	4	Auto-extracted signal retr_ctr_add_block from protocol_control_fsm.vhd
can_bus.protocol_control_fsm_retr_ctr_add_block_clr	0xa6c	4	Auto-extracted signal retr_ctr_add_block_clr from protocol_control_fsm.vhd

Name	Offset	Length	Description
can_bus.protocol_control_fsm_block_txtb_unlock	0xa70	4	Auto-extracted signal block_txtb_unlock from protocol_control_fsm.vhd
can_bus.protocol_control_fsm_tx_frame_no_sof_d	0xa74	4	Auto-extracted signal tx_frame_no_sof_d from protocol_control_fsm.vhd
can_bus.protocol_control_fsm_tx_frame_no_sof_q	0xa78	4	Auto-extracted signal tx_frame_no_sof_q from protocol_control_fsm.vhd
can_bus.protocol_control_fsm_ctrl_signal_upd	0xa7c	4	Auto-extracted signal ctrl_signal_upd from protocol_control_fsm.vhd
can_bus.protocol_control_fsm_clr_bus_off_rst_flg	0xa80	4	Auto-extracted signal clr_bus_off_rst_flg from protocol_control_fsm.vhd
can_bus.protocol_control_fsm_pex_on_fdf_enable	0xa84	4	Auto-extracted signal pex_on_fdf_enable from protocol_control_fsm.vhd
can_bus.protocol_control_fsm_pex_on_res_enable	0xa88	4	Auto-extracted signal pex_on_res_enable from protocol_control_fsm.vhd
can_bus.protocol_control_fsm_rx_data_nbs_prev	0xa8c	4	Auto-extracted signal rx_data_nbs_prev from protocol_control_fsm.vhd
can_bus.protocol_control_fsm_pexs_set	0xa90	4	Auto-extracted signal pexs_set from protocol_control_fsm.vhd
can_bus.protocol_control_fsm_tran_frame_type_i	0xa94	4	Auto-extracted signal tran_frame_type_i from protocol_control_fsm.vhd
can_bus.protocol_control_fsm_txtb_clk_en_d	0xa98	4	Auto-extracted signal txtb_clk_en_d from protocol_control_fsm.vhd
can_bus.protocol_control_fsm_txtb_clk_en_q	0xa9c	4	Auto-extracted signal txtb_clk_en_q from protocol_control_fsm.vhd
can_bus.reintegration_counter_reinteg_ctr_ce	0xaa0	4	Auto-extracted signal reinteg_ctr_ce from reintegration_counter.vhd
can_bus.retransmitt_counter_retr_ctr_ce	0xaa4	4	Auto-extracted signal retr_ctr_ce from retransmitt_counter.vhd
can_bus.rst_sync_rff	0xaa8	4	Auto-extracted signal rff from rst_sync.vhd
can_bus.rx_buffer_drv_erase_rx	0xaac	4	Auto-extracted signal drv_erase_rx from rx_buffer.vhd

Name	Offset	Length	Description
can_bus.rx_buffer_drv_read_start	0xab0	4	Auto-extracted signal drv_read_start from rx_buffer.vhd
can_bus.rx_buffer_drv_clr_ovr	0xab4	4	Auto-extracted signal drv_clr_ovr from rx_buffer.vhd
can_bus.rx_buffer_drv_rtsopt	0xab8	4	Auto-extracted signal drv_rtsopt from rx_buffer.vhd
can_bus.rx_buffer_read_pointer	0xabc	4	Auto-extracted signal read_pointer from rx_buffer.vhd
can_bus.rx_buffer_read_pointer_inc_1	0xac0	4	Auto-extracted signal read_pointer_inc_1 from rx_buffer.vhd
can_bus.rx_buffer_write_pointer	0xac4	4	Auto-extracted signal write_pointer from rx_buffer.vhd
can_bus.rx_buffer_write_pointer_raw	0xac8	4	Auto-extracted signal write_pointer_raw from rx_buffer.vhd
can_bus.rx_buffer_write_pointer_ts	0xacc	4	Auto-extracted signal write_pointer_ts from rx_buffer.vhd
can_bus.rx_buffer_rx_mem_free_i	0xad0	4	Auto-extracted signal rx_mem_free_i from rx_buffer.vhd
can_bus.rx_buffer_memory_write_data	0xad4	4	Auto-extracted signal memory_write_data from rx_buffer.vhd
can_bus.rx_buffer_data_overrun_flg	0xad8	4	Auto-extracted signal data_overrun_flg from rx_buffer.vhd
can_bus.rx_buffer_data_overrun_i	0xadc	4	Auto-extracted signal data_overrun_i from rx_buffer.vhd
can_bus.rx_buffer_overrun_condition	0xae0	4	Auto-extracted signal overrun_condition from rx_buffer.vhd
can_bus.rx_buffer_rx_empty_i	0xae4	4	Auto-extracted signal rx_empty_i from rx_buffer.vhd
can_bus.rx_buffer_is_free_word	0xae8	4	Auto-extracted signal is_free_word from rx_buffer.vhd
can_bus.rx_buffer_commit_rx_frame	0xaec	4	Auto-extracted signal commit_rx_frame from rx_buffer.vhd
can_bus.rx_buffer_commit_overrun_abort	0xaf0	4	Auto-extracted signal commit_overrun_abort from rx_buffer.vhd

Name	Offset	Length	Description
can_bus.rx_buffer_read_increment	0xaf4	4	Auto-extracted signal read_increment from rx_buffer.vhd
can_bus.rx_buffer_write_raw_OK	0xaf8	4	Auto-extracted signal write_raw_OK from rx_buffer.vhd
can_bus.rx_buffer_write_raw_intent	0xafc	4	Auto-extracted signal write_raw_intent from rx_buffer.vhd
can_bus.rx_buffer_write_ts	0xb00	4	Auto-extracted signal write_ts from rx_buffer.vhd
can_bus.rx_buffer_stored_ts	0xb04	4	Auto-extracted signal stored_ts from rx_buffer.vhd
can_bus.rx_buffer_data_selector	0xb08	4	Auto-extracted signal data_selector from rx_buffer.vhd
can_bus.rx_buffer_store_ts_wr_ptr	0xb0c	4	Auto-extracted signal store_ts_wr_ptr from rx_buffer.vhd
can_bus.rx_buffer_inc_ts_wr_ptr	0xb10	4	Auto-extracted signal inc_ts_wr_ptr from rx_buffer.vhd
can_bus.rx_buffer_reset_overrun_flag	0xb14	4	Auto-extracted signal reset_overrun_flag from rx_buffer.vhd
can_bus.rx_buffer_frame_form_w	0xb18	4	Auto-extracted signal frame_form_w from rx_buffer.vhd
can_bus.rx_buffer_timestamp_capture	0xb1c	4	Auto-extracted signal timestamp_capture from rx_buffer.vhd
can_bus.rx_buffer_timestamp_capture_ce	0xb20	4	Auto-extracted signal timestamp_capture_ce from rx_buffer.vhd
can_bus.rx_buffer_RAM_write	0xb24	4	Auto-extracted signal RAM_write from rx_buffer.vhd
can_bus.rx_buffer_RAM_data_out	0xb28	4	Auto-extracted signal RAM_data_out from rx_buffer.vhd
can_bus.rx_buffer_RAM_write_address	0xb2c	4	Auto-extracted signal RAM_write_address from rx_buffer.vhd
can_bus.rx_buffer_RAM_read_address	0xb30	4	Auto-extracted signal RAM_read_address from rx_buffer.vhd

Name	Offset	Length	Description
can_bus.rx_buffer_rx_buf_res_n_d	0xb34	4	Auto-extracted signal rx_buf_res_n_d from rx_buffer.vhd
can_bus.rx_buffer_rx_buf_res_n_q	0xb38	4	Auto-extracted signal rx_buf_res_n_q from rx_buffer.vhd
can_bus.rx_buffer_rx_buf_res_n_q_scan	0xb3c	4	Auto-extracted signal rx_buf_res_n_q_scan from rx_buffer.vhd
can_bus.rx_buffer_rx_buf_ram_clk_en	0xb40	4	Auto-extracted signal rx_buf_ram_clk_en from rx_buffer.vhd
can_bus.rx_buffer_clk_ram	0xb44	4	Auto-extracted signal clk_ram from rx_buffer.vhd
can_bus.rx_buffer_fsm_rx_fsm_ce	0xb48	4	Auto-extracted signal rx_fsm_ce from rx_buffer_fsm.vhd
can_bus.rx_buffer_fsm_cmd_join	0xb4c	4	Auto-extracted signal cmd_join from rx_buffer_fsm.vhd
can_bus.rx_buffer_pointers_write_pointer_raw_ce	0xb50	4	Auto-extracted signal write_pointer_raw_ce from rx_buffer_pointers.vhd
can_bus.rx_buffer_pointers_write_pointer_ts_ce	0xb54	4	Auto-extracted signal write_pointer_ts_ce from rx_buffer_pointers.vhd
can_bus.rx_buffer_ram_port_a_address_i	0xb58	4	Auto-extracted signal port_a_address_i from rx_buffer_ram.vhd
can_bus.rx_buffer_ram_port_a_write_i	0xb5c	4	Auto-extracted signal port_a_write_i from rx_buffer_ram.vhd
can_bus.rx_buffer_ram_port_a_data_in_i	0xb60	4	Auto-extracted signal port_a_data_in_i from rx_buffer_ram.vhd
can_bus.rx_buffer_ram_port_b_address_i	0xb64	4	Auto-extracted signal port_b_address_i from rx_buffer_ram.vhd
can_bus.rx_buffer_ram_port_b_data_out_i	0xb68	4	Auto-extracted signal port_b_data_out_i from rx_buffer_ram.vhd
can_bus.rx_buffer_ram_tst_ena	0xb6c	4	Auto-extracted signal tst_ena from rx_buffer_ram.vhd
can_bus.rx_buffer_ram_tst_addr	0xb70	4	Auto-extracted signal tst_addr from rx_buffer_ram.vhd
can_bus.rx_shift_reg_res_n_i_d	0xb74	4	Auto-extracted signal res_n_i_d from rx_shift_reg.vhd

Name	Offset	Length	Description
can_bus.rx_shift_reg_res_n_i_q	0xb78	4	Auto-extracted signal res_n_i_q from rx_shift_reg.vhd
can_bus.rx_shift_reg_res_n_i_q_scan	0xb7c	4	Auto-extracted signal res_n_i_q_scan from rx_shift_reg.vhd
can_bus.rx_shift_reg_rx_shift_reg_q	0xb80	4	Auto-extracted signal rx_shift_reg_q from rx_shift_reg.vhd
can_bus.rx_shift_reg_rx_shift_cmd	0xb84	4	Auto-extracted signal rx_shift_cmd from rx_shift_reg.vhd
can_bus.rx_shift_reg_rx_shift_in_sel_demuxed	0xb88	4	Auto-extracted signal rx_shift_in_sel_demuxed from rx_shift_reg.vhd
can_bus.rx_shift_reg_rec_is_rtr_i	0xb8c	4	Auto-extracted signal rec_is_rtr_i from rx_shift_reg.vhd
can_bus.rx_shift_reg_rec_frame_type_i	0xb90	4	Auto-extracted signal rec_frame_type_i from rx_shift_reg.vhd
can_bus.sample_mux_sample	0xb94	4	Auto-extracted signal sample from sample_mux.vhd
can_bus.sample_mux_prev_sample_d	0xb98	4	Auto-extracted signal prev_sample_d from sample_mux.vhd
can_bus.sample_mux_prev_sample_q	0xb9c	4	Auto-extracted signal prev_sample_q from sample_mux.vhd
can_bus.segment_end_detector_req_input	0xba0	4	Auto-extracted signal req_input from segment_end_detector.vhd
can_bus.segment_end_detector_segm_end_req_capt_d	0xba4	4	Auto-extracted signal segm_end_req_capt_d from segment_end_detector.vhd
can_bus.segment_end_detector_segm_end_req_capt_q	0xba8	4	Auto-extracted signal segm_end_req_capt_q from segment_end_detector.vhd
can_bus.segment_end_detector_segm_end_req_capt_ce	0xbac	4	Auto-extracted signal segm_end_req_capt_ce from segment_end_detector.vhd
can_bus.segment_end_detector_segm_end_req_capt_clr	0xbb0	4	Auto-extracted signal segm_end_req_capt_clr from segment_end_detector.vhd
can_bus.segment_end_detector_segm_end_req_capt_dq	0xbb4	4	Auto-extracted signal segm_end_req_capt_dq from segment_end_detector.vhd

Name	Offset	Length	Description
can_bus.segment_end_detector_segm_end_nbt_valid	0xbb8	4	Auto-extracted signal segm_end_nbt_valid from segment_end_detector.vhd
can_bus.segment_end_detector_segm_end_dbt_valid	0xbbc	4	Auto-extracted signal segm_end_dbt_valid from segment_end_detector.vhd
can_bus.segment_end_detector_segm_end_nbt_dbt_valid	0xbc0	4	Auto-extracted signal segm_end_nbt_dbt_valid from segment_end_detector.vhd
can_bus.segment_end_detector_tseg1_end_req_valid	0xbc4	4	Auto-extracted signal tseg1_end_req_valid from segment_end_detector.vhd
can_bus.segment_end_detector_tseg2_end_req_valid	0xbc8	4	Auto-extracted signal tseg2_end_req_valid from segment_end_detector.vhd
can_bus.segment_end_detector_h_sync_valid_i	0xbcc	4	Auto-extracted signal h_sync_valid_i from segment_end_detector.vhd
can_bus.segment_end_detector_segment_end_i	0xbd0	4	Auto-extracted signal segment_end_i from segment_end_detector.vhd
can_bus.segment_end_detector_nbt_tq_active	0xbd4	4	Auto-extracted signal nbt_tq_active from segment_end_detector.vhd
can_bus.segment_end_detector_dbt_tq_active	0xbd8	4	Auto-extracted signal dbt_tq_active from segment_end_detector.vhd
can_bus.segment_end_detector_bt_ctr_clear_i	0xbdc	4	Auto-extracted signal bt_ctr_clear_i from segment_end_detector.vhd
can_bus.shift_reg_shift_regs	0xbe0	4	Auto-extracted signal shift_regs from shift_reg.vhd
can_bus.shift_reg_next_shift_reg_val	0xbe4	4	Auto-extracted signal next_shift_reg_val from shift_reg.vhd
can_bus.shift_reg_byte_shift_reg_in	0xbe8	4	Auto-extracted signal shift_reg_in from shift_reg_byte.vhd
can_bus.shift_reg_preload_shift_regs	0xbec	4	Auto-extracted signal shift_regs from shift_reg_preload.vhd
can_bus.shift_reg_preload_next_shift_reg_val	0xbf0	4	Auto-extracted signal next_shift_reg_val from shift_reg_preload.vhd
can_bus.sig_sync_rff	0xbf4	4	Auto-extracted signal rff from sig_sync.vhd

Name	Offset	Length	Description
can_bus.ssp_generator_btmc_d	0xbf8	4	Auto-extracted signal btmc_d from ssp_generator.vhd
can_bus.ssp_generator_btmc_q	0xbfc	4	Auto-extracted signal btmc_q from ssp_generator.vhd
can_bus.ssp_generator_btmc_add	0xc00	4	Auto-extracted signal btmc_add from ssp_generator.vhd
can_bus.ssp_generator_btmc_ce	0xc04	4	Auto-extracted signal btmc_ce from ssp_generator.vhd
can_bus.ssp_generator_btmc_meas_running_d	0xc08	4	Auto-extracted signal btmc_meas_running_d from ssp_generator.vhd
can_bus.ssp_generator_btmc_meas_running_q	0xc0c	4	Auto-extracted signal btmc_meas_running_q from ssp_generator.vhd
can_bus.ssp_generator_sspc_d	0xc10	4	Auto-extracted signal sspc_d from ssp_generator.vhd
can_bus.ssp_generator_sspc_q	0xc14	4	Auto-extracted signal sspc_q from ssp_generator.vhd
can_bus.ssp_generator_sspc_ce	0xc18	4	Auto-extracted signal sspc_ce from ssp_generator.vhd
can_bus.ssp_generator_sspc_expired	0xc1c	4	Auto-extracted signal sspc_expired from ssp_generator.vhd
can_bus.ssp_generator_sspc_threshold	0xc20	4	Auto-extracted signal sspc_threshold from ssp_generator.vhd
can_bus.ssp_generator_sspc_add	0xc24	4	Auto-extracted signal sspc_add from ssp_generator.vhd
can_bus.ssp_generator_first_ssp_d	0xc28	4	Auto-extracted signal first_ssp_d from ssp_generator.vhd
can_bus.ssp_generator_first_ssp_q	0xc2c	4	Auto-extracted signal first_ssp_q from ssp_generator.vhd
can_bus.ssp_generator_sspc_ena_d	0xc30	4	Auto-extracted signal sspc_ena_d from ssp_generator.vhd
can_bus.ssp_generator_sspc_ena_q	0xc34	4	Auto-extracted signal sspc_ena_q from ssp_generator.vhd
can_bus.ssp_generator_ssp_delay_padded	0xc38	4	Auto-extracted signal ssp_delay_padded from ssp_generator.vhd
can_bus.synchronisation_checker_resync_edge	0xc3c	4	Auto-extracted signal resync_edge from synchronisation_checker.vhd

Name	Offset	Length	Description
can_bus.synchronisation_checker_h_sync_edge	0xc40	4	Auto-extracted signal h_sync_edge from synchronisation_checker.vhd
can_bus.synchronisation_checker_h_or_re_sync_edge	0xc44	4	Auto-extracted signal h_or_re_sync_edge from synchronisation_checker.vhd
can_bus.synchronisation_checker_sync_flag	0xc48	4	Auto-extracted signal sync_flag from synchronisation_checker.vhd
can_bus.synchronisation_checker_sync_flag_ce	0xc4c	4	Auto-extracted signal sync_flag_ce from synchronisation_checker.vhd
can_bus.synchronisation_checker_sync_flag_nxt	0xc50	4	Auto-extracted signal sync_flag_nxt from synchronisation_checker.vhd
can_bus.test_registers_reg_map_reg_sel	0xc54	4	Auto-extracted signal reg_sel from test_registers_reg_map.vhd
can_bus.test_registers_reg_map_read_data_mux_in	0xc58	4	Auto-extracted signal read_data_mux_in from test_registers_reg_map.vhd
can_bus.test_registers_reg_map_read_data_mask_n	0xc5c	4	Auto-extracted signal read_data_mask_n from test_registers_reg_map.vhd
can_bus.test_registers_reg_map_read_mux_ena	0xc60	4	Auto-extracted signal read_mux_ena from test_registers_reg_map.vhd
can_bus.trigger_generator_rx_trig_req_q	0xc64	4	Auto-extracted signal rx_trig_req_q from trigger_generator.vhd
can_bus.trigger_generator_tx_trig_req_flag_d	0xc68	4	Auto-extracted signal tx_trig_req_flag_d from trigger_generator.vhd
can_bus.trigger_generator_tx_trig_req_flag_q	0xc6c	4	Auto-extracted signal tx_trig_req_flag_q from trigger_generator.vhd
can_bus.trigger_generator_tx_trig_req_flag_dq	0xc70	4	Auto-extracted signal tx_trig_req_flag_dq from trigger_generator.vhd
can_bus.trigger_mux_tx_trigger_q	0xc74	4	Auto-extracted signal tx_trigger_q from trigger_mux.vhd
can_bus.trv_delay_meas_trv_meas_progress_d	0xc78	4	Auto-extracted signal trv_meas_progress_d from trv_delay_meas.vhd
can_bus.trv_delay_meas_trv_meas_progress_q	0xc7c	4	Auto-extracted signal trv_meas_progress_q from trv_delay_meas.vhd

Name	Offset	Length	Description
can_bus.trv_delay_meas_trv_meas_progress_del	0xc80	4	Auto-extracted signal trv_meas_progress_del from trv_delay_meas.vhd
can_bus.trv_delay_meas_trv_delay_ctr_q	0xc84	4	Auto-extracted signal trv_delay_ctr_q from trv_delay_meas.vhd
can_bus.trv_delay_meas_trv_delay_ctr_d	0xc88	4	Auto-extracted signal trv_delay_ctr_d from trv_delay_meas.vhd
can_bus.trv_delay_meas_trv_delay_ctr_add	0xc8c	4	Auto-extracted signal trv_delay_ctr_add from trv_delay_meas.vhd
can_bus.trv_delay_meas_trv_delay_ctr_q_padded	0xc90	4	Auto-extracted signal trv_delay_ctr_q_padded from trv_delay_meas.vhd
can_bus.trv_delay_meas_trv_delay_ctr_rst_d	0xc94	4	Auto-extracted signal trv_delay_ctr_rst_d from trv_delay_meas.vhd
can_bus.trv_delay_meas_trv_delay_ctr_rst_q	0xc98	4	Auto-extracted signal trv_delay_ctr_rst_q from trv_delay_meas.vhd
can_bus.trv_delay_meas_trv_delay_ctr_rst_q_scan	0xc9c	4	Auto-extracted signal trv_delay_ctr_rst_q_scan from trv_delay_meas.vhd
can_bus.trv_delay_meas_ssp_shadow_ce	0xca0	4	Auto-extracted signal ssp_shadow_ce from trv_delay_meas.vhd
can_bus.trv_delay_meas_ssp_delay_raw	0xca4	4	Auto-extracted signal ssp_delay_raw from trv_delay_meas.vhd
can_bus.trv_delay_meas_ssp_delay_saturated	0xca8	4	Auto-extracted signal ssp_delay_saturated from trv_delay_meas.vhd
can_bus.trv_delay_meas_trv_delay_sum	0xcac	4	Auto-extracted signal trv_delay_sum from trv_delay_meas.vhd
can_bus.tx_arbitrator_select_buf_avail	0xcb0	4	Auto-extracted signal select_buf_avail from tx_arbitrator.vhd
can_bus.tx_arbitrator_txtb_selected_input	0xcb4	4	Auto-extracted signal txtb_selected_input from tx_arbitrator.vhd
can_bus.tx_arbitrator_txtb_timestamp	0xcb8	4	Auto-extracted signal txtb_timestamp from tx_arbitrator.vhd

Name	Offset	Length	Description
can_bus.tx_arbitrator_timestamp_valid	0xcbc	4	Auto-extracted signal timestamp_valid from tx_arbitrator.vhd
can_bus.tx_arbitrator_select_index_changed	0xcc0	4	Auto-extracted signal select_index_changed from tx_arbitrator.vhd
can_bus.tx_arbitrator_validated_buffer	0xcc4	4	Auto-extracted signal validated_buffer from tx_arbitrator.vhd
can_bus.tx_arbitrator_ts_low_internal	0xcc8	4	Auto-extracted signal ts_low_internal from tx_arbitrator.vhd
can_bus.tx_arbitrator_tran_dlc_dbl_buf	0xccc	4	Auto-extracted signal tran_dlc_dbl_buf from tx_arbitrator.vhd
can_bus.tx_arbitrator_tran_is_rtr_dbl_buf	0xcd0	4	Auto-extracted signal tran_is_rtr_dbl_buf from tx_arbitrator.vhd
can_bus.tx_arbitrator_tran_ident_type_dbl_buf	0xcd4	4	Auto-extracted signal tran_ident_type_dbl_buf from tx_arbitrator.vhd
can_bus.tx_arbitrator_tran_frame_type_dbl_buf	0xcd8	4	Auto-extracted signal tran_frame_type_dbl_buf from tx_arbitrator.vhd
can_bus.tx_arbitrator_tran_brs_dbl_buf	0xcdc	4	Auto-extracted signal tran_brs_dbl_buf from tx_arbitrator.vhd
can_bus.tx_arbitrator_tran_dlc_com	0xce0	4	Auto-extracted signal tran_dlc_com from tx_arbitrator.vhd
can_bus.tx_arbitrator_tran_is_rtr_com	0xce4	4	Auto-extracted signal tran_is_rtr_com from tx_arbitrator.vhd
can_bus.tx_arbitrator_tran_ident_type_com	0xce8	4	Auto-extracted signal tran_ident_type_com from tx_arbitrator.vhd
can_bus.tx_arbitrator_tran_frame_type_com	0xcec	4	Auto-extracted signal tran_frame_type_com from tx_arbitrator.vhd
can_bus.tx_arbitrator_tran_brs_com	0xcf0	4	Auto-extracted signal tran_brs_com from tx_arbitrator.vhd
can_bus.tx_arbitrator_tran_frame_valid_com	0xcf4	4	Auto-extracted signal tran_frame_valid_com from tx_arbitrator.vhd

Name	Offset	Length	Description
can_bus.tx_arbitrator_tran_identifier_com	0xcf8	4	Auto-extracted signal tran_identifier_com from tx_arbitrator.vhd
can_bus.tx_arbitrator_load_ts_lw_addr	0xcfc	4	Auto-extracted signal load_ts_lw_addr from tx_arbitrator.vhd
can_bus.tx_arbitrator_load_ts_uw_addr	0xd00	4	Auto-extracted signal load_ts_uw_addr from tx_arbitrator.vhd
can_bus.tx_arbitrator_load_ffmt_w_addr	0xd04	4	Auto-extracted signal load_ffmt_w_addr from tx_arbitrator.vhd
can_bus.tx_arbitrator_load_ident_w_addr	0xd08	4	Auto-extracted signal load_ident_w_addr from tx_arbitrator.vhd
can_bus.tx_arbitrator_store_ts_l_w	0xd0c	4	Auto-extracted signal store_ts_l_w from tx_arbitrator.vhd
can_bus.tx_arbitrator_store_md_w	0xd10	4	Auto-extracted signal store_md_w from tx_arbitrator.vhd
can_bus.tx_arbitrator_store_ident_w	0xd14	4	Auto-extracted signal store_ident_w from tx_arbitrator.vhd
can_bus.tx_arbitrator_buffer_md_w	0xd18	4	Auto-extracted signal buffer_md_w from tx_arbitrator.vhd
can_bus.tx_arbitrator_store_last_txtb_index	0xd1c	4	Auto-extracted signal store_last_txtb_index from tx_arbitrator.vhd
can_bus.tx_arbitrator_frame_valid_com_set	0xd20	4	Auto-extracted signal frame_valid_com_set from tx_arbitrator.vhd
can_bus.tx_arbitrator_frame_valid_com_clear	0xd24	4	Auto-extracted signal frame_valid_com_clear from tx_arbitrator.vhd
can_bus.tx_arbitrator_tx_arb_locked	0xd28	4	Auto-extracted signal tx_arb_locked from tx_arbitrator.vhd
can_bus.tx_arbitrator_txtb_meta_clk_en	0xd2c	4	Auto-extracted signal txtb_meta_clk_en from tx_arbitrator.vhd
can_bus.tx_arbitrator_drv_tttm_ena	0xd30	4	Auto-extracted signal drv_tttm_ena from tx_arbitrator.vhd

Name	Offset	Length	Description
can_bus.tx_arbitrator_fsm_tx_arb_fsm_ce	0xd34	4	Auto-extracted signal tx_arb_fsm_ce from tx_arbitrator_fsm.vhd
can_bus.tx_arbitrator_fsm_fsm_wait_state_d	0xd38	4	Auto-extracted signal fsm_wait_state_d from tx_arbitrator_fsm.vhd
can_bus.tx_arbitrator_fsm_fsm_wait_state_q	0xd3c	4	Auto-extracted signal fsm_wait_state_q from tx_arbitrator_fsm.vhd
can_bus.tx_data_cache_tx_cache_mem	0xd40	4	Auto-extracted signal tx_cache_mem from tx_data_cache.vhd
can_bus.tx_shift_reg_tx_sr_output	0xd44	4	Auto-extracted signal tx_sr_output from tx_shift_reg.vhd
can_bus.tx_shift_reg_tx_sr_ce	0xd48	4	Auto-extracted signal tx_sr_ce from tx_shift_reg.vhd
can_bus.tx_shift_reg_tx_sr_pload	0xd4c	4	Auto-extracted signal tx_sr_pload from tx_shift_reg.vhd
can_bus.tx_shift_reg_tx_sr_pload_val	0xd50	4	Auto-extracted signal tx_sr_pload_val from tx_shift_reg.vhd
can_bus.tx_shift_reg_tx_base_id	0xd54	4	Auto-extracted signal tx_base_id from tx_shift_reg.vhd
can_bus.tx_shift_reg_tx_ext_id	0xd58	4	Auto-extracted signal tx_ext_id from tx_shift_reg.vhd
can_bus.tx_shift_reg_tx_crc	0xd5c	4	Auto-extracted signal tx_crc from tx_shift_reg.vhd
can_bus.tx_shift_reg_bst_ctr_grey	0xd60	4	Auto-extracted signal bst_ctr_grey from tx_shift_reg.vhd
can_bus.tx_shift_reg_bst_parity	0xd64	4	Auto-extracted signal bst_parity from tx_shift_reg.vhd
can_bus.tx_shift_reg_stuff_count	0xd68	4	Auto-extracted signal stuff_count from tx_shift_reg.vhd
can_bus.txt_buffer_txtb_user_accessible	0xd6c	4	Auto-extracted signal txtb_user_accessible from txt_buffer.vhd
can_bus.txt_buffer_hw_cbs	0xd70	4	Auto-extracted signal hw_cbs from txt_buffer.vhd
can_bus.txt_buffer_sw_cbs	0xd74	4	Auto-extracted signal sw_cbs from txt_buffer.vhd
can_bus.txt_buffer_txtb_unmask_data_ram	0xd78	4	Auto-extracted signal txtb_unmask_data_ram from txt_buffer.vhd

Name	Offset	Length	Description
can_bus.txt_buffer_txtb_port_b_data_i	0xd7c	4	Auto-extracted signal txtb_port_b_data_i from txt_buffer.vhd
can_bus.txt_buffer_ram_write	0xd80	4	Auto-extracted signal ram_write from txt_buffer.vhd
can_bus.txt_buffer_ram_read_address	0xd84	4	Auto-extracted signal ram_read_address from txt_buffer.vhd
can_bus.txt_buffer_txtb_ram_clk_en	0xd88	4	Auto-extracted signal txtb_ram_clk_en from txt_buffer.vhd
can_bus.txt_buffer_clk_ram	0xd8c	4	Auto-extracted signal clk_ram from txt_buffer.vhd
can_bus.txt_buffer_fsm_abort_applied	0xd90	4	Auto-extracted signal abort_applied from txt_buffer_fsm.vhd
can_bus.txt_buffer_fsm_txt_fsm_ce	0xd94	4	Auto-extracted signal txt_fsm_ce from txt_buffer_fsm.vhd
can_bus.txt_buffer_fsm_go_to_failed	0xd98	4	Auto-extracted signal go_to_failed from txt_buffer_fsm.vhd
can_bus.txt_buffer_fsm_transient_state	0xd9c	4	Auto-extracted signal transient_state from txt_buffer_fsm.vhd
can_bus.txt_buffer_ram_port_a_address_i	0xda0	4	Auto-extracted signal port_a_address_i from txt_buffer_ram.vhd
can_bus.txt_buffer_ram_port_a_write_i	0xda4	4	Auto-extracted signal port_a_write_i from txt_buffer_ram.vhd
can_bus.txt_buffer_ram_port_a_data_in_i	0xda8	4	Auto-extracted signal port_a_data_in_i from txt_buffer_ram.vhd
can_bus.txt_buffer_ram_port_b_address_i	0xdac	4	Auto-extracted signal port_b_address_i from txt_buffer_ram.vhd
can_bus.txt_buffer_ram_port_b_data_out_i	0xdb0	4	Auto-extracted signal port_b_data_out_i from txt_buffer_ram.vhd
can_bus.txt_buffer_ram_tst_ena	0xdb4	4	Auto-extracted signal tst_ena from txt_buffer_ram.vhd
can_bus.txt_buffer_ram_tst_addr	0xdb8	4	Auto-extracted signal tst_addr from txt_buffer_ram.vhd
can_bus.access_signaler_be_active	0xdbc	4	Auto-extracted signal be_active from access_signaler.vhd

Name	Offset	Length	Description
can_bus.access_signaler_access_in	0xdc0	4	Auto-extracted signal access_in from access_signaler.vhd
can_bus.access_signaler_access_active	0xdc4	4	Auto-extracted signal access_active from access_signaler.vhd
can_bus.access_signaler_access_active_reg	0xdc8	4	Auto-extracted signal access_active_reg from access_signaler.vhd
can_bus.address_decoder_addr_dec_i	0xdcc	4	Auto-extracted signal addr_dec_i from address_decoder.vhd
can_bus.address_decoder_addr_dec_enabled_i	0xdd0	4	Auto-extracted signal addr_dec_enabled_i from address_decoder.vhd

2.105 ahb_ifc_hsel_valid

Auto-extracted signal hsel_valid from ahb_ifc.vhd - Offset: `0x0` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.105.1 Fields

`{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "`

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.106 ahb_ifc_write_acc_d

Auto-extracted signal write_acc_d from ahb_ifc.vhd - Offset: `0x4` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.106.1 Fields

`{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "`

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.107 ahb_ifc_write_acc_q

Auto-extracted signal write_acc_q from ahb_ifc.vhd - Offset: `0x8` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.107.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.108 ahb_ifc_haddr_q

Auto-extracted signal haddr_q from ahb_ifc.vhd - Offset: `0xc` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.108.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.109 ahb_ifc_h_ready_raw

Auto-extracted signal h_ready_raw from ahb_ifc.vhd - Offset: `0x10` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.109.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.110 ahb_ifc_sbe_d

Auto-extracted signal sbe_d from ahb_ifc.vhd - Offset: `0x14` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.110.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.111 ahb_ifc_sbe_q

Auto-extracted signal sbe_q from ahb_ifc.vhd - Offset: `0x18` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.111.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.112 ahb_ifc_swr_i

Auto-extracted signal swr_i from ahb_ifc.vhd - Offset: `0x1c` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.112.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.113 ahb_ifc_srd_i

Auto-extracted signal srd_i from ahb_ifc.vhd - Offset: `0x20` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.113.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.114 bit_destuffing_discard_stuff_bit

Auto-extracted signal discard_stuff_bit from bit_destuffing.vhd - Offset: `0x24` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.114.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.115 bit_destuffing_non_fix_to_fix_chng

Auto-extracted signal non_fix_to_fix_chng from bit_destuffing.vhd - Offset: `0x28` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.115.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.116 bit_destuffing_stuff_lvl_reached

Auto-extracted signal stuff_lvl_reached from bit_destuffing.vhd - Offset: `0x2c` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.116.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.117 bit_destuffing_stuff_rule_violate

Auto-extracted signal stuff_rule_violate from bit_destuffing.vhd - Offset: `0x30` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.117.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.118 bit_destuffing_enable_prev

Auto-extracted signal enable_prev from bit_destuffing.vhd - Offset: `0x34` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.118.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.119 bit_destuffing_fixed_prev_q

Auto-extracted signal fixed_prev_q from bit_destuffing.vhd - Offset: `0x38` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.119.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.120 bit_destuffing_fixed_prev_d

Auto-extracted signal fixed_prev_d from bit_destuffing.vhd - Offset: `0x3c` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.120.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.121 bit_destuffing_same_bits_erase

Auto-extracted signal same_bits_erase from bit_destuffing.vhd - Offset: `0x40` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.121.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.122 bit_destuffing_destuffed_q

Auto-extracted signal destuffed_q from bit_destuffing.vhd - Offset: `0x44` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.122.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.123 bit_destuffing_destuffed_d

Auto-extracted signal destuffed_d from bit_destuffing.vhd - Offset: `0x48` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.123.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.124 bit_destuffing_stuff_err_q

Auto-extracted signal stuff_err_q from bit_destuffing.vhd - Offset: `0x4c` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.124.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.125 bit_destuffing_stuff_err_d

Auto-extracted signal stuff_err_d from bit_destuffing.vhd - Offset: `0x50` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.125.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.126 bit_destuffing_prev_val_q

Auto-extracted signal prev_val_q from bit_destuffing.vhd - Offset: `0x54` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.126.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.127 bit_destuffing_prev_val_d

Auto-extracted signal prev_val_d from bit_destuffing.vhd - Offset: `0x58` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.127.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.128 bit_err_detector_bit_err_d

Auto-extracted signal bit_err_d from bit_err_detector.vhd - Offset: `0x5c` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.128.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.129 bit_err_detector_bit_err_q

Auto-extracted signal bit_err_q from bit_err_detector.vhd - Offset: `0x60` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.129.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.130 bit_err_detector_bit_err_ssp_capt_d

Auto-extracted signal bit_err_ssp_capt_d from bit_err_detector.vhd - Offset: `0x64` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.130.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.131 bit_err_detector_bit_err_ssp_capt_q

Auto-extracted signal bit_err_ssp_capt_q from bit_err_detector.vhd - Offset: `0x68` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.131.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.132 bit_err_detector_bit_err_ssp_valid

Auto-extracted signal bit_err_ssp_valid from bit_err_detector.vhd - Offset: `0x6c` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.132.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.133 bit_err_detector_bit_err_ssp_condition

Auto-extracted signal bit_err_ssp_condition from bit_err_detector.vhd - Offset: `0x70` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.133.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.134 bit_err_detector_bit_err_norm_valid

Auto-extracted signal bit_err_norm_valid from bit_err_detector.vhd - Offset: `0x74` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.134.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.135 bit_filter_masked_input

Auto-extracted signal masked_input from bit_filter.vhd - Offset: `0x78` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.135.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.136 bit_filter_masked_value

Auto-extracted signal masked_value from bit_filter.vhd - Offset: `0x7c` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.136.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.137 bit_segment_meter_sel_tseg1

Auto-extracted signal sel_tseg1 from bit_segment_meter.vhd - Offset: `0x80` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.137.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.138 bit_segment_meter_exp_seg_length_ce

Auto-extracted signal exp_seg_length_ce from bit_segment_meter.vhd - Offset: `0x84` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.138.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.139 bit_segment_meter_phase_err_mt_sjw

Auto-extracted signal phase_err_mt_sjw from bit_segment_meter.vhd - Offset: `0x88` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.139.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.140 bit_segment_meter_phase_err_eq_sjw

Auto-extracted signal phase_err_eq_sjw from bit_segment_meter.vhd - Offset: `0x8c` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.140.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.141 bit_segment_meter_exit_ph2_immediate

Auto-extracted signal exit_ph2_immediate from bit_segment_meter.vhd - Offset: `0x90` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.141.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.142 bit_segment_meter_exit_segm_regular

Auto-extracted signal exit_segm_regular from bit_segment_meter.vhd - Offset: `0x94` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.142.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.143 bit_segment_meter_exit_segm_regular_tseg1

Auto-extracted signal exit_segm_regular_tseg1 from bit_segment_meter.vhd - Offset: `0x98` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.143.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.144 bit_segment_meter_exit_segm_regular_tseg2

Auto-extracted signal exit_segm_regular_tseg2 from bit_segment_meter.vhd - Offset: `0x9c` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.144.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.145 bit_segment_meter_sjw_mt_zero

Auto-extracted signal sjw_mt_zero from bit_segment_meter.vhd - Offset: `0xa0` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.145.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.146 bit_segment_meter_use_basic_segm_length

Auto-extracted signal use_basic_segm_length from bit_segment_meter.vhd - Offset: `0xa4` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.146.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.147 bit_segment_meter_phase_err_sjw_by_one

Auto-extracted signal phase_err_sjw_by_one from bit_segment_meter.vhd - Offset: `0xa8` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.147.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.148 bit_segment_meter_shorten_tseg1_after_tseg2

Auto-extracted signal shorten_tseg1_after_tseg2 from bit_segment_meter.vhd - Offset: `0xac` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.148.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.149 bit_stuffing_data_out_i

Auto-extracted signal data_out_i from bit_stuffing.vhd - Offset: `0xb0` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.149.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.150 bit_stuffing_data_halt_q

Auto-extracted signal data_halt_q from bit_stuffing.vhd - Offset: `0xb4` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.150.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.151 bit_stuffing_data_halt_d

Auto-extracted signal data_halt_d from bit_stuffing.vhd - Offset: `0xb8` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.151.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.152 bit_stuffing_fixed_reg_q

Auto-extracted signal fixed_reg_q from bit_stuffing.vhd - Offset: `0xbc` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.152.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.153 bit_stuffing_fixed_reg_d

Auto-extracted signal fixed_reg_d from bit_stuffing.vhd - Offset: `0xc0` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.153.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.154 bit_stuffing_enable_prev

Auto-extracted signal enable_prev from bit_stuffing.vhd - Offset: `0xc4` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.154.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.155 bit_stuffing_non_fix_to_fix_chng

Auto-extracted signal non_fix_to_fix_chng from bit_stuffing.vhd - Offset: `0xc8` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.155.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.156 bit_stuffing_stuff_lvl_reached

Auto-extracted signal stuff_lvl_reached from bit_stuffing.vhd - Offset: `0xcc` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.156.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.157 bit_stuffing_same_bits_rst_trig

Auto-extracted signal same_bits_rst_trig from bit_stuffing.vhd - Offset: `0xd0` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.157.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.158 bit_stuffing_same_bits_rst

Auto-extracted signal same_bits_rst from bit_stuffing.vhd - Offset: `0xd4` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.158.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.159 bit_stuffing_insert_stuff_bit

Auto-extracted signal insert_stuff_bit from bit_stuffing.vhd - Offset: `0xd8` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.159.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.160 bit_stuffing_data_out_d_ena

Auto-extracted signal data_out_d_ena from bit_stuffing.vhd - Offset: `0xdc` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.160.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.161 bit_stuffing_data_out_d

Auto-extracted signal data_out_d from bit_stuffing.vhd - Offset: `0xe0` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.161.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.162 bit_stuffing_data_out_ce

Auto-extracted signal data_out_ce from bit_stuffing.vhd - Offset: `0xe4` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.162.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.163 bit_time_cfg_capture_drv_tq_nbt

Auto-extracted signal drv_tq_nbt from bit_time_cfg_capture.vhd - Offset: `0xe8` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.163.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.164 bit_time_cfg_capture_drv_prs_nbt

Auto-extracted signal drv_prs_nbt from bit_time_cfg_capture.vhd - Offset: `0xec` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.164.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.165 bit_time_cfg_capture_drv_ph1_nbt

Auto-extracted signal drv_ph1_nbt from bit_time_cfg_capture.vhd - Offset: `0xf0` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.165.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.166 bit_time_cfg_capture_drv_ph2_nbt

Auto-extracted signal drv_ph2_nbt from bit_time_cfg_capture.vhd - Offset: `0xf4` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.166.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.167 bit_time_cfg_capture_drv_sjw_nbt

Auto-extracted signal drv_sjw_nbt from bit_time_cfg_capture.vhd - Offset: `0xf8` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.167.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.168 bit_time_cfg_capture_drv_tq_dbt

Auto-extracted signal drv_tq_dbt from bit_time_cfg_capture.vhd - Offset: `0xfc` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.168.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.169 bit_time_cfg_capture_drv_prs_dbt

Auto-extracted signal drv_prs_dbt from bit_time_cfg_capture.vhd - Offset: `0x100` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.169.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.170 bit_time_cfg_capture_drv_ph1_dbt

Auto-extracted signal drv_ph1_dbt from bit_time_cfg_capture.vhd - Offset: `0x104` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.170.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.171 bit_time_cfg_capture_drv_ph2_dbt

Auto-extracted signal drv_ph2_dbt from bit_time_cfg_capture.vhd - Offset: `0x108` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.171.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.172 bit_time_cfg_capture_drv_sjw_dbt

Auto-extracted signal drv_sjw_dbt from bit_time_cfg_capture.vhd - Offset: `0x10c` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.172.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.173 bit_time_cfg_capture_tseg1_nbt_d

Auto-extracted signal tseg1_nbt_d from bit_time_cfg_capture.vhd - Offset: `0x110` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.173.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.174 bit_time_cfg_capture_tseg1_dbt_d

Auto-extracted signal tseg1_dbt_d from bit_time_cfg_capture.vhd - Offset: `0x114` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.174.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.175 bit_time_cfg_capture_drv_ena

Auto-extracted signal drv_ena from bit_time_cfg_capture.vhd - Offset: `0x118` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.175.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.176 bit_time_cfg_capture_drv_ena_reg

Auto-extracted signal drv_ena_reg from bit_time_cfg_capture.vhd - Offset: `0x11c` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.176.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.177 bit_time_cfg_capture_drv_ena_reg_2

Auto-extracted signal drv_ena_reg_2 from bit_time_cfg_capture.vhd - Offset: `0x120` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.177.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.178 bit_time_cfg_capture_capture

Auto-extracted signal capture from bit_time_cfg_capture.vhd - Offset: `0x124` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.178.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.179 bit_time_counters_tq_counter_d

Auto-extracted signal tq_counter_d from bit_time_counters.vhd - Offset: `0x128` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.179.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.180 bit_time_counters_tq_counter_q

Auto-extracted signal tq_counter_q from bit_time_counters.vhd - Offset: `0x12c` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.180.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.181 bit_time_counters_tq_counter_ce

Auto-extracted signal tq_counter_ce from bit_time_counters.vhd - Offset: `0x130` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.181.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.182 bit_time_counters_tq_counter_allow

Auto-extracted signal tq_counter_allow from bit_time_counters.vhd - Offset: `0x134` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.182.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.183 bit_time_counters_tq_edge_i

Auto-extracted signal tq_edge_i from bit_time_counters.vhd - Offset: `0x138` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.183.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.184 bit_time_counters_segm_counter_d

Auto-extracted signal segm_counter_d from bit_time_counters.vhd - Offset: `0x13c` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.184.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.185 bit_time_counters_segm_counter_q

Auto-extracted signal segm_counter_q from bit_time_counters.vhd - Offset: `0x140` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.185.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.186 bit_time_counters_segm_counter_ce

Auto-extracted signal segm_counter_ce from bit_time_counters.vhd - Offset: `0x144` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.186.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.187 bit_time_fsm_bt_fsm_ce

Auto-extracted signal bt_fsm_ce from bit_time_fsm.vhd - Offset: `0x148` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.187.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.188 bus_sampling_drv_ena

Auto-extracted signal drv_ena from bus_sampling.vhd - Offset: `0x14c` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.188.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.189 bus_sampling_drv_ssp_offset

Auto-extracted signal drv_ssp_offset from bus_sampling.vhd - Offset: `0x150` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.189.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.190 bus_sampling_drv_ssp_delay_select

Auto-extracted signal drv_ssp_delay_select from bus_sampling.vhd - Offset: `0x154` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.190.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.191 bus_sampling_data_rx_synced

Auto-extracted signal data_rx_synced from bus_sampling.vhd - Offset: `0x158` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.191.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.192 bus_sampling_prev_Sample

Auto-extracted signal prev_Sample from bus_sampling.vhd - Offset: `0x15c` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.192.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.193 bus_sampling_sample_sec_i

Auto-extracted signal sample_sec_i from bus_sampling.vhd - Offset: `0x160` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.193.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.194 bus_sampling_data_tx_delayed

Auto-extracted signal data_tx_delayed from bus_sampling.vhd - Offset: `0x164` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.194.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.195 bus_sampling_edge_rx_valid

Auto-extracted signal edge_rx_valid from bus_sampling.vhd - Offset: `0x168` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.195.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.196 bus_sampling_edge_tx_valid

Auto-extracted signal edge_tx_valid from bus_sampling.vhd - Offset: `0x16c` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.196.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.197 bus_sampling_ssp_delay

Auto-extracted signal ssp_delay from bus_sampling.vhd - Offset: `0x170` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.197.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.198 bus_sampling_tx_trigger_q

Auto-extracted signal tx_trigger_q from bus_sampling.vhd - Offset: `0x174` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.198.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.199 bus_sampling_tx_trigger_ssp

Auto-extracted signal tx_trigger_ssp from bus_sampling.vhd - Offset: `0x178` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.199.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.200 bus_sampling_shift_regs_res_d

Auto-extracted signal shift_regs_res_d from bus_sampling.vhd - Offset: `0x17c` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.200.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.201 bus_sampling_shift_regs_res_q

Auto-extracted signal shift_regs_res_q from bus_sampling.vhd - Offset: `0x180` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.201.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.202 bus_sampling_shift_regs_res_q_scan

Auto-extracted signal shift_regs_res_q_scan from bus_sampling.vhd - Offset: `0x184` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.202.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.203 bus_sampling_ssp_enable

Auto-extracted signal ssp_enable from bus_sampling.vhd - Offset: `0x188` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.203.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.204 bus_traffic_counters_tx_ctr_i

Auto-extracted signal tx_ctr_i from bus_traffic_counters.vhd - Offset: `0x18c` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.204.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.205 bus_traffic_counters_rx_ctr_i

Auto-extracted signal rx_ctr_i from bus_traffic_counters.vhd - Offset: `0x190` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.205.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.206 bus_traffic_counters_tx_ctr_rst_n_d

Auto-extracted signal tx_ctr_rst_n_d from bus_traffic_counters.vhd - Offset: `0x194` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.206.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.207 bus_traffic_counters_tx_ctr_rst_n_q

Auto-extracted signal tx_ctr_rst_n_q from bus_traffic_counters.vhd - Offset: `0x198` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.207.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.208 bus_traffic_counters_tx_ctr_rst_n_q_scan

Auto-extracted signal tx_ctr_rst_n_q_scan from bus_traffic_counters.vhd - Offset: `0x19c` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.208.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.209 bus_traffic_counters_rx_ctr_rst_n_d

Auto-extracted signal rx_ctr_rst_n_d from bus_traffic_counters.vhd - Offset: `0x1a0` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.209.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.210 bus_traffic_counters_rx_ctr_rst_n_q

Auto-extracted signal rx_ctr_rst_n_q from bus_traffic_counters.vhd - Offset: `0x1a4` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.210.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.211 bus_traffic_counters_rx_ctr_rst_n_q_scan

Auto-extracted signal rx_ctr_rst_n_q_scan from bus_traffic_counters.vhd - Offset: `0x1a8` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.211.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.212 can_apb_tb_s_apb_paddr

Auto-extracted signal s_apb_paddr from can_apb_tb.vhd - Offset: `0x1ac` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.212.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.213 can_apb_tb_s_apb_penable

Auto-extracted signal s_apb_penable from can_apb_tb.vhd - Offset: `0x1b0` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.213.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.214 can_apb_tb_s_apb_pprot

Auto-extracted signal s_apb_pprot from can_apb_tb.vhd - Offset: `0x1b4` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.214.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.215 can_apb_tb_s_apb_prdata

Auto-extracted signal s_apb_prdata from can_apb_tb.vhd - Offset: `0x1b8` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.215.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.216 can_apb_tb_s_apb_pready

Auto-extracted signal s_apb_pready from can_apb_tb.vhd - Offset: `0x1bc` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.216.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.217 can_apb_tb_s_apb_psel

Auto-extracted signal s_apb_psel from can_apb_tb.vhd - Offset: `0x1c0` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.217.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.218 can_apb_tb_s_apb_pslverr

Auto-extracted signal s_apb_pslverr from can_apb_tb.vhd - Offset: `0x1c4` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.218.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.219 can_apb_tb_s_apb_pstrb

Auto-extracted signal s_apb_pstrb from can_apb_tb.vhd - Offset: `0x1c8` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.219.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.220 can_apb_tb_s_apb_pwdata

Auto-extracted signal s_apb_pwdata from can_apb_tb.vhd - Offset: `0x1cc` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.220.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.221 can_apb_tb_s_apb_pwrite

Auto-extracted signal s_apb_pwrite from can_apb_tb.vhd - Offset: `0x1d0` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.221.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.222 can_core_drv_clr_rx_ctr

Auto-extracted signal drv_clr_rx_ctr from can_core.vhd - Offset: `0x1d4` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.222.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.223 can_core_drv_clr_tx_ctr

Auto-extracted signal drv_clr_tx_ctr from can_core.vhd - Offset: `0x1d8` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.223.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.224 can_core_drv_bus_mon_ena

Auto-extracted signal drv_bus_mon_ena from can_core.vhd - Offset: `0x1dc` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.224.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.225 can_core_drv_ena

Auto-extracted signal drv_ena from can_core.vhd - Offset: `0x1e0` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.225.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.226 can_core_rec_ident_i

Auto-extracted signal rec_ident_i from can_core.vhd - Offset: `0x1e4` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.226.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.227 can_core_rec_dlc_i

Auto-extracted signal rec_dlc_i from can_core.vhd - Offset: `0x1e8` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.227.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.228 can_core_rec_ident_type_i

Auto-extracted signal rec_ident_type_i from can_core.vhd - Offset: `0x1ec` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.228.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.229 can_core_rec_frame_type_i

Auto-extracted signal rec_frame_type_i from can_core.vhd - Offset: `0x1f0` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.229.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.230 can_core_rec_is_rtr_i

Auto-extracted signal rec_is_rtr_i from can_core.vhd - Offset: `0x1f4` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.230.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.231 can_core_rec_brs_i

Auto-extracted signal rec_brs_i from can_core.vhd - Offset: `0x1f8` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.231.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.232 can_core_rec_esi_i

Auto-extracted signal rec_esi_i from can_core.vhd - Offset: `0x1fc` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.232.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.233 can_core_alc

Auto-extracted signal alc from can_core.vhd - Offset: `0x200` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.233.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.234 can_core_erc_capture

Auto-extracted signal erc_capture from can_core.vhd - Offset: `0x204` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.234.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.235 can_core_is_transmitter

Auto-extracted signal is_transmitter from can_core.vhd - Offset: `0x208` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.235.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.236 can_core_is_receiver

Auto-extracted signal is_receiver from can_core.vhd - Offset: `0x20c` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.236.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.237 can_core_is_idle

Auto-extracted signal is_idle from can_core.vhd - Offset: `0x210` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.237.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.238 can_core_arbitration_lost_i

Auto-extracted signal arbitration_lost_i from can_core.vhd - Offset: `0x214` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.238.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.239 can_core_set_transmitter

Auto-extracted signal set_transmitter from can_core.vhd - Offset: `0x218` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.239.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.240 can_core_set_receiver

Auto-extracted signal set_receiver from can_core.vhd - Offset: `0x21c` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.240.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.241 can_core_set_idle

Auto-extracted signal set_idle from can_core.vhd - Offset: `0x220` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.241.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.242 can_core_is_err_active

Auto-extracted signal is_err_active from can_core.vhd - Offset: `0x224` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.242.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.243 can_core_is_err_passive

Auto-extracted signal is_err_passive from can_core.vhd - Offset: `0x228` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.243.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.244 can_core_is_bus_off_i

Auto-extracted signal is_bus_off_i from can_core.vhd - Offset: `0x22c` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.244.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.245 can_core_err_detected_i

Auto-extracted signal err_detected_i from can_core.vhd - Offset: `0x230` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.245.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.246 can_core_primary_err

Auto-extracted signal primary_err from can_core.vhd - Offset: `0x234` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.246.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.247 can_core_act_err_ovr_flag

Auto-extracted signal act_err_ovr_flag from can_core.vhd - Offset: `0x238` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.247.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.248 can_core_err_delim_late

Auto-extracted signal err_delim_late from can_core.vhd - Offset: `0x23c` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.248.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.249 can_core_set_err_active

Auto-extracted signal set_err_active from can_core.vhd - Offset: `0x240` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.249.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.250 can_core_err_ctrs_unchanged

Auto-extracted signal err_ctrs_unchanged from can_core.vhd - Offset: `0x244` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.250.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.251 can_core_stuff_enable

Auto-extracted signal stuff_enable from can_core.vhd - Offset: `0x248` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.251.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.252 can_core_destuff_enable

Auto-extracted signal destuff_enable from can_core.vhd - Offset: `0x24c` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.252.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.253 can_core_fixed_stuff

Auto-extracted signal fixed_stuff from can_core.vhd - Offset: `0x250` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.253.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.254 can_core_tx_frame_no_sof

Auto-extracted signal tx_frame_no_sof from can_core.vhd - Offset: `0x254` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.254.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.255 can_core_stuff_length

Auto-extracted signal stuff_length from can_core.vhd - Offset: `0x258` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.255.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.256 can_core_dst_ctr

Auto-extracted signal dst_ctr from can_core.vhd - Offset: `0x25c` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.256.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.257 can_core_bst_ctr

Auto-extracted signal bst_ctr from can_core.vhd - Offset: `0x260` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.257.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.258 can_core_stuff_err

Auto-extracted signal stuff_err from can_core.vhd - Offset: `0x264` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.258.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.259 can_core_crc_enable

Auto-extracted signal crc_enable from can_core.vhd - Offset: `0x268` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.259.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.260 can_core_crc_spec_enable

Auto-extracted signal crc_spec_enable from can_core.vhd - Offset: `0x26c` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.260.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.261 can_core_crc_calc_from_rx

Auto-extracted signal crc_calc_from_rx from can_core.vhd - Offset: `0x270` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.261.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.262 can_core_crc_15

Auto-extracted signal crc_15 from can_core.vhd - Offset: `0x274` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.262.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.263 can_core_crc_17

Auto-extracted signal crc_17 from can_core.vhd - Offset: `0x278` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.263.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.264 can_core_crc_21

Auto-extracted signal crc_21 from can_core.vhd - Offset: `0x27c` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.264.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.265 can_core_sp_control_i

Auto-extracted signal sp_control_i from can_core.vhd - Offset: `0x280` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.265.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.266 can_core_sp_control_q

Auto-extracted signal sp_control_q from can_core.vhd - Offset: `0x284` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.266.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.267 can_core_sync_control_i

Auto-extracted signal sync_control_i from can_core.vhd - Offset: `0x288` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.267.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.268 can_core_ssp_reset_i

Auto-extracted signal ssp_reset_i from can_core.vhd - Offset: `0x28c` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.268.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.269 can_core_tran_delay_meas_i

Auto-extracted signal tran_delay_meas_i from can_core.vhd - Offset: `0x290` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.269.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.270 can_core_tran_valid_i

Auto-extracted signal tran_valid_i from can_core.vhd - Offset: `0x294` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.270.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.271 can_core_rec_valid_i

Auto-extracted signal rec_valid_i from can_core.vhd - Offset: `0x298` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.271.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.272 can_core_br_shifted_i

Auto-extracted signal br_shifted_i from can_core.vhd - Offset: `0x29c` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.272.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.273 can_core_fcs_changed_i

Auto-extracted signal fcs_changed_i from can_core.vhd - Offset: `0x2a0` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.273.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.274 can_core_err_warning_limit_i

Auto-extracted signal err_warning_limit_i from can_core.vhd - Offset: `0x2a4` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.274.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.275 can_core_tx_err_ctr

Auto-extracted signal tx_err_ctr from can_core.vhd - Offset: `0x2a8` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.275.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.276 can_core_rx_err_ctr

Auto-extracted signal rx_err_ctr from can_core.vhd - Offset: `0x2ac` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.276.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.277 can_core_norm_err_ctr

Auto-extracted signal norm_err_ctr from can_core.vhd - Offset: `0x2b0` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.277.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.278 can_core_data_err_ctr

Auto-extracted signal data_err_ctr from can_core.vhd - Offset: `0x2b4` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.278.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.279 can_core_pc_tx_trigger

Auto-extracted signal pc_tx_trigger from can_core.vhd - Offset: `0x2b8` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.279.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.280 can_core_pc_rx_trigger

Auto-extracted signal pc_rx_trigger from can_core.vhd - Offset: `0x2bc` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.280.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.281 can_core_pc_tx_data_nbs

Auto-extracted signal pc_tx_data_nbs from can_core.vhd - Offset: `0x2c0` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.281.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.282 can_core_pc_rx_data_nbs

Auto-extracted signal pc_rx_data_nbs from can_core.vhd - Offset: `0x2c4` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.282.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.283 can_core_crc_data_tx_wbs

Auto-extracted signal crc_data_tx_wbs from can_core.vhd - Offset: `0x2c8` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.283.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.284 can_core_crc_data_tx_nbs

Auto-extracted signal crc_data_tx_nbs from can_core.vhd - Offset: `0x2cc` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.284.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.285 can_core_crc_data_rx_wbs

Auto-extracted signal crc_data_rx_wbs from can_core.vhd - Offset: `0x2d0` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.285.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.286 can_core_crc_data_rx_nbs

Auto-extracted signal crc_data_rx_nbs from can_core.vhd - Offset: `0x2d4` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.286.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.287 can_core_crc_trig_tx_wbs

Auto-extracted signal crc_trig_tx_wbs from can_core.vhd - Offset: `0x2d8` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.287.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.288 can_core_crc_trig_tx_nbs

Auto-extracted signal crc_trig_tx_nbs from can_core.vhd - Offset: `0x2dc` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.288.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.289 can_core_crc_trig_rx_wbs

Auto-extracted signal crc_trig_rx_wbs from can_core.vhd - Offset: `0x2e0` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.289.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.290 can_core_crc_trig_rx_nbs

Auto-extracted signal crc_trig_rx_nbs from can_core.vhd - Offset: `0x2e4` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.290.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.291 can_core_bst_data_in

Auto-extracted signal bst_data_in from can_core.vhd - Offset: `0x2e8` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.291.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.292 can_core_bst_data_out

Auto-extracted signal bst_data_out from can_core.vhd - Offset: `0x2ec` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.292.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.293 can_core_bst_trigger

Auto-extracted signal bst_trigger from can_core.vhd - Offset: `0x2f0` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.293.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.294 can_core_data_halt

Auto-extracted signal data_halt from can_core.vhd - Offset: `0x2f4` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.294.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.295 can_core_bds_data_in

Auto-extracted signal bds_data_in from can_core.vhd - Offset: `0x2f8` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.295.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.296 can_core_bds_data_out

Auto-extracted signal bds_data_out from can_core.vhd - Offset: `0x2fc` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.296.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.297 can_core_bds_trigger

Auto-extracted signal bds_trigger from can_core.vhd - Offset: `0x300` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.297.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.298 can_core_destuffed

Auto-extracted signal destuffed from can_core.vhd - Offset: `0x304` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.298.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.299 can_core_tx_ctr

Auto-extracted signal tx_ctr from can_core.vhd - Offset: `0x308` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.299.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.300 can_core_rx_ctr

Auto-extracted signal rx_ctr from can_core.vhd - Offset: `0x30c` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.300.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.301 can_core_tx_data_wbs_i

Auto-extracted signal tx_data_wbs_i from can_core.vhd - Offset: `0x310` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.301.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.302 can_core_lpb_dominant

Auto-extracted signal lpb_dominant from can_core.vhd - Offset: `0x314` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.302.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.303 can_core_form_err

Auto-extracted signal form_err from can_core.vhd - Offset: `0x318` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.303.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.304 can_core_ack_err

Auto-extracted signal ack_err from can_core.vhd - Offset: `0x31c` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.304.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.305 can_core_crc_err

Auto-extracted signal crc_err from can_core.vhd - Offset: `0x320` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.305.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.306 can_core_is_arbitration

Auto-extracted signal is_arbitration from can_core.vhd - Offset: `0x324` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.306.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.307 can_core_is_control

Auto-extracted signal is_control from can_core.vhd - Offset: `0x328` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.307.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.308 can_core_is_data

Auto-extracted signal is_data from can_core.vhd - Offset: `0x32c` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.308.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.309 can_core_is_stuff_count

Auto-extracted signal is_stuff_count from can_core.vhd - Offset: `0x330` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.309.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.310 can_core_is_crc

Auto-extracted signal is_crc from can_core.vhd - Offset: `0x334` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.310.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.311 can_core_is_crc_delim

Auto-extracted signal is_crc_delim from can_core.vhd - Offset: `0x338` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.311.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.312 can_core_is_ack_field

Auto-extracted signal is_ack_field from can_core.vhd - Offset: `0x33c` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.312.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.313 can_core_is_ack_delim

Auto-extracted signal is_ack_delim from can_core.vhd - Offset: `0x340` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.313.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.314 can_core_is_eof

Auto-extracted signal is_eof from can_core.vhd - Offset: `0x344` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.314.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.315 can_core_is_err_frm

Auto-extracted signal is_err_frm from can_core.vhd - Offset: `0x348` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.315.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.316 can_core_is_intermission

Auto-extracted signal is_intermission from can_core.vhd - Offset: `0x34c` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.316.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.317 can_core_is_suspend

Auto-extracted signal is_suspend from can_core.vhd - Offset: `0x350` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.317.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.318 can_core_is_overload_i

Auto-extracted signal is_overload_i from can_core.vhd - Offset: `0x354` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.318.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.319 can_core_is_sof

Auto-extracted signal is_sof from can_core.vhd - Offset: `0x358` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.319.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.320 can_core_sof_pulse_i

Auto-extracted signal sof_pulse_i from can_core.vhd - Offset: `0x35c` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.320.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.321 can_core_load_init_vect

Auto-extracted signal load_init_vect from can_core.vhd - Offset: `0x360` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.321.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.322 can_core_retr_ctr_i

Auto-extracted signal retr_ctr_i from can_core.vhd - Offset: `0x364` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.322.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.323 can_core_decrement_rec

Auto-extracted signal decrement_rec from can_core.vhd - Offset: `0x368` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.323.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.324 can_core_bit_err_after_ack_err

Auto-extracted signal bit_err_after_ack_err from can_core.vhd - Offset: `0x36c` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.324.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.325 can_core_is_pexs

Auto-extracted signal is_pexs from can_core.vhd - Offset: `0x370` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.325.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.326 can_crc_drv_fd_type

Auto-extracted signal drv_fd_type from can_crc.vhd - Offset: `0x374` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.326.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.327 can_crc_init_vect_15

Auto-extracted signal init_vect_15 from can_crc.vhd - Offset: `0x378` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.327.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.328 can_crc_init_vect_17

Auto-extracted signal init_vect_17 from can_crc.vhd - Offset: `0x37c` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.328.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.329 can_crc_init_vect_21

Auto-extracted signal init_vect_21 from can_crc.vhd - Offset: `0x380` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.329.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.330 can_crc_crc_17_21_data_in

Auto-extracted signal crc_17_21_data_in from can_crc.vhd - Offset: `0x384` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.330.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.331 can_crc_crc_17_21_trigger

Auto-extracted signal crc_17_21_trigger from can_crc.vhd - Offset: `0x388` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.331.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.332 can_crc_crc_15_data_in

Auto-extracted signal crc_15_data_in from can_crc.vhd - Offset: `0x38c` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.332.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.333 can_crc_crc_15_trigger

Auto-extracted signal crc_15_trigger from can_crc.vhd - Offset: `0x390` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.333.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.334 can_crc_crc_ena_15

Auto-extracted signal crc_ena_15 from can_crc.vhd - Offset: `0x394` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.334.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.335 can_crc_crc_ena_17_21

Auto-extracted signal crc_ena_17_21 from can_crc.vhd - Offset: `0x398` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.335.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.336 can_top_ahb_ctu_can_data_in

Auto-extracted signal ctu_can_data_in from can_top_ahb.vhd - Offset: `0x39c` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.336.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.337 can_top_ahb_ctu_can_data_out

Auto-extracted signal ctu_can_data_out from can_top_ahb.vhd - Offset: `0x3a0` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.337.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.338 can_top_ahb_ctu_can_adress

Auto-extracted signal ctu_can_adress from can_top_ahb.vhd - Offset: `0x3a4` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.338.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.339 can_top_ahb_ctu_can_scs

Auto-extracted signal ctu_can_scs from can_top_ahb.vhd - Offset: `0x3a8` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.339.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.340 can_top_ahb_ctu_can_srd

Auto-extracted signal ctu_can_srd from can_top_ahb.vhd - Offset: `0x3ac` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.340.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.341 can_top_ahb_ctu_can_swr

Auto-extracted signal ctu_can_swr from can_top_ahb.vhd - Offset: `0x3b0` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.341.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.342 can_top_ahb_ctu_can_sbe

Auto-extracted signal ctu_can_sbe from can_top_ahb.vhd - Offset: `0x3b4` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.342.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.343 can_top_ahb_res_n_out_i

Auto-extracted signal res_n_out_i from can_top_ahb.vhd - Offset: `0x3b8` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.343.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.344 can_top_apb_reg_data_in

Auto-extracted signal reg_data_in from can_top_apb.vhd - Offset: `0x3bc` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.344.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.345 can_top_apb_reg_data_out

Auto-extracted signal reg_data_out from can_top_apb.vhd - Offset: `0x3c0` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.345.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.346 can_top_apb_reg_addr

Auto-extracted signal reg_addr from can_top_apb.vhd - Offset: `0x3c4` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.346.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.347 can_top_apb_reg_be

Auto-extracted signal reg_be from can_top_apb.vhd - Offset: `0x3c8` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.347.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.348 can_top_apb_reg_rden

Auto-extracted signal reg_rden from can_top_apb.vhd - Offset: `0x3cc` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.348.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.349 can_top_apb_reg_wren

Auto-extracted signal reg_wren from can_top_apb.vhd - Offset: `0x3d0` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.349.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.350 can_top_level_drv_bus

Auto-extracted signal drv_bus from can_top_level.vhd - Offset: `0x3d4` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.350.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.351 can_top_level_stat_bus

Auto-extracted signal stat_bus from can_top_level.vhd - Offset: `0x3d8` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.351.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.352 can_top_level_res_n_sync

Auto-extracted signal res_n_sync from can_top_level.vhd - Offset: `0x3dc` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.352.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.353 can_top_level_res_core_n

Auto-extracted signal res_core_n from can_top_level.vhd - Offset: `0x3e0` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.353.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.354 can_top_level_res_soft_n

Auto-extracted signal res_soft_n from can_top_level.vhd - Offset: `0x3e4` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.354.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.355 can_top_level_sp_control

Auto-extracted signal sp_control from can_top_level.vhd - Offset: `0x3e8` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.355.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.356 can_top_level_rx_buf_size

Auto-extracted signal rx_buf_size from can_top_level.vhd - Offset: `0x3ec` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.356.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.357 can_top_level_rx_full

Auto-extracted signal rx_full from can_top_level.vhd - Offset: `0x3f0` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.357.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.358 can_top_level_rx_empty

Auto-extracted signal rx_empty from can_top_level.vhd - Offset: `0x3f4` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.358.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.359 can_top_level_rx_frame_count

Auto-extracted signal rx_frame_count from can_top_level.vhd - Offset: `0x3f8` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.359.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.360 can_top_level_rx_mem_free

Auto-extracted signal rx_mem_free from can_top_level.vhd - Offset: `0x3fc` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.360.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.361 can_top_level_rx_read_pointer

Auto-extracted signal rx_read_pointer from can_top_level.vhd - Offset: `0x400` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.361.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.362 can_top_level_rx_write_pointer

Auto-extracted signal rx_write_pointer from can_top_level.vhd - Offset: `0x404` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.362.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.363 can_top_level_rx_data_overrun

Auto-extracted signal rx_data_overrun from can_top_level.vhd - Offset: `0x408` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.363.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.364 can_top_level_rx_read_buff

Auto-extracted signal rx_read_buff from can_top_level.vhd - Offset: `0x40c` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.364.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.365 can_top_level_rx_mof

Auto-extracted signal rx_mof from can_top_level.vhd - Offset: `0x410` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.365.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.366 can_top_level_txtb_port_a_data

Auto-extracted signal txtb_port_a_data from can_top_level.vhd - Offset: `0x414` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.366.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.367 can_top_level_txtb_port_a_address

Auto-extracted signal txtb_port_a_address from can_top_level.vhd - Offset: `0x418` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.367.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.368 can_top_level_txtb_port_a_cs

Auto-extracted signal txtb_port_a_cs from can_top_level.vhd - Offset: `0x41c` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.368.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.369 can_top_level_txtb_port_a_be

Auto-extracted signal txtb_port_a_be from can_top_level.vhd - Offset: `0x420` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.369.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.370 can_top_level_txtb_sw_cmd_index

Auto-extracted signal txtb_sw_cmd_index from can_top_level.vhd - Offset: `0x424` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.370.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.371 can_top_level_txt_buf_failed_bof

Auto-extracted signal txt_buf_failed_bof from can_top_level.vhd - Offset: `0x428` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.371.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.372 can_top_level_int_vector

Auto-extracted signal int_vector from can_top_level.vhd - Offset: `0x42c` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.372.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.373 can_top_level_int_ena

Auto-extracted signal int_ena from can_top_level.vhd - Offset: `0x430` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.373.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.374 can_top_level_int_mask

Auto-extracted signal int_mask from can_top_level.vhd - Offset: `0x434` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.374.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.375 can_top_level_rec_ident

Auto-extracted signal rec_ident from can_top_level.vhd - Offset: `0x438` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.375.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.376 can_top_level_rec_dlc

Auto-extracted signal rec_dlc from can_top_level.vhd - Offset: `0x43c` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.376.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.377 can_top_level_rec_ident_type

Auto-extracted signal rec_ident_type from can_top_level.vhd - Offset: `0x440` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.377.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.378 can_top_level_rec_frame_type

Auto-extracted signal rec_frame_type from can_top_level.vhd - Offset: `0x444` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.378.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.379 can_top_level_rec_is_rtr

Auto-extracted signal rec_is_rtr from can_top_level.vhd - Offset: `0x448` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.379.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.380 can_top_level_rec_brs

Auto-extracted signal rec_brs from can_top_level.vhd - Offset: `0x44c` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.380.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.381 can_top_level_rec_esi

Auto-extracted signal rec_esi from can_top_level.vhd - Offset: `0x450` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.381.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.382 can_top_level_store_data_word

Auto-extracted signal store_data_word from can_top_level.vhd - Offset: `0x454` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.382.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.383 can_top_level_sof_pulse

Auto-extracted signal sof_pulse from can_top_level.vhd - Offset: `0x458` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.383.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.384 can_top_level_store_metadata

Auto-extracted signal store_metadata from can_top_level.vhd - Offset: `0x45c` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.384.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.385 can_top_level_store_data

Auto-extracted signal store_data from can_top_level.vhd - Offset: `0x460` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.385.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.386 can_top_level_rec_valid

Auto-extracted signal rec_valid from can_top_level.vhd - Offset: `0x464` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.386.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.387 can_top_level_rec_abort

Auto-extracted signal rec_abort from can_top_level.vhd - Offset: `0x468` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.387.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.388 can_top_level_store_metadata_f

Auto-extracted signal store_metadata_f from can_top_level.vhd - Offset: `0x46c` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.388.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.389 can_top_level_store_data_f

Auto-extracted signal store_data_f from can_top_level.vhd - Offset: `0x470` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.389.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.390 can_top_level_rec_valid_f

Auto-extracted signal rec_valid_f from can_top_level.vhd - Offset: `0x474` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.390.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.391 can_top_level_rec_abort_f

Auto-extracted signal rec_abort_f from can_top_level.vhd - Offset: `0x478` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.391.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.392 can_top_level_txtb_hw_cmd_int

Auto-extracted signal txtb_hw_cmd_int from can_top_level.vhd - Offset: `0x47c` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.392.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.393 can_top_level_is_bus_off

Auto-extracted signal is_bus_off from can_top_level.vhd - Offset: `0x480` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.393.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.394 can_top_level_txtb_available

Auto-extracted signal txtb_available from can_top_level.vhd - Offset: `0x484` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.394.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.395 can_top_level_txtb_port_b_clk_en

Auto-extracted signal txtb_port_b_clk_en from can_top_level.vhd - Offset: `0x488` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.395.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.396 can_top_level_tran_dlc

Auto-extracted signal tran_dlc from can_top_level.vhd - Offset: `0x48c` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.396.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.397 can_top_level_tran_is_rtr

Auto-extracted signal tran_is_rtr from can_top_level.vhd - Offset: `0x490` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.397.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.398 can_top_level_tran_ident_type

Auto-extracted signal tran_ident_type from can_top_level.vhd - Offset: `0x494` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.398.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.399 can_top_level_tran_frame_type

Auto-extracted signal tran_frame_type from can_top_level.vhd - Offset: `0x498` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.399.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.400 can_top_level_tran_brs

Auto-extracted signal tran_brs from can_top_level.vhd - Offset: `0x49c` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.400.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.401 can_top_level_tran_identifier

Auto-extracted signal tran_identifier from can_top_level.vhd - Offset: `0x4a0` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.401.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.402 can_top_level_tran_word

Auto-extracted signal tran_word from can_top_level.vhd - Offset: `0x4a4` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.402.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.403 can_top_level_tran_frame_valid

Auto-extracted signal tran_frame_valid from can_top_level.vhd - Offset: `0x4a8` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.403.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.404 can_top_level_txtb_changed

Auto-extracted signal txtb_changed from can_top_level.vhd - Offset: `0x4ac` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.404.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.405 can_top_level_txtb_clk_en

Auto-extracted signal txtb_clk_en from can_top_level.vhd - Offset: `0x4b0` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.405.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.406 can_top_level_err_detected

Auto-extracted signal err_detected from can_top_level.vhd - Offset: `0x4b4` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.406.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.407 can_top_level_fcs_changed

Auto-extracted signal fcs_changed from can_top_level.vhd - Offset: `0x4b8` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.407.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.408 can_top_level_err_warning_limit

Auto-extracted signal err_warning_limit from can_top_level.vhd - Offset: `0x4bc` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.408.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.409 can_top_level_arbitration_lost

Auto-extracted signal arbitration_lost from can_top_level.vhd - Offset: `0x4c0` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.409.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.410 can_top_level_tran_valid

Auto-extracted signal tran_valid from can_top_level.vhd - Offset: `0x4c4` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.410.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.411 can_top_level_br_shifted

Auto-extracted signal br_shifted from can_top_level.vhd - Offset: `0x4c8` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.411.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.412 can_top_level_is_overload

Auto-extracted signal is_overload from can_top_level.vhd - Offset: `0x4cc` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.412.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.413 can_top_level_rx_triggers

Auto-extracted signal rx_triggers from can_top_level.vhd - Offset: `0x4d0` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.413.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.414 can_top_level_tx_trigger

Auto-extracted signal tx_trigger from can_top_level.vhd - Offset: `0x4d4` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.414.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.415 can_top_level_sync_control

Auto-extracted signal sync_control from can_top_level.vhd - Offset: `0x4d8` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.415.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.416 can_top_level_no_pos_resync

Auto-extracted signal no_pos_resync from can_top_level.vhd - Offset: `0x4dc` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.416.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.417 can_top_level_nbt_ctrs_en

Auto-extracted signal nbt_ctrs_en from can_top_level.vhd - Offset: `0x4e0` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.417.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.418 can_top_level_dbt_ctrs_en

Auto-extracted signal dbt_ctrs_en from can_top_level.vhd - Offset: `0x4e4` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.418.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.419 can_top_level_trv_delay

Auto-extracted signal trv_delay from can_top_level.vhd - Offset: `0x4e8` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.419.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.420 can_top_level_rx_data_wbs

Auto-extracted signal rx_data_wbs from can_top_level.vhd - Offset: `0x4ec` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.420.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.421 can_top_level_tx_data_wbs

Auto-extracted signal tx_data_wbs from can_top_level.vhd - Offset: `0x4f0` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.421.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.422 can_top_level_ssp_reset

Auto-extracted signal ssp_reset from can_top_level.vhd - Offset: `0x4f4` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.422.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.423 can_top_level_tran_delay_meas

Auto-extracted signal tran_delay_meas from can_top_level.vhd - Offset: `0x4f8` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.423.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.424 can_top_level_bit_err

Auto-extracted signal bit_err from can_top_level.vhd - Offset: `0x4fc` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.424.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.425 can_top_level_sample_sec

Auto-extracted signal sample_sec from can_top_level.vhd - Offset: `0x500` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.425.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.426 can_top_level_btmc_reset

Auto-extracted signal btmc_reset from can_top_level.vhd - Offset: `0x504` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.426.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.427 can_top_level_dbt_measure_start

Auto-extracted signal dbt_measure_start from can_top_level.vhd - Offset: `0x508` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.427.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.428 can_top_level_gen_first_ssp

Auto-extracted signal gen_first_ssp from can_top_level.vhd - Offset: `0x50c` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.428.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.429 can_top_level_sync_edge

Auto-extracted signal sync_edge from can_top_level.vhd - Offset: `0x510` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.429.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.430 can_top_level_tq_edge

Auto-extracted signal tq_edge from can_top_level.vhd - Offset: `0x514` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.430.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.431 can_top_level_tst_rdata_rx_buf

Auto-extracted signal tst_rdata_rx_buf from can_top_level.vhd - Offset: `0x518` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.431.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.432 clk_gate_clk_en_q

Auto-extracted signal clk_en_q from clk_gate.vhd - Offset: `0x51c` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.432.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.433 control_counter_ctrl_ctr_ce

Auto-extracted signal ctrl_ctr_ce from control_counter.vhd - Offset: `0x520` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.433.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.434 control_counter_compl_ctr_ce

Auto-extracted signal compl_ctr_ce from control_counter.vhd - Offset: `0x524` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.434.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.435 control_registers_reg_map_reg_sel

Auto-extracted signal reg_sel from control_registers_reg_map.vhd - Offset: `0x528` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.435.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.436 control_registers_reg_map_read_data_mux_in

Auto-extracted signal read_data_mux_in from control_registers_reg_map.vhd - Offset: `0x52c` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.436.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.437 control_registers_reg_map_read_data_mask_n

Auto-extracted signal read_data_mask_n from control_registers_reg_map.vhd - Offset: `0x530` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.437.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.438 control_registers_reg_map_read_mux_ena

Auto-extracted signal read_mux_ena from control_registers_reg_map.vhd - Offset: `0x534` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.438.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.439 crc_calc_crc_q

Auto-extracted signal crc_q from crc_calc.vhd - Offset: `0x538` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.439.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.440 crc_calc_crc_nxt

Auto-extracted signal crc_nxt from crc_calc.vhd - Offset: `0x53c` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.440.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.441 crc_calc_crc_shift

Auto-extracted signal crc_shift from crc_calc.vhd - Offset: `0x540` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.441.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.442 crc_calc_crc_shift_n_xor

Auto-extracted signal crc_shift_n_xor from crc_calc.vhd - Offset: `0x544` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.442.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.443 crc_calc_crc_d

Auto-extracted signal crc_d from crc_calc.vhd - Offset: `0x548` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.443.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.444 crc_calc_crc_ce

Auto-extracted signal crc_ce from crc_calc.vhd - Offset: `0x54c` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.444.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.445 data_edge_detector_rx_data_prev

Auto-extracted signal rx_data_prev from data_edge_detector.vhd - Offset: `0x550` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.445.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.446 data_edge_detector_tx_data_prev

Auto-extracted signal tx_data_prev from data_edge_detector.vhd - Offset: `0x554` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.446.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.447 data_edge_detector_rx_data_sync_prev

Auto-extracted signal rx_data_sync_prev from data_edge_detector.vhd - Offset: `0x558` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.447.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.448 data_edge_detector_rx_edge_i

Auto-extracted signal rx_edge_i from data_edge_detector.vhd - Offset: `0x55c` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.448.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.449 data_edge_detector_tx_edge_i

Auto-extracted signal tx_edge_i from data_edge_detector.vhd - Offset: `0x560` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.449.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.450 data_mux_sel_data

Auto-extracted signal sel_data from data_mux.vhd - Offset: `0x564` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.450.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.451 data_mux_saturated_data

Auto-extracted signal saturated_data from data_mux.vhd - Offset: `0x568` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.451.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.452 data_mux_masked_data

Auto-extracted signal masked_data from data_mux.vhd - Offset: `0x56c` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.452.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.453 dlc_decoder_data_len_8_to_64

Auto-extracted signal data_len_8_to_64 from dlc_decoder.vhd - Offset: `0x570` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.453.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.454 dlc_decoder_data_len_can_2_0

Auto-extracted signal data_len_can_2_0 from dlc_decoder.vhd - Offset: `0x574` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.454.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.455 dlc_decoder_data_len_can_fd

Auto-extracted signal data_len_can_fd from dlc_decoder.vhd - Offset: `0x578` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.455.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.456 endian_swapper_swapped

Auto-extracted signal swapped from endian_swapper.vhd - Offset: `0x57c` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.456.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.457 err_counters_tx_err_ctr_ce

Auto-extracted signal tx_err_ctr_ce from err_counters.vhd - Offset: `0x580` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.457.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.458 err_counters_rx_err_ctr_ce

Auto-extracted signal rx_err_ctr_ce from err_counters.vhd - Offset: `0x584` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.458.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.459 err_counters_modif_tx_ctr

Auto-extracted signal modif_tx_ctr from err_counters.vhd - Offset: `0x588` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.459.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.460 err_counters_modif_rx_ctr

Auto-extracted signal modif_rx_ctr from err_counters.vhd - Offset: `0x58c` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.460.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.461 err_counters_nom_err_ctr_ce

Auto-extracted signal nom_err_ctr_ce from err_counters.vhd - Offset: `0x590` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.461.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.462 err_counters_data_err_ctr_ce

Auto-extracted signal data_err_ctr_ce from err_counters.vhd - Offset: `0x594` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.462.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.463 err_counters_res_err_ctrs_d

Auto-extracted signal res_err_ctrs_d from err_counters.vhd - Offset: `0x598` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.463.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.464 err_counters_res_err_ctrs_q

Auto-extracted signal res_err_ctrs_q from err_counters.vhd - Offset: `0x59c` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.464.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.465 err_counters_res_err_ctrs_q_scan

Auto-extracted signal res_err_ctrs_q_scan from err_counters.vhd - Offset: `0x5a0` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.465.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.466 err_detector_err_frm_req_i

Auto-extracted signal err_frm_req_i from err_detector.vhd - Offset: `0x5a4` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.466.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.467 err_detector_err_type_d

Auto-extracted signal err_type_d from err_detector.vhd - Offset: `0x5a8` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.467.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.468 err_detector_err_type_q

Auto-extracted signal err_type_q from err_detector.vhd - Offset: `0x5ac` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.468.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.469 err_detector_err_pos_q

Auto-extracted signal err_pos_q from err_detector.vhd - Offset: `0x5b0` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.469.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.470 err_detector_form_err_i

Auto-extracted signal form_err_i from err_detector.vhd - Offset: `0x5b4` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.470.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.471 err_detector_crc_match_c

Auto-extracted signal crc_match_c from err_detector.vhd - Offset: `0x5b8` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.471.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.472 err_detector_crc_match_d

Auto-extracted signal crc_match_d from err_detector.vhd - Offset: `0x5bc` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.472.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.473 err_detector_crc_match_q

Auto-extracted signal crc_match_q from err_detector.vhd - Offset: `0x5c0` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.473.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.474 err_detector_dst_ctr_grey

Auto-extracted signal dst_ctr_grey from err_detector.vhd - Offset: `0x5c4` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.474.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.475 err_detector_dst_parity

Auto-extracted signal dst_parity from err_detector.vhd - Offset: `0x5c8` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.475.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.476 err_detector_stuff_count_check

Auto-extracted signal stuff_count_check from err_detector.vhd - Offset: `0x5cc` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.476.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.477 err_detector_crc_15_ok

Auto-extracted signal crc_15_ok from err_detector.vhd - Offset: `0x5d0` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.477.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.478 err_detector_crc_17_ok

Auto-extracted signal crc_17_ok from err_detector.vhd - Offset: `0x5d4` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.478.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.479 err_detector_crc_21_ok

Auto-extracted signal crc_21_ok from err_detector.vhd - Offset: `0x5d8` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.479.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.480 err_detector_stuff_count_ok

Auto-extracted signal stuff_count_ok from err_detector.vhd - Offset: `0x5dc` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.480.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.481 err_detector_rx_crc_15

Auto-extracted signal rx_crc_15 from err_detector.vhd - Offset: `0x5e0` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.481.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.482 err_detector_rx_crc_17

Auto-extracted signal rx_crc_17 from err_detector.vhd - Offset: `0x5e4` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.482.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.483 err_detector_rx_crc_21

Auto-extracted signal rx_crc_21 from err_detector.vhd - Offset: `0x5e8` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.483.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.484 fault_confinement_drv_ewl

Auto-extracted signal drv_ewl from fault_confinement.vhd - Offset: `0x5ec` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.484.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.485 fault_confinement_drv_erp

Auto-extracted signal drv_erp from fault_confinement.vhd - Offset: `0x5f0` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.485.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.486 fault_confinement_drv_ctr_val

Auto-extracted signal drv_ctr_val from fault_confinement.vhd - Offset: `0x5f4` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.486.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.487 fault_confinement_drv_ctr_sel

Auto-extracted signal drv_ctr_sel from fault_confinement.vhd - Offset: `0x5f8` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.487.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.488 fault_confinement_drv_ena

Auto-extracted signal drv_ena from fault_confinement.vhd - Offset: `0x5fc` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.488.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.489 fault_confinement_tx_err_ctr_i

Auto-extracted signal tx_err_ctr_i from fault_confinement.vhd - Offset: `0x600` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.489.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.490 fault_confinement_rx_err_ctr_i

Auto-extracted signal rx_err_ctr_i from fault_confinement.vhd - Offset: `0x604` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.490.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.491 fault_confinement_inc_one

Auto-extracted signal inc_one from fault_confinement.vhd - Offset: `0x608` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.491.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.492 fault_confinement_inc_eight

Auto-extracted signal inc_eight from fault_confinement.vhd - Offset: `0x60c` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.492.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.493 fault_confinement_dec_one

Auto-extracted signal dec_one from fault_confinement.vhd - Offset: `0x610` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.493.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.494 fault_confinement_drv_rom_ena

Auto-extracted signal drv_rom_ena from fault_confinement.vhd - Offset: `0x614` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.494.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.495 fault_confinement_fsm_tx_err_ctr_mt_erp

Auto-extracted signal tx_err_ctr_mt_erp from fault_confinement_fsm.vhd - Offset: `0x618` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.495.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.496 fault_confinement_fsm_rx_err_ctr_mt_erp

Auto-extracted signal rx_err_ctr_mt_erp from fault_confinement_fsm.vhd - Offset: `0x61c` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.496.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.497 fault_confinement_fsm_tx_err_ctr_mt_ewl

Auto-extracted signal tx_err_ctr_mt_ewl from fault_confinement_fsm.vhd - Offset: `0x620` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.497.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.498 fault_confinement_fsm_rx_err_ctr_mt_ewl

Auto-extracted signal rx_err_ctr_mt_ewl from fault_confinement_fsm.vhd - Offset: `0x624` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.498.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.499 fault_confinement_fsm_tx_err_ctr_mt_255

Auto-extracted signal tx_err_ctr_mt_255 from fault_confinement_fsm.vhd - Offset: `0x628` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.499.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.500 fault_confinement_fsm_err_warning_limit_d

Auto-extracted signal err_warning_limit_d from fault_confinement_fsm.vhd - Offset: `0x62c` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.500.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.501 fault_confinement_fsm_err_warning_limit_q

Auto-extracted signal err_warning_limit_q from fault_confinement_fsm.vhd - Offset: `0x630` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.501.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.502 fault_confinement_fsm_fc_fsm_res_d

Auto-extracted signal fc_fsm_res_d from fault_confinement_fsm.vhd - Offset: `0x634` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.502.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.503 fault_confinement_fsm_fc_fsm_res_q

Auto-extracted signal fc_fsm_res_q from fault_confinement_fsm.vhd - Offset: `0x638` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.503.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.504 fault_confinement_rules_inc_one_i

Auto-extracted signal inc_one_i from fault_confinement_rules.vhd - Offset: `0x63c` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.504.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.505 fault_confinement_rules_inc_eight_i

Auto-extracted signal inc_eight_i from fault_confinement_rules.vhd - Offset: `0x640` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.505.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.506 frame_filters_drv_filter_A_mask

Auto-extracted signal drv_filter_A_mask from frame_filters.vhd - Offset: `0x644` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.506.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.507 frame_filters_drv_filter_A_ctrl

Auto-extracted signal drv_filter_A_ctrl from frame_filters.vhd - Offset: `0x648` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.507.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.508 frame_filters_drv_filter_A_bits

Auto-extracted signal drv_filter_A_bits from frame_filters.vhd - Offset: `0x64c` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.508.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.509 frame_filters_int_filter_A_valid

Auto-extracted signal int_filter_A_valid from frame_filters.vhd - Offset: `0x650` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.509.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.510 frame_filters_drv_filter_B_mask

Auto-extracted signal drv_filter_B_mask from frame_filters.vhd - Offset: `0x654` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.510.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.511 frame_filters_drv_filter_B_ctrl

Auto-extracted signal drv_filter_B_ctrl from frame_filters.vhd - Offset: `0x658` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.511.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.512 frame_filters_drv_filter_B_bits

Auto-extracted signal drv_filter_B_bits from frame_filters.vhd - Offset: `0x65c` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.512.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.513 frame_filters_int_filter_B_valid

Auto-extracted signal int_filter_B_valid from frame_filters.vhd - Offset: `0x660` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.513.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.514 frame_filters_drv_filter_C_mask

Auto-extracted signal drv_filter_C_mask from frame_filters.vhd - Offset: `0x664` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.514.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.515 frame_filters_drv_filter_C_ctrl

Auto-extracted signal drv_filter_C_ctrl from frame_filters.vhd - Offset: `0x668` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.515.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.516 frame_filters_drv_filter_C_bits

Auto-extracted signal drv_filter_C_bits from frame_filters.vhd - Offset: `0x66c` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.516.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.517 frame_filters_int_filter_C_valid

Auto-extracted signal int_filter_C_valid from frame_filters.vhd - Offset: `0x670` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.517.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.518 frame_filters_drv_filter_ran_ctrl

Auto-extracted signal drv_filter_ran_ctrl from frame_filters.vhd - Offset: `0x674` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.518.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.519 frame_filters_drv_filter_ran_lo_th

Auto-extracted signal drv_filter_ran_lo_th from frame_filters.vhd - Offset: `0x678` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.519.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.520 frame_filters_drv_filter_ran_hi_th

Auto-extracted signal drv_filter_ran_hi_th from frame_filters.vhd - Offset: `0x67c` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.520.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.521 frame_filters_int_filter_ran_valid

Auto-extracted signal int_filter_ran_valid from frame_filters.vhd - Offset: `0x680` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.521.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.522 frame_filters_drv_filters_ena

Auto-extracted signal drv_filters_ena from frame_filters.vhd - Offset: `0x684` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.522.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.523 frame_filters_int_data_type

Auto-extracted signal int_data_type from frame_filters.vhd - Offset: `0x688` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.523.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.524 frame_filters_int_data_ctrl

Auto-extracted signal int_data_ctrl from frame_filters.vhd - Offset: `0x68c` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.524.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.525 frame_filters_filter_A_enable

Auto-extracted signal filter_A_enable from frame_filters.vhd - Offset: `0x690` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.525.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.526 frame_filters_filter_B_enable

Auto-extracted signal filter_B_enable from frame_filters.vhd - Offset: `0x694` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.526.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.527 frame_filters_filter_C_enable

Auto-extracted signal filter_C_enable from frame_filters.vhd - Offset: `0x698` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.527.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.528 frame_filters_filter_range_enable

Auto-extracted signal filter_range_enable from frame_filters.vhd - Offset: `0x69c` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.528.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.529 frame_filters_filter_result

Auto-extracted signal filter_result from frame_filters.vhd - Offset: `0x6a0` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.529.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.530 frame_filters_ident_valid_d

Auto-extracted signal ident_valid_d from frame_filters.vhd - Offset: `0x6a4` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.530.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.531 frame_filters_ident_valid_q

Auto-extracted signal ident_valid_q from frame_filters.vhd - Offset: `0x6a8` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.531.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.532 frame_filters_drv_drop_remote_frames

Auto-extracted signal drv_drop_remote_frames from frame_filters.vhd - Offset: `0x6ac` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.532.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.533 frame_filters_drop_rtr_frame

Auto-extracted signal drop_rtr_frame from frame_filters.vhd - Offset: `0x6b0` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.533.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.534 inf_ram_wrapper_int_read_data

Auto-extracted signal int_read_data from inf_ram_wrapper.vhd - Offset: `0x6b4` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.534.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.535 inf_ram_wrapper_byte_we

Auto-extracted signal byte_we from inf_ram_wrapper.vhd - Offset: `0x6b8` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.535.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.536 int_manager_drv_int_vect_clr

Auto-extracted signal drv_int_vect_clr from int_manager.vhd - Offset: `0x6bc` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.536.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.537 int_manager_drv_int_ena_set

Auto-extracted signal drv_int_ena_set from int_manager.vhd - Offset: `0x6c0` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.537.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.538 int_manager_drv_int_ena_clr

Auto-extracted signal drv_int_ena_clr from int_manager.vhd - Offset: `0x6c4` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.538.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.539 int_manager_drv_int_mask_set

Auto-extracted signal drv_int_mask_set from int_manager.vhd - Offset: `0x6c8` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.539.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.540 int_manager_drv_int_mask_clr

Auto-extracted signal drv_int_mask_clr from int_manager.vhd - Offset: `0x6cc` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.540.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.541 int_manager_int_ena_i

Auto-extracted signal int_ena_i from int_manager.vhd - Offset: `0x6d0` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.541.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.542 int_manager_int_mask_i

Auto-extracted signal int_mask_i from int_manager.vhd - Offset: `0x6d4` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.542.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.543 int_manager_int_vect_i

Auto-extracted signal int_vect_i from int_manager.vhd - Offset: `0x6d8` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.543.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.544 int_manager_int_input_active

Auto-extracted signal int_input_active from int_manager.vhd - Offset: `0x6dc` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.544.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.545 int_manager_int_i

Auto-extracted signal int_i from int_manager.vhd - Offset: `0x6e0` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.545.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.546 int_module_int_mask_i

Auto-extracted signal int_mask_i from int_module.vhd - Offset: `0x6e4` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.546.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.547 int_module_int_ena_i

Auto-extracted signal int_ena_i from int_module.vhd - Offset: `0x6e8` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.547.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.548 int_module_int_mask_load

Auto-extracted signal int_mask_load from int_module.vhd - Offset: `0x6ec` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.548.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.549 int_module_int_mask_next

Auto-extracted signal int_mask_next from int_module.vhd - Offset: `0x6f0` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.549.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.550 memory_reg_reg_value_r

Auto-extracted signal reg_value_r from memory_reg.vhd - Offset: `0x6f4` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.550.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.551 memory_reg_wr_select

Auto-extracted signal wr_select from memory_reg.vhd - Offset: `0x6f8` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.551.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.552 memory_reg_wr_select_expanded

Auto-extracted signal wr_select_expanded from memory_reg.vhd - Offset: `0x6fc` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.552.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.553 memory_registers_status_comb

Auto-extracted signal status_comb from memory_registers.vhd - Offset: `0x700` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.553.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.554 memory_registers_can_core_cs

Auto-extracted signal can_core_cs from memory_registers.vhd - Offset: `0x704` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.554.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.555 memory_registers_control_registers_cs

Auto-extracted signal control_registers_cs from memory_registers.vhd - Offset: `0x708` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.555.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.556 memory_registers_control_registers_cs_reg

Auto-extracted signal control_registers_cs_reg from memory_registers.vhd - Offset: `0x70c` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.556.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.557 memory_registers_test_registers_cs

Auto-extracted signal test_registers_cs from memory_registers.vhd - Offset: `0x710` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.557.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.558 memory_registers_test_registers_cs_reg

Auto-extracted signal test_registers_cs_reg from memory_registers.vhd - Offset: `0x714` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.558.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.559 memory_registers_control_registers_rdata

Auto-extracted signal control_registers_rdata from memory_registers.vhd - Offset: `0x718` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.559.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.560 memory_registers_test_registers_rdata

Auto-extracted signal test_registers_rdata from memory_registers.vhd - Offset: `0x71c` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.560.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.561 memory_registers_is_err_active

Auto-extracted signal is_err_active from memory_registers.vhd - Offset: `0x720` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.561.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.562 memory_registers_is_err_passive

Auto-extracted signal is_err_passive from memory_registers.vhd - Offset: `0x724` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.562.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.563 memory_registers_is_bus_off

Auto-extracted signal is_bus_off from memory_registers.vhd - Offset: `0x728` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.563.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.564 memory_registers_is_transmitter

Auto-extracted signal is_transmitter from memory_registers.vhd - Offset: `0x72c` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.564.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.565 memory_registers_is_receiver

Auto-extracted signal is_receiver from memory_registers.vhd - Offset: `0x730` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.565.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.566 memory_registers_is_idle

Auto-extracted signal is_idle from memory_registers.vhd - Offset: `0x734` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.566.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.567 memory_registers_reg_lock_1_active

Auto-extracted signal reg_lock_1_active from memory_registers.vhd - Offset: `0x738` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.567.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.568 memory_registers_reg_lock_2_active

Auto-extracted signal reg_lock_2_active from memory_registers.vhd - Offset: `0x73c` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.568.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.569 memory_registers_soft_res_q_n

Auto-extracted signal soft_res_q_n from memory_registers.vhd - Offset: `0x740` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.569.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.570 memory_registers_ewl_padded

Auto-extracted signal ewl_padded from memory_registers.vhd - Offset: `0x744` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.570.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.571 memory_registers_control_regs_clk_en

Auto-extracted signal control_regs_clk_en from memory_registers.vhd - Offset: `0x748` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.571.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.572 memory_registers_test_regs_clk_en

Auto-extracted signal test_regs_clk_en from memory_registers.vhd - Offset: `0x74c` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.572.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.573 memory_registers_clk_control_regs

Auto-extracted signal clk_control_regs from memory_registers.vhd - Offset: `0x750` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.573.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.574 memory_registers_clk_test_regs

Auto-extracted signal clk_test_regs from memory_registers.vhd - Offset: `0x754` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.574.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.575 memory_registers_rx_buf_mode

Auto-extracted signal rx_buf_mode from memory_registers.vhd - Offset: `0x758` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.575.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.576 memory_registers_rx_move_cmd

Auto-extracted signal rx_move_cmd from memory_registers.vhd - Offset: `0x75c` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.576.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.577 memory_registers_ctr_pres_sel_q

Auto-extracted signal ctr_pres_sel_q from memory_registers.vhd - Offset: `0x760` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.577.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.578 operation_control_drv_ena

Auto-extracted signal drv_ena from operation_control.vhd - Offset: `0x764` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.578.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.579 operation_control_go_to_off

Auto-extracted signal go_to_off from operation_control.vhd - Offset: `0x768` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.579.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.580 prescaler_drv_ena

Auto-extracted signal drv_ena from prescaler.vhd - Offset: `0x76c` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.580.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.581 prescaler_tseg1_nbt

Auto-extracted signal tseg1_nbt from prescaler.vhd - Offset: `0x770` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.581.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.582 prescaler_tseg2_nbt

Auto-extracted signal tseg2_nbt from prescaler.vhd - Offset: `0x774` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.582.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.583 prescaler_brp_nbt

Auto-extracted signal brp_nbt from prescaler.vhd - Offset: `0x778` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.583.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.584 prescaler_sjw_nbt

Auto-extracted signal sjw_nbt from prescaler.vhd - Offset: `0x77c` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.584.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.585 prescaler_tseg1_dbt

Auto-extracted signal tseg1_dbt from prescaler.vhd - Offset: `0x780` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.585.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.586 prescaler_tseg2_dbt

Auto-extracted signal tseg2_dbt from prescaler.vhd - Offset: `0x784` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.586.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.587 prescaler_brp_dbt

Auto-extracted signal brp_dbt from prescaler.vhd - Offset: `0x788` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.587.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.588 prescaler_sjw_dbt

Auto-extracted signal sjw_dbt from prescaler.vhd - Offset: `0x78c` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.588.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.589 prescaler_segment_end

Auto-extracted signal segment_end from prescaler.vhd - Offset: `0x790` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.589.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.590 prescaler_h_sync_valid

Auto-extracted signal h_sync_valid from prescaler.vhd - Offset: `0x794` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.590.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.591 prescaler__is__tseg1

Auto-extracted signal is_tseg1 from prescaler.vhd - Offset: `0x798` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.591.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.592 prescaler__is__tseg2

Auto-extracted signal is_tseg2 from prescaler.vhd - Offset: `0x79c` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.592.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.593 prescaler__resync__edge__valid

Auto-extracted signal resync__edge__valid from prescaler.vhd - Offset: `0x7a0` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.593.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.594 prescaler__h_sync_edge_valid

Auto-extracted signal h_sync_edge_valid from prescaler.vhd - Offset: `0x7a4` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.594.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.595 prescaler__segm_counter__nbt

Auto-extracted signal segm_counter_nbt from prescaler.vhd - Offset: `0x7a8` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.595.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.596 prescaler__segm_counter__dbt

Auto-extracted signal segm_counter_dbt from prescaler.vhd - Offset: `0x7ac` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.596.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.597 prescaler__exit__segm__req__nbt

Auto-extracted signal exit__segm__req__nbt from prescaler.vhd - Offset: `0x7b0` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.597.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.598 prescaler__exit__segm__req__dbt

Auto-extracted signal exit__segm__req__dbt from prescaler.vhd - Offset: `0x7b4` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.598.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.599 prescaler__tq__edge__nbt

Auto-extracted signal tq__edge__nbt from prescaler.vhd - Offset: `0x7b8` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.599.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.600 prescaler_tq_edge_dbt

Auto-extracted signal tq_edge_dbt from prescaler.vhd - Offset: `0x7bc` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.600.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.601 prescaler_rx_trig_req

Auto-extracted signal rx_trig_req from prescaler.vhd - Offset: `0x7c0` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.601.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.602 prescaler_tx_trig_req

Auto-extracted signal tx_trig_req from prescaler.vhd - Offset: `0x7c4` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.602.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.603 prescaler_start_edge

Auto-extracted signal start_edge from prescaler.vhd - Offset: `0x7c8` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.603.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.604 prescaler_bt_ctr_clear

Auto-extracted signal bt_ctr_clear from prescaler.vhd - Offset: `0x7cc` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.604.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.605 priority_decoder_l0_valid

Auto-extracted signal l0_valid from priority_decoder.vhd - Offset: `0x7d0` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.605.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.606 priority_decoder_l1_valid

Auto-extracted signal l1_valid from priority_decoder.vhd - Offset: `0x7d4` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.606.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.607 priority_decoder_l1_winner

Auto-extracted signal l1_winner from priority_decoder.vhd - Offset: `0x7d8` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.607.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.608 priority_decoder_l2_valid

Auto-extracted signal l2_valid from priority_decoder.vhd - Offset: `0x7dc` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.608.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.609 priority_decoder_l2_winner

Auto-extracted signal l2_winner from priority_decoder.vhd - Offset: `0x7e0` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.609.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.610 priority_decoder_l3_valid

Auto-extracted signal l3_valid from priority_decoder.vhd - Offset: `0x7e4` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.610.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.611 priority_decoder_l3_winner

Auto-extracted signal l3_winner from priority_decoder.vhd - Offset: `0x7e8` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.611.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.612 protocol_control_drv_can_fd_ena

Auto-extracted signal drv_can_fd_ena from protocol_control.vhd - Offset: `0x7ec` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.612.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.613 protocol_control_drv_bus_mon_ena

Auto-extracted signal drv_bus_mon_ena from protocol_control.vhd - Offset: `0x7f0` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.613.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.614 protocol_control_drv_retr_lim_ena

Auto-extracted signal drv_retr_lim_ena from protocol_control.vhd - Offset: `0x7f4` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.614.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.615 protocol_control_drv_retr_th

Auto-extracted signal drv_retr_th from protocol_control.vhd - Offset: `0x7f8` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.615.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.616 protocol_control_drv_self_test_ena

Auto-extracted signal drv_self_test_ena from protocol_control.vhd - Offset: `0x7fc` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.616.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.617 protocol_control_drv_ack_forb

Auto-extracted signal drv_ack_forb from protocol_control.vhd - Offset: `0x800` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.617.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.618 protocol_control_drv_ena

Auto-extracted signal drv_ena from protocol_control.vhd - Offset: `0x804` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.618.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.619 protocol_control_drv_fd_type

Auto-extracted signal drv_fd_type from protocol_control.vhd - Offset: `0x808` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.619.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.620 protocol_control_drv_int_loopback_ena

Auto-extracted signal drv_int_loopback_ena from protocol_control.vhd - Offset: `0x80c` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.620.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.621 protocol_control_drv_bus_off_reset

Auto-extracted signal drv_bus_off_reset from protocol_control.vhd - Offset: `0x810` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.621.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.622 protocol_control_drv_ssp_delay_select

Auto-extracted signal drv_ssp_delay_select from protocol_control.vhd - Offset: `0x814` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.622.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.623 protocol_control_drv_pex

Auto-extracted signal drv_pex from protocol_control.vhd - Offset: `0x818` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.623.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.624 protocol_control_drv_cpexs

Auto-extracted signal drv_cpexs from protocol_control.vhd - Offset: `0x81c` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.624.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.625 protocol_control_tran_word_swapped

Auto-extracted signal tran_word_swapped from protocol_control.vhd - Offset: `0x820` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.625.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.626 protocol_control_err_frm_req

Auto-extracted signal err_frm_req from protocol_control.vhd - Offset: `0x824` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.626.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.627 protocol_control_tx_load_base_id

Auto-extracted signal tx_load_base_id from protocol_control.vhd - Offset: `0x828` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.627.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.628 protocol_control_tx_load_ext_id

Auto-extracted signal tx_load_ext_id from protocol_control.vhd - Offset: `0x82c` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.628.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.629 protocol_control_tx_load_dlc

Auto-extracted signal tx_load_dlc from protocol_control.vhd - Offset: `0x830` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.629.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.630 protocol_control_tx_load_data_word

Auto-extracted signal tx_load_data_word from protocol_control.vhd - Offset: `0x834` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.630.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.631 protocol_control_tx_load_stuff_count

Auto-extracted signal tx_load_stuff_count from protocol_control.vhd - Offset: `0x838` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.631.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.632 protocol_control_tx_load_crc

Auto-extracted signal tx_load_crc from protocol_control.vhd - Offset: `0x83c` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.632.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.633 protocol_control_tx_shift_ena

Auto-extracted signal tx_shift_ena from protocol_control.vhd - Offset: `0x840` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.633.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.634 protocol_control_tx_dominant

Auto-extracted signal tx_dominant from protocol_control.vhd - Offset: `0x844` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.634.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.635 protocol_control_rx_clear

Auto-extracted signal rx_clear from protocol_control.vhd - Offset: `0x848` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.635.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.636 protocol_control_rx_store_base_id

Auto-extracted signal rx_store_base_id from protocol_control.vhd - Offset: `0x84c` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.636.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.637 protocol_control_rx_store_ext_id

Auto-extracted signal rx_store_ext_id from protocol_control.vhd - Offset: `0x850` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.637.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.638 protocol_control_rx_store_ide

Auto-extracted signal rx_store_ide from protocol_control.vhd - Offset: `0x854` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.638.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.639 protocol_control_rx_store_rtr

Auto-extracted signal rx_store_rtr from protocol_control.vhd - Offset: `0x858` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.639.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.640 protocol_control_rx_store_edl

Auto-extracted signal rx_store_edl from protocol_control.vhd - Offset: `0x85c` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.640.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.641 protocol_control_rx_store_dlc

Auto-extracted signal rx_store_dlc from protocol_control.vhd - Offset: `0x860` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.641.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.642 protocol_control_rx_store_esi

Auto-extracted signal rx_store_esi from protocol_control.vhd - Offset: `0x864` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.642.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.643 protocol_control_rx_store_brs

Auto-extracted signal rx_store_brs from protocol_control.vhd - Offset: `0x868` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.643.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.644 protocol_control_rx_store_stuff_count

Auto-extracted signal rx_store_stuff_count from protocol_control.vhd - Offset: `0x86c` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.644.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.645 protocol_control_rx_shift_ena

Auto-extracted signal rx_shift_ena from protocol_control.vhd - Offset: `0x870` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.645.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.646 protocol_control_rx_shift_in_sel

Auto-extracted signal rx_shift_in_sel from protocol_control.vhd - Offset: `0x874` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.646.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.647 protocol_control_rec_is_rtr_i

Auto-extracted signal rec_is_rtr_i from protocol_control.vhd - Offset: `0x878` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.647.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.648 protocol_control_rec_dlc_d

Auto-extracted signal rec_dlc_d from protocol_control.vhd - Offset: `0x87c` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.648.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.649 protocol_control_rec_dlc_q

Auto-extracted signal rec_dlc_q from protocol_control.vhd - Offset: `0x880` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.649.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.650 protocol_control_rec_frame_type_i

Auto-extracted signal rec_frame_type_i from protocol_control.vhd - Offset: `0x884` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.650.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.651 protocol_control_ctrl_ctr_pload

Auto-extracted signal ctrl_ctr_pload from protocol_control.vhd - Offset: `0x888` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.651.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.652 protocol_control_ctrl_ctr_pload_val

Auto-extracted signal ctrl_ctr_pload_val from protocol_control.vhd - Offset: `0x88c` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.652.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.653 protocol_control_ctrl_ctr_ena

Auto-extracted signal ctrl_ctr_ena from protocol_control.vhd - Offset: `0x890` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.653.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.654 protocol_control_ctrl_ctr_zero

Auto-extracted signal ctrl_ctr_zero from protocol_control.vhd - Offset: `0x894` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.654.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.655 protocol_control_ctrl_ctr_one

Auto-extracted signal ctrl_ctr_one from protocol_control.vhd - Offset: `0x898` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.655.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.656 protocol_control_ctrl_counted_byte

Auto-extracted signal ctrl_counted_byte from protocol_control.vhd - Offset: `0x89c` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.656.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.657 protocol_control_ctrl_counted_byte_index

Auto-extracted signal ctrl_counted_byte_index from protocol_control.vhd - Offset: `0x8a0` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.657.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.658 protocol_control_ctrl_ctr_mem_index

Auto-extracted signal ctrl_ctr_mem_index from protocol_control.vhd - Offset: `0x8a4` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.658.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.659 protocol_control_compl_ctr_ena

Auto-extracted signal compl_ctr_ena from protocol_control.vhd - Offset: `0x8a8` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.659.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.660 protocol_control_reinteg_ctr_clr

Auto-extracted signal reinteg_ctr_clr from protocol_control.vhd - Offset: `0x8ac` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.660.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.661 protocol_control_reinteg_ctr_enable

Auto-extracted signal reinteg_ctr_enable from protocol_control.vhd - Offset: `0x8b0` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.661.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.662 protocol_control_reinteg_ctr_expired

Auto-extracted signal reinteg_ctr_expired from protocol_control.vhd - Offset: `0x8b4` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.662.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.663 protocol_control_retr_ctr_clear

Auto-extracted signal retr_ctr_clear from protocol_control.vhd - Offset: `0x8b8` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.663.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.664 protocol_control_retr_ctr_add

Auto-extracted signal retr_ctr_add from protocol_control.vhd - Offset: `0x8bc` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.664.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.665 protocol_control_retr_limit_reached

Auto-extracted signal retr_limit_reached from protocol_control.vhd - Offset: `0x8c0` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.665.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.666 protocol_control_form_err_i

Auto-extracted signal form_err_i from protocol_control.vhd - Offset: `0x8c4` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.666.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.667 protocol_control_ack_err_i

Auto-extracted signal ack_err_i from protocol_control.vhd - Offset: `0x8c8` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.667.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.668 protocol_control_crc_check

Auto-extracted signal crc_check from protocol_control.vhd - Offset: `0x8cc` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.668.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.669 protocol_control_bit_err_arb

Auto-extracted signal bit_err_arb from protocol_control.vhd - Offset: `0x8d0` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.669.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.670 protocol_control_crc_match

Auto-extracted signal crc_match from protocol_control.vhd - Offset: `0x8d4` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.670.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.671 protocol_control_crc_err_i

Auto-extracted signal crc_err_i from protocol_control.vhd - Offset: `0x8d8` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.671.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.672 protocol_control_crc_clear_match_flag

Auto-extracted signal crc_clear_match_flag from protocol_control.vhd - Offset: `0x8dc` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.672.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.673 protocol_control_crc_src

Auto-extracted signal crc_src from protocol_control.vhd - Offset: `0x8e0` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.673.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.674 protocol_control_err_pos

Auto-extracted signal err_pos from protocol_control.vhd - Offset: `0x8e4` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.674.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.675 protocol_control_is_arbitration_i

Auto-extracted signal is_arbitration_i from protocol_control.vhd - Offset: `0x8e8` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.675.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.676 protocol_control_bit_err_enable

Auto-extracted signal bit_err_enable from protocol_control.vhd - Offset: `0x8ec` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.676.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.677 protocol_control_tx_data_nbs_i

Auto-extracted signal tx_data_nbs_i from protocol_control.vhd - Offset: `0x8f0` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.677.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.678 protocol_control_rx_crc

Auto-extracted signal rx_crc from protocol_control.vhd - Offset: `0x8f4` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.678.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.679 protocol_control_rx_stuff_count

Auto-extracted signal rx_stuff_count from protocol_control.vhd - Offset: `0x8f8` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.679.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.680 protocol_control_fixed_stuff_i

Auto-extracted signal fixed_stuff_i from protocol_control.vhd - Offset: `0x8fc` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.680.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.681 protocol_control_arbitration_lost_i

Auto-extracted signal arbitration_lost_i from protocol_control.vhd - Offset: `0x900` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.681.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.682 protocol_control_alc_id_field

Auto-extracted signal alc_id_field from protocol_control.vhd - Offset: `0x904` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.682.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.683 protocol_control_drv_rom_ena

Auto-extracted signal drv_rom_ena from protocol_control.vhd - Offset: `0x908` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.683.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.684 protocol_control_fsm_state_reg_ce

Auto-extracted signal state_reg_ce from protocol_control_fsm.vhd - Offset: `0x90c` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.684.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.685 protocol_control_fsm_no_data_transmitter

Auto-extracted signal no_data_transmitter from protocol_control_fsm.vhd - Offset: `0x910` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.685.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.686 protocol_control_fsm_no_data_receiver

Auto-extracted signal no_data_receiver from protocol_control_fsm.vhd - Offset: `0x914` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.686.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.687 protocol_control_fsm_no_data_field

Auto-extracted signal no_data_field from protocol_control_fsm.vhd - Offset: `0x918` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.687.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.688 protocol_control_fsm_ctrl_ctr_pload_i

Auto-extracted signal ctrl_ctr_pload_i from protocol_control_fsm.vhd - Offset: `0x91c` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.688.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.689 protocol_control_fsm_ctrl_ctr_pload_unaliged

Auto-extracted signal ctrl_ctr_pload_unaliged from protocol_control_fsm.vhd - Offset: `0x920` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.689.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.690 protocol_control_fsm_crc_use_21

Auto-extracted signal crc_use_21 from protocol_control_fsm.vhd - Offset: `0x924` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.690.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.691 protocol_control_fsm_crc_use_17

Auto-extracted signal crc_use_17 from protocol_control_fsm.vhd - Offset: `0x928` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.691.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.692 protocol_control_fsm_crc_src_i

Auto-extracted signal crc_src_i from protocol_control_fsm.vhd - Offset: `0x92c` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.692.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.693 protocol_control_fsm_crc_length_i

Auto-extracted signal crc_length_i from protocol_control_fsm.vhd - Offset: `0x930` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.693.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.694 protocol_control_fsm_tran_data_length

Auto-extracted signal tran_data_length from protocol_control_fsm.vhd - Offset: `0x934` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.694.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.695 protocol_control_fsm_rec_data_length

Auto-extracted signal rec_data_length from protocol_control_fsm.vhd - Offset: `0x938` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.695.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.696 protocol_control_fsm_rec_data_length_c

Auto-extracted signal rec_data_length_c from protocol_control_fsm.vhd - Offset: `0x93c` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.696.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.697 protocol_control_fsm_data_length_c

Auto-extracted signal data_length_c from protocol_control_fsm.vhd - Offset: `0x940` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.697.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.698 protocol_control_fsm_data_length_shifted_c

Auto-extracted signal data_length_shifted_c from protocol_control_fsm.vhd - Offset: `0x944` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.698.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.699 protocol_control_fsm_data_length_bits_c

Auto-extracted signal data_length_bits_c from protocol_control_fsm.vhd - Offset: `0x948` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.699.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.700 protocol_control_fsm_is_fd_frame

Auto-extracted signal is_fd_frame from protocol_control_fsm.vhd - Offset: `0x94c` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.700.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.701 protocol_control_fsm_frame_start

Auto-extracted signal frame_start from protocol_control_fsm.vhd - Offset: `0x950` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.701.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.702 protocol_control_fsm_tx_frame_ready

Auto-extracted signal tx_frame_ready from protocol_control_fsm.vhd - Offset: `0x954` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.702.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.703 protocol_control_fsm_ide_is_arbitration

Auto-extracted signal ide_is_arbitration from protocol_control_fsm.vhd - Offset: `0x958` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.703.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.704 protocol_control_fsm_arbitration_lost_condition

Auto-extracted signal arbitration_lost_condition from protocol_control_fsm.vhd - Offset: `0x95c` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.704.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.705 protocol_control_fsm_arbitration_lost_i

Auto-extracted signal arbitration_lost_i from protocol_control_fsm.vhd - Offset: `0x960` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.705.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.706 protocol_control_fsm_tx_failed

Auto-extracted signal tx_failed from protocol_control_fsm.vhd - Offset: `0x964` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.706.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.707 protocol_control_fsm_store_metadata_d

Auto-extracted signal store_metadata_d from protocol_control_fsm.vhd - Offset: `0x968` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.707.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.708 protocol_control_fsm_store_data_d

Auto-extracted signal store_data_d from protocol_control_fsm.vhd - Offset: `0x96c` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.708.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.709 protocol_control_fsm_rec_valid_d

Auto-extracted signal rec_valid_d from protocol_control_fsm.vhd - Offset: `0x970` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.709.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.710 protocol_control_fsm_rec_abort_d

Auto-extracted signal rec_abort_d from protocol_control_fsm.vhd - Offset: `0x974` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.710.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.711 protocol_control_fsm_go_to_suspend

Auto-extracted signal go_to_suspend from protocol_control_fsm.vhd - Offset: `0x978` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.711.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.712 protocol_control_fsm_go_to_stuff_count

Auto-extracted signal go_to_stuff_count from protocol_control_fsm.vhd - Offset: `0x97c` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.712.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.713 protocol_control_fsm_rx_store_base_id_i

Auto-extracted signal rx_store_base_id_i from protocol_control_fsm.vhd - Offset: `0x980` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.713.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.714 protocol_control_fsm_rx_store_ext_id_i

Auto-extracted signal rx_store_ext_id_i from protocol_control_fsm.vhd - Offset: `0x984` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.714.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.715 protocol_control_fsm_rx_store_ide_i

Auto-extracted signal rx_store_ide_i from protocol_control_fsm.vhd - Offset: `0x988` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.715.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.716 protocol_control_fsm_rx_store_rtr_i

Auto-extracted signal rx_store_rtr_i from protocol_control_fsm.vhd - Offset: `0x98c` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.716.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.717 protocol_control_fsm_rx_store_edl_i

Auto-extracted signal rx_store_edl_i from protocol_control_fsm.vhd - Offset: `0x990` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.717.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.718 protocol_control_fsm_rx_store_dlc_i

Auto-extracted signal rx_store_dlc_i from protocol_control_fsm.vhd - Offset: `0x994` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.718.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.719 protocol_control_fsm_rx_store_esi_i

Auto-extracted signal rx_store_esi_i from protocol_control_fsm.vhd - Offset: `0x998` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.719.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.720 protocol_control_fsm_rx_store_brs_i

Auto-extracted signal rx_store_brs_i from protocol_control_fsm.vhd - Offset: `0x99c` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.720.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.721 protocol_control_fsm_rx_store_stuff_count_i

Auto-extracted signal rx_store_stuff_count_i from protocol_control_fsm.vhd - Offset: `0x9a0` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.721.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.722 protocol_control_fsm_rx_clear_i

Auto-extracted signal rx_clear_i from protocol_control_fsm.vhd - Offset: `0x9a4` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.722.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.723 protocol_control_fsm_tx_load_base_id_i

Auto-extracted signal tx_load_base_id_i from protocol_control_fsm.vhd - Offset: `0x9a8` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.723.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.724 protocol_control_fsm_tx_load_ext_id_i

Auto-extracted signal tx_load_ext_id_i from protocol_control_fsm.vhd - Offset: `0x9ac` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.724.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.725 protocol_control_fsm_tx_load_dlc_i

Auto-extracted signal tx_load_dlc_i from protocol_control_fsm.vhd - Offset: `0x9b0` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.725.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.726 protocol_control_fsm_tx_load_data_word_i

Auto-extracted signal tx_load_data_word_i from protocol_control_fsm.vhd - Offset: `0x9b4` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.726.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.727 protocol_control_fsm_tx_load_stuff_count_i

Auto-extracted signal tx_load_stuff_count_i from protocol_control_fsm.vhd - Offset: `0x9b8` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.727.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.728 protocol_control_fsm_tx_load_crc_i

Auto-extracted signal tx_load_crc_i from protocol_control_fsm.vhd - Offset: `0x9bc` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.728.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.729 protocol_control_fsm_tx_shift_ena_i

Auto-extracted signal tx_shift_ena_i from protocol_control_fsm.vhd - Offset: `0x9c0` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.729.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.730 protocol_control_fsm_form_err_i

Auto-extracted signal form_err_i from protocol_control_fsm.vhd - Offset: `0x9c4` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.730.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.731 protocol_control_fsm_ack_err_i

Auto-extracted signal ack_err_i from protocol_control_fsm.vhd - Offset: `0x9c8` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.731.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.732 protocol_control_fsm_ack_err_flag

Auto-extracted signal ack_err_flag from protocol_control_fsm.vhd - Offset: `0x9cc` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.732.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.733 protocol_control_fsm_ack_err_flag_clr

Auto-extracted signal ack_err_flag_clr from protocol_control_fsm.vhd - Offset: `0x9d0` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.733.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.734 protocol_control_fsm_crc_err_i

Auto-extracted signal crc_err_i from protocol_control_fsm.vhd - Offset: `0x9d4` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.734.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.735 protocol_control_fsm_bit_err_arb_i

Auto-extracted signal bit_err_arb_i from protocol_control_fsm.vhd - Offset: `0x9d8` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.735.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.736 protocol_control_fsm_sp_control_switch_data

Auto-extracted signal sp_control_switch_data from protocol_control_fsm.vhd - Offset: `0x9dc` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.736.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.737 protocol_control_fsm_sp_control_switch_nominal

Auto-extracted signal sp_control_switch_nominal from protocol_control_fsm.vhd - Offset: `0x9e0` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.737.1 Fields

```
{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "
```

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.738 protocol_control_fsm_switch_to_ssp

Auto-extracted signal switch_to_ssp from protocol_control_fsm.vhd - Offset: `0x9e4` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.738.1 Fields

```
{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "
```

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.739 protocol_control_fsm_sp_control_ce

Auto-extracted signal sp_control_ce from protocol_control_fsm.vhd - Offset: `0x9e8` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.739.1 Fields

```
{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "
```

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.740 protocol_control_fsm_sp_control_d

Auto-extracted signal sp_control_d from protocol_control_fsm.vhd - Offset: `0x9ec` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.740.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.741 protocol_control_fsm_sp_control_q_i

Auto-extracted signal sp_control_q_i from protocol_control_fsm.vhd - Offset: `0x9f0` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.741.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.742 protocol_control_fsm_ssp_reset_i

Auto-extracted signal ssp_reset_i from protocol_control_fsm.vhd - Offset: `0x9f4` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.742.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.743 protocol_control_fsm_sync_control_d

Auto-extracted signal sync_control_d from protocol_control_fsm.vhd - Offset: `0x9f8` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.743.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.744 protocol_control_fsm_sync_control_q

Auto-extracted signal sync_control_q from protocol_control_fsm.vhd - Offset: `0x9fc` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.744.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.745 protocol_control_fsm_perform_hsync

Auto-extracted signal perform_hsync from protocol_control_fsm.vhd - Offset: `0xa00` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.745.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.746 protocol_control_fsm_primary_err_i

Auto-extracted signal primary_err_i from protocol_control_fsm.vhd - Offset: `0xa04` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.746.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.747 protocol_control_fsm_err_delim_late_i

Auto-extracted signal err_delim_late_i from protocol_control_fsm.vhd - Offset: `0xa08` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.747.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.748 protocol_control_fsm_set_err_active_i

Auto-extracted signal set_err_active_i from protocol_control_fsm.vhd - Offset: `0xa0c` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.748.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.749 protocol_control_fsm_set_transmitter_i

Auto-extracted signal set_transmitter_i from protocol_control_fsm.vhd - Offset: `0xa10` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.749.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.750 protocol_control_fsm_set_receiver_i

Auto-extracted signal set_receiver_i from protocol_control_fsm.vhd - Offset: `0xa14` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.750.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.751 protocol_control_fsm_set_idle_i

Auto-extracted signal set_idle_i from protocol_control_fsm.vhd - Offset: `0xa18` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.751.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.752 protocol_control_fsm_first_err_delim_d

Auto-extracted signal first_err_delim_d from protocol_control_fsm.vhd - Offset: `0xa1c` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.752.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.753 protocol_control_fsm_first_err_delim_q

Auto-extracted signal first_err_delim_q from protocol_control_fsm.vhd - Offset: `0xa20` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.753.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.754 protocol_control_fsm_stuff_enable_set

Auto-extracted signal stuff_enable_set from protocol_control_fsm.vhd - Offset: `0xa24` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.754.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.755 protocol_control_fsm_stuff_enable_clear

Auto-extracted signal stuff_enable_clear from protocol_control_fsm.vhd - Offset: `0xa28` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.755.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.756 protocol_control_fsm_destuff_enable_set

Auto-extracted signal destuff_enable_set from protocol_control_fsm.vhd - Offset: `0xa2c` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.756.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.757 protocol_control_fsm_destuff_enable_clear

Auto-extracted signal destuff_enable_clear from protocol_control_fsm.vhd - Offset: `0xa30` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.757.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.758 protocol_control_fsm_bit_err_disable

Auto-extracted signal bit_err_disable from protocol_control_fsm.vhd - Offset: `0xa34` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.758.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.759 protocol_control_fsm_bit_err_disable_receiver

Auto-extracted signal bit_err_disable_receiver from protocol_control_fsm.vhd - Offset: `0xa38` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.759.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.760 protocol_control_fsm_sof_pulse_i

Auto-extracted signal sof_pulse_i from protocol_control_fsm.vhd - Offset: `0xa3c` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.760.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.761 protocol_control_fsm_compl_ctr_ena_i

Auto-extracted signal compl_ctr_ena_i from protocol_control_fsm.vhd - Offset: `0xa40` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.761.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.762 protocol_control_fsm_tick_state_reg

Auto-extracted signal tick_state_reg from protocol_control_fsm.vhd - Offset: `0xa44` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.762.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.763 protocol_control_fsm_br_shifted_i

Auto-extracted signal br_shifted_i from protocol_control_fsm.vhd - Offset: `0xa48` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.763.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.764 protocol_control_fsm_is_arbitration_i

Auto-extracted signal is_arbitration_i from protocol_control_fsm.vhd - Offset: `0xa4c` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.764.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.765 protocol_control_fsm_crc_spec_enable_i

Auto-extracted signal crc_spec_enable_i from protocol_control_fsm.vhd - Offset: `0xa50` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.765.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.766 protocol_control_fsm_load_init_vect_i

Auto-extracted signal load_init_vect_i from protocol_control_fsm.vhd - Offset: `0xa54` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.766.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.767 protocol_control_fsm_drv_bus_off_reset_q

Auto-extracted signal drv_bus_off_reset_q from protocol_control_fsm.vhd - Offset: `0xa58` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.767.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.768 protocol_control_fsm_retr_ctr_clear_i

Auto-extracted signal retr_ctr_clear_i from protocol_control_fsm.vhd - Offset: `0xa5c` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.768.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.769 protocol_control_fsm_retr_ctr_add_i

Auto-extracted signal retr_ctr_add_i from protocol_control_fsm.vhd - Offset: `0xa60` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.769.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.770 protocol_control_fsm_decrement_rec_i

Auto-extracted signal decrement_rec_i from protocol_control_fsm.vhd - Offset: `0xa64` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.770.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.771 protocol_control_fsm_retr_ctr_add_block

Auto-extracted signal retr_ctr_add_block from protocol_control_fsm.vhd - Offset: `0xa68` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.771.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.772 protocol_control_fsm_retr_ctr_add_block_clr

Auto-extracted signal retr_ctr_add_block_clr from protocol_control_fsm.vhd - Offset: `0xa6c` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.772.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.773 protocol_control_fsm_block_txtb_unlock

Auto-extracted signal block_txtb_unlock from protocol_control_fsm.vhd - Offset: `0xa70` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.773.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.774 protocol_control_fsm_tx_frame_no_sof_d

Auto-extracted signal tx_frame_no_sof_d from protocol_control_fsm.vhd - Offset: `0xa74` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.774.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.775 protocol_control_fsm_tx_frame_no_sof_q

Auto-extracted signal tx_frame_no_sof_q from protocol_control_fsm.vhd - Offset: `0xa78` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.775.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.776 protocol_control_fsm_ctrl_signal_upd

Auto-extracted signal ctrl_signal_upd from protocol_control_fsm.vhd - Offset: `0xa7c` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.776.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.777 protocol_control_fsm_clr_bus_off_rst_flg

Auto-extracted signal clr_bus_off_rst_flg from protocol_control_fsm.vhd - Offset: `0xa80` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.777.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.778 protocol_control_fsm_pex_on_fdf_enable

Auto-extracted signal pex_on_fdf_enable from protocol_control_fsm.vhd - Offset: `0xa84` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.778.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.779 protocol_control_fsm_pex_on_res_enable

Auto-extracted signal pex_on_res_enable from protocol_control_fsm.vhd - Offset: `0xa88` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.779.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.780 protocol_control_fsm_rx_data_nbs_prev

Auto-extracted signal rx_data_nbs_prev from protocol_control_fsm.vhd - Offset: `0xa8c` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.780.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.781 protocol_control_fsm_pexs_set

Auto-extracted signal pexs_set from protocol_control_fsm.vhd - Offset: `0xa90` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.781.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.782 protocol_control_fsm_tran_frame_type_i

Auto-extracted signal tran_frame_type_i from protocol_control_fsm.vhd - Offset: `0xa94` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.782.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.783 protocol_control_fsm_txtb_clk_en_d

Auto-extracted signal txtb_clk_en_d from protocol_control_fsm.vhd - Offset: `0xa98` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.783.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.784 protocol_control_fsm_txtb_clk_en_q

Auto-extracted signal txtb_clk_en_q from protocol_control_fsm.vhd - Offset: `0xa9c` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.784.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.785 reintegration_counter_reinteg_ctr_ce

Auto-extracted signal reinteg_ctr_ce from reintegration_counter.vhd - Offset: `0xaa0` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.785.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.786 retransmitt_counter_retr_ctr_ce

Auto-extracted signal retr_ctr_ce from retransmitt_counter.vhd - Offset: `0xaa4` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.786.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.787 rst_sync_rff

Auto-extracted signal rff from rst_sync.vhd - Offset: `0xaa8` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.787.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.788 rx_buffer_drv_erase_rx

Auto-extracted signal drv_erase_rx from rx_buffer.vhd - Offset: `0xaac` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.788.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.789 rx_buffer_drv_read_start

Auto-extracted signal drv_read_start from rx_buffer.vhd - Offset: `0xab0` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.789.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.790 rx_buffer_drv_clr_ovr

Auto-extracted signal drv_clr_ovr from rx_buffer.vhd - Offset: `0xab4` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.790.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.791 rx_buffer_drv_rtsopt

Auto-extracted signal drv_rtsopt from rx_buffer.vhd - Offset: `0xab8` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.791.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.792 rx_buffer_read_pointer

Auto-extracted signal read_pointer from rx_buffer.vhd - Offset: `0xabc` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.792.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.793 rx_buffer_read_pointer_inc_1

Auto-extracted signal read_pointer_inc_1 from rx_buffer.vhd - Offset: `0xac0` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.793.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.794 rx_buffer_write_pointer

Auto-extracted signal write_pointer from rx_buffer.vhd - Offset: `0xac4` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.794.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.795 rx_buffer_write_pointer_raw

Auto-extracted signal write_pointer_raw from rx_buffer.vhd - Offset: `0xac8` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.795.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.796 rx_buffer_write_pointer_ts

Auto-extracted signal write_pointer_ts from rx_buffer.vhd - Offset: `0xacc` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.796.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.797 rx_buffer_rx_mem_free_i

Auto-extracted signal rx_mem_free_i from rx_buffer.vhd - Offset: `0xad0` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.797.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.798 rx_buffer_memory_write_data

Auto-extracted signal memory_write_data from rx_buffer.vhd - Offset: `0xad4` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.798.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.799 rx_buffer_data_overrun_flg

Auto-extracted signal data_overrun_flg from rx_buffer.vhd - Offset: `0xad8` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.799.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.800 rx_buffer_data_overrun_i

Auto-extracted signal data_overrun_i from rx_buffer.vhd - Offset: `0xadc` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.800.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.801 rx_buffer_overrun_condition

Auto-extracted signal overrun_condition from rx_buffer.vhd - Offset: `0xae0` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.801.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.802 rx_buffer_rx_empty_i

Auto-extracted signal rx_empty_i from rx_buffer.vhd - Offset: `0xae4` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.802.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.803 rx_buffer_is_free_word

Auto-extracted signal is_free_word from rx_buffer.vhd - Offset: `0xae8` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.803.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.804 rx_buffer_commit_rx_frame

Auto-extracted signal commit_rx_frame from rx_buffer.vhd - Offset: `0xaec` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.804.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.805 rx_buffer_commit_overrun_abort

Auto-extracted signal commit_overrun_abort from rx_buffer.vhd - Offset: `0xaf0` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.805.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.806 rx_buffer_read_increment

Auto-extracted signal read_increment from rx_buffer.vhd - Offset: `0xaf4` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.806.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.807 rx_buffer_write_raw_OK

Auto-extracted signal write_raw_OK from rx_buffer.vhd - Offset: `0xaf8` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.807.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.808 rx_buffer_write_raw_intent

Auto-extracted signal write_raw_intent from rx_buffer.vhd - Offset: `0xafc` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.808.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.809 rx_buffer_write_ts

Auto-extracted signal write_ts from rx_buffer.vhd - Offset: `0xb00` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.809.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.810 rx_buffer_stored_ts

Auto-extracted signal stored_ts from rx_buffer.vhd - Offset: `0xb04` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.810.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.811 rx_buffer_data_selector

Auto-extracted signal data_selector from rx_buffer.vhd - Offset: `0xb08` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.811.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.812 rx_buffer_store_ts_wr_ptr

Auto-extracted signal store_ts_wr_ptr from rx_buffer.vhd - Offset: `0xb0c` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.812.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.813 rx_buffer_inc_ts_wr_ptr

Auto-extracted signal inc_ts_wr_ptr from rx_buffer.vhd - Offset: `0xb10` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.813.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.814 rx_buffer_reset_overrun_flag

Auto-extracted signal reset_overrun_flag from rx_buffer.vhd - Offset: `0xb14` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.814.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.815 rx_buffer_frame_form_w

Auto-extracted signal frame_form_w from rx_buffer.vhd - Offset: `0xb18` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.815.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.816 rx_buffer_timestamp_capture

Auto-extracted signal timestamp_capture from rx_buffer.vhd - Offset: `0xb1c` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.816.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.817 rx_buffer_timestamp_capture_ce

Auto-extracted signal timestamp_capture_ce from rx_buffer.vhd - Offset: `0xb20` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.817.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.818 rx_buffer_RAM_write

Auto-extracted signal RAM_write from rx_buffer.vhd - Offset: `0xb24` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.818.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.819 rx_buffer_RAM_data_out

Auto-extracted signal RAM_data_out from rx_buffer.vhd - Offset: `0xb28` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.819.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.820 rx_buffer_RAM_write_address

Auto-extracted signal RAM_write_address from rx_buffer.vhd - Offset: `0xb2c` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.820.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.821 rx_buffer_RAM_read_address

Auto-extracted signal RAM_read_address from rx_buffer.vhd - Offset: `0xb30` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.821.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.822 rx_buffer_rx_buf_res_n_d

Auto-extracted signal rx_buf_res_n_d from rx_buffer.vhd - Offset: `0xb34` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.822.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.823 rx_buffer_rx_buf_res_n_q

Auto-extracted signal rx_buf_res_n_q from rx_buffer.vhd - Offset: `0xb38` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.823.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.824 rx_buffer_rx_buf_res_n_q_scan

Auto-extracted signal rx_buf_res_n_q_scan from rx_buffer.vhd - Offset: `0xb3c` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.824.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.825 rx_buffer_rx_buf_ram_clk_en

Auto-extracted signal rx_buf_ram_clk_en from rx_buffer.vhd - Offset: `0xb40` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.825.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.826 rx_buffer_clk_ram

Auto-extracted signal clk_ram from rx_buffer.vhd - Offset: `0xb44` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.826.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.827 rx_buffer_fsm_rx_fsm_ce

Auto-extracted signal rx_fsm_ce from rx_buffer_fsm.vhd - Offset: `0xb48` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.827.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.828 rx_buffer_fsm_cmd_join

Auto-extracted signal cmd_join from rx_buffer_fsm.vhd - Offset: `0xb4c` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.828.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.829 rx_buffer_pointers_write_pointer_raw_ce

Auto-extracted signal write_pointer_raw_ce from rx_buffer_pointers.vhd - Offset: `0xb50` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.829.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.830 rx_buffer_pointers_write_pointer_ts_ce

Auto-extracted signal write_pointer_ts_ce from rx_buffer_pointers.vhd - Offset: `0xb54` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.830.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.831 rx_buffer_ram_port_a_address_i

Auto-extracted signal port_a_address_i from rx_buffer_ram.vhd - Offset: `0xb58` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.831.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.832 rx_buffer_ram_port_a_write_i

Auto-extracted signal port_a_write_i from rx_buffer_ram.vhd - Offset: `0xb5c` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.832.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.833 rx_buffer_ram_port_a_data_in_i

Auto-extracted signal port_a_data_in_i from rx_buffer_ram.vhd - Offset: `0xb60` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.833.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.834 rx_buffer_ram_port_b_address_i

Auto-extracted signal port_b_address_i from rx_buffer_ram.vhd - Offset: `0xb64` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.834.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.835 rx_buffer_ram_port_b_data_out_i

Auto-extracted signal port_b_data_out_i from rx_buffer_ram.vhd - Offset: `0xb68` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.835.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.836 rx_buffer_ram_tst_ena

Auto-extracted signal tst_ena from rx_buffer_ram.vhd - Offset: `0xb6c` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.836.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.837 rx_buffer_ram_tst_addr

Auto-extracted signal tst_addr from rx_buffer_ram.vhd - Offset: `0xb70` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.837.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.838 rx_shift_reg_res_n_i_d

Auto-extracted signal res_n_i_d from rx_shift_reg.vhd - Offset: `0xb74` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.838.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.839 rx_shift_reg_res_n_i_q

Auto-extracted signal res_n_i_q from rx_shift_reg.vhd - Offset: `0xb78` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.839.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.840 rx_shift_reg_res_n_i_q_scan

Auto-extracted signal res_n_i_q_scan from rx_shift_reg.vhd - Offset: `0xb7c` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.840.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.841 rx_shift_reg_rx_shift_reg_q

Auto-extracted signal rx_shift_reg_q from rx_shift_reg.vhd - Offset: `0xb80` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.841.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.842 rx_shift_reg_rx_shift_cmd

Auto-extracted signal rx_shift_cmd from rx_shift_reg.vhd - Offset: `0xb84` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.842.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.843 rx_shift_reg_rx_shift_in_sel_demuxed

Auto-extracted signal rx_shift_in_sel_demuxed from rx_shift_reg.vhd - Offset: `0xb88` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.843.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.844 rx_shift_reg_rec_is_rtr_i

Auto-extracted signal rec_is_rtr_i from rx_shift_reg.vhd - Offset: `0xb8c` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.844.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.845 rx_shift_reg_rec_frame_type_i

Auto-extracted signal rec_frame_type_i from rx_shift_reg.vhd - Offset: `0xb90` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.845.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.846 sample_mux_sample

Auto-extracted signal sample from sample_mux.vhd - Offset: `0xb94` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.846.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.847 sample_mux_prev_sample_d

Auto-extracted signal prev_sample_d from sample_mux.vhd - Offset: `0xb98` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.847.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.848 sample_mux_prev_sample_q

Auto-extracted signal prev_sample_q from sample_mux.vhd - Offset: `0xb9c` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.848.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.849 segment_end_detector_req_input

Auto-extracted signal req_input from segment_end_detector.vhd - Offset: `0xba0` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.849.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.850 segment_end_detector_segm_end_req_capt_d

Auto-extracted signal segm_end_req_capt_d from segment_end_detector.vhd - Offset: `0xba4` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.850.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.851 segment_end_detector_segm_end_req_capt_q

Auto-extracted signal segm_end_req_capt_q from segment_end_detector.vhd - Offset: `0xba8` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.851.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.852 segment_end_detector_segm_end_req_capt_ce

Auto-extracted signal segm_end_req_capt_ce from segment_end_detector.vhd - Offset: `0xbac` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.852.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.853 segment_end_detector_segm_end_req_capt_clr

Auto-extracted signal segm_end_req_capt_clr from segment_end_detector.vhd - Offset: `0xbb0` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.853.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.854 segment_end_detector_segm_end_req_capt_dq

Auto-extracted signal segm_end_req_capt_dq from segment_end_detector.vhd - Offset: `0xbb4` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.854.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.855 segment_end_detector_segm_end_nbt_valid

Auto-extracted signal segm_end_nbt_valid from segment_end_detector.vhd - Offset: `0xbb8` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.855.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.856 segment_end_detector_segm_end_dbt_valid

Auto-extracted signal segm_end_dbt_valid from segment_end_detector.vhd - Offset: `0xbbc` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.856.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.857 segment_end_detector_segm_end_nbt_dbt_valid

Auto-extracted signal segm_end_nbt_dbt_valid from segment_end_detector.vhd - Offset: `0xbc0` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.857.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.858 segment_end_detector_tseg1_end_req_valid

Auto-extracted signal tseg1_end_req_valid from segment_end_detector.vhd - Offset: `0xbc4` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.858.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.859 segment_end_detector_tseg2_end_req_valid

Auto-extracted signal tseg2_end_req_valid from segment_end_detector.vhd - Offset: `0xbc8` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.859.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.860 segment_end_detector_h_sync_valid_i

Auto-extracted signal h_sync_valid_i from segment_end_detector.vhd - Offset: `0xbcc` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.860.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.861 segment_end_detector_segment_end_i

Auto-extracted signal segment_end_i from segment_end_detector.vhd - Offset: `0xbd0` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.861.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.862 segment_end_detector_nbt_tq_active

Auto-extracted signal nbt_tq_active from segment_end_detector.vhd - Offset: `0xbd4` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.862.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.863 segment_end_detector_dbt_tq_active

Auto-extracted signal dbt_tq_active from segment_end_detector.vhd - Offset: `0xbd8` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.863.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.864 segment_end_detector_bt_ctr_clear_i

Auto-extracted signal bt_ctr_clear_i from segment_end_detector.vhd - Offset: `0xbdc` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.864.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.865 shift_reg_shift_regs

Auto-extracted signal shift_regs from shift_reg.vhd - Offset: `0xbe0` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.865.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.866 shift_reg_next_shift_reg_val

Auto-extracted signal next_shift_reg_val from shift_reg.vhd - Offset: `0xbe4` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.866.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.867 shift_reg_byte_shift_reg_in

Auto-extracted signal shift_reg_in from shift_reg_byte.vhd - Offset: `0xbe8` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.867.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.868 shift_reg_preload_shift_regs

Auto-extracted signal shift_regs from shift_reg_preload.vhd - Offset: `0xbec` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.868.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.869 shift_reg_preload_next_shift_reg_val

Auto-extracted signal next_shift_reg_val from shift_reg_preload.vhd - Offset: `0xbf0` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.869.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.870 sig_sync_rff

Auto-extracted signal rff from sig_sync.vhd - Offset: `0xbf4` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.870.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.871 ssp_generator_btmc_d

Auto-extracted signal btmc_d from ssp_generator.vhd - Offset: `0xbf8` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.871.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.872 ssp_generator_btmc_q

Auto-extracted signal btmc_q from ssp_generator.vhd - Offset: `0xbfc` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.872.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.873 ssp_generator_btmc_add

Auto-extracted signal btmc_add from ssp_generator.vhd - Offset: `0xc00` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.873.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.874 ssp_generator_btmc_ce

Auto-extracted signal btmc_ce from ssp_generator.vhd - Offset: `0xc04` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.874.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.875 ssp_generator_btmc_meas_running_d

Auto-extracted signal btmc_meas_running_d from ssp_generator.vhd - Offset: `0xc08` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.875.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.876 ssp_generator_btmc_meas_running_q

Auto-extracted signal btmc_meas_running_q from ssp_generator.vhd - Offset: `0xc0c` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.876.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.877 ssp_generator_sspc_d

Auto-extracted signal sspc_d from ssp_generator.vhd - Offset: `0xc10` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.877.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.878 ssp_generator_sspc_q

Auto-extracted signal sspc_q from ssp_generator.vhd - Offset: `0xc14` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.878.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.879 ssp_generator_sspc_ce

Auto-extracted signal sspc_ce from ssp_generator.vhd - Offset: `0xc18` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.879.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.880 ssp_generator_sspc_expired

Auto-extracted signal sspc_expired from ssp_generator.vhd - Offset: `0xc1c` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.880.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.881 ssp_generator_sspc_threshold

Auto-extracted signal sspc_threshold from ssp_generator.vhd - Offset: `0xc20` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.881.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.882 ssp_generator_sspc_add

Auto-extracted signal sspc_add from ssp_generator.vhd - Offset: `0xc24` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.882.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.883 ssp_generator_first_ssp_d

Auto-extracted signal first_ssp_d from ssp_generator.vhd - Offset: `0xc28` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.883.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.884 ssp_generator_first_ssp_q

Auto-extracted signal first_ssp_q from ssp_generator.vhd - Offset: `0xc2c` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.884.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.885 ssp_generator_sspc_ena_d

Auto-extracted signal sspc_ena_d from ssp_generator.vhd - Offset: `0xc30` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.885.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.886 ssp_generator_sspc_ena_q

Auto-extracted signal sspc_ena_q from ssp_generator.vhd - Offset: `0xc34` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.886.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.887 ssp_generator_ssp_delay_padded

Auto-extracted signal ssp_delay_padded from ssp_generator.vhd - Offset: `0xc38` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.887.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.888 synchronisation_checker_resync_edge

Auto-extracted signal resync_edge from synchronisation_checker.vhd - Offset: `0xc3c` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.888.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.889 synchronisation_checker_h_sync_edge

Auto-extracted signal h_sync_edge from synchronisation_checker.vhd - Offset: `0xc40` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.889.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.890 synchronisation_checker_h_or_re_sync_edge

Auto-extracted signal h_or_re_sync_edge from synchronisation_checker.vhd - Offset: `0xc44` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.890.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.891 synchronisation_checker_sync_flag

Auto-extracted signal sync_flag from synchronisation_checker.vhd - Offset: `0xc48` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.891.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.892 synchronisation_checker_sync_flag_ce

Auto-extracted signal sync_flag_ce from synchronisation_checker.vhd - Offset: `0xc4c` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.892.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.893 synchronisation_checker_sync_flag_nxt

Auto-extracted signal sync_flag_nxt from synchronisation_checker.vhd - Offset: `0xc50` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.893.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.894 test_registers_reg_map_reg_sel

Auto-extracted signal reg_sel from test_registers_reg_map.vhd - Offset: `0xc54` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.894.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.895 test_registers_reg_map_read_data_mux_in

Auto-extracted signal read_data_mux_in from test_registers_reg_map.vhd - Offset: `0xc58` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.895.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.896 test_registers_reg_map_read_data_mask_n

Auto-extracted signal read_data_mask_n from test_registers_reg_map.vhd - Offset: `0xc5c` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.896.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.897 test_registers_reg_map_read_mux_ena

Auto-extracted signal read_mux_ena from test_registers_reg_map.vhd - Offset: `0xc60` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.897.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.898 trigger_generator_rx_trig_req_q

Auto-extracted signal rx_trig_req_q from trigger_generator.vhd - Offset: `0xc64` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.898.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.899 trigger_generator_tx_trig_req_flag_d

Auto-extracted signal tx_trig_req_flag_d from trigger_generator.vhd - Offset: `0xc68` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.899.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.900 trigger_generator_tx_trig_req_flag_q

Auto-extracted signal tx_trig_req_flag_q from trigger_generator.vhd - Offset: `0xc6c` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.900.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.901 trigger_generator_tx_trig_req_flag_dq

Auto-extracted signal tx_trig_req_flag_dq from trigger_generator.vhd - Offset: `0xc70` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.901.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.902 trigger_mux_tx_trigger_q

Auto-extracted signal tx_trigger_q from trigger_mux.vhd - Offset: `0xc74` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.902.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.903 trv_delay_meas_trv_meas_progress_d

Auto-extracted signal trv_meas_progress_d from trv_delay_meas.vhd - Offset: `0xc78` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.903.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.904 trv_delay_meas_trv_meas_progress_q

Auto-extracted signal trv_meas_progress_q from trv_delay_meas.vhd - Offset: `0xc7c` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.904.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.905 trv_delay_meas_trv_meas_progress_del

Auto-extracted signal trv_meas_progress_del from trv_delay_meas.vhd - Offset: `0xc80` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.905.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.906 trv_delay_meas_trv_delay_ctr_q

Auto-extracted signal trv_delay_ctr_q from trv_delay_meas.vhd - Offset: `0xc84` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.906.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.907 trv_delay_meas_trv_delay_ctr_d

Auto-extracted signal trv_delay_ctr_d from trv_delay_meas.vhd - Offset: `0xc88` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.907.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.908 trv_delay_meas_trv_delay_ctr_add

Auto-extracted signal trv_delay_ctr_add from trv_delay_meas.vhd - Offset: `0xc8c` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.908.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.909 trv_delay_meas_trv_delay_ctr_q_padded

Auto-extracted signal trv_delay_ctr_q_padded from trv_delay_meas.vhd - Offset: `0xc90` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.909.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.910 trv_delay_meas_trv_delay_ctr_rst_d

Auto-extracted signal trv_delay_ctr_rst_d from trv_delay_meas.vhd - Offset: `0xc94` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.910.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.911 trv_delay_meas_trv_delay_ctr_rst_q

Auto-extracted signal trv_delay_ctr_rst_q from trv_delay_meas.vhd - Offset: `0xc98` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.911.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.912 trv_delay_meas_trv_delay_ctr_rst_q_scan

Auto-extracted signal trv_delay_ctr_rst_q_scan from trv_delay_meas.vhd - Offset: `0xc9c` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.912.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.913 trv_delay_meas_ssp_shadow_ce

Auto-extracted signal ssp_shadow_ce from trv_delay_meas.vhd - Offset: `0xca0` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.913.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.914 trv_delay_meas_ssp_delay_raw

Auto-extracted signal ssp_delay_raw from trv_delay_meas.vhd - Offset: `0xca4` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.914.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.915 trv_delay_meas_ssp_delay_saturated

Auto-extracted signal ssp_delay_saturated from trv_delay_meas.vhd - Offset: `0xca8` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.915.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.916 trv_delay_meas_trv_delay_sum

Auto-extracted signal trv_delay_sum from trv_delay_meas.vhd - Offset: `0xcac` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.916.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.917 tx_arbitrator_select_buf_avail

Auto-extracted signal select_buf_avail from tx_arbitrator.vhd - Offset: `0xcb0` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.917.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.918 tx_arbitrator_txtb_selected_input

Auto-extracted signal txtb_selected_input from tx_arbitrator.vhd - Offset: `0xcb4` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.918.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.919 tx_arbitrator_txtb_timestamp

Auto-extracted signal txtb_timestamp from tx_arbitrator.vhd - Offset: `0xcb8` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.919.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.920 tx_arbitrator_timestamp_valid

Auto-extracted signal timestamp_valid from tx_arbitrator.vhd - Offset: `0xcbc` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.920.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.921 tx_arbitrator_select_index_changed

Auto-extracted signal select_index_changed from tx_arbitrator.vhd - Offset: `0xcc0` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.921.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.922 tx_arbitrator_validated_buffer

Auto-extracted signal validated_buffer from tx_arbitrator.vhd - Offset: `0xcc4` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.922.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.923 tx_arbitrator_ts_low_internal

Auto-extracted signal ts_low_internal from tx_arbitrator.vhd - Offset: `0xcc8` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.923.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.924 tx_arbitrator_tran_dlc_dbl_buf

Auto-extracted signal tran_dlc_dbl_buf from tx_arbitrator.vhd - Offset: `0xccc` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.924.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.925 tx_arbitrator_tran_is_rtr_dbl_buf

Auto-extracted signal tran_is_rtr_dbl_buf from tx_arbitrator.vhd - Offset: `0xcd0` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.925.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.926 tx_arbitrator_tran_ident_type_dbl_buf

Auto-extracted signal tran_ident_type_dbl_buf from tx_arbitrator.vhd - Offset: `0xcd4` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.926.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.927 tx_arbitrator_tran_frame_type_dbl_buf

Auto-extracted signal tran_frame_type_dbl_buf from tx_arbitrator.vhd - Offset: `0xcd8` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.927.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.928 tx_arbitrator_tran_brs_dbl_buf

Auto-extracted signal tran_brs_dbl_buf from tx_arbitrator.vhd - Offset: `0xcdc` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.928.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.929 tx_arbitrator_tran_dlc_com

Auto-extracted signal tran_dlc_com from tx_arbitrator.vhd - Offset: `0xce0` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.929.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.930 tx_arbitrator_tran_is_rtr_com

Auto-extracted signal tran_is_rtr_com from tx_arbitrator.vhd - Offset: `0xce4` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.930.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.931 tx_arbitrator_tran_ident_type_com

Auto-extracted signal tran_ident_type_com from tx_arbitrator.vhd - Offset: `0xce8` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.931.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.932 tx_arbitrator_tran_frame_type_com

Auto-extracted signal tran_frame_type_com from tx_arbitrator.vhd - Offset: `0xcec` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.932.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.933 tx_arbitrator_tran_brs_com

Auto-extracted signal tran_brs_com from tx_arbitrator.vhd - Offset: `0xcf0` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.933.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.934 tx_arbitrator_tran_frame_valid_com

Auto-extracted signal tran_frame_valid_com from tx_arbitrator.vhd - Offset: `0xcf4` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.934.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.935 tx_arbitrator_tran_identifier_com

Auto-extracted signal tran_identifier_com from tx_arbitrator.vhd - Offset: `0xcf8` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.935.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.936 tx_arbitrator_load_ts_lw_addr

Auto-extracted signal load_ts_lw_addr from tx_arbitrator.vhd - Offset: `0xcfc` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.936.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.937 tx_arbitrator_load_ts_uw_addr

Auto-extracted signal load_ts_uw_addr from tx_arbitrator.vhd - Offset: `0xd00` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.937.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.938 tx_arbitrator_load_ffmt_w_addr

Auto-extracted signal load_ffmt_w_addr from tx_arbitrator.vhd - Offset: `0xd04` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.938.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.939 tx_arbitrator_load_ident_w_addr

Auto-extracted signal load_ident_w_addr from tx_arbitrator.vhd - Offset: `0xd08` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.939.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.940 tx_arbitrator_store_ts_l_w

Auto-extracted signal store_ts_l_w from tx_arbitrator.vhd - Offset: `0xd0c` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.940.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.941 tx_arbitrator_store_md_w

Auto-extracted signal store_md_w from tx_arbitrator.vhd - Offset: `0xd10` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.941.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.942 tx_arbitrator_store_ident_w

Auto-extracted signal store_ident_w from tx_arbitrator.vhd - Offset: `0xd14` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.942.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.943 tx_arbitrator_buffer_md_w

Auto-extracted signal buffer_md_w from tx_arbitrator.vhd - Offset: `0xd18` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.943.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.944 tx_arbitrator_store_last_txtb_index

Auto-extracted signal store_last_txtb_index from tx_arbitrator.vhd - Offset: `0xd1c` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.944.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.945 tx_arbitrator_frame_valid_com_set

Auto-extracted signal frame_valid_com_set from tx_arbitrator.vhd - Offset: `0xd20` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.945.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.946 tx_arbitrator_frame_valid_com_clear

Auto-extracted signal frame_valid_com_clear from tx_arbitrator.vhd - Offset: `0xd24` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.946.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.947 tx_arbitrator_tx_arb_locked

Auto-extracted signal tx_arb_locked from tx_arbitrator.vhd - Offset: `0xd28` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.947.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.948 tx_arbitrator_txtb_meta_clk_en

Auto-extracted signal txtb_meta_clk_en from tx_arbitrator.vhd - Offset: `0xd2c` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.948.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.949 tx_arbitrator_drv_tttm_ena

Auto-extracted signal drv_tttm_ena from tx_arbitrator.vhd - Offset: `0xd30` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.949.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.950 tx_arbitrator_fsm_tx_arb_fsm_ce

Auto-extracted signal tx_arb_fsm_ce from tx_arbitrator_fsm.vhd - Offset: `0xd34` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.950.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.951 tx_arbitrator_fsm_fsm_wait_state_d

Auto-extracted signal fsm_wait_state_d from tx_arbitrator_fsm.vhd - Offset: `0xd38` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.951.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.952 tx_arbitrator_fsm_fsm_wait_state_q

Auto-extracted signal fsm_wait_state_q from tx_arbitrator_fsm.vhd - Offset: `0xd3c` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.952.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.953 tx_data_cache_tx_cache_mem

Auto-extracted signal tx_cache_mem from tx_data_cache.vhd - Offset: `0xd40` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.953.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.954 tx_shift_reg_tx_sr_output

Auto-extracted signal tx_sr_output from tx_shift_reg.vhd - Offset: `0xd44` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.954.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.955 tx_shift_reg_tx_sr_ce

Auto-extracted signal tx_sr_ce from tx_shift_reg.vhd - Offset: `0xd48` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.955.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.956 tx_shift_reg_tx_sr_pload

Auto-extracted signal tx_sr_pload from tx_shift_reg.vhd - Offset: `0xd4c` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.956.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.957 tx_shift_reg_tx_sr_pload_val

Auto-extracted signal tx_sr_pload_val from tx_shift_reg.vhd - Offset: `0xd50` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.957.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.958 tx_shift_reg_tx_base_id

Auto-extracted signal tx_base_id from tx_shift_reg.vhd - Offset: `0xd54` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.958.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.959 tx_shift_reg_tx_ext_id

Auto-extracted signal tx_ext_id from tx_shift_reg.vhd - Offset: `0xd58` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.959.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.960 tx_shift_reg_tx_crc

Auto-extracted signal tx_crc from tx_shift_reg.vhd - Offset: `0xd5c` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.960.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.961 tx_shift_reg_bst_ctr_grey

Auto-extracted signal bst_ctr_grey from tx_shift_reg.vhd - Offset: `0xd60` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.961.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.962 tx_shift_reg_bst_parity

Auto-extracted signal bst_parity from tx_shift_reg.vhd - Offset: `0xd64` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.962.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.963 tx_shift_reg_stuff_count

Auto-extracted signal stuff_count from tx_shift_reg.vhd - Offset: `0xd68` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.963.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.964 txt_buffer_txtb_user_accessible

Auto-extracted signal txtb_user_accessible from txt_buffer.vhd - Offset: `0xd6c` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.964.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.965 txt_buffer_hw_cbs

Auto-extracted signal hw_cbs from txt_buffer.vhd - Offset: `0xd70` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.965.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.966 txt_buffer_sw_cbs

Auto-extracted signal sw_cbs from txt_buffer.vhd - Offset: `0xd74` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.966.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.967 txt_buffer_txtb_unmask_data_ram

Auto-extracted signal txtb_unmask_data_ram from txt_buffer.vhd - Offset: `0xd78` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.967.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.968 txt_buffer_txtb_port_b_data_i

Auto-extracted signal txtb_port_b_data_i from txt_buffer.vhd - Offset: `0xd7c` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.968.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.969 txt_buffer_ram_write

Auto-extracted signal ram_write from txt_buffer.vhd - Offset: `0xd80` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.969.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.970 txt_buffer_ram_read_address

Auto-extracted signal ram_read_address from txt_buffer.vhd - Offset: `0xd84` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.970.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.971 txt_buffer_txtb_ram_clk_en

Auto-extracted signal txtb_ram_clk_en from txt_buffer.vhd - Offset: `0xd88` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.971.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.972 txt_buffer_clk_ram

Auto-extracted signal clk_ram from txt_buffer.vhd - Offset: `0xd8c` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.972.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.973 txt_buffer_fsm_abort_applied

Auto-extracted signal abort_applied from txt_buffer_fsm.vhd - Offset: `0xd90` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.973.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.974 txt_buffer_fsm_txt_fsm_ce

Auto-extracted signal txt_fsm_ce from txt_buffer_fsm.vhd - Offset: `0xd94` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.974.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.975 txt_buffer_fsm_go_to_failed

Auto-extracted signal go_to_failed from txt_buffer_fsm.vhd - Offset: `0xd98` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.975.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.976 txt_buffer_fsm_transient_state

Auto-extracted signal transient_state from txt_buffer_fsm.vhd - Offset: `0xd9c` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.976.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.977 txt_buffer_ram_port_a_address_i

Auto-extracted signal port_a_address_i from txt_buffer_ram.vhd - Offset: `0xda0` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.977.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.978 txt_buffer_ram_port_a_write_i

Auto-extracted signal port_a_write_i from txt_buffer_ram.vhd - Offset: `0xda4` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.978.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.979 txt_buffer_ram_port_a_data_in_i

Auto-extracted signal port_a_data_in_i from txt_buffer_ram.vhd - Offset: `0xda8` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.979.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.980 txt_buffer_ram_port_b_address_i

Auto-extracted signal port_b_address_i from txt_buffer_ram.vhd - Offset: `0xdac` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.980.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.981 txt_buffer_ram_port_b_data_out_i

Auto-extracted signal port_b_data_out_i from txt_buffer_ram.vhd - Offset: `0xdb0` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.981.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.982 txt_buffer_ram_tst_ena

Auto-extracted signal tst_ena from txt_buffer_ram.vhd - Offset: `0xdb4` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.982.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.983 txt_buffer_ram_tst_addr

Auto-extracted signal tst_addr from txt_buffer_ram.vhd - Offset: `0xdb8` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.983.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.984 access_signaler_be_active

Auto-extracted signal be_active from access_signaler.vhd - Offset: `0xdbc` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.984.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.985 access_signaler_access_in

Auto-extracted signal access_in from access_signaler.vhd - Offset: `0xdc0` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.985.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.986 access_signaler_access_active

Auto-extracted signal access_active from access_signaler.vhd - Offset: `0xdc4` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.986.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.987 access_signaler_access_active_reg

Auto-extracted signal access_active_reg from access_signaler.vhd - Offset: `0xdc8` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.987.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.988 address_decoder_addr_dec_i

Auto-extracted signal addr_dec_i from address_decoder.vhd - Offset: `0xdcc` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.988.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.989 address_decoder_addr_dec_enabled_i

Auto-extracted signal addr_dec_enabled_i from address_decoder.vhd - Offset: `0xdd0` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.989.1 Fields

{"reg": [{"name": "value", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	value	Placeholder 32-bit field for extracted signal

2.990 carfield_regs / doc / carfield_regs.md

2.991 Summary

Name	Offset	Length	Description
carfield.VERSION0	0x0	4	Cheshire sha256 commit
carfield.VERSION1	0x4	4	Safety Island sha256 commit
carfield.VERSION2	0x8	4	Security Island sha256 commit
carfield.VERSION3	0xc	4	PULP Cluster sha256 commit
carfield.VERSION4	0x10	4	Spatz CLuster sha256 commit
carfield.JEDEC_IDCODE	0x14	4	JEDEC ID CODE -TODO assign-
carfield.GENERIC_SCRATCH0	0x18	4	Scratch
carfield.GENERIC_SCRATCH1	0x1c	4	Scratch
carfield.HOST_RST	0x20	4	Host Domain reset -active high, inverted in HW-
carfield.PERIPH_RST	0x24	4	Periph Domain reset -active high, inverted in HW-
carfield.SAFETY_ISLAND_RST	0x28	4	Safety Island reset -active high, inverted in HW-
carfield.SECURITY_ISLAND_RST	0x2c	4	Security Island reset -active high, inverted in HW-
carfield.PULP_CLUSTER_RST	0x30	4	PULP Cluster reset -active high, inverted in HW-
carfield.SPATZ_CLUSTER_RST	0x34	4	Spatz Cluster reset -active high, inverted in HW-
carfield.L2_RST	0x38	4	L2 reset -active high, inverted in HW-
carfield.PERIPH_ISOLATE	0x3c	4	Periph Domain AXI isolate
carfield.SAFETY_ISLAND_ISOLATE	0x40	4	Safety Island AXI isolate
carfield.SECURITY_ISLAND_ISOLATE	0x44	4	Security Island AXI isolate
carfield.PULP_CLUSTER_ISOLATE	0x48	4	PULP Cluster AXI isolate
carfield.SPATZ_CLUSTER_ISOLATE	0x4c	4	Spatz Cluster AXI isolate
carfield.L2_ISOLATE	0x50	4	L2 AXI isolate
carfield.PERIPH_ISOLATE_STATUS	0x54	4	Periph Domain AXI isolate status
carfield.SAFETY_ISLAND_ISOLATE_STATUS	0x58	4	Safety Island AXI isolate status
carfield.SECURITY_ISLAND_ISOLATE_STATUS	0x5c	4	Security Island AXI isolate status
carfield.PULP_CLUSTER_ISOLATE_STATUS	0x60	4	PULP Cluster AXI isolate status
carfield.SPATZ_CLUSTER_ISOLATE_STATUS	0x64	4	Spatz Cluster AXI isolate status

Name	Offset	Length	Description
carfield.L2_ISOLATE_STATUS	0x68	4	L2 AXI isolate status
carfield.PERIPH_CLK_EN	0x6c	4	Periph Domain clk gate enable
carfield.SAFETY_ISLAND_CLK_EN	0x70	4	Safety Island clk gate enable
carfield.SECURITY_ISLAND_CLK_EN	0x74	4	Security Island clk gate enable
carfield.PULP_CLUSTER_CLK_EN	0x78	4	PULP Cluster clk gate enable
carfield.SPATZ_CLUSTER_CLK_EN	0x7c	4	Spatz Cluster clk gate enable
carfield.L2_CLK_EN	0x80	4	Shared L2 memory clk gate enable
carfield.PERIPH_CLK_SEL	0x84	4	Periph Domain pll select (0 -> host pll, 1 -> alt PLL, 2 -> per pll)
carfield.SAFETY_ISLAND_CLK_SEL	0x88	4	Safety Island pll select (0 -> host pll, 1 -> alt PLL, 2 -> per pll)
carfield.SECURITY_ISLAND_CLK_SEL	0x8c	4	Security Island pll select (0 -> host pll, 1 -> alt PLL, 2 -> per pll)
carfield.PULP_CLUSTER_CLK_SEL	0x90	4	PULP Cluster pll select (0 -> host pll, 1 -> alt PLL, 2 -> per pll)
carfield.SPATZ_CLUSTER_CLK_SEL	0x94	4	Spatz Cluster pll select (0 -> host pll, 1 -> alt PLL, 2 -> per pll)
carfield.L2_CLK_SEL	0x98	4	L2 Memory pll select (0 -> host pll, 1 -> alt PLL, 2 -> per pll)
carfield.PERIPH_CLK_DIV_VALUE	0x9c	4	Periph Domain clk divider value
carfield.SAFETY_ISLAND_CLK_DIV_VALUE	0xa0	4	Safety Island clk divider value
carfield.SECURITY_ISLAND_CLK_DIV_VALUE	0xa4	4	Security Island clk divider value
carfield.PULP_CLUSTER_CLK_DIV_VALUE	0xa8	4	PULP Cluster clk divider value
carfield.SPATZ_CLUSTER_CLK_DIV_VALUE	0xac	4	Spatz Cluster clk divider value
carfield.L2_CLK_DIV_VALUE	0xb0	4	L2 Memory clk divider value
carfield.HOST_FETCH_ENABLE	0xb4	4	Host Domain fetch enable
carfield.SAFETY_ISLAND_FETCH_ENABLE	0xb8	4	Safety Island fetch enable
carfield.SECURITY_ISLAND_FETCH_ENABLE	0xbc	4	Security Island fetch enable
carfield.PULP_CLUSTER_FETCH_ENABLE	0xc0	4	PULP Cluster fetch enable
carfield.SPATZ_CLUSTER_DEBUG_REQ	0xc4	4	Spatz Cluster debug req
carfield.HOST_BOOT_ADDR	0xc8	4	Host boot address
carfield.SAFETY_ISLAND_BOOT_ADDR	0xcc	4	Safety Island boot address
carfield.SECURITY_ISLAND_BOOT_ADDR	0xd0	4	Security Island boot address
carfield.PULP_CLUSTER_BOOT_ADDR	0xd4	4	PULP Cluster boot address
carfield.SPATZ_CLUSTER_BOOT_ADDR	0xd8	4	Spatz Cluster boot address
carfield.PULP_CLUSTER_BOOT_ENABLE	0xdc	4	PULP Cluster boot enable
carfield.SPATZ_CLUSTER_BUSY	0xe0	4	Spatz Cluster busy
carfield.PULP_CLUSTER_BUSY	0xe4	4	PULP Cluster busy
carfield.PULP_CLUSTER_EOC	0xe8	4	PULP Cluster end of computation
carfield.ETH_RGMII_PHY_CLK_DIV_EN	0xec	4	Ethernet RGMII PHY clock divider enable bit
carfield.ETH_RGMII_PHY_CLK_DIV_VALUE	0xf0	4	Ethernet RGMII PHY clock divider value
carfield.ETH_MDIO_CLK_DIV_EN	0xf4	4	Ethernet MDIO clock divider enable bit

carfield.ETH_MDIO_CLK_DIV_VALUE	0xf8	4	Ethernet MDIO clock divider value

2.992 VERSION0

Cheshire sha256 commit - Offset: `0x0` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.992.1 Fields


```
{"reg": [{"name": "VERSION0", "bits": 32, "attr": ["ro"], "rotate": 0}], "config": {"lanes": 1
```


Bits	Type	Reset	Name	Description
31:0	ro	0x0	VERSION0	

2.993 VERSION1

Safety Island sha256 commit - Offset: `0x4` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.993.1 Fields


```
{"reg": [{"name": "VERSION1", "bits": 32, "attr": ["ro"], "rotate": 0}], "config": {"lanes": 1
```


Bits	Type	Reset	Name	Description
31:0	ro	0x0	VERSION1	

2.994 VERSION2

Security Island sha256 commit - Offset: `0x8` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.994.1 Fields


```
{"reg": [{"name": "VERSION2", "bits": 32, "attr": ["ro"], "rotate": 0}], "config": {"lanes": 1
```


Bits	Type	Reset	Name	Description
31:0	ro	0x0	VERSION2	

2.995 VERSION3

PULP Cluster sha256 commit - Offset: `0xc` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.995.1 Fields

{"reg": [{"name": "VERSION3", "bits": 32, "attr": ["ro"], "rotate": 0}], "config": {"lanes": 1

Bits	Type	Reset	Name	Description
31:0	ro	0x0	VERSION3	

2.996 VERSION4

Spatz CLuster sha256 commit - Offset: `0x10` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.996.1 Fields

{"reg": [{"name": "VERSION4", "bits": 32, "attr": ["ro"], "rotate": 0}], "config": {"lanes": 1

Bits	Type	Reset	Name	Description
31:0	ro	0x0	VERSION4	

2.997 JEDEC_IDCODE

JEDEC ID CODE -TODO assign- - Offset: `0x14` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.997.1 Fields

{"reg": [{"name": "JEDEC_IDCODE", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes"

Bits	Type	Reset	Name	Description
31:0	rw	0x0	JEDEC_IDCODE	

2.998 GENERIC_SCRATCH0

Scratch - Offset: `0x18` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.998.1 Fields

{"reg": [{"name": "GENERIC_SCRATCH0", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"la

Bits	Type	Reset	Name	Description
31:0	rw	0x0	GENERIC_SCRATCH0	

2.999 GENERIC_SCRATCH1

Scratch - Offset: `0x1c` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.999.1 Fields

`{"reg": [{"name": "GENERIC_SCRATCH1", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"la`

Bits	Type	Reset	Name	Description
31:0	rw	0x0	GENERIC_SCRATCH1	

2.1000 HOST_RST

Host Domain reset -active high, inverted in HW- - Offset: `0x20` - Reset default: `0x0` - Reset mask: `0x1`

2.1000.1 Fields

`{"reg": [{"name": "HOST_RST", "bits": 1, "attr": ["ro"], "rotate": -90}, {"bits": 31}], "config`

Bits	Type	Reset	Name	Description
31:1				Reserved
0	ro	0x0	HOST_RST	

2.1001 PERIPH_RST

Periph Domain reset -active high, inverted in HW- - Offset: `0x24` - Reset default: `0x0` - Reset mask: `0x1`

2.1001.1 Fields

`{"reg": [{"name": "PERIPH_RST", "bits": 1, "attr": ["rw"], "rotate": -90}, {"bits": 31}], "con`

Bits	Type	Reset	Name	Description
31:1				Reserved

Bits	Type	Reset	Name	Description
0	rw	0x0	PERIPH_RST	

2.1002 SAFETY_ISLAND_RST

Safety Island reset -active high, inverted in HW- - Offset: `0x28` - Reset default: `0x0` - Reset mask: `0x1`

2.1002.1 Fields


```
{"reg": [{"name": "SAFETY_ISLAND_RST", "bits": 1, "attr": ["rw"], "rotate": -90}, {"bits": 31}]
```


Bits	Type	Reset	Name	Description
31:1				Reserved
0	rw	0x0	SAFETY_ISLAND_RST	

2.1003 SECURITY_ISLAND_RST

Security Island reset -active high, inverted in HW- - Offset: `0x2c` - Reset default: `0x0` - Reset mask: `0x1`

2.1003.1 Fields


```
{"reg": [{"name": "SECURITY_ISLAND_RST", "bits": 1, "attr": ["rw"], "rotate": -90}, {"bits": 3
```


Bits	Type	Reset	Name	Description
31:1				Reserved
0	rw	0x0	SECURITY_ISLAND_RST	

2.1004 PULP_CLUSTER_RST

PULP Cluster reset -active high, inverted in HW- - Offset: `0x30` - Reset default: `0x0` - Reset mask: `0x1`

2.1004.1 Fields


```
{"reg": [{"name": "PULP_CLUSTER_RST", "bits": 1, "attr": ["rw"], "rotate": -90}, {"bits": 31}]
```

Bits	Type	Reset	Name	Description
31:1				Reserved
0	rw	0x0	PULP_CLUSTER_RST	

2.1005 SPATZ_CLUSTER_RST

Spatz Cluster reset -active high, inverted in HW- - Offset: `0x34` - Reset default: `0x0` - Reset mask: `0x1`

2.1005.1 Fields


```
{"reg": [{"name": "SPATZ_CLUSTER_RST", "bits": 1, "attr": ["rw"], "rotate": -90}, {"bits": 31}]
```


Bits	Type	Reset	Name	Description
31:1				Reserved
0	rw	0x0	SPATZ_CLUSTER_RST	

2.1006 L2_RST

L2 reset -active high, inverted in HW- - Offset: `0x38` - Reset default: `0x0` - Reset mask: `0x1`

2.1006.1 Fields


```
{"reg": [{"name": "L2_RST", "bits": 1, "attr": ["rw"], "rotate": -90}, {"bits": 31}], "config"
```


Bits	Type	Reset	Name	Description
31:1				Reserved
0	rw	0x0	L2_RST	

2.1007 PERIPH_ISOLATE

Periph Domain AXI isolate - Offset: `0x3c` - Reset default: `0x0` - Reset mask: `0x1`

2.1007.1 Fields


```
{"reg": [{"name": "PERIPH_ISOLATE", "bits": 1, "attr": ["rw"], "rotate": -90}, {"bits": 31}],
```

Bits	Type	Reset	Name	Description
31:1				Reserved
0	rw	0x0	PERIPH_ISOLATE	

2.1008 SAFETY_ISLAND_ISOLATE

Safety Island AXI isolate - Offset: `0x40` - Reset default: `0x1` - Reset mask: `0x1`

2.1008.1 Fields


```
{"reg": [{"name": "SAFETY_ISLAND_ISOLATE", "bits": 1, "attr": ["rw"], "rotate": -90}, {"bits":
```


Bits	Type	Reset	Name	Description
31:1				Reserved
0	rw	0x1	SAFETY_ISLAND_ISOLATE	

2.1009 SECURITY_ISLAND_ISOLATE

Security Island AXI isolate - Offset: `0x44` - Reset default: `0x1` - Reset mask: `0x1`

2.1009.1 Fields


```
{"reg": [{"name": "SECURITY_ISLAND_ISOLATE", "bits": 1, "attr": ["rw"], "rotate": -90}, {"bits"
```


Bits	Type	Reset	Name	Description
31:1				Reserved
0	rw	0x1	SECURITY_ISLAND_ISOLATE	

2.1010 PULP_CLUSTER_ISOLATE

PULP Cluster AXI isolate - Offset: `0x48` - Reset default: `0x1` - Reset mask: `0x1`

2.1010.1 Fields


```
{"reg": [{"name": "PULP_CLUSTER_ISOLATE", "bits": 1, "attr": ["rw"], "rotate": -90}, {"bits": 3
```


Bits	Type	Reset	Name	Description
31:1				Reserved

Bits	Type	Reset	Name	Description
0	rw	0x1	PULP_CLUSTER_ISOLATE	

2.1011 SPATZ_CLUSTER_ISOLATE

Spatz Cluster AXI isolate - Offset: `0x4c` - Reset default: `0x1` - Reset mask: `0x1`

2.1011.1 Fields


```
{"reg": [{"name": "SPATZ_CLUSTER_ISOLATE", "bits": 1, "attr": ["rw"], "rotate": -90}, {"bits":
```


Bits	Type	Reset	Name	Description
31:1				Reserved
0	rw	0x1	SPATZ_CLUSTER_ISOLATE	

2.1012 L2_ISOLATE

L2 AXI isolate - Offset: `0x50` - Reset default: `0x0` - Reset mask: `0x1`

2.1012.1 Fields


```
{"reg": [{"name": "L2_ISOLATE", "bits": 1, "attr": ["rw"], "rotate": -90}, {"bits": 31}], "con
```


Bits	Type	Reset	Name	Description
31:1				Reserved
0	rw	0x0	L2_ISOLATE	

2.1013 PERIPH_ISOLATE_STATUS

Periph Domain AXI isolate status - Offset: `0x54` - Reset default: `0x0` - Reset mask: `0x1`

2.1013.1 Fields


```
{"reg": [{"name": "PERIPH_ISOLATE_STATUS", "bits": 1, "attr": ["rw"], "rotate": -90}, {"bits":
```


Bits	Type	Reset	Name	Description
31:1				Reserved
0	rw	0x0	PERIPH_ISOLATE_STATUS	

2.1014 SAFETY_ISLAND_ISOLATE_STATUS

Safety Island AXI isolate status - Offset: `0x58` - Reset default: `0x0` - Reset mask: `0x1`

2.1014.1 Fields


```
{"reg": [{"name": "SAFETY_ISLAND_ISOLATE_STATUS", "bits": 1, "attr": ["rw"], "rotate": -90}, {"
```


Bits	Type	Reset	Name	Description
31:1				Reserved
0	rw	0x0	SAFETY_ISLAND_ISOLATE_STATUS	

2.1015 SECURITY_ISLAND_ISOLATE_STATUS

Security Island AXI isolate status - Offset: `0x5c` - Reset default: `0x0` - Reset mask: `0x1`

2.1015.1 Fields


```
{"reg": [{"name": "SECURITY_ISLAND_ISOLATE_STATUS", "bits": 1, "attr": ["rw"], "rotate": -90},
```


Bits	Type	Reset	Name	Description
31:1				Reserved
0	rw	0x0	SECURITY_ISLAND_ISOLATE_STATUS	

2.1016 PULP_CLUSTER_ISOLATE_STATUS

PULP Cluster AXI isolate status - Offset: `0x60` - Reset default: `0x0` - Reset mask: `0x1`

2.1016.1 Fields


```
{"reg": [{"name": "PULP_CLUSTER_ISOLATE_STATUS", "bits": 1, "attr": ["rw"], "rotate": -90}, {"
```


Bits	Type	Reset	Name	Description
31:1				Reserved
0	rw	0x0	PULP_CLUSTER_ISOLATE_STATUS	

2.1017 SPATZ_CLUSTER_ISOLATE_STATUS

Spatz Cluster AXI isolate status - Offset: `0x64` - Reset default: `0x0` - Reset mask: `0x1`

2.1017.1 Fields

{"reg": [{"name": "SPATZ_CLUSTER_ISOLATE_STATUS", "bits": 1, "attr": ["rw"], "rotate": -90}, {

Bits	Type	Reset	Name	Description
31:1				Reserved
0	rw	0x0	SPATZ_CLUSTER_ISOLATE_STATUS	

2.1018 L2_ISOLATE_STATUS

L2 AXI isolate status - Offset: `0x68` - Reset default: `0x0` - Reset mask: `0x1`

2.1018.1 Fields

{"reg": [{"name": "L2_ISOLATE_STATUS", "bits": 1, "attr": ["rw"], "rotate": -90}, {"bits": 31}]

Bits	Type	Reset	Name	Description
31:1				Reserved
0	rw	0x0	L2_ISOLATE_STATUS	

2.1019 PERIPH_CLK_EN

Periph Domain clk gate enable - Offset: `0x6c` - Reset default: `0x1` - Reset mask: `0x1`

2.1019.1 Fields

{"reg": [{"name": "PERIPH_CLK_EN", "bits": 1, "attr": ["rw"], "rotate": -90}, {"bits": 31}], "

Bits	Type	Reset	Name	Description
31:1				Reserved
0	rw	0x1	PERIPH_CLK_EN	

2.1020 SAFETY_ISLAND_CLK_EN

Safety Island clk gate enable - Offset: `0x70` - Reset default: `0x0` - Reset mask: `0x1`

2.1020.1 Fields

{"reg": [{"name": "SAFETY_ISLAND_CLK_EN", "bits": 1, "attr": ["rw"], "rotate": -90}, {"bits": 3

Bits	Type	Reset	Name	Description
31:1				Reserved
0	rw	0x0	SAFETY_ISLAND_CLK_EN	

2.1021 SECURITY_ISLAND_CLK_EN

Security Island clk gate enable - Offset: `0x74` - Reset default: `0x0` - Reset mask: `0x1`

2.1021.1 Fields

{"reg": [{"name": "SECURITY_ISLAND_CLK_EN", "bits": 1, "attr": ["rw"], "rotate": -90}, {"bits"

Bits	Type	Reset	Name	Description
31:1				Reserved
0	rw	0x0	SECURITY_ISLAND_CLK_EN	

2.1022 PULP_CLUSTER_CLK_EN

PULP Cluster clk gate enable - Offset: `0x78` - Reset default: `0x0` - Reset mask: `0x1`

2.1022.1 Fields

{"reg": [{"name": "PULP_CLUSTER_CLK_EN", "bits": 1, "attr": ["rw"], "rotate": -90}, {"bits": 3

Bits	Type	Reset	Name	Description
31:1				Reserved
0	rw	0x0	PULP_CLUSTER_CLK_EN	

2.1023 SPATZ_CLUSTER_CLK_EN

Spatz Cluster clk gate enable - Offset: `0x7c` - Reset default: `0x0` - Reset mask: `0x1`

2.1023.1 Fields

{"reg": [{"name": "SPATZ_CLUSTER_CLK_EN", "bits": 1, "attr": ["rw"], "rotate": -90}, {"bits": 3

Bits	Type	Reset	Name	Description
31:1				Reserved
0	rw	0x0	SPATZ_CLUSTER_CLK_EN	

2.1024 L2_CLK_EN

Shared L2 memory clk gate enable - Offset: `0x80` - Reset default: `0x1` - Reset mask: `0x1`

2.1024.1 Fields

{"reg": [{"name": "L2_CLK_EN", "bits": 1, "attr": ["rw"], "rotate": -90}, {"bits": 31}], "confi

Bits	Type	Reset	Name	Description
31:1				Reserved
0	rw	0x1	L2_CLK_EN	

2.1025 PERIPH_CLK_SEL

Periph Domain pll select (0 -> host pll, 1 -> alt PLL, 2 -> per pll) - Offset: `0x84` - Reset default: `0x2` - Reset mask: `0x3`

2.1025.1 Fields

{"reg": [{"name": "PERIPH_CLK_SEL", "bits": 2, "attr": ["rw"], "rotate": -90}, {"bits": 30}], "

Bits	Type	Reset	Name	Description
31:2				Reserved
1:0	rw	0x2	PERIPH_CLK_SEL	

2.1026 SAFETY_ISLAND_CLK_SEL

Safety Island pll select (0 -> host pll, 1 -> alt PLL, 2 -> per pll) - Offset: `0x88` - Reset default: `0x1` - Reset mask: `0x3`

2.1026.1 Fields

{"reg": [{"name": "SAFETY_ISLAND_CLK_SEL", "bits": 2, "attr": ["rw"], "rotate": -90}, {"bits":

Bits	Type	Reset	Name	Description
31:2				Reserved
1:0	rw	0x1	SAFETY_ISLAND_CLK_SEL	

2.1027 SECURITY_ISLAND_CLK_SEL

Security Island pll select (0 -> host pll, 1 -> alt PLL, 2 -> per pll) - Offset: `0x8c` - Reset default: `0x1` - Reset mask: `0x3`

2.1027.1 Fields

{"reg": [{"name": "SECURITY_ISLAND_CLK_SEL", "bits": 2, "attr": ["rw"], "rotate": -90}, {"bits"

Bits	Type	Reset	Name	Description
31:2				Reserved
1:0	rw	0x1	SECURITY_ISLAND_CLK_SEL	

2.1028 PULP_CLUSTER_CLK_SEL

PULP Cluster pll select (0 -> host pll, 1 -> alt PLL, 2 -> per pll) - Offset: `0x90` - Reset default: `0x1` - Reset mask: `0x3`

2.1028.1 Fields

{"reg": [{"name": "PULP_CLUSTER_CLK_SEL", "bits": 2, "attr": ["rw"], "rotate": -90}, {"bits": 3

Bits	Type	Reset	Name	Description
31:2				Reserved
1:0	rw	0x1	PULP_CLUSTER_CLK_SEL	

2.1029 SPATZ_CLUSTER_CLK_SEL

Spatz Cluster pll select (0 -> host pll, 1 -> alt PLL, 2 -> per pll) - Offset: `0x94` - Reset default: `0x1` - Reset mask: `0x3`

2.1029.1 Fields

{"reg": [{"name": "SPATZ_CLUSTER_CLK_SEL", "bits": 2, "attr": ["rw"], "rotate": -90}, {"bits":

Bits	Type	Reset	Name	Description
31:2				Reserved
1:0	rw	0x1	SPATZ_CLUSTER_CLK_SEL	

2.1030 L2_CLK_SEL

L2 Memory pll select (0 -> host pll, 1 -> alt PLL, 2 -> per pll) - Offset: `0x98` - Reset default: `0x1` - Reset mask: `0x3`

2.1030.1 Fields

{"reg": [{"name": "L2_CLK_SEL", "bits": 2, "attr": ["rw"], "rotate": -90}, {"bits": 30}], "con

Bits	Type	Reset	Name	Description
31:2				Reserved
1:0	rw	0x1	L2_CLK_SEL	

2.1031 PERIPH_CLK_DIV_VALUE

Periph Domain clk divider value - Offset: `0x9c` - Reset default: `0x1` - Reset mask: `0xffffff`

2.1031.1 Fields

{"reg": [{"name": "PERIPH_CLK_DIV_VALUE", "bits": 24, "attr": ["rw"], "rotate": 0}, {"bits": 8

Bits	Type	Reset	Name	Description
31:24				Reserved
23:0	rw	0x1	PERIPH_CLK_DIV_VALUE	

2.1032 SAFETY_ISLAND_CLK_DIV_VALUE

Safety Island clk divider value - Offset: `0xa0` - Reset default: `0x1` - Reset mask: `0xffffff`

2.1032.1 Fields

{"reg": [{"name": "SAFETY_ISLAND_CLK_DIV_VALUE", "bits": 24, "attr": ["rw"], "rotate": 0}, {"bi

Bits	Type	Reset	Name	Description
31:24				Reserved
23:0	rw	0x1	SAFETY_ISLAND_CLK_DIV_VALUE	

2.1033 SECURITY_ISLAND_CLK_DIV_VALUE

Security Island clk divider value - Offset: `0xa4` - Reset default: `0x1` - Reset mask: `0xffffff`

2.1033.1 Fields

{"reg": [{"name": "SECURITY_ISLAND_CLK_DIV_VALUE", "bits": 24, "attr": ["rw"], "rotate": 0}, {"

Bits	Type	Reset	Name	Description
31:24				Reserved
23:0	rw	0x1	SECURITY_ISLAND_CLK_DIV_VALUE	

2.1034 PULP_CLUSTER_CLK_DIV_VALUE

PULP Cluster clk divider value - Offset: `0xa8` - Reset default: `0x1` - Reset mask: `0xffffff`

2.1034.1 Fields

{"reg": [{"name": "PULP_CLUSTER_CLK_DIV_VALUE", "bits": 24, "attr": ["rw"], "rotate": 0}, {"bit

Bits	Type	Reset	Name	Description
31:24				Reserved
23:0	rw	0x1	PULP_CLUSTER_CLK_DIV_VALUE	

2.1035 SPATZ_CLUSTER_CLK_DIV_VALUE

Spatz Cluster clk divider value - Offset: `0xac` - Reset default: `0x1` - Reset mask: `0xffffff`

2.1035.1 Fields

{"reg": [{"name": "SPATZ_CLUSTER_CLK_DIV_VALUE", "bits": 24, "attr": ["rw"], "rotate": 0}, {"bi

Bits	Type	Reset	Name	Description
31:24				Reserved
23:0	rw	0x1	SPATZ_CLUSTER_CLK_DIV_VALUE	

2.1036 L2_CLK_DIV_VALUE

L2 Memory clk divider value - Offset: `0xb0` - Reset default: `0x1` - Reset mask: `0xffffff`

2.1036.1 Fields

{"reg": [{"name": "L2_CLK_DIV_VALUE", "bits": 24, "attr": ["rw"], "rotate": 0}, {"bits": 8}], "

Bits	Type	Reset	Name	Description
31:24				Reserved
23:0	rw	0x1	L2_CLK_DIV_VALUE	

2.1037 HOST_FETCH_ENABLE

Host Domain fetch enable - Offset: `0xb4` - Reset default: `0x0` - Reset mask: `0x1`

2.1037.1 Fields

{"reg": [{"name": "HOST_FETCH_ENABLE", "bits": 1, "attr": ["ro"], "rotate": -90}, {"bits": 31}]

Bits	Type	Reset	Name	Description
31:1				Reserved
0	ro	0x0	HOST_FETCH_ENABLE	

2.1038 SAFETY_ISLAND_FETCH_ENABLE

Safety Island fetch enable - Offset: `0xb8` - Reset default: `0x0` - Reset mask: `0x1`

2.1038.1 Fields

{"reg": [{"name": "SAFETY_ISLAND_FETCH_ENABLE", "bits": 1, "attr": ["rw"], "rotate": -90}, {"bi

Bits	Type	Reset	Name	Description
31:1				Reserved
0	rw	0x0	SAFETY_ISLAND_FETCH_ENABLE	

2.1039 SECURITY_ISLAND_FETCH_ENABLE

Security Island fetch enable - Offset: `0xbc` - Reset default: `0x0` - Reset mask: `0x1`

2.1039.1 Fields

{"reg": [{"name": "SECURITY_ISLAND_FETCH_ENABLE", "bits": 1, "attr": ["rw"], "rotate": -90}, {"

Bits	Type	Reset	Name	Description
31:1				Reserved
0	rw	0x0	SECURITY_ISLAND_FETCH_ENABLE	

2.1040 PULP_CLUSTER_FETCH_ENABLE

PULP Cluster fetch enable - Offset: `0xc0` - Reset default: `0x0` - Reset mask: `0x1`

2.1040.1 Fields

{"reg": [{"name": "PULP_CLUSTER_FETCH_ENABLE", "bits": 1, "attr": ["rw"], "rotate": -90}, {"bit

Bits	Type	Reset	Name	Description
31:1				Reserved
0	rw	0x0	PULP_CLUSTER_FETCH_ENABLE	

2.1041 SPATZ_CLUSTER_DEBUG_REQ

Spatz Cluster debug req - Offset: `0xc4` - Reset default: `0x0` - Reset mask: `0x3`

2.1041.1 Fields

{"reg": [{"name": "SPATZ_CLUSTER_DEBUG_REQ", "bits": 2, "attr": ["rw"], "rotate": -90}, {"bits"

Bits	Type	Reset	Name	Description
31:2				Reserved
1:0	rw	0x0	SPATZ_CLUSTER_DEBUG_REQ	

2.1042 HOST_BOOT_ADDR

Host boot address - Offset: `0xc8` - Reset default: `0x1000` - Reset mask: `0xffffffff`

2.1042.1 Fields

{"reg": [{"name": "HOST_BOOT_ADDR", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lan

Bits	Type	Reset	Name	Description
31:0	rw	0x1000	HOST_BOOT_ADDR	

2.1043 SAFETY_ISLAND_BOOT_ADDR

Safety Island boot address - Offset: `0xcc` - Reset default: `0x70000000` - Reset mask: `0xffffffff`

2.1043.1 Fields

{"reg": [{"name": "SAFETY_ISLAND_BOOT_ADDR", "bits": 32, "attr": ["rw"], "rotate": 0}], "confi

Bits	Type	Reset	Name	Description
31:0	rw	0x70000000	SAFETY_ISLAND_BOOT_ADDR	

2.1044 SECURITY_ISLAND_BOOT_ADDR

Security Island boot address - Offset: `0xd0` - Reset default: `0x70000000` - Reset mask: `0xffffffff`

2.1044.1 Fields

{"reg": [{"name": "SECURITY_ISLAND_BOOT_ADDR", "bits": 32, "attr": ["rw"], "rotate": 0}], "con

Bits	Type	Reset	Name	Description
31:0	rw	0x70000000	SECURITY_ISLAND_BOOT_ADDR	

2.1045 PULP_CLUSTER_BOOT_ADDR

PULP Cluster boot address - Offset: `0xd4` - Reset default: `0x70000000` - Reset mask: `0xffffffff`

2.1045.1 Fields


```
{"reg": [{"name": "PULP_CLUSTER_BOOT_ADDR", "bits": 32, "attr": ["rw"], "rotate": 0}], "config
```


Bits	Type	Reset	Name	Description
31:0	rw	0x70000000	PULP_CLUSTER_BOOT_ADDR	

2.1046 SPATZ_CLUSTER_BOOT_ADDR

Spatz Cluster boot address - Offset: `0xd8` - Reset default: `0x70000000` - Reset mask: `0xffffffff`

2.1046.1 Fields


```
{"reg": [{"name": "SPATZ_CLUSTER_BOOT_ADDR", "bits": 32, "attr": ["rw"], "rotate": 0}], "confi
```


Bits	Type	Reset	Name	Description
31:0	rw	0x70000000	SPATZ_CLUSTER_BOOT_ADDR	

2.1047 PULP_CLUSTER_BOOT_ENABLE

PULP Cluster boot enable - Offset: `0xdc` - Reset default: `0x0` - Reset mask: `0x1`

2.1047.1 Fields


```
{"reg": [{"name": "PULP_CLUSTER_BOOT_ENABLE", "bits": 1, "attr": ["rw"], "rotate": -90}, {"bits
```


Bits	Type	Reset	Name	Description
31:1				Reserved
0	rw	0x0	PULP_CLUSTER_BOOT_ENABLE	

2.1048 SPATZ_CLUSTER_BUSY

Spatz Cluster busy - Offset: `0xe0` - Reset default: `0x0` - Reset mask: `0x1`

2.1048.1 Fields

{"reg": [{"name": "SPATZ_CLUSTER_BUSY", "bits": 1, "attr": ["ro"], "rotate": -90}, {"bits": 31

Bits	Type	Reset	Name	Description
31:1				Reserved
0	ro	0x0	SPATZ_CLUSTER_BUSY	

2.1049 PULP_CLUSTER_BUSY

PULP Cluster busy - Offset: `0xe4` - Reset default: `0x0` - Reset mask: `0x1`

2.1049.1 Fields

{"reg": [{"name": "PULP_CLUSTER_BUSY", "bits": 1, "attr": ["ro"], "rotate": -90}, {"bits": 31}

Bits	Type	Reset	Name	Description
31:1				Reserved
0	ro	0x0	PULP_CLUSTER_BUSY	

2.1050 PULP_CLUSTER_EOC

PULP Cluster end of computation - Offset: `0xe8` - Reset default: `0x0` - Reset mask: `0x1`

2.1050.1 Fields

{"reg": [{"name": "PULP_CLUSTER_EOC", "bits": 1, "attr": ["ro"], "rotate": -90}, {"bits": 31}]

Bits	Type	Reset	Name	Description
31:1				Reserved
0	ro	0x0	PULP_CLUSTER_EOC	

2.1051 ETH_RGMII_PHY_CLK_DIV_EN

Ethernet RGMII PHY clock divider enable bit - Offset: `0xec` - Reset default: `0x1` - Reset mask: `0x1`

2.1051.1 Fields

{"reg": [{"name": "ETH_RGMII_PHY_CLK_DIV_EN", "bits": 1, "attr": ["rw"], "rotate": -90}, {"bits

Bits	Type	Reset	Name	Description
31:1				Reserved
0	rw	0x1	ETH_RGMII_PHY_CLK_DIV_EN	

2.1052 ETH_RGMII_PHY_CLK_DIV_VALUE

Ethernet RGMII PHY clock divider value - Offset: `0xf0` - Reset default: `0x64` - Reset mask: `0xfffff`

2.1052.1 Fields

{"reg": [{"name": "ETH_RGMII_PHY_CLK_DIV_VALUE", "bits": 20, "attr": ["rw"], "rotate": 0}, {"b

Bits	Type	Reset	Name	Description
31:20				Reserved
19:0	rw	0x64	ETH_RGMII_PHY_CLK_DIV_VALUE	

2.1053 ETH_MDIO_CLK_DIV_EN

Ethernet MDIO clock divider enable bit - Offset: `0xf4` - Reset default: `0x1` - Reset mask: `0x1`

2.1053.1 Fields

{"reg": [{"name": "ETH_MDIO_CLK_DIV_EN", "bits": 1, "attr": ["rw"], "rotate": -90}, {"bits": 3

Bits	Type	Reset	Name	Description
31:1				Reserved
0	rw	0x1	ETH_MDIO_CLK_DIV_EN	

2.1054 ETH_MDIO_CLK_DIV_VALUE

Ethernet MDIO clock divider value - Offset: `0xf8` - Reset default: `0x64` - Reset mask: `0xffffff`

2.1054.1 Fields

{"reg": [{"name": "ETH_MDIO_CLK_DIV_VALUE", "bits": 20, "attr": ["rw"], "rotate": 0}, {"bits":

Bits	Type	Reset	Name	Description
31:20				Reserved
19:0	rw	0x64	ETH_MDIO_CLK_DIV_VALUE	

2.1055 cheshire / doc / registers.md

2.1056 Summary

Name	Offset	Length	Description
cheshire.scratch_0	0x0	4	Registers for use by software
cheshire.scratch_1	0x4	4	Registers for use by software
cheshire.scratch_2	0x8	4	Registers for use by software
cheshire.scratch_3	0xc	4	Registers for use by software
cheshire.scratch_4	0x10	4	Registers for use by software
cheshire.scratch_5	0x14	4	Registers for use by software
cheshire.scratch_6	0x18	4	Registers for use by software
cheshire.scratch_7	0x1c	4	Registers for use by software
cheshire.scratch_8	0x20	4	Registers for use by software
cheshire.scratch_9	0x24	4	Registers for use by software
cheshire.scratch_10	0x28	4	Registers for use by software
cheshire.scratch_11	0x2c	4	Registers for use by software
cheshire.scratch_12	0x30	4	Registers for use by software
cheshire.scratch_13	0x34	4	Registers for use by software
cheshire.scratch_14	0x38	4	Registers for use by software
cheshire.scratch_15	0x3c	4	Registers for use by software
cheshire.boot_mode	0x40	4	Method to load boot code (connected to input pins)
cheshire.rtc_freq	0x44	4	Frequency (Hz) configured for RTC
cheshire.platform_rom	0x48	4	Address of platform ROM
cheshire.num_int_harts	0x4c	4	Number of internal harts
cheshire.hw_features	0x50	4	Specifies which hardware features are available
cheshire.llc_size	0x54	4	Total size of LLC in bytes
cheshire.vga_params	0x58	4	VGA hardware parameters

2.1057 scratch

Registers for use by software - Reset default: `0x0` - Reset mask: `0xffffffff`

2.1057.1 Instances

Name	Offset
scratch_0	0x0
scratch_1	0x4
scratch_2	0x8
scratch_3	0xc
scratch_4	0x10
scratch_5	0x14
scratch_6	0x18
scratch_7	0x1c
scratch_8	0x20
scratch_9	0x24
scratch_10	0x28
scratch_11	0x2c
scratch_12	0x30
scratch_13	0x34
scratch_14	0x38
scratch_15	0x3c

2.1057.2 Fields

`{"reg": [{"name": "scratch", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1,`

Bits	Type	Reset	Name	Description
31:0	rw	0x0	scratch	Registers for use by software

2.1058 boot_mode

Method to load boot code (connected to input pins) - Offset: `0x40` - Reset default: `0x0` - Reset mask: `0x3`

2.1058.1 Fields

`{"reg": [{"name": "boot_mode", "bits": 2, "attr": ["ro"], "rotate": -90}, {"bits": 30}], "confi`

Bits	Type	Reset	Name
31:2			Reserved
1:0	ro	x	boot_mode

2.1058.2 boot_mode . boot_mode

Method to load boot code (connected to input pins)

Value	Name	Description
0x0	passive	Wait for external preload and launch
0x1	spi_sdcard	Boot from SD Card in SPI mode
0x2	spi_s25fs512s	Boot from S25FS512S SPI NOR flash
0x3	i2c_24xx1025	Boot from 24xx1025 I2C EEPROM

2.1059 rtc_freq

Frequency (Hz) configured for RTC - Offset: `0x44` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.1059.1 Fields


```
{"reg": [{"name": "ref_freq", "bits": 32, "attr": ["ro"], "rotate": 0}], "config": {"lanes": 1
```


Bits	Type	Reset	Name	Description
31:0	ro	x	ref_freq	Frequency (Hz) configured for RTC

2.1060 platform_rom

Address of platform ROM - Offset: `0x48` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.1060.1 Fields


```
{"reg": [{"name": "platform_rom", "bits": 32, "attr": ["ro"], "rotate": 0}], "config": {"lanes"
```


Bits	Type	Reset	Name	Description
31:0	ro	x	platform_rom	Address of platform ROM

2.1061 num_int_harts

Number of internal harts - Offset: `0x4c` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.1061.1 Fields

{"reg": [{"name": "num_harts", "bits": 32, "attr": ["ro"], "rotate": 0}], "config": {"lanes": 1

Bits	Type	Reset	Name	Description
31:0	ro	x	num_harts	Number of internal harts

2.1062 hw_features

Specifies which hardware features are available - Offset: `0x50` - Reset default: `0x0` - Reset mask: `0x1fff`

2.1062.1 Fields

{"reg": [{"name": "bootrom", "bits": 1, "attr": ["ro"], "rotate": -90}, {"name": "llc", "bits"

Bits	Type	Reset	Name	Description
31:13				Reserved
12	ro	x	bus_err	Whether UNBENT is available
11	ro	x	irq_router	Whether IRQ router is available
10	ro	x	clic	Whether CLIC is available
9	ro	x	axirt	Whether AXI RT is available
8	ro	x	vga	Whether VGA is available
7	ro	x	serial_link	Whether serial link is available
6	ro	x	dma	Whether DMA is available
5	ro	x	gpio	Whether GPIO is available
4	ro	x	i2c	Whether I2C is available
3	ro	x	spi_host	Whether SPI host is available
2	ro	x	uart	Whether UART is available
1	ro	x	llc	Whether LLC is available
0	ro	x	bootrom	Whether boot ROM is available

2.1063 llc_size

Total size of LLC in bytes - Offset: `0x54` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.1063.1 Fields

{"reg": [{"name": "llc_size", "bits": 32, "attr": ["ro"], "rotate": 0}], "config": {"lanes": 1

Bits	Type	Reset	Name	Description
31:0	ro	x	llc_size	Total size of LLC in bytes

2.1064 vga_params

VGA hardware parameters - Offset: `0x58` - Reset default: `0x0` - Reset mask: `0xffffff`

2.1064.1 Fields


```
{"reg": [{"name": "red_width", "bits": 8, "attr": ["ro"], "rotate": 0}, {"name": "green_width"
```


Bits	Type	Reset	Name	Description
31:24				Reserved
23:16	ro	x	blue_width	Blue channel width
15:8	ro	x	green_width	Green channel width
7:0	ro	x	red_width	Red channel width

2.1065 clic / doc / clicint_registers.md

2.1066 Summary

Name	Offset	Length	Description
CLICINT.CLICINT	0x0	4	CLIC interrupt pending, enable, attribute and control

2.1067 CLICINT

CLIC interrupt pending, enable, attribute and control - Offset: `0x0` - Reset default: `0xc00000` - Reset mask: `0xffc70101`

2.1067.1 Fields


```
{"reg": [{"name": "IP", "bits": 1, "attr": ["rw"], "rotate": -90}, {"bits": 7}, {"name": "IE",
```


Bits	Type	Reset	Name	Description
31:24	rw	0x0	CTL	interrupt control for interrupt
23:22	rw	0x3	ATTR_MODE	privilege mode of this interrupt
21:19				Reserved
18:17	rw	0x0	ATTR_TRIG	specify trigger type for this interrupt

Bits	Type	Reset	Name	Description
16	rw	0x0	ATTR_SHV	enable hardware vectoring for this interrupt
15:9				Reserved
8	rw	0x0	IE	interrupt enable for interrupt
7:1				Reserved
0	rw	0x0	IP	interrupt pending for interrupt

2.1068 clic / doc / clictv_registers.md

2.1069 Summary

Name	Offset	Length	Description
CLICINTV.CLICINTV	0x0	4	CLIC interrupt virtualization

2.1070 CLICINTV

CLIC interrupt virtualization - Offset: `0x0` - Reset default: `0x0` - Reset mask: `0xfdfdfdfd`

2.1070.1 Fields

`{"reg": [{"name": "V0", "bits": 1, "attr": ["rw"], "rotate": -90}, {"bits": 1}, {"name": "VSID0`

Bits	Type	Reset	Name	Description
31:26	rw	0x0	VSID3	interrupt VS id
25				Reserved
24	rw	0x0	V3	interrupt delegated to VS-mode
23:18	rw	0x0	VSID2	interrupt VS id
17				Reserved
16	rw	0x0	V2	interrupt delegated to VS-mode
15:10	rw	0x0	VSID1	interrupt VS id
9				Reserved
8	rw	0x0	V1	interrupt delegated to VS-mode
7:2	rw	0x0	VSID0	interrupt VS id
1				Reserved
0	rw	0x0	V0	interrupt delegated to VS-mode

2.1071 clic / doc / clicvs_registers.md

2.1072 Summary

Name	Offset	Length	Description
CLICVS.vsprio	0x0	4	CLIC virtual supervisor priority

2.1073 vsprio

CLIC virtual supervisor priority - Offset: `0x0` - Reset default: `0x0` - Reset mask: `0x1010101`

2.1073.1 Fields

`{"reg": [{"name": "prio0", "bits": 1, "attr": ["rw"], "rotate": -90}, {"bits": 7}, {"name": "pr`

Bits	Type	Reset	Name	Description
31:25				Reserved
24	rw	0x0	prio3	VS3 priority
23:17				Reserved
16	rw	0x0	prio2	VS2 priority
15:9				Reserved
8	rw	0x0	prio1	VS1 priority
7:1				Reserved
0	rw	0x0	prio0	VS0 priority

2.1074 clic / doc / mclic_registers.md

2.1075 Summary

Name	Offset	Length	Description
MCLIC.MCLICCFG	0x0	4	CLIC configuration
MCLIC.CLICMNXTICONF	0x4	4	CLIC enable mnxti irq forwarding logic

2.1076 MCLICCFG

CLIC configuration - Offset: `0x0` - Reset default: `0x0` - Reset mask: `0xff0f003f`

2.1076.1 Fields

`{"reg": [{"name": "mnlbits", "bits": 4, "attr": ["rw"], "rotate": -90}, {"name": "nmbits", "bit`

Bits	Type	Reset	Name	Description
31:28	ro	0x0	reserved	reserved
27:24	rw	0x0	unlbits	number of privilege mode bits in user mode
23:20				Reserved
19:16	rw	0x0	snlbits	number of privilege mode bits in supervisor mode
15:6				Reserved
5:4	rw	0x0	nmbits	number of privilege mode bits
3:0	rw	0x0	mnlbits	number of interrupt level bits in machine mode

2.1077 CLICMNXTICONF

CLIC enable mnxti irq forwarding logic - Offset: `0x4` - Reset default: `0x0` - Reset mask: `0x1`

2.1077.1 Fields

{"reg": [{"name": "CLICMNXTICONF", "bits": 1, "attr": ["rw"], "rotate": -90}, {"bits": 31}], "

Bits	Type	Reset	Name	Description
31:1				Reserved
0	rw	0x0	CLICMNXTICONF	

2.1078 clint / doc / registers.md

2.1079 Summary

Name	Offset	Length	Description
CLINT.MSIP_0	0x0	4	Machine Software Interrupt Pending
CLINT.MSIP_1	0x4	4	Machine Software Interrupt Pending
CLINT.MTIMECMP_LOW0	0x4000	4	Machine Timer Compare for Core 0
CLINT.MTIMECMP_HIGH0	0x4004	4	Machine Timer Compare for Core 0
CLINT.MTIMECMP_LOW1	0x4008	4	Machine Timer Compare for Core 1
CLINT.MTIMECMP_HIGH1	0x400c	4	Machine Timer Compare for Core 1
CLINT.MTIME_LOW	0xbff8	4	Timer Register Low
CLINT.MTIME_HIGH	0xbffc	4	Timer Register High

2.1080 MSIP

Machine Software Interrupt Pending - Reset default: `0x0` - Reset mask: `0xffffffff`

2.1080.1 Instances

Name	Offset
MSIP_0	0x0
MSIP_1	0x4

2.1080.2 Fields

{"reg": [{"name": "P", "bits": 1, "attr": ["rw"], "rotate": -90}, {"name": "RSVD", "bits": 31,

Bits	Type	Reset	Name	Description
31:1	ro	0x0	RSVD	Reserved
0	rw	0x0	P	Machine Software Interrupt Pending

2.1081 MTIMECMP_LOW0

Machine Timer Compare for Core 0 - Offset: `0x4000` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.1081.1 Fields

{"reg": [{"name": "MTIMECMP_LOW", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes"

Bits	Type	Reset	Name	Description
31:0	rw	0x0	MTIMECMP_LOW	Machine Time Compare (Low) Core 0

2.1082 MTIMECMP_HIGH0

Machine Timer Compare for Core 0 - Offset: `0x4004` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.1082.1 Fields

{"reg": [{"name": "MTIMECMP_HIGH", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes

Bits	Type	Reset	Name	Description
31:0	rw	0x0	MTIMECMP_HIGH	Machine Time Compare (High) Core 0

2.1083 MTIMECMP_LOW1

Machine Timer Compare for Core 1 - Offset: `0x4008` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.1083.1 Fields


```
{"reg": [{"name": "MTIMECMP_LOW", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes"
```


Bits	Type	Reset	Name	Description
31:0	rw	0x0	MTIMECMP_LOW	Machine Time Compare (Low) Core 1

2.1084 MTIMECMP_HIGH1

Machine Timer Compare for Core 1 - Offset: `0x400c` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.1084.1 Fields


```
{"reg": [{"name": "MTIMECMP_HIGH", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes
```


Bits	Type	Reset	Name	Description
31:0	rw	0x0	MTIMECMP_HIGH	Machine Time Compare (High) Core 1

2.1085 MTIME_LOW

Timer Register Low - Offset: `0xbff8` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.1085.1 Fields


```
{"reg": [{"name": "MTIME_LOW", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes":
```


Bits	Type	Reset	Name	Description
31:0	rw	0x0	MTIME_LOW	Machine Time (Low)

2.1086 MTIME_HIGH

Timer Register High - Offset: `0xbffc` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.1086.1 Fields

{"reg": [{"name": "MTIME_HIGH", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes":

Bits	Type	Reset	Name	Description
31:0	rw	0x0	MTIME_HIGH	Machine Time (High)

2.1087 cl_event_unit / doc / registers.md

2.1088 Summary

Name	Offset	Length	Description
cluster_event_unit.EVT_MASK	0x0	4	Input event mask configuration register.
cluster_event_unit.EVT_MASK_AND	0x4	4	Input event mask update command register with bitwise AND operation.
cluster_event_unit.EVT_MASK_OR	0x8	4	Input event mask update command register with bitwise OR operation.
cluster_event_unit.IRQ_MASK	0xc	4	Interrupt request mask configuration register.
cluster_event_unit.IRQ_MASK_AND	0x10	4	Interrupt request mask update command register with bitwise AND operation.
cluster_event_unit.IRQ_MASK_OR	0x14	4	Interrupt request mask update command register with bitwise OR operation.
cluster_event_unit.CLOCK_STATUS	0x18	4	Cluster cores clock status register.
cluster_event_unit.EVENT_BUFFER	0x1c	4	Pending input events status register.
cluster_event_unit.EVENT_BUFFER_MASKED	0x20	4	Pending input events status register with EVT_MASK applied.
cluster_event_unit.EVENT_BUFFER_IRQ_MASKED	0x24	4	Pending input events status register with IRQ_MASK applied.
cluster_event_unit.EVENT_BUFFER_CLEAR	0x28	4	Pending input events status clear command register.
cluster_event_unit.SW_EVENT_MASK	0x2c	4	Software events cluster cores destination mask configuration register.
cluster_event_unit.SW_EVENT_MASK_AND	0x30	4	Software events cluster cores destination mask update command register with bitwise AND operation.
cluster_event_unit.SW_EVENT_MASK_OR	0x34	4	Software events cluster cores destination mask update command register with bitwise OR operation.
cluster_event_unit.EVENT_WAIT	0x38	4	Input event wait command register.
cluster_event_unit.EVENT_WAIT_CLEAR	0x3c	4	Input event wait and clear command register.
cluster_event_unit.HW_DISPATCH_PUSH_TASK	0x40	4	Hardware task dispatcher push command register.

Name	Offset	Length	Description
cluster_event_unit.HW_DISPATCH_POP_TASK	0x44	4	Hardware task dispatcher pop command register.
cluster_event_unit.HW_DISPATCH_PUSH_TEAM_CONFIG	0x48	4	Hardware task dispatcher cluster core team configuration register.
cluster_event_unit.HW_MUTEX_0_MSG_PUT	0x4c	4	Hardware mutex 0 non-blocking put command register.
cluster_event_unit.HW_MUTEX_0_MSG_GET	0x50	4	Hardware mutex 0 blocking get command register.
cluster_event_unit.HW_MUTEX_1_MSG_PUT	0x54	4	Hardware mutex 1 non-blocking put command register.
cluster_event_unit.HW_MUTEX_1_MSG_GET	0x58	4	Hardware mutex 1 blocking get command register.
cluster_event_unit.SW_EVENT_0_TRIG	0x5c	4	Cluster Software event 0 trigger command register.
cluster_event_unit.SW_EVENT_1_TRIG	0x60	4	Cluster Software event 1 trigger command register.
cluster_event_unit.SW_EVENT_2_TRIG	0x64	4	Cluster Software event 2 trigger command register.
cluster_event_unit.SW_EVENT_3_TRIG	0x68	4	Cluster Software event 3 trigger command register.
cluster_event_unit.SW_EVENT_4_TRIG	0x6c	4	Cluster Software event 4 trigger command register.
cluster_event_unit.SW_EVENT_5_TRIG	0x70	4	Cluster Software event 5 trigger command register.
cluster_event_unit.SW_EVENT_6_TRIG	0x74	4	Cluster Software event 6 trigger command register.
cluster_event_unit.SW_EVENT_7_TRIG	0x78	4	Cluster Software event 7 trigger command register.
cluster_event_unit.SW_EVENT_0_TRIG_WAIT	0x7c	4	Cluster Software event 0 trigger and wait command register.
cluster_event_unit.SW_EVENT_1_TRIG_WAIT	0x80	4	Cluster Software event 1 trigger and wait command register.
cluster_event_unit.SW_EVENT_2_TRIG_WAIT	0x84	4	Cluster Software event 2 trigger and wait command register.
cluster_event_unit.SW_EVENT_3_TRIG_WAIT	0x88	4	Cluster Software event 3 trigger and wait command register.
cluster_event_unit.SW_EVENT_4_TRIG_WAIT	0x8c	4	Cluster Software event 4 trigger and wait command register.
cluster_event_unit.SW_EVENT_5_TRIG_WAIT	0x90	4	Cluster Software event 5 trigger and wait command register.
cluster_event_unit.SW_EVENT_6_TRIG_WAIT	0x94	4	Cluster Software event 6 trigger and wait command register.
cluster_event_unit.SW_EVENT_7_TRIG_WAIT	0x98	4	Cluster Software event 7 trigger and wait command register.
cluster_event_unit.SW_EVENT_0_TRIG_WAIT_CLEAR	0x9c	4	Cluster Software event 0 trigger, wait and clear command register.

Name	Offset	Length	Description
cluster_event_unit.SW_EVENT_1_TRIG_WAIT_CLEAR	0x10	4	Cluster Software event 1 trigger, wait and clear command register.
cluster_event_unit.SW_EVENT_2_TRIG_WAIT_CLEAR	0x14	4	Cluster Software event 2 trigger, wait and clear command register.
cluster_event_unit.SW_EVENT_3_TRIG_WAIT_CLEAR	0x18	4	Cluster Software event 3 trigger, wait and clear command register.
cluster_event_unit.SW_EVENT_4_TRIG_WAIT_CLEAR	0x1c	4	Cluster Software event 4 trigger, wait and clear command register.
cluster_event_unit.SW_EVENT_5_TRIG_WAIT_CLEAR	0x20	4	Cluster Software event 5 trigger, wait and clear command register.
cluster_event_unit.SW_EVENT_6_TRIG_WAIT_CLEAR	0x24	4	Cluster Software event 6 trigger, wait and clear command register.
cluster_event_unit.SW_EVENT_7_TRIG_WAIT_CLEAR	0x28	4	Cluster Software event 7 trigger, wait and clear command register.
cluster_event_unit.SOC_PERIPH_EVENT_ID	0x3c	4	Cluster SoC peripheral event ID status register.
cluster_event_unit.HW_BARRIER_0_TRIG_MASK	0x40	4	Cluster hardware barrier 0 trigger mask configuration register.
cluster_event_unit.HW_BARRIER_1_TRIG_MASK	0x44	4	Cluster hardware barrier 1 trigger mask configuration register.
cluster_event_unit.HW_BARRIER_2_TRIG_MASK	0x48	4	Cluster hardware barrier 2 trigger mask configuration register.
cluster_event_unit.HW_BARRIER_3_TRIG_MASK	0x4c	4	Cluster hardware barrier 3 trigger mask configuration register.
cluster_event_unit.HW_BARRIER_4_TRIG_MASK	0x50	4	Cluster hardware barrier 4 trigger mask configuration register.
cluster_event_unit.HW_BARRIER_5_TRIG_MASK	0x54	4	Cluster hardware barrier 5 trigger mask configuration register.
cluster_event_unit.HW_BARRIER_6_TRIG_MASK	0x58	4	Cluster hardware barrier 6 trigger mask configuration register.
cluster_event_unit.HW_BARRIER_7_TRIG_MASK	0x5c	4	Cluster hardware barrier 7 trigger mask configuration register.
cluster_event_unit.HW_BARRIER_0_STATUS	0x80	4	Cluster hardware barrier 0 status register.
cluster_event_unit.HW_BARRIER_1_STATUS	0x84	4	Cluster hardware barrier 1 status register.
cluster_event_unit.HW_BARRIER_2_STATUS	0x88	4	Cluster hardware barrier 2 status register.
cluster_event_unit.HW_BARRIER_3_STATUS	0x8c	4	Cluster hardware barrier 3 status register.
cluster_event_unit.HW_BARRIER_4_STATUS	0x90	4	Cluster hardware barrier 4 status register.
cluster_event_unit.HW_BARRIER_5_STATUS	0x94	4	Cluster hardware barrier 5 status register.
cluster_event_unit.HW_BARRIER_6_STATUS	0x98	4	Cluster hardware barrier 6 status register.
cluster_event_unit.HW_BARRIER_7_STATUS	0x9c	4	Cluster hardware barrier 7 status register.
cluster_event_unit.HW_BARRIER_0_STATUS_SUM	0x100	4	Cluster hardware barrier summary status register.
cluster_event_unit.HW_BARRIER_1_STATUS_SUM	0x104	4	Cluster hardware barrier summary status register.
cluster_event_unit.HW_BARRIER_2_STATUS_SUM	0x108	4	Cluster hardware barrier summary status register.

Name	Offset	Length	Description
cluster_event_unit.HW_BARRIER_3_STATUS_SUM	0x10c	4	Cluster hardware barrier summary status register.
cluster_event_unit.HW_BARRIER_4_STATUS_SUM	0x110	4	Cluster hardware barrier summary status register.
cluster_event_unit.HW_BARRIER_5_STATUS_SUM	0x114	4	Cluster hardware barrier summary status register.
cluster_event_unit.HW_BARRIER_6_STATUS_SUM	0x118	4	Cluster hardware barrier summary status register.
cluster_event_unit.HW_BARRIER_7_STATUS_SUM	0x11c	4	Cluster hardware barrier summary status register.
cluster_event_unit.HW_BARRIER_0_TARGET_MASK	0x120	4	Cluster hardware barrier 0 target mask configuration register.
cluster_event_unit.HW_BARRIER_1_TARGET_MASK	0x124	4	Cluster hardware barrier 1 target mask configuration register.
cluster_event_unit.HW_BARRIER_2_TARGET_MASK	0x128	4	Cluster hardware barrier 2 target mask configuration register.
cluster_event_unit.HW_BARRIER_3_TARGET_MASK	0x12c	4	Cluster hardware barrier 3 target mask configuration register.
cluster_event_unit.HW_BARRIER_4_TARGET_MASK	0x130	4	Cluster hardware barrier 4 target mask configuration register.
cluster_event_unit.HW_BARRIER_5_TARGET_MASK	0x134	4	Cluster hardware barrier 5 target mask configuration register.
cluster_event_unit.HW_BARRIER_6_TARGET_MASK	0x138	4	Cluster hardware barrier 6 target mask configuration register.
cluster_event_unit.HW_BARRIER_7_TARGET_MASK	0x13c	4	Cluster hardware barrier 7 target mask configuration register.
cluster_event_unit.HW_BARRIER_0_TRIG	0x140	4	Cluster hardware barrier 0 trigger command register.
cluster_event_unit.HW_BARRIER_1_TRIG	0x144	4	Cluster hardware barrier 1 trigger command register.
cluster_event_unit.HW_BARRIER_2_TRIG	0x148	4	Cluster hardware barrier 2 trigger command register.
cluster_event_unit.HW_BARRIER_3_TRIG	0x14c	4	Cluster hardware barrier 3 trigger command register.
cluster_event_unit.HW_BARRIER_4_TRIG	0x150	4	Cluster hardware barrier 4 trigger command register.
cluster_event_unit.HW_BARRIER_5_TRIG	0x154	4	Cluster hardware barrier 5 trigger command register.
cluster_event_unit.HW_BARRIER_6_TRIG	0x158	4	Cluster hardware barrier 6 trigger command register.
cluster_event_unit.HW_BARRIER_7_TRIG	0x15c	4	Cluster hardware barrier 7 trigger command register.
cluster_event_unit.HW_BARRIER_0_SELF_TRIG	0x160	4	Cluster hardware barrier 0 self trigger command register.
cluster_event_unit.HW_BARRIER_1_SELF_TRIG	0x164	4	Cluster hardware barrier 1 self trigger command register.

Name	Offset	Length	Description
cluster_event_unit.HW_BARRIER_2_SELF_TRIG	0x1168	4	Cluster hardware barrier 2 self trigger command register.
cluster_event_unit.HW_BARRIER_3_SELF_TRIG	0x116C	4	Cluster hardware barrier 3 self trigger command register.
cluster_event_unit.HW_BARRIER_4_SELF_TRIG	0x1170	4	Cluster hardware barrier 4 self trigger command register.
cluster_event_unit.HW_BARRIER_5_SELF_TRIG	0x1174	4	Cluster hardware barrier 5 self trigger command register.
cluster_event_unit.HW_BARRIER_6_SELF_TRIG	0x1178	4	Cluster hardware barrier 6 self trigger command register.
cluster_event_unit.HW_BARRIER_7_SELF_TRIG	0x117C	4	Cluster hardware barrier 7 self trigger command register.
cluster_event_unit.HW_BARRIER_0_TRIGWAIT	0x1180	4	Cluster hardware barrier 0 trigger and wait command register.
cluster_event_unit.HW_BARRIER_1_TRIGWAIT	0x1184	4	Cluster hardware barrier 1 trigger and wait command register.
cluster_event_unit.HW_BARRIER_2_TRIGWAIT	0x1188	4	Cluster hardware barrier 2 trigger and wait command register.
cluster_event_unit.HW_BARRIER_3_TRIGWAIT	0x118C	4	Cluster hardware barrier 3 trigger and wait command register.
cluster_event_unit.HW_BARRIER_4_TRIGWAIT	0x1190	4	Cluster hardware barrier 4 trigger and wait command register.
cluster_event_unit.HW_BARRIER_5_TRIGWAIT	0x1194	4	Cluster hardware barrier 5 trigger and wait command register.
cluster_event_unit.HW_BARRIER_6_TRIGWAIT	0x1198	4	Cluster hardware barrier 6 trigger and wait command register.
cluster_event_unit.HW_BARRIER_7_TRIGWAIT	0x119C	4	Cluster hardware barrier 7 trigger and wait command register.
cluster_event_unit.HW_BARRIER_0_TRIGWAIT_CLEAR	0x11A0	4	Cluster hardware barrier 0 trigger, wait and clear command register.
cluster_event_unit.HW_BARRIER_1_TRIGWAIT_CLEAR	0x11A4	4	Cluster hardware barrier 1 trigger, wait and clear command register.
cluster_event_unit.HW_BARRIER_2_TRIGWAIT_CLEAR	0x11A8	4	Cluster hardware barrier 2 trigger, wait and clear command register.
cluster_event_unit.HW_BARRIER_3_TRIGWAIT_CLEAR	0x11AC	4	Cluster hardware barrier 3 trigger, wait and clear command register.
cluster_event_unit.HW_BARRIER_4_TRIGWAIT_CLEAR	0x11B0	4	Cluster hardware barrier 4 trigger, wait and clear command register.
cluster_event_unit.HW_BARRIER_5_TRIGWAIT_CLEAR	0x11B4	4	Cluster hardware barrier 5 trigger, wait and clear command register.
cluster_event_unit.HW_BARRIER_6_TRIGWAIT_CLEAR	0x11B8	4	Cluster hardware barrier 6 trigger, wait and clear command register.
cluster_event_unit.HW_BARRIER_7_TRIGWAIT_CLEAR	0x11BC	4	Cluster hardware barrier 7 trigger, wait and clear command register.

2.1089 EVT_MASK

Input event mask configuration register. - Offset: `0x0` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.1089.1 Fields

`{"reg": [{"name": "EMCL", "bits": 30, "attr": ["rw"], "rotate": 0}, {"name": "EMINTCL", "bits"`

Bits	Type	Reset	Name	Description
31	rw	0x0	EMSOC	Soc peripheral input event mask configuration bitfield: - EMSOC[i]=1'b0: Input event request i is masked - EMSOC[i]=1'b1: Input event request i is not masked
30	rw	0x0	EMINTCL	Inter-cluster input event mask configuration bitfield: - EMINTCL[i]=1'b0: Input event request i is masked - EMINTCL[i]=1'b1: Input event request i is not masked
29:0	rw	0x0	EMCL	Cluster internal input event mask configuration bitfield: - EMCL[i]=1'b0: Input event request i is masked - EMCL[i]=1'b1: Input event request i is not masked

2.1090 EVT_MASK_AND

Input event mask update command register with bitwise AND operation. - Offset: `0x4` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.1090.1 Fields

`{"reg": [{"name": "EMA", "bits": 32, "attr": ["wo"], "rotate": 0}], "config": {"lanes": 1, "fo`

Bits	Type	Reset	Name	Description
31:0	wo	0x0	EMA	Input event mask configuration bitfield update with bitwise AND operation. It allows clearing EMCL[i], EMINTCL[i] or EMSOC[i] if EMA[i]=1'b1.

2.1091 EVT_MASK_OR

Input event mask update command register with bitwise OR operation. - Offset: `0x8` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.1091.1 Fields

{"reg": [{"name": "EMO", "bits": 32, "attr": ["wo"], "rotate": 0}], "config": {"lanes": 1, "fo

Bits	Type	Reset	Name	Description
31:0	wo	0x0	EMO	Input event mask configuration bitfield update with bitwise OR operation. It allows setting EMCL[i], EMINTCL[i] or EMSOC[i] if EMO[i]=1'b1.

2.1092 IRQ_MASK

Interrupt request mask configuration register. - Offset: `0xc` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.1092.1 Fields

{"reg": [{"name": "IMCL", "bits": 30, "attr": ["rw"], "rotate": 0}, {"name": "IMINTCL", "bits"

Bits	Type	Reset	Name	Description
31	rw	0x0	IMSOC	Soc peripheral interrupt request mask configuration bitfield: - bit[i]=1'b0: Interrupt request i is masked - bit[i]=1'b1: Interrupt request i is not masked
30	rw	0x0	IMINTCL	Inter-cluster interrupt request mask configuration bitfield: - bit[i]=1'b0: Interrupt request i is masked - bit[i]=1'b1: Interrupt request i is not masked
29:0	rw	0x0	IMCL	Cluster internal interrupt request mask configuration bitfield: - bit[i]=1'b0: Interrupt request i is masked - bit[i]=1'b1: Interrupt request i is not masked

2.1093 IRQ_MASK_AND

Interrupt request mask update command register with bitwise AND operation. - Offset: `0x10` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.1093.1 Fields

{"reg": [{"name": "IMA", "bits": 32, "attr": ["wo"], "rotate": 0}], "config": {"lanes": 1, "fo

Bits	Type	Reset	Name	Description
31:0	wo	0x0	IMA	Interrupt request mask configuration bitfield update with bitwise AND operation. It allows clearing IMCL[i], IMINTCL[i] or IMSOC[i] if IMA[i]=1'b1.

2.1094 IRQ_MASK_OR

Interrupt request mask update command register with bitwise OR operation. - Offset: `0x14` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.1094.1 Fields

`{"reg": [{"name": "IMO", "bits": 32, "attr": ["wo"], "rotate": 0}], "config": {"lanes": 1, "fo`

Bits	Type	Reset	Name	Description
31:0	wo	0x0	IMO	Interrupt request mask configuration bitfield update with bitwise OR operation. It allows setting IMCL[i], IMINTCL[i] or IMSOC[i] if IMO[i]=1'b1.

2.1095 CLOCK_STATUS

Cluster cores clock status register. - Offset: `0x18` - Reset default: `0x0` - Reset mask: `0x1`

2.1095.1 Fields

`{"reg": [{"name": "CS", "bits": 1, "attr": ["ro"], "rotate": -90}, {"bits": 31}], "config": {"`

Bits	Type	Reset	Name	Description
31:1				Reserved
0	ro	0x0	CS	Cluster core clock status bitfield: - 1'b0: Cluster core clocked is gated - 1'b1: Cluster core clocked is running

2.1096 EVENT_BUFFER

Pending input events status register. - Offset: `0x1c` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.1096.1 Fields

{"reg": [{"name": "EB", "bits": 32, "attr": ["ro"], "rotate": 0}], "config": {"lanes": 1, "font

Bits	Type	Reset	Name	Description
31:0	ro	0x0	EB	Pending input events status bitfield. EB[i]=1'b1: one or more input event i request are pending.

2.1097 EVENT_BUFFER_MASKED

Pending input events status register with EVT_MASK applied. - Offset: `0x20` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.1097.1 Fields

{"reg": [{"name": "EBM", "bits": 32, "attr": ["ro"], "rotate": 0}], "config": {"lanes": 1, "fon

Bits	Type	Reset	Name	Description
31:0	ro	0x0	EBM	Pending input events status bitfield with EVT_MASK applied. EBM[i]=1'b1: one or more input event i request are pending.

2.1098 EVENT_BUFFER_IRQ_MASKED

Pending input events status register with IRQ_MASK applied. - Offset: `0x24` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.1098.1 Fields

{"reg": [{"name": "IBM", "bits": 32, "attr": ["ro"], "rotate": 0}], "config": {"lanes": 1, "fon

Bits	Type	Reset	Name	Description
31:0	ro	0x0	IBM	Pending input events status bitfield with IRQ_MASK applied. IBM[i]=1'b1: one or more input events i are pending.

2.1099 EVENT_BUFFER_CLEAR

Pending input events status clear command register. - Offset: `0x28` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.1099.1 Fields

{"reg": [{"name": "EBC", "bits": 32, "attr": ["wo"], "rotate": 0}], "config": {"lanes": 1, "fo

Bits	Type	Reset	Name	Description
31:0	wo	0x0	EBC	Pending input events status clear command bitfield. It allows clearing EB[i] if EBC[i]=1'b1.

2.1100 SW_EVENT_MASK

Software events cluster cores destination mask configuration register. - Offset: `0x2c` - Reset default: `0x0` - Reset mask: `0xff`

2.1100.1 Fields

{"reg": [{"name": "SWEM", "bits": 8, "attr": ["rw"], "rotate": 0}, {"bits": 24}], "config": {"

Bits	Type	Reset	Name	Description
31:8				Reserved
7:0	rw	0x0	SWEM	Software events mask configuration bitfield: - bit[i]=1'b0: software events are masked for CL_CORE[i] - bit[i]=1'b1: software events are not masked for CL_CORE[i]

2.1101 SW_EVENT_MASK_AND

Software events cluster cores destination mask update command register with bitwise AND operation. - Offset: `0x30` - Reset default: `0x0` - Reset mask: `0xff`

2.1101.1 Fields

{"reg": [{"name": "SWEMA", "bits": 8, "attr": ["wo"], "rotate": 0}, {"bits": 24}], "config": {

Bits	Type	Reset	Name	Description
31:8				Reserved
7:0	wo	0x0	SWEMA	Software event mask configuration bitfield update with bitwise AND operation. It allows clearing SWEM[i] if SWEMA[i]=1'b1.

2.1102 SW_EVENT_MASK_OR

Software events cluster cores destination mask update command register with bitwise OR operation. - Offset: `0x34` - Reset default: `0x0` - Reset mask: `0xff`

2.1102.1 Fields

{"reg": [{"name": "SWEMO", "bits": 8, "attr": ["wo"], "rotate": 0}, {"bits": 24}], "config": {"

Bits	Type	Reset	Name	Description
31:8				Reserved
7:0	wo	0x0	SWEMO	Software event mask configuration bitfield update with bitwise OR operation. It allows setting SWEM[i] if SWEMO[i]=1'b1.

2.1103 EVENT_WAIT

Input event wait command register. - Offset: `0x38` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.1103.1 Fields

{"reg": [{"name": "EBM", "bits": 32, "attr": ["ro"], "rotate": 0}], "config": {"lanes": 1, "for

Bits	Type	Reset	Name	Description
31:0	ro	0x0	EBM	Reading this register will gate the Cluster core clock until at least one unmasked event occurs. The read content of this bitfield is equivalent to EVENT_BUFFER_MASKED.EBM

2.1104 EVENT_WAIT_CLEAR

Input event wait and clear command register. - Offset: `0x3c` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.1104.1 Fields

{"reg": [{"name": "EBM", "bits": 32, "attr": ["ro"], "rotate": 0}], "config": {"lanes": 1, "for

Bits	Type	Reset	Name	Description
31:0	ro	0x0	EBM	Reading this register has the same effect as reading EVENT_WAIT.EBM. In addition, EVENT_BUFFER.EB[i] bits are cleared if EVT_MASK[i]=1'b1. The read content of this bitfield is equivalent to EVENT_BUFFER_MASKED.EBM

2.1105 HW_DISPATCH_PUSH_TASK

Hardware task dispatcher push command register. - Offset: `0x40` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.1105.1 Fields

{"reg": [{"name": "MSG", "bits": 32, "attr": ["wo"], "rotate": 0}], "config": {"lanes": 1, "fo

Bits	Type	Reset	Name	Description
31:0	wo	0x0	MSG	Message to dispatch to all cluster cores selected in HW_DISPATCH_PUSH_TEAM_CONFIG.CT configuration bitfield.

2.1106 HW_DISPATCH_POP_TASK

Hardware task dispatcher pop command register. - Offset: `0x44` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.1106.1 Fields

{"reg": [{"name": "MSG", "bits": 32, "attr": ["ro"], "rotate": 0}], "config": {"lanes": 1, "fo

Bits	Type	Reset	Name	Description
31:0	ro	0x0	MSG	Message dispatched using HW_DISPATCH_PUSH_TASK command and popped by cluster core who issued HW_DISPATCH_POP_TASK command.

2.1107 HW_DISPATCH_PUSH_TEAM_CONFIG

Hardware task dispatcher cluster core team configuration register. - Offset: `0x48` - Reset default: `0x0` - Reset mask: `0xff`

2.1107.1 Fields

{"reg": [{"name": "CT", "bits": 8, "attr": ["rw"], "rotate": 0}, {"bits": 24}], "config": {"la

Bits	Type	Reset	Name	Description
31:8				Reserved
7:0	rw	0x0	CT	Cluster cores team selection configuration bitfield. It allows to transmit HW_DISPATCH_PUSH_TASK.MSG to cluster core i if CT[i]=1'b1.

2.1108 HW_MUTEX_0_MSG_PUT

Hardware mutex 0 non-blocking put command register. - Offset: `0x4c` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.1108.1 Fields

{"reg": [{"name": "MSG", "bits": 32, "attr": ["wo"], "rotate": 0}], "config": {"lanes": 1, "fo

Bits	Type	Reset	Name	Description
31:0	wo	0x0	MSG	Message pushed when releasing hardware mutex 0 configuration bitfiled. It is a non-blocking access.

2.1109 HW_MUTEX_0_MSG_GET

Hardware mutex 0 blocking get command register. - Offset: `0x50` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.1109.1 Fields

{"reg": [{"name": "MSG", "bits": 32, "attr": ["ro"], "rotate": 0}], "config": {"lanes": 1, "fo

Bits	Type	Reset	Name	Description
31:0	ro	0x0	MSG	Message popped when taking hardware mutex 0 data bitfiled. It is a blocking access.

2.1110 HW_MUTEX_1_MSG_PUT

Hardware mutex 1 non-blocking put command register. - Offset: `0x54` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.1110.1 Fields

{"reg": [{"name": "MSG", "bits": 32, "attr": ["wo"], "rotate": 0}], "config": {"lanes": 1, "fo

Bits	Type	Reset	Name	Description
31:0	wo	0x0	MSG	Message pushed when releasing hardware mutex 1 configuration bitfiled. It is a non-blocking access.

2.1111 HW_MUTEX_1_MSG_GET

Hardware mutex 1 blocking get command register. - Offset: `0x58` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.1111.1 Fields

{"reg": [{"name": "MSG", "bits": 32, "attr": ["ro"], "rotate": 0}], "config": {"lanes": 1, "fo

Bits	Type	Reset	Name	Description
31:0	ro	0x0	MSG	Message popped when taking hardware mutex 1 data bitfiled. It is a blocking access.

2.1112 SW_EVENT_0_TRIG

Cluster Software event 0 trigger command register. - Offset: `0x5c` - Reset default: `0x0` - Reset mask: `0xff`

2.1112.1 Fields

{"reg": [{"name": "SW0T", "bits": 8, "attr": ["wo"], "rotate": 0}, {"bits": 24}], "config": {"

Bits	Type	Reset	Name	Description
31:8				Reserved
7:0	wo	0x0	SW0T	Triggers software event 0 for cluster core i if SW0T[i]=1'b1.

2.1113 SW_EVENT_1_TRIG

Cluster Software event 1 trigger command register. - Offset: `0x60` - Reset default: `0x0` - Reset mask: `0xff`

2.1113.1 Fields

{"reg": [{"name": "SW1T", "bits": 8, "attr": ["wo"], "rotate": 0}, {"bits": 24}], "config": {"

Bits	Type	Reset	Name	Description
31:8				Reserved
7:0	wo	0x0	SW1T	Triggers software event 1 for cluster core i if SW1T[i]=1'b1.

2.1114 SW_EVENT_2_TRIG

Cluster Software event 2 trigger command register. - Offset: `0x64` - Reset default: `0x0` - Reset mask: `0xff`

2.1114.1 Fields

{"reg": [{"name": "SW2T", "bits": 8, "attr": ["wo"], "rotate": 0}, {"bits": 24}], "config": {"

Bits	Type	Reset	Name	Description
31:8				Reserved
7:0	wo	0x0	SW2T	Triggers software event 2 for cluster core i if SW2T[i]=1'b1.

2.1115 SW_EVENT_3_TRIG

Cluster Software event 3 trigger command register. - Offset: `0x68` - Reset default: `0x0` - Reset mask: `0xff`

2.1115.1 Fields

{"reg": [{"name": "SW3T", "bits": 8, "attr": ["wo"], "rotate": 0}, {"bits": 24}], "config": {"

Bits	Type	Reset	Name	Description
31:8				Reserved
7:0	wo	0x0	SW3T	Triggers software event 3 for cluster core i if SW3T[i]=1'b1.

2.1116 SW_EVENT_4_TRIG

Cluster Software event 4 trigger command register. - Offset: `0x6c` - Reset default: `0x0` - Reset mask: `0xff`

2.1116.1 Fields

{"reg": [{"name": "SW4T", "bits": 8, "attr": ["wo"], "rotate": 0}, {"bits": 24}], "config": {"

Bits	Type	Reset	Name	Description
31:8				Reserved
7:0	wo	0x0	SW4T	Triggers software event 4 for cluster core i if SW4T[i]=1'b1.

2.1117 SW_EVENT_5_TRIG

Cluster Software event 5 trigger command register. - Offset: `0x70` - Reset default: `0x0` - Reset mask: `0xff`

2.1117.1 Fields

{"reg": [{"name": "SW5T", "bits": 8, "attr": ["wo"], "rotate": 0}, {"bits": 24}], "config": {"

Bits	Type	Reset	Name	Description
31:8				Reserved
7:0	wo	0x0	SW5T	Triggers software event 5 for cluster core i if SW5T[i]=1'b1.

2.1118 SW_EVENT_6_TRIG

Cluster Software event 6 trigger command register. - Offset: `0x74` - Reset default: `0x0` - Reset mask: `0xff`

2.1118.1 Fields

{"reg": [{"name": "SW6T", "bits": 8, "attr": ["wo"], "rotate": 0}, {"bits": 24}], "config": {"

Bits	Type	Reset	Name	Description
31:8				Reserved
7:0	wo	0x0	SW6T	Triggers software event 6 for cluster core i if SW6T[i]=1'b1.

2.1119 SW_EVENT_7_TRIG

Cluster Software event 7 trigger command register. - Offset: `0x78` - Reset default: `0x0` - Reset mask: `0xff`

2.1119.1 Fields

{"reg": [{"name": "SW7T", "bits": 8, "attr": ["wo"], "rotate": 0}, {"bits": 24}], "config": {"

Bits	Type	Reset	Name	Description
31:8				Reserved
7:0	wo	0x0	SW7T	Triggers software event 7 for cluster core i if SW7T[i]=1'b1.

2.1120 SW_EVENT_0_TRIG_WAIT

Cluster Software event 0 trigger and wait command register. - Offset: `0x7c` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.1120.1 Fields

{"reg": [{"name": "EBM", "bits": 32, "attr": ["ro"], "rotate": 0}], "config": {"lanes": 1, "fo

Bits	Type	Reset	Name	Description
31:0	ro	0x0	EBM	Triggers software event 0 to all cluster cores targeted in SW_EVENT_MASK and gate the issuing cluster core clock until at least one unmasked event occurs. The read content of this bitfield is equivalent to EVENT_BUFFER_MASKED.EBM

2.1121 SW_EVENT_1_TRIG_WAIT

Cluster Software event 1 trigger and wait command register. - Offset: `0x80` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.1121.1 Fields

{"reg": [{"name": "EBM", "bits": 32, "attr": ["ro"], "rotate": 0}], "config": {"lanes": 1, "fo

Bits	Type	Reset	Name	Description
31:0	ro	0x0	EBM	Triggers software event 1 to all cluster cores targeted in SW_EVENT_MASK and gate the issuing cluster core clock until at least one unmasked event occurs. The read content of this bitfield is equivalent to EVENT_BUFFER_MASKED.EBM

2.1122 SW_EVENT_2_TRIG_WAIT

Cluster Software event 2 trigger and wait command register. - Offset: `0x84` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.1122.1 Fields

{"reg": [{"name": "EBM", "bits": 32, "attr": ["ro"], "rotate": 0}], "config": {"lanes": 1, "fo

Bits	Type	Reset	Name	Description
31:0	ro	0x0	EBM	Triggers software event 2 to all cluster cores targeted in SW_EVENT_MASK and gate the issuing cluster core clock until at least one unmasked event occurs. The read content of this bitfield is equivalent to EVENT_BUFFER_MASKED.EBM

2.1123 SW_EVENT_3_TRIG_WAIT

Cluster Software event 3 trigger and wait command register. - Offset: `0x88` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.1123.1 Fields

{"reg": [{"name": "EBM", "bits": 32, "attr": ["ro"], "rotate": 0}], "config": {"lanes": 1, "fo

Bits	Type	Reset	Name	Description
31:0	ro	0x0	EBM	Triggers software event 3 to all cluster cores targeted in SW_EVENT_MASK and gate the issuing cluster core clock until at least one unmasked event occurs. The read content of this bitfield is equivalent to EVENT_BUFFER_MASKED.EBM

2.1124 SW_EVENT_4_TRIG_WAIT

Cluster Software event 4 trigger and wait command register. - Offset: `0x8c` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.1124.1 Fields

{"reg": [{"name": "EBM", "bits": 32, "attr": ["ro"], "rotate": 0}], "config": {"lanes": 1, "fo

Bits	Type	Reset	Name	Description
31:0	ro	0x0	EBM	Triggers software event 4 to all cluster cores targeted in SW_EVENT_MASK and gate the issuing cluster core clock until at least one unmasked event occurs. The read content of this bitfield is equivalent to EVENT_BUFFER_MASKED.EBM

2.1125 SW_EVENT_5_TRIG_WAIT

Cluster Software event 5 trigger and wait command register. - Offset: `0x90` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.1125.1 Fields

{"reg": [{"name": "EBM", "bits": 32, "attr": ["ro"], "rotate": 0}], "config": {"lanes": 1, "fo

Bits	Type	Reset	Name	Description
31:0	ro	0x0	EBM	Triggers software event 5 to all cluster cores targeted in SW_EVENT_MASK and gate the issuing cluster core clock until at least one unmasked event occurs. The read content of this bitfield is equivalent to EVENT_BUFFER_MASKED.EBM

2.1126 SW_EVENT_6_TRIG_WAIT

Cluster Software event 6 trigger and wait command register. - Offset: `0x94` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.1126.1 Fields

`{"reg": [{"name": "EBM", "bits": 32, "attr": ["ro"], "rotate": 0}], "config": {"lanes": 1, "for`

Bits	Type	Reset	Name	Description
31:0	ro	0x0	EBM	Triggers software event 6 to all cluster cores targeted in SW_EVENT_MASK and gate the issuing cluster core clock until at least one unmasked event occurs. The read content of this bitfield is equivalent to EVENT_BUFFER_MASKED.EBM

2.1127 SW_EVENT_7_TRIG_WAIT

Cluster Software event 7 trigger and wait command register. - Offset: `0x98` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.1127.1 Fields

`{"reg": [{"name": "EBM", "bits": 32, "attr": ["ro"], "rotate": 0}], "config": {"lanes": 1, "for`

Bits	Type	Reset	Name	Description
31:0	ro	0x0	EBM	Triggers software event 7 to all cluster cores targeted in SW_EVENT_MASK and gate the issuing cluster core clock until at least one unmasked event occurs. The read content of this bitfield is equivalent to EVENT_BUFFER_MASKED.EBM

2.1128 SW_EVENT_0_TRIG_WAIT_CLEAR

Cluster Software event 0 trigger, wait and clear command register. - Offset: `0x9c` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.1128.1 Fields

{"reg": [{"name": "EBM", "bits": 32, "attr": ["ro"], "rotate": 0}], "config": {"lanes": 1, "fo

Bits	Type	Reset	Name
31:0	ro	0x0	EBM

2.1128.2 SW_EVENT_0_TRIG_WAIT_CLEAR . EBM

Triggers software event 0 to all cluster cores targeted in SW_EVENT_MASK and gate the issuing cluster core clock until at least one unmasked event occurs. In addition, EVENT_BUFFER.EB[i] bits are cleared after the read if EVT_MASK[i]=1'b1. The read content of this bitfield is equivalent to EVENT_BUFFER_MASKED.EBM

2.1129 SW_EVENT_1_TRIG_WAIT_CLEAR

Cluster Software event 1 trigger, wait and clear command register. - Offset: `0xa0` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.1129.1 Fields

{"reg": [{"name": "EBM", "bits": 32, "attr": ["ro"], "rotate": 0}], "config": {"lanes": 1, "fo

Bits	Type	Reset	Name
31:0	ro	0x0	EBM

2.1129.2 SW_EVENT_1_TRIG_WAIT_CLEAR . EBM

Triggers software event 1 to all cluster cores targeted in SW_EVENT_MASK and gate the issuing cluster core clock until at least one unmasked event occurs. In addition, EVENT_BUFFER.EB[i] bits are cleared after the read if EVT_MASK[i]=1'b1. The read content of this bitfield is equivalent to EVENT_BUFFER_MASKED.EBM

2.1130 SW_EVENT_2_TRIG_WAIT_CLEAR

Cluster Software event 2 trigger, wait and clear command register. - Offset: `0xa4` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.1130.1 Fields

{"reg": [{"name": "EBM", "bits": 32, "attr": ["ro"], "rotate": 0}], "config": {"lanes": 1, "fo

Bits	Type	Reset	Name
31:0	ro	0x0	EBM

2.1130.2 SW_EVENT_2_TRIG_WAIT_CLEAR . EBM

Triggers software event 2 to all cluster cores targeted in SW_EVENT_MASK and gate the issuing cluster core clock until at least one unmasked event occurs. In addition, EVENT_BUFFER.EB[i] bits are cleared after the read if EVT_MASK[i]=1'b1. The read content of this bitfield is equivalent to EVENT_BUFFER_MASKED.EBM

2.1131 SW_EVENT_3_TRIG_WAIT_CLEAR

Cluster Software event 3 trigger, wait and clear command register. - Offset: `0xa8` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.1131.1 Fields

{"reg": [{"name": "EBM", "bits": 32, "attr": ["ro"], "rotate": 0}], "config": {"lanes": 1, "fo

Bits	Type	Reset	Name
31:0	ro	0x0	EBM

2.1131.2 SW_EVENT_3_TRIG_WAIT_CLEAR . EBM

Triggers software event 3 to all cluster cores targeted in SW_EVENT_MASK and gate the issuing cluster core clock until at least one unmasked event occurs. In addition, EVENT_BUFFER.EB[i] bits are cleared after the read if EVT_MASK[i]=1'b1. The read content of this bitfield is equivalent to EVENT_BUFFER_MASKED.EBM

2.1132 SW_EVENT_4_TRIG_WAIT_CLEAR

Cluster Software event 4 trigger, wait and clear command register. - Offset: `0xac` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.1132.1 Fields

{"reg": [{"name": "EBM", "bits": 32, "attr": ["ro"], "rotate": 0}], "config": {"lanes": 1, "fo

Bits	Type	Reset	Name
31:0	ro	0x0	EBM

2.1132.2 SW_EVENT_4_TRIG_WAIT_CLEAR . EBM

Triggers software event 4 to all cluster cores targeted in SW_EVENT_MASK and gate the issuing cluster core clock until at least one unmasked event occurs. In addition, EVENT_BUFFER.EB[i] bits are cleared after the read if EVT_MASK[i]=1'b1. The read content of this bitfield is equivalent to EVENT_BUFFER_MASKED.EBM

2.1133 SW_EVENT_5_TRIG_WAIT_CLEAR

Cluster Software event 5 trigger, wait and clear command register. - Offset: `0xb0` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.1133.1 Fields

{"reg": [{"name": "EBM", "bits": 32, "attr": ["ro"], "rotate": 0}], "config": {"lanes": 1, "fo

Bits	Type	Reset	Name
31:0	ro	0x0	EBM

2.1133.2 SW_EVENT_5_TRIG_WAIT_CLEAR . EBM

Triggers software event 5 to all cluster cores targeted in SW_EVENT_MASK and gate the issuing cluster core clock until at least one unmasked event occurs. In addition, EVENT_BUFFER.EB[i] bits are cleared after the read if EVT_MASK[i]=1'b1. The read content of this bitfield is equivalent to EVENT_BUFFER_MASKED.EBM

2.1134 SW_EVENT_6_TRIG_WAIT_CLEAR

Cluster Software event 6 trigger, wait and clear command register. - Offset: `0xb4` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.1134.1 Fields

{"reg": [{"name": "EBM", "bits": 32, "attr": ["ro"], "rotate": 0}], "config": {"lanes": 1, "fo

Bits	Type	Reset	Name
31:0	ro	0x0	EBM

2.1134.2 SW_EVENT_6_TRIG_WAIT_CLEAR . EBM

Triggers software event 6 to all cluster cores targeted in SW_EVENT_MASK and gate the issuing cluster core clock until at least one unmasked event occurs. In addition, EVENT_BUFFER.EB[i] bits are cleared after the read if EVT_MASK[i]=1'b1. The read content of this bitfield is equivalent to EVENT_BUFFER_MASKED.EBM

2.1135 SW_EVENT_7_TRIG_WAIT_CLEAR

Cluster Software event 7 trigger, wait and clear command register. - Offset: `0xb8` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.1135.1 Fields

{"reg": [{"name": "EBM", "bits": 32, "attr": ["ro"], "rotate": 0}], "config": {"lanes": 1, "fo

Bits	Type	Reset	Name
31:0	ro	0x0	EBM

2.1135.2 SW_EVENT_7_TRIG_WAIT_CLEAR . EBM

Triggers software event 7 to all cluster cores targeted in SW_EVENT_MASK and gate the issuing cluster core clock until at least one unmasked event occurs. In addition, EVENT_BUFFER.EB[i] bits are cleared after the read if EVT_MASK[i]=1'b1. The read content of this bitfield is equivalent to EVENT_BUFFER_MASKED.EBM

2.1136 SOC_PERIPH_EVENT_ID

Cluster SoC peripheral event ID status register. - Offset: `0xbc` - Reset default: `0x0` - Reset mask: `0x800000ff`

2.1136.1 Fields

{"reg": [{"name": "ID", "bits": 8, "attr": ["ro"], "rotate": 0}, {"bits": 23}, {"name": "VALID"

Bits	Type	Reset	Name	Description
31	ro	0x0	VALID	Validity bit of SOC_PERIPH_EVENT_ID.ID bitfield.
30:8				Reserved
7:0	ro	0x0	ID	Oldest SoC peripheral event ID status bitfield.

2.1137 HW_BARRIER_0_TRIG_MASK

Cluster hardware barrier 0 trigger mask configuration register. - Offset: `0xc0` - Reset default: `0x0` - Reset mask: `0xff`

2.1137.1 Fields

{"reg": [{"name": "HB0TM", "bits": 8, "attr": ["rw"], "rotate": 0}, {"bits": 24}], "config": {"

Bits	Type	Reset	Name	Description
31:8				Reserved
7:0	rw	0x0	HB0TM	Trigger mask for hardware barrier 0 bitfield. Hardware barrier 0 will be triggered only if for all HB0TM[i] = 1'b1, HW_BARRIER_0_STATUS.HB0S[i]=1'b1. HB0TM=0 means that hardware barrier 0 is disabled.

2.1138 HW_BARRIER_1_TRIG_MASK

Cluster hardware barrier 1 trigger mask configuration register. - Offset: `0xc4` - Reset default: `0x0` - Reset mask: `0xff`

2.1138.1 Fields

{"reg": [{"name": "HB1TM", "bits": 8, "attr": ["rw"], "rotate": 0}, {"bits": 24}], "config": {"

Bits	Type	Reset	Name	Description
31:8				Reserved

Bits	Type	Reset	Name	Description
7:0	rw	0x0	HB1TM	Trigger mask for hardware barrier 1 bitfield. Hardware barrier 1 will be triggered only if for all HB1TM[i] = 1'b1, HW_BARRIER_1_STATUS.HB1S[i]=1'b1. HB1TM=0 means that hardware barrier 1 is disabled.

2.1139 HW_BARRIER_2_TRIG_MASK

Cluster hardware barrier 2 trigger mask configuration register. - Offset: `0xc8` - Reset default: `0x0` - Reset mask: `0xff`

2.1139.1 Fields


```
{"reg": [{"name": "HB2TM", "bits": 8, "attr": ["rw"], "rotate": 0}, {"bits": 24}], "config": {
```


Bits	Type	Reset	Name	Description
31:8				Reserved
7:0	rw	0x0	HB2TM	Trigger mask for hardware barrier 2 bitfield. Hardware barrier 2 will be triggered only if for all HB2TM[i] = 1'b1, HW_BARRIER_2_STATUS.HB2S[i]=1'b1. HB2TM=0 means that hardware barrier 2 is disabled.

2.1140 HW_BARRIER_3_TRIG_MASK

Cluster hardware barrier 3 trigger mask configuration register. - Offset: `0xcc` - Reset default: `0x0` - Reset mask: `0xff`

2.1140.1 Fields


```
{"reg": [{"name": "HB3TM", "bits": 8, "attr": ["rw"], "rotate": 0}, {"bits": 24}], "config": {
```


Bits	Type	Reset	Name	Description
31:8				Reserved
7:0	rw	0x0	HB3TM	Trigger mask for hardware barrier 3 bitfield. Hardware barrier 3 will be triggered only if for all HB3TM[i] = 1'b1, HW_BARRIER_3_STATUS.HB3S[i]=1'b1. HB3TM=0 means that hardware barrier 3 is disabled.

2.1141 HW_BARRIER_4_TRIG_MASK

Cluster hardware barrier 4 trigger mask configuration register. - Offset: `0xd0` - Reset default: `0x0` - Reset mask: `0xff`

2.1141.1 Fields

{"reg": [{"name": "HB4TM", "bits": 8, "attr": ["rw"], "rotate": 0}, {"bits": 24}], "config": {

Bits	Type	Reset	Name	Description
31:8				Reserved
7:0	rw	0x0	HB4TM	Trigger mask for hardware barrier 4 bitfield. Hardware barrier 4 will be triggered only if for all HB4TM[i] = 1'b1, HW_BARRIER_4_STATUS.HB4S[i]=1'b1. HB4TM=0 means that hardware barrier 4 is disabled.

2.1142 HW_BARRIER_5_TRIG_MASK

Cluster hardware barrier 5 trigger mask configuration register. - Offset: `0xd4` - Reset default: `0x0` - Reset mask: `0xff`

2.1142.1 Fields

{"reg": [{"name": "HB5TM", "bits": 8, "attr": ["rw"], "rotate": 0}, {"bits": 24}], "config": {

Bits	Type	Reset	Name	Description
31:8				Reserved
7:0	rw	0x0	HB5TM	Trigger mask for hardware barrier 5 bitfield. Hardware barrier 5 will be triggered only if for all HB5TM[i] = 1'b1, HW_BARRIER_5_STATUS.HB5S[i]=1'b1. HB5TM=0 means that hardware barrier 5 is disabled.

2.1143 HW_BARRIER_6_TRIG_MASK

Cluster hardware barrier 6 trigger mask configuration register. - Offset: `0xd8` - Reset default: `0x0` - Reset mask: `0xff`

2.1143.1 Fields

{"reg": [{"name": "HB6TM", "bits": 8, "attr": ["rw"], "rotate": 0}, {"bits": 24}], "config": {

Bits	Type	Reset	Name	Description
31:8				Reserved

Bits	Type	Reset	Name	Description
7:0	rw	0x0	HB6TM	Trigger mask for hardware barrier 6 bitfield. Hardware barrier 6 will be triggered only if for all HB6TM[i] = 1'b1, HW_BARRIER_6_STATUS.HB6S[i]=1'b1. HB6TM=0 means that hardware barrier 6 is disabled.

2.1144 HW_BARRIER_7_TRIG_MASK

Cluster hardware barrier 7 trigger mask configuration register. - Offset: `0xdc` - Reset default: `0x0` - Reset mask: `0xff`

2.1144.1 Fields

`{"reg": [{"name": "HB7TM", "bits": 8, "attr": ["rw"], "rotate": 0}, {"bits": 24}], "config": {`

Bits	Type	Reset	Name	Description
31:8				Reserved
7:0	rw	0x0	HB7TM	Trigger mask for hardware barrier 7 bitfield. Hardware barrier 7 will be triggered only if for all HB7TM[i] = 1'b1, HW_BARRIER_7_STATUS.HB7S[i]=1'b1. HB7TM=0 means that hardware barrier 7 is disabled.

2.1145 HW_BARRIER_0_STATUS

Cluster hardware barrier 0 status register. - Offset: `0xe0` - Reset default: `0x0` - Reset mask: `0xff`

2.1145.1 Fields

`{"reg": [{"name": "HBS", "bits": 8, "attr": ["ro"], "rotate": 0}, {"bits": 24}], "config": {"la`

Bits	Type	Reset	Name	Description
31:8				Reserved
7:0	ro	0x0	HBS	Current status of hardware barrier 0 bitfield. HBS[i]=1'b1 means that cluster core i has triggered hardware barrier 0. It is cleared when HBS matches HW_BARRIER_0_TRIG_MASK.HB0TM.

2.1146 HW_BARRIER_1_STATUS

Cluster hardware barrier 1 status register. - Offset: `0xe4` - Reset default: `0x0` - Reset mask: `0xff`

2.1146.1 Fields

{"reg": [{"name": "HBS", "bits": 8, "attr": ["ro"], "rotate": 0}, {"bits": 24}], "config": {"la

Bits	Type	Reset	Name	Description
31:8				Reserved
7:0	ro	0x0	HBS	Current status of hardware barrier 1 bitfield. HBS[i]=1'b1 means that cluster core i has triggered hardware barrier 1. It is cleared when HBS matches HW_BARRIER_1_TRIG_MASK.HB1TM.

2.1147 HW_BARRIER_2_STATUS

Cluster hardware barrier 2 status register. - Offset: `0xe8` - Reset default: `0x0` - Reset mask: `0xff`

2.1147.1 Fields

{"reg": [{"name": "HBS", "bits": 8, "attr": ["ro"], "rotate": 0}, {"bits": 24}], "config": {"la

Bits	Type	Reset	Name	Description
31:8				Reserved
7:0	ro	0x0	HBS	Current status of hardware barrier 2 bitfield. HBS[i]=1'b1 means that cluster core i has triggered hardware barrier 2. It is cleared when HBS matches HW_BARRIER_2_TRIG_MASK.HB2TM.

2.1148 HW_BARRIER_3_STATUS

Cluster hardware barrier 3 status register. - Offset: `0xec` - Reset default: `0x0` - Reset mask: `0xff`

2.1148.1 Fields

{"reg": [{"name": "HBS", "bits": 8, "attr": ["ro"], "rotate": 0}, {"bits": 24}], "config": {"la

Bits	Type	Reset	Name	Description
31:8				Reserved
7:0	ro	0x0	HBS	Current status of hardware barrier 3 bitfield. HBS[i]=1'b1 means that cluster core i has triggered hardware barrier 3. It is cleared when HBS matches HW_BARRIER_3_TRIG_MASK.HB3TM.

2.1149 HW_BARRIER_4_STATUS

Cluster hardware barrier 4 status register. - Offset: `0xf0` - Reset default: `0x0` - Reset mask: `0xff`

2.1149.1 Fields

{"reg": [{"name": "HBS", "bits": 8, "attr": ["ro"], "rotate": 0}, {"bits": 24}], "config": {"la

Bits	Type	Reset	Name	Description
31:8				Reserved
7:0	ro	0x0	HBS	Current status of hardware barrier 4 bitfield. HBS[i]=1'b1 means that cluster core i has triggered hardware barrier 4. It is cleared when HBS matches HW_BARRIER_4_TRIG_MASK.HB4TM.

2.1150 HW_BARRIER_5_STATUS

Cluster hardware barrier 5 status register. - Offset: `0xf4` - Reset default: `0x0` - Reset mask: `0xff`

2.1150.1 Fields

{"reg": [{"name": "HBS", "bits": 8, "attr": ["ro"], "rotate": 0}, {"bits": 24}], "config": {"la

Bits	Type	Reset	Name	Description
31:8				Reserved
7:0	ro	0x0	HBS	Current status of hardware barrier 5 bitfield. HBS[i]=1'b1 means that cluster core i has triggered hardware barrier 5. It is cleared when HBS matches HW_BARRIER_5_TRIG_MASK.HB5TM.

2.1151 HW_BARRIER_6_STATUS

Cluster hardware barrier 6 status register. - Offset: `0xf8` - Reset default: `0x0` - Reset mask: `0xff`

2.1151.1 Fields

{"reg": [{"name": "HBS", "bits": 8, "attr": ["ro"], "rotate": 0}, {"bits": 24}], "config": {"la

Bits	Type	Reset	Name	Description
31:8				Reserved
7:0	ro	0x0	HBS	Current status of hardware barrier 6 bitfield. HBS[i]=1'b1 means that cluster core i has triggered hardware barrier 6. It is cleared when HBS matches HW_BARRIER_6_TRIG_MASK.HB6TM.

2.1152 HW_BARRIER_7_STATUS

Cluster hardware barrier 7 status register. - Offset: `0xfc` - Reset default: `0x0` - Reset mask: `0xff`

2.1152.1 Fields

{"reg": [{"name": "HBS", "bits": 8, "attr": ["ro"], "rotate": 0}, {"bits": 24}], "config": {"la

Bits	Type	Reset	Name	Description
31:8				Reserved
7:0	ro	0x0	HBS	Current status of hardware barrier 7 bitfield. HBS[i]=1'b1 means that cluster core i has triggered hardware barrier 7. It is cleared when HBS matches HW_BARRIER_7_TRIG_MASK.HB7TM.

2.1153 HW_BARRIER_0_STATUS_SUM

Cluster hardware barrier summary status register. - Offset: `0x100` - Reset default: `0x0` - Reset mask: `0xff`

2.1153.1 Fields

{"reg": [{"name": "HBSS", "bits": 8, "attr": ["ro"], "rotate": 0}, {"bits": 24}], "config": {"

Bits	Type	Reset	Name	Description
31:8				Reserved
7:0	ro	0x0	HBSS	Current status of hardware barrier 0. HBSS[i] represents a summary of the barrier status for core i.

2.1154 HW_BARRIER_1_STATUS_SUM

Cluster hardware barrier summary status register. - Offset: `0x104` - Reset default: `0x0` - Reset mask: `0xff`

2.1154.1 Fields

{"reg": [{"name": "HBSS", "bits": 8, "attr": ["ro"], "rotate": 0}, {"bits": 24}], "config": {"

Bits	Type	Reset	Name	Description
31:8				Reserved
7:0	ro	0x0	HBSS	Current status of hardware barrier 1. HBSS[i] represents a summary of the barrier status for core i.

2.1155 HW_BARRIER_2_STATUS_SUM

Cluster hardware barrier summary status register. - Offset: `0x108` - Reset default: `0x0` - Reset mask: `0xff`

2.1155.1 Fields

{"reg": [{"name": "HBSS", "bits": 8, "attr": ["ro"], "rotate": 0}, {"bits": 24}], "config": {"

Bits	Type	Reset	Name	Description
31:8				Reserved
7:0	ro	0x0	HBSS	Current status of hardware barrier 2. HBSS[i] represents a summary of the barrier status for core i.

2.1156 HW_BARRIER_3_STATUS_SUM

Cluster hardware barrier summary status register. - Offset: `0x10c` - Reset default: `0x0` - Reset mask: `0xff`

2.1156.1 Fields

{"reg": [{"name": "HBSS", "bits": 8, "attr": ["ro"], "rotate": 0}, {"bits": 24}], "config": {"

Bits	Type	Reset	Name	Description
31:8				Reserved
7:0	ro	0x0	HBSS	Current status of hardware barrier 3. HBSS[i] represents a summary of the barrier status for core i.

2.1157 HW_BARRIER_4_STATUS_SUM

Cluster hardware barrier summary status register. - Offset: `0x110` - Reset default: `0x0` - Reset mask: `0xff`

2.1157.1 Fields

{"reg": [{"name": "HBSS", "bits": 8, "attr": ["ro"], "rotate": 0}, {"bits": 24}], "config": {"

Bits	Type	Reset	Name	Description
31:8				Reserved
7:0	ro	0x0	HBSS	Current status of hardware barrier 4. HBSS[i] represents a summary of the barrier status for core i.

2.1158 HW_BARRIER_5_STATUS_SUM

Cluster hardware barrier summary status register. - Offset: `0x114` - Reset default: `0x0` - Reset mask: `0xff`

2.1158.1 Fields

{"reg": [{"name": "HBSS", "bits": 8, "attr": ["ro"], "rotate": 0}, {"bits": 24}], "config": {"

Bits	Type	Reset	Name	Description
31:8				Reserved
7:0	ro	0x0	HBSS	Current status of hardware barrier 5. HBSS[i] represents a summary of the barrier status for core i.

2.1159 HW_BARRIER_6_STATUS_SUM

Cluster hardware barrier summary status register. - Offset: `0x118` - Reset default: `0x0` - Reset mask: `0xff`

2.1159.1 Fields

{"reg": [{"name": "HBSS", "bits": 8, "attr": ["ro"], "rotate": 0}, {"bits": 24}], "config": {"

Bits	Type	Reset	Name	Description
31:8				Reserved
7:0	ro	0x0	HBSS	Current status of hardware barrier 6. HBSS[i] represents a summary of the barrier status for core i.

2.1160 HW_BARRIER_7_STATUS_SUM

Cluster hardware barrier summary status register. - Offset: `0x11c` - Reset default: `0x0` - Reset mask: `0xff`

2.1160.1 Fields

{"reg": [{"name": "HBSS", "bits": 8, "attr": ["ro"], "rotate": 0}, {"bits": 24}], "config": {"

Bits	Type	Reset	Name	Description
31:8				Reserved
7:0	ro	0x0	HBSS	Current status of hardware barrier 7. HBSS[i] represents a summary of the barrier status for core i.

2.1161 HW_BARRIER_0_TARGET_MASK

Cluster hardware barrier 0 target mask configuration register. - Offset: `0x120` - Reset default: `0x0` - Reset mask: `0xff`

2.1161.1 Fields

{"reg": [{"name": "HBTAM", "bits": 8, "attr": ["rw"], "rotate": 0}, {"bits": 24}], "config": {

Bits	Type	Reset	Name	Description
31:8				Reserved
7:0	rw	0x0	HBTAM	Cluster hardware barrier 0 target mask configuration bitfield. HBATM[i]=1'b1 means that cluster core i will receive hardware barrier 0 event when HW_BARRIER_0_STATUS will match HW_BARRIER_0_TRIG_MASK.

2.1162 HW_BARRIER_1_TARGET_MASK

Cluster hardware barrier 1 target mask configuration register. - Offset: `0x124` - Reset default: `0x0` - Reset mask: `0xff`

2.1162.1 Fields

{"reg": [{"name": "HBTAM", "bits": 8, "attr": ["rw"], "rotate": 0}, {"bits": 24}], "config": {

Bits	Type	Reset	Name	Description
31:8				Reserved
7:0	rw	0x0	HBTAM	Cluster hardware barrier 1 target mask configuration bitfield. HBATM[i]=1'b1 means that cluster core i will receive hardware barrier 1 event when HW_BARRIER_1_STATUS will match HW_BARRIER_1_TRIG_MASK.

2.1163 HW_BARRIER_2_TARGET_MASK

Cluster hardware barrier 2 target mask configuration register. - Offset: `0x128` - Reset default: `0x0` - Reset mask: `0xff`

2.1163.1 Fields

{"reg": [{"name": "HBTAM", "bits": 8, "attr": ["rw"], "rotate": 0}, {"bits": 24}], "config": {

Bits	Type	Reset	Name	Description
31:8				Reserved

Bits	Type	Reset	Name	Description
7:0	rw	0x0	HBTAM	Cluster hardware barrier 2 target mask configuration bitfield. HBATM[i]=1'b1 means that cluster core i will receive hardware barrier 2 event when HW_BARRIER_2_STATUS will match HW_BARRIER_2_TRIG_MASK.

2.1164 HW_BARRIER_3_TARGET_MASK

Cluster hardware barrier 3 target mask configuration register. - Offset: `0x12c` - Reset default: `0x0` - Reset mask: `0xff`

2.1164.1 Fields

`{"reg": [{"name": "HBTAM", "bits": 8, "attr": ["rw"], "rotate": 0}, {"bits": 24}], "config": {`

Bits	Type	Reset	Name	Description
31:8				Reserved
7:0	rw	0x0	HBTAM	Cluster hardware barrier 3 target mask configuration bitfield. HBATM[i]=1'b1 means that cluster core i will receive hardware barrier 3 event when HW_BARRIER_3_STATUS will match HW_BARRIER_3_TRIG_MASK.

2.1165 HW_BARRIER_4_TARGET_MASK

Cluster hardware barrier 4 target mask configuration register. - Offset: `0x130` - Reset default: `0x0` - Reset mask: `0xff`

2.1165.1 Fields

`{"reg": [{"name": "HBTAM", "bits": 8, "attr": ["rw"], "rotate": 0}, {"bits": 24}], "config": {`

Bits	Type	Reset	Name	Description
31:8				Reserved
7:0	rw	0x0	HBTAM	Cluster hardware barrier 4 target mask configuration bitfield. HBATM[i]=1'b1 means that cluster core i will receive hardware barrier 4 event when HW_BARRIER_4_STATUS will match HW_BARRIER_4_TRIG_MASK.

2.1166 HW_BARRIER_5_TARGET_MASK

Cluster hardware barrier 5 target mask configuration register. - Offset: `0x134` - Reset default: `0x0` - Reset mask: `0xff`

2.1166.1 Fields

{"reg": [{"name": "HBTAM", "bits": 8, "attr": ["rw"], "rotate": 0}, {"bits": 24}], "config": {

Bits	Type	Reset	Name	Description
31:8				Reserved
7:0	rw	0x0	HBTAM	Cluster hardware barrier 5 target mask configuration bitfield. HBATM[i]=1'b1 means that cluster core i will receive hardware barrier 5 event when HW_BARRIER_5_STATUS will match HW_BARRIER_5_TRIG_MASK.

2.1167 HW_BARRIER_6_TARGET_MASK

Cluster hardware barrier 6 target mask configuration register. - Offset: `0x138` - Reset default: `0x0` - Reset mask: `0xff`

2.1167.1 Fields

{"reg": [{"name": "HBTAM", "bits": 8, "attr": ["rw"], "rotate": 0}, {"bits": 24}], "config": {

Bits	Type	Reset	Name	Description
31:8				Reserved
7:0	rw	0x0	HBTAM	Cluster hardware barrier 6 target mask configuration bitfield. HBATM[i]=1'b1 means that cluster core i will receive hardware barrier 6 event when HW_BARRIER_6_STATUS will match HW_BARRIER_6_TRIG_MASK.

2.1168 HW_BARRIER_7_TARGET_MASK

Cluster hardware barrier 7 target mask configuration register. - Offset: `0x13c` - Reset default: `0x0` - Reset mask: `0xff`

2.1168.1 Fields

{"reg": [{"name": "HBTAM", "bits": 8, "attr": ["rw"], "rotate": 0}, {"bits": 24}], "config": {

Bits	Type	Reset	Name	Description
31:8				Reserved

Bits	Type	Reset	Name	Description
7:0	rw	0x0	HBTATM	Cluster hardware barrier 7 target mask configuration bitfield. HBATM[i]=1'b1 means that cluster core i will receive hardware barrier 7 event when HW_BARRIER_7_STATUS will match HW_BARRIER_7_TRIG_MASK.

2.1169 HW_BARRIER_0_TRIG

Cluster hardware barrier 0 trigger command register. - Offset: `0x140` - Reset default: `0x0` - Reset mask: `0xff`

2.1169.1 Fields

`{"reg": [{"name": "T", "bits": 8, "attr": ["wo"], "rotate": 0}, {"bits": 24}], "config": {"lane`

Bits	Type	Reset	Name	Description
31:8				Reserved
7:0	wo	0x0	T	Sets HW_BARRIER_0_STATUS.HBS[i] to 1'b1 when T[i]=1'b1.

2.1170 HW_BARRIER_1_TRIG

Cluster hardware barrier 1 trigger command register. - Offset: `0x144` - Reset default: `0x0` - Reset mask: `0xff`

2.1170.1 Fields

`{"reg": [{"name": "T", "bits": 8, "attr": ["wo"], "rotate": 0}, {"bits": 24}], "config": {"lane`

Bits	Type	Reset	Name	Description
31:8				Reserved
7:0	wo	0x0	T	Sets HW_BARRIER_1_STATUS.HBS[i] to 1'b1 when T[i]=1'b1.

2.1171 HW_BARRIER_2_TRIG

Cluster hardware barrier 2 trigger command register. - Offset: `0x148` - Reset default: `0x0` - Reset mask: `0xff`

2.1171.1 Fields

{"reg": [{"name": "T", "bits": 8, "attr": ["wo"], "rotate": 0}, {"bits": 24}], "config": {"lane

Bits	Type	Reset	Name	Description
31:8				Reserved
7:0	wo	0x0	T	Sets HW_BARRIER_2_STATUS.HBS[i] to 1'b1 when T[i]=1'b1.

2.1172 HW_BARRIER_3_TRIG

Cluster hardware barrier 3 trigger command register. - Offset: `0x14c` - Reset default: `0x0` - Reset mask: `0xff`

2.1172.1 Fields

{"reg": [{"name": "T", "bits": 8, "attr": ["wo"], "rotate": 0}, {"bits": 24}], "config": {"lane

Bits	Type	Reset	Name	Description
31:8				Reserved
7:0	wo	0x0	T	Sets HW_BARRIER_3_STATUS.HBS[i] to 1'b1 when T[i]=1'b1.

2.1173 HW_BARRIER_4_TRIG

Cluster hardware barrier 4 trigger command register. - Offset: `0x150` - Reset default: `0x0` - Reset mask: `0xff`

2.1173.1 Fields

{"reg": [{"name": "T", "bits": 8, "attr": ["wo"], "rotate": 0}, {"bits": 24}], "config": {"lane

Bits	Type	Reset	Name	Description
31:8				Reserved
7:0	wo	0x0	T	Sets HW_BARRIER_4_STATUS.HBS[i] to 1'b1 when T[i]=1'b1.

2.1174 HW_BARRIER_5_TRIG

Cluster hardware barrier 5 trigger command register. - Offset: `0x154` - Reset default: `0x0` - Reset mask: `0xff`

2.1174.1 Fields

{"reg": [{"name": "T", "bits": 8, "attr": ["wo"], "rotate": 0}, {"bits": 24}], "config": {"lane

Bits	Type	Reset	Name	Description
31:8				Reserved
7:0	wo	0x0	T	Sets HW_BARRIER_5_STATUS.HBS[i] to 1'b1 when T[i]=1'b1.

2.1175 HW_BARRIER_6_TRIG

Cluster hardware barrier 6 trigger command register. - Offset: `0x158` - Reset default: `0x0` - Reset mask: `0xff`

2.1175.1 Fields

{"reg": [{"name": "T", "bits": 8, "attr": ["wo"], "rotate": 0}, {"bits": 24}], "config": {"lane

Bits	Type	Reset	Name	Description
31:8				Reserved
7:0	wo	0x0	T	Sets HW_BARRIER_6_STATUS.HBS[i] to 1'b1 when T[i]=1'b1.

2.1176 HW_BARRIER_7_TRIG

Cluster hardware barrier 7 trigger command register. - Offset: `0x15c` - Reset default: `0x0` - Reset mask: `0xff`

2.1176.1 Fields

{"reg": [{"name": "T", "bits": 8, "attr": ["wo"], "rotate": 0}, {"bits": 24}], "config": {"lane

Bits	Type	Reset	Name	Description
31:8				Reserved
7:0	wo	0x0	T	Sets HW_BARRIER_7_STATUS.HBS[i] to 1'b1 when T[i]=1'b1.

2.1177 HW_BARRIER_0_SELF_TRIG

Cluster hardware barrier 0 self trigger command register. - Offset: `0x160` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.1177.1 Fields

{"reg": [{"name": "T", "bits": 32, "attr": ["ro"], "rotate": 0}], "config": {"lanes": 1, "fonts

Bits	Type	Reset	Name	Description
31:0	ro	0x0	T	Sets HW_BARRIER_0_STATUS.HBS[i] to 1'b1 when issued by cluster core i.

2.1178 HW_BARRIER_1_SELF_TRIG

Cluster hardware barrier 1 self trigger command register. - Offset: `0x164` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.1178.1 Fields

{"reg": [{"name": "T", "bits": 32, "attr": ["ro"], "rotate": 0}], "config": {"lanes": 1, "fonts

Bits	Type	Reset	Name	Description
31:0	ro	0x0	T	Sets HW_BARRIER_1_STATUS.HBS[i] to 1'b1 when issued by cluster core i.

2.1179 HW_BARRIER_2_SELF_TRIG

Cluster hardware barrier 2 self trigger command register. - Offset: `0x168` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.1179.1 Fields

{"reg": [{"name": "T", "bits": 32, "attr": ["ro"], "rotate": 0}], "config": {"lanes": 1, "fonts

Bits	Type	Reset	Name	Description
31:0	ro	0x0	T	Sets HW_BARRIER_2_STATUS.HBS[i] to 1'b1 when issued by cluster core i.

2.1180 HW_BARRIER_3_SELF_TRIG

Cluster hardware barrier 3 self trigger command register. - Offset: `0x16c` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.1180.1 Fields

{"reg": [{"name": "T", "bits": 32, "attr": ["ro"], "rotate": 0}], "config": {"lanes": 1, "fonts

Bits	Type	Reset	Name	Description
31:0	ro	0x0	T	Sets HW_BARRIER_3_STATUS.HBS[i] to 1'b1 when issued by cluster core i.

2.1181 HW_BARRIER_4_SELF_TRIG

Cluster hardware barrier 4 self trigger command register. - Offset: `0x170` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.1181.1 Fields

{"reg": [{"name": "T", "bits": 32, "attr": ["ro"], "rotate": 0}], "config": {"lanes": 1, "fonts

Bits	Type	Reset	Name	Description
31:0	ro	0x0	T	Sets HW_BARRIER_4_STATUS.HBS[i] to 1'b1 when issued by cluster core i.

2.1182 HW_BARRIER_5_SELF_TRIG

Cluster hardware barrier 5 self trigger command register. - Offset: `0x174` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.1182.1 Fields

{"reg": [{"name": "T", "bits": 32, "attr": ["ro"], "rotate": 0}], "config": {"lanes": 1, "fonts

Bits	Type	Reset	Name	Description
31:0	ro	0x0	T	Sets HW_BARRIER_5_STATUS.HBS[i] to 1'b1 when issued by cluster core i.

2.1183 HW_BARRIER_6_SELF_TRIG

Cluster hardware barrier 6 self trigger command register. - Offset: `0x178` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.1183.1 Fields

{"reg": [{"name": "T", "bits": 32, "attr": ["ro"], "rotate": 0}], "config": {"lanes": 1, "fonts

Bits	Type	Reset	Name	Description
31:0	ro	0x0	T	Sets HW_BARRIER_6_STATUS.HBS[i] to 1'b1 when issued by cluster core i.

2.1184 HW_BARRIER_7_SELF_TRIG

Cluster hardware barrier 7 self trigger command register. - Offset: `0x17c` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.1184.1 Fields

{"reg": [{"name": "T", "bits": 32, "attr": ["ro"], "rotate": 0}], "config": {"lanes": 1, "fonts

Bits	Type	Reset	Name	Description
31:0	ro	0x0	T	Sets HW_BARRIER_7_STATUS.HBS[i] to 1'b1 when issued by cluster core i.

2.1185 HW_BARRIER_0_TRIG_WAIT

Cluster hardware barrier 0 trigger and wait command register. - Offset: `0x180` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.1185.1 Fields

{"reg": [{"name": "EBM", "bits": 32, "attr": ["ro"], "rotate": 0}], "config": {"lanes": 1, "fo

Bits	Type	Reset	Name	Description
31:0	ro	0x0	EBM	Set HW_BARRIER_0[i] when issued by cluster core i and gate the issuing cluster core i clock until HW_BARRIER_0 is released. The read content of this bitfield is equivalent to EVENT_BUFFER_MASKED.EBM

2.1186 HW_BARRIER_1_TRIG_WAIT

Cluster hardware barrier 1 trigger and wait command register. - Offset: `0x184` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.1186.1 Fields

{"reg": [{"name": "EBM", "bits": 32, "attr": ["ro"], "rotate": 0}], "config": {"lanes": 1, "fo

Bits	Type	Reset	Name	Description
31:0	ro	0x0	EBM	Set HW_BARRIER_1[i] when issued by cluster core i and gate the issuing cluster core i clock until HW_BARRIER_1 is released. The read content of this bitfield is equivalent to EVENT_BUFFER_MASKED.EBM

2.1187 HW_BARRIER_2_TRIG_WAIT

Cluster hardware barrier 2 trigger and wait command register. - Offset: `0x188` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.1187.1 Fields

{"reg": [{"name": "EBM", "bits": 32, "attr": ["ro"], "rotate": 0}], "config": {"lanes": 1, "fo

Bits	Type	Reset	Name	Description
31:0	ro	0x0	EBM	Set HW_BARRIER_2[i] when issued by cluster core i and gate the issuing cluster core i clock until HW_BARRIER_2 is released. The read content of this bitfield is equivalent to EVENT_BUFFER_MASKED.EBM

2.1188 HW_BARRIER_3_TRIG_WAIT

Cluster hardware barrier 3 trigger and wait command register. - Offset: `0x18c` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.1188.1 Fields

{"reg": [{"name": "EBM", "bits": 32, "attr": ["ro"], "rotate": 0}], "config": {"lanes": 1, "fo

Bits	Type	Reset	Name	Description
31:0	ro	0x0	EBM	Set HW_BARRIER_3[i] when issued by cluster core i and gate the issuing cluster core i clock until HW_BARRIER_3 is released. The read content of this bitfield is equivalent to EVENT_BUFFER_MASKED.EBM

2.1189 HW_BARRIER_4_TRIG_WAIT

Cluster hardware barrier 4 trigger and wait command register. - Offset: `0x190` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.1189.1 Fields

{"reg": [{"name": "EBM", "bits": 32, "attr": ["ro"], "rotate": 0}], "config": {"lanes": 1, "fo

Bits	Type	Reset	Name	Description
31:0	ro	0x0	EBM	Set HW_BARRIER_4[i] when issued by cluster core i and gate the issuing cluster core i clock until HW_BARRIER_4 is released. The read content of this bitfield is equivalent to EVENT_BUFFER_MASKED.EBM

2.1190 HW_BARRIER_5_TRIG_WAIT

Cluster hardware barrier 5 trigger and wait command register. - Offset: `0x194` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.1190.1 Fields

{"reg": [{"name": "EBM", "bits": 32, "attr": ["ro"], "rotate": 0}], "config": {"lanes": 1, "fo

Bits	Type	Reset	Name	Description
31:0	ro	0x0	EBM	Set HW_BARRIER_5[i] when issued by cluster core i and gate the issuing cluster core i clock until HW_BARRIER_5 is released. The read content of this bitfield is equivalent to EVENT_BUFFER_MASKED.EBM

2.1191 HW_BARRIER_6_TRIG_WAIT

Cluster hardware barrier 6 trigger and wait command register. - Offset: `0x198` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.1191.1 Fields

{"reg": [{"name": "EBM", "bits": 32, "attr": ["ro"], "rotate": 0}], "config": {"lanes": 1, "fo

Bits	Type	Reset	Name	Description
31:0	ro	0x0	EBM	Set HW_BARRIER_6[i] when issued by cluster core i and gate the issuing cluster core i clock until HW_BARRIER_6 is released. The read content of this bitfield is equivalent to EVENT_BUFFER_MASKED.EBM

2.1192 HW_BARRIER_7_TRIG_WAIT

Cluster hardware barrier 7 trigger and wait command register. - Offset: `0x19c` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.1192.1 Fields

{"reg": [{"name": "EBM", "bits": 32, "attr": ["ro"], "rotate": 0}], "config": {"lanes": 1, "fo

Bits	Type	Reset	Name	Description
31:0	ro	0x0	EBM	Set HW_BARRIER_7[i] when issued by cluster core i and gate the issuing cluster core i clock until HW_BARRIER_7 is released. The read content of this bitfield is equivalent to EVENT_BUFFER_MASKED.EBM

2.1193 HW_BARRIER_0_TRIG_WAIT_CLEAR

Cluster hardware barrier 0 trigger, wait and clear command register. - Offset: `0x1a0` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.1193.1 Fields

{"reg": [{"name": "EBM", "bits": 32, "attr": ["ro"], "rotate": 0}], "config": {"lanes": 1, "fo

Bits	Type	Reset	Name
31:0	ro	0x0	EBM

2.1193.2 HW_BARRIER_0_TRIG_WAIT_CLEAR . EBM

Set HW_BARRIER_0[i] when issued by cluster core i and gate the issuing cluster core i clock until HW_BARRIER_0 is released. In addition, EVENT_BUFFER.EB[i] bits are cleared after the read if EVT_MASK[i]=1'b1. The read content of this bitfield is equivalent to EVENT_BUFFER_MASKED.EBM

2.1194 HW_BARRIER_1_TRIG_WAIT_CLEAR

Cluster hardware barrier 1 trigger, wait and clear command register. - Offset: `0x1a4` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.1194.1 Fields

{"reg": [{"name": "EBM", "bits": 32, "attr": ["ro"], "rotate": 0}], "config": {"lanes": 1, "fo

Bits	Type	Reset	Name
31:0	ro	0x0	EBM

2.1194.2 HW_BARRIER_1_TRIG_WAIT_CLEAR . EBM

Set HW_BARRIER_1[i] when issued by cluster core i and gate the issuing cluster core i clock until HW_BARRIER_1 is released. In addition, EVENT_BUFFER.EB[i] bits are cleared after the read if EVT_MASK[i]=1'b1. The read content of this bitfield is equivalent to EVENT_BUFFER_MASKED.EBM

2.1195 HW_BARRIER_2_TRIG_WAIT_CLEAR

Cluster hardware barrier 2 trigger, wait and clear command register. - Offset: `0x1a8` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.1195.1 Fields

{"reg": [{"name": "EBM", "bits": 32, "attr": ["ro"], "rotate": 0}], "config": {"lanes": 1, "fo

Bits	Type	Reset	Name
31:0	ro	0x0	EBM

2.1195.2 HW_BARRIER_2_TRIG_WAIT_CLEAR . EBM

Set HW_BARRIER_2[i] when issued by cluster core i and gate the issuing cluster core i clock until HW_BARRIER_2 is released. In addition, EVENT_BUFFER.EB[i] bits are cleared after the read if EVT_MASK[i]=1'b1. The read content of this bitfield is equivalent to EVENT_BUFFER_MASKED.EBM

2.1196 HW_BARRIER_3_TRIG_WAIT_CLEAR

Cluster hardware barrier 3 trigger, wait and clear command register. - Offset: `0x1ac` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.1196.1 Fields

{"reg": [{"name": "EBM", "bits": 32, "attr": ["ro"], "rotate": 0}], "config": {"lanes": 1, "fo

Bits	Type	Reset	Name
31:0	ro	0x0	EBM

2.1196.2 HW_BARRIER_3_TRIG_WAIT_CLEAR . EBM

Set HW_BARRIER_3[i] when issued by cluster core i and gate the issuing cluster core i clock until HW_BARRIER_3 is released. In addition, EVENT_BUFFER.EB[i] bits are cleared after the read if EVT_MASK[i]=1'b1. The read content of this bitfield is equivalent to EVENT_BUFFER_MASKED.EBM

2.1197 HW_BARRIER_4_TRIG_WAIT_CLEAR

Cluster hardware barrier 4 trigger, wait and clear command register. - Offset: `0x1b0` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.1197.1 Fields

{"reg": [{"name": "EBM", "bits": 32, "attr": ["ro"], "rotate": 0}], "config": {"lanes": 1, "fo

Bits	Type	Reset	Name
31:0	ro	0x0	EBM

2.1197.2 HW_BARRIER_4_TRIG_WAIT_CLEAR . EBM

Set HW_BARRIER_4[i] when issued by cluster core i and gate the issuing cluster core i clock until HW_BARRIER_4 is released. In addition, EVENT_BUFFER.EB[i] bits are cleared after the read if EVT_MASK[i]=1'b1. The read content of this bitfield is equivalent to EVENT_BUFFER_MASKED.EBM

2.1198 HW_BARRIER_5_TRIG_WAIT_CLEAR

Cluster hardware barrier 5 trigger, wait and clear command register. - Offset: `0x1b4` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.1198.1 Fields

{"reg": [{"name": "EBM", "bits": 32, "attr": ["ro"], "rotate": 0}], "config": {"lanes": 1, "fo

Bits	Type	Reset	Name
31:0	ro	0x0	EBM

2.1198.2 HW_BARRIER_5_TRIG_WAIT_CLEAR . EBM

Set HW_BARRIER_5[i] when issued by cluster core i and gate the issuing cluster core i clock until HW_BARRIER_5 is released. In addition, EVENT_BUFFER.EB[i] bits are cleared after the read if EVT_MASK[i]=1'b1. The read content of this bitfield is equivalent to EVENT_BUFFER_MASKED.EBM

2.1199 HW_BARRIER_6_TRIG_WAIT_CLEAR

Cluster hardware barrier 6 trigger, wait and clear command register. - Offset: `0x1b8` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.1199.1 Fields

{"reg": [{"name": "EBM", "bits": 32, "attr": ["ro"], "rotate": 0}], "config": {"lanes": 1, "fo

Bits	Type	Reset	Name
31:0	ro	0x0	EBM

2.1199.2 HW_BARRIER_6_TRIG_WAIT_CLEAR . EBM

Set HW_BARRIER_6[i] when issued by cluster core i and gate the issuing cluster core i clock until HW_BARRIER_6 is released. In addition, EVENT_BUFFER.EB[i] bits are cleared after the read if EVT_MASK[i]=1'b1. The read content of this bitfield is equivalent to EVENT_BUFFER_MASKED.EBM

2.1200 HW_BARRIER_7_TRIG_WAIT_CLEAR

Cluster hardware barrier 7 trigger, wait and clear command register. - Offset: `0x1bc` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.1200.1 Fields

{"reg": [{"name": "EBM", "bits": 32, "attr": ["ro"], "rotate": 0}], "config": {"lanes": 1, "fo

Bits	Type	Reset	Name
31:0	ro	0x0	EBM

2.1200.2 HW_BARRIER_7_TRIG_WAIT_CLEAR . EBM

Set HW_BARRIER_7[i] when issued by cluster core i and gate the issuing cluster core i clock until HW_BARRIER_7 is released. In addition, EVENT_BUFFER.EB[i] bits are cleared after the read if EVT_MASK[i]=1'b1. The read content of this bitfield is equivalent to EVENT_BUFFER_MASKED.EBM

2.1201 cluster_ctrl_unit / doc / registers.md

2.1202 Summary

Name	Offset	Length	Description
cluster_control_unit.EOC	0x0	4	End Of Computation status register.
cluster_control_unit.FETCH_EN	0x4	4	Cluster cores fetch enable configuration register.
cluster_control_unit.CLOCK_GATE	0x8	4	Cluster clock gate configuration register.
cluster_control_unit.DBG_RESUME	0xc	4	Cluster cores debug resume register.
cluster_control_unit.DBG_HALT_STATUS	0x10	4	Cluster cores debug halt status register.
cluster_control_unit.DBG_HALT_MASK	0x14	4	Cluster cores debug halt mask configuration register.
cluster_control_unit.BOOT_ADDR0	0x18	4	Cluster core 0 boot address configuration register.
cluster_control_unit.TCDM_ARB_POLICY_CH0	0x1c	4	TCDM arbitration policy ch0 for cluster cores configuration register.
cluster_control_unit.TCDM_ARB_POLICY_CH1	0x20	4	TCDM arbitration policy ch1 for DMA/HWCE configuration register.
cluster_control_unit.TCDM_ARB_POLICY_CH0_RDP	0x24	4	Read only duplicate of TCDM_ARB_POLICY_CH0 register
cluster_control_unit.TCDM_ARB_POLICY_CH1_RDP	0x28	4	Read only duplicate of TCDM_ARB_POLICY_CH1 register

2.1203 EOC

End Of Computation status register. - Offset: `0x0` - Reset default: `0x0` - Reset mask: `0x1`

2.1203.1 Fields

{"reg": [{"name": "eoc", "bits": 1, "attr": ["rw"], "rotate": -90}, {"bits": 31}], "config": {

Bits	Type	Reset	Name	Description
31:1				Reserved
0	rw	0x0	eoc	End of computation status flag bitfield: - 1'b0: program execution under going - 1'b1: end of computation reached

2.1204 FETCH_EN

Cluster cores fetch enable configuration register. - Offset: `0x4` - Reset default: `0x0` - Reset mask: `0xff`

2.1204.1 Fields

{"reg": [{"name": "CORE0", "bits": 1, "attr": ["rw"], "rotate": -90}, {"name": "CORE1", "bits"

Bits	Type	Reset	Name	Description
31:8				Reserved
7	rw	0x0	CORE7	Core 7 fetch enable configuration bitfield: - 1'b0: disabled - 1'b1: enabled
6	rw	0x0	CORE6	Core 6 fetch enable configuration bitfield: - 1'b0: disabled - 1'b1: enabled
5	rw	0x0	CORE5	Core 5 fetch enable configuration bitfield: - 1'b0: disabled - 1'b1: enabled
4	rw	0x0	CORE4	Core 4 fetch enable configuration bitfield: - 1'b0: disabled - 1'b1: enabled
3	rw	0x0	CORE3	Core 3 fetch enable configuration bitfield: - 1'b0: disabled - 1'b1: enabled
2	rw	0x0	CORE2	Core 2 fetch enable configuration bitfield: - 1'b0: disabled - 1'b1: enabled
1	rw	0x0	CORE1	Core 1 fetch enable configuration bitfield: - 1'b0: disabled - 1'b1: enabled
0	rw	0x0	CORE0	Core 0 fetch enable configuration bitfield: - 1'b0: disabled - 1'b1: enabled

2.1205 CLOCK_GATE

Cluster clock gate configuration register. - Offset: `0x8` - Reset default: `0x0` - Reset mask: `0x1`

2.1205.1 Fields

{"reg": [{"name": "EN", "bits": 1, "attr": ["rw"], "rotate": -90}, {"bits": 31}], "config": {"

Bits	Type	Reset	Name	Description
31:1				Reserved
0	rw	0x0	EN	Cluster clock gate configuration bitfield: - 1'b0: disabled - 1'b1: enabled

2.1206 DBG_RESUME

Cluster cores debug resume register. - Offset: `0xc` - Reset default: `0x0` - Reset mask: `0xff`

2.1206.1 Fields


```
{"reg": [{"name": "CORE0", "bits": 1, "attr": ["wo"], "rotate": -90}, {"name": "CORE1", "bits"
```


Bits	Type	Reset	Name	Description
31:8				Reserved
7	wo	0x0	CORE7	Core 7 debug resume configuration bitfield: - 1'b0: stay halted - 1'b1: resume core 7
6	wo	0x0	CORE6	Core 6 debug resume configuration bitfield: - 1'b0: stay halted - 1'b1: resume core 6
5	wo	0x0	CORE5	Core 5 debug resume configuration bitfield: - 1'b0: stay halted - 1'b1: resume core 5
4	wo	0x0	CORE4	Core 4 debug resume configuration bitfield: - 1'b0: stay halted - 1'b1: resume core 4
3	wo	0x0	CORE3	Core 3 debug resume configuration bitfield: - 1'b0: stay halted - 1'b1: resume core 3
2	wo	0x0	CORE2	Core 2 debug resume configuration bitfield: - 1'b0: stay halted - 1'b1: resume core 2
1	wo	0x0	CORE1	Core 1 debug resume configuration bitfield: - 1'b0: stay halted - 1'b1: resume core 1
0	wo	0x0	CORE0	Core 0 debug resume configuration bitfield: - 1'b0: stay halted - 1'b1: resume core 0

2.1207 DBG_HALT_STATUS

Cluster cores debug halt status register. - Offset: `0x10` - Reset default: `0x0` - Reset mask: `0xff`

2.1207.1 Fields


```
{"reg": [{"name": "CORE0", "bits": 1, "attr": ["ro"], "rotate": -90}, {"name": "CORE1", "bits"
```

Bits	Type	Reset	Name	Description
31:8				Reserved
7	ro	0x0	CORE7	Core 7 debug halt status flag bitfield: - 1'b0: running - 1'b1: halted
6	ro	0x0	CORE6	Core 6 debug halt status flag bitfield: - 1'b0: running - 1'b1: halted
5	ro	0x0	CORE5	Core 5 debug halt status flag bitfield: - 1'b0: running - 1'b1: halted
4	ro	0x0	CORE4	Core 4 debug halt status flag bitfield: - 1'b0: running - 1'b1: halted
3	ro	0x0	CORE3	Core 3 debug halt status flag bitfield: - 1'b0: running - 1'b1: halted
2	ro	0x0	CORE2	Core 2 debug halt status flag bitfield: - 1'b0: running - 1'b1: halted
1	ro	0x0	CORE1	Core 1 debug halt status flag bitfield: - 1'b0: running - 1'b1: halted
0	ro	0x0	CORE0	Core 0 debug halt status flag bitfield: - 1'b0: running - 1'b1: halted

2.1208 DBG_HALT_MASK

Cluster cores debug halt mask configuration register. - Offset: `0x14` - Reset default: `0x0` - Reset mask: `0xff`

2.1208.1 Fields

{"reg": [{"name": "CORE0", "bits": 1, "attr": ["rw"], "rotate": -90}, {"name": "CORE1", "bits"

Bits	Type	Reset	Name	Description
31:8				Reserved
7	rw	0x0	CORE7	Core 7 debug halt mask bitfield. When bit is set, core will be part of mask group and stopped when one of the members of the group stops.
6	rw	0x0	CORE6	Core 6 debug halt mask bitfield. When bit is set, core will be part of mask group and stopped when one of the members of the group stops.
5	rw	0x0	CORE5	Core 5 debug halt mask bitfield. When bit is set, core will be part of mask group and stopped when one of the members of the group stops.
4	rw	0x0	CORE4	Core 4 debug halt mask bitfield. When bit is set, core will be part of mask group and stopped when one of the members of the group stops.
3	rw	0x0	CORE3	Core 3 debug halt mask bitfield. When bit is set, core will be part of mask group and stopped when one of the members of the group stops.
2	rw	0x0	CORE2	Core 2 debug halt mask bitfield. When bit is set, core will be part of mask group and stopped when one of the members of the group stops.
1	rw	0x0	CORE1	Core 1 debug halt mask bitfield. When bit is set, core will be part of mask group and stopped when one of the members of the group stops.

Bits	Type	Reset	Name	Description
0	rw	0x0	CORE0	Core 0 debug halt mask bitfield. When bit is set, core will be part of mask group and stopped when one of the members of the group stops.

2.1209 BOOT_ADDR0

Cluster core 0 boot address configuration register. - Offset: `0x18` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.1209.1 Fields

`{"reg": [{"name": "BA", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "fon`

Bits	Type	Reset	Name	Description
31:0	rw	0x0	BA	Cluster core 0 boot address configuration bitfield.

2.1210 TCDM_ARB_POLICY_CH0

TCDM arbitration policy ch0 for cluster cores configuration register. - Offset: `0x1c` - Reset default: `0x0` - Reset mask: `0x1`

2.1210.1 Fields

`{"reg": [{"name": "POL", "bits": 1, "attr": ["rw"], "rotate": -90}, {"bits": 31}], "config": {`

Bits	Type	Reset	Name	Description
31:1				Reserved
0	rw	0x0	POL	TCDM arbitration policy for cluster cores configuration bitfield: - 1'b0: fair round robin - 1'b1: fixed order

2.1211 TCDM_ARB_POLICY_CH1

TCDM arbitration policy ch1 for DMA/HWCE configuration register. - Offset: `0x20` - Reset default: `0x0` - Reset mask: `0x1`

2.1211.1 Fields

`{"reg": [{"name": "POL", "bits": 1, "attr": ["rw"], "rotate": -90}, {"bits": 31}], "config": {`

Bits	Type	Reset	Name	Description
31:1				Reserved
0	rw	0x0	POL	TCDM arbitration policy for DMA/HWCE configuration bitfield: - 1'b0: fair round robin - 1'b1: fixed order

2.1212 TCDM_ARB_POLICY_CH0_REP

Read only duplicate of TCDM_ARB_POLICY_CH0 register - Offset: `0x24` - Reset default: `0x0` - Reset mask: `0x1`

2.1212.1 Fields

`{"reg": [{"name": "POL", "bits": 1, "attr": ["rw"], "rotate": -90}, {"bits": 31}], "config": {`

Bits	Type	Reset	Name	Description
31:1				Reserved
0	rw	0x0	POL	TCDM arbitration policy for cluster cores configuration bitfield: - 1'b0: fair round robin - 1'b1: fixed order

2.1213 TCDM_ARB_POLICY_CH1_REP

Read only duplicate of TCDM_ARB_POLICY_CH1 register - Offset: `0x28` - Reset default: `0x0` - Reset mask: `0x1`

2.1213.1 Fields

`{"reg": [{"name": "POL", "bits": 1, "attr": ["rw"], "rotate": -90}, {"bits": 31}], "config": {`

Bits	Type	Reset	Name	Description
31:1				Reserved
0	rw	0x0	POL	TCDM arbitration policy for DMA/HWCE configuration bitfield: - 1'b0: fair round robin - 1'b1: fixed order

2.1214 cluster_icache_ctrl / doc / registers.md

2.1215 Summary

Name	Offset	Length	Description
cluster_icache_ctrl.ENABLE	0x0	4	Cluster instruction cache unit enable configuration register.
cluster_icache_ctrl.FLUSH	0x4	4	Cluster instruction cache unit flush command register.
cluster_icache_ctrl.L0_FLUSH	0x8	4	Cluster level 0 instruction cache unit flush command register.
cluster_icache_ctrl.SEL_FLUSH	0xc	4	Cluster instruction cache unit selective flush command register.
cluster_icache_ctrl.L1_L15_PREFETCH	0x10	4	Enable L1 and L1.5 prefetch register.

2.1216 ENABLE

Cluster instruction cache unit enable configuration register. - Offset: `0x0` - Reset default: `0x0` - Reset mask: `0x1`

2.1216.1 Fields

`{"reg": [{"name": "EN", "bits": 1, "attr": ["rw"], "rotate": -90}, {"bits": 31}], "config": {"`

Bits	Type	Reset	Name	Description
31:1				Reserved
0	rw	0x0	EN	Cluster instruction cache enable configuration bitfield: - 1'b0: disabled - 1'b1: enabled

2.1217 FLUSH

Cluster instruction cache unit flush command register. - Offset: `0x4` - Reset default: `0x0` - Reset mask: `0x1`

2.1217.1 Fields

`{"reg": [{"name": "FL", "bits": 1, "attr": ["rw"], "rotate": -90}, {"bits": 31}], "config": {"`

Bits	Type	Reset	Name	Description
31:1				Reserved
0	rw	0x0	FL	Cluster instruction cache full flush command.

2.1218 L0_FLUSH

Cluster level 0 instruction cache unit flush command register. - Offset: `0x8` - Reset default: `0x0` - Reset mask: `0x1`

2.1218.1 Fields

{"reg": [{"name": "L0_FL", "bits": 1, "attr": ["rw"], "rotate": -90}, {"bits": 31}], "config":

Bits	Type	Reset	Name	Description
31:1				Reserved
0	rw	0x0	L0_FL	Cluster level 0 instruction cache full flush command.

2.1219 SEL_FLUSH

Cluster instruction cache unit selective flush command register. - Offset: `0xc` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.1219.1 Fields

{"reg": [{"name": "ADDR", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "f

Bits	Type	Reset	Name	Description
31:0	rw	0x0	ADDR	Cluster instruction cache selective flush address configuration bitfield.

2.1220 L1_L15_PREFETCH

Enable L1 and L1.5 prefetch register. - Offset: `0x10` - Reset default: `0x0` - Reset mask: `0xff`

2.1220.1 Fields

{"reg": [{"name": "CORE0", "bits": 1, "attr": ["rw"], "rotate": -90}, {"name": "CORE1", "bits"

Bits	Type	Reset	Name	Description
31:8				Reserved
7	rw	0x0	CORE7	Core 7 icache prefetch enable configuration bitfield: - 1'b0: disabled - 1'b1: enabled
6	rw	0x0	CORE6	Core 6 icache prefetch enable configuration bitfield: - 1'b0: disabled - 1'b1: enabled
5	rw	0x0	CORE5	Core 5 icache prefetch enable configuration bitfield: - 1'b0: disabled - 1'b1: enabled
4	rw	0x0	CORE4	Core 4 icache prefetch enable configuration bitfield: - 1'b0: disabled - 1'b1: enabled

Bits	Type	Reset	Name	Description
3	rw	0x0	CORE3	Core 3 icache prefetch enable configuration bitfield: - 1'b0: disabled - 1'b1: enabled
2	rw	0x0	CORE2	Core 2 icache prefetch enable configuration bitfield: - 1'b0: disabled - 1'b1: enabled
1	rw	0x0	CORE1	Core 1 icache prefetch enable configuration bitfield: - 1'b0: disabled - 1'b1: enabled
0	rw	0x0	CORE0	Core 0 icache prefetch enable configuration bitfield: - 1'b0: disabled - 1'b1: enabled

2.1221 ethernet / doc / registers.md

2.1222 Summary

Name	Offset	Length	Description
eth_framing.CONFIG0	0x0	4	Configures the lower 4 bytes of the devices MAC address
eth_framing.CONFIG1	0x4	4	Configures the: upper 2 bytes of the devices MAC address, promiscuous flag, MDIO interface
eth_framing.CONFIG2	0x8	4	The FCS TX status
eth_framing.CONFIG3	0xc	4	The FCS RX status

2.1223 CONFIG0

Configures the lower 4 bytes of the devices MAC address - Offset: `0x0` - Reset default: `0x890702` - Reset mask: `0xffffffff`

2.1223.1 Fields

`{"reg": [{"name": "lower_mac_address", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"`

Bits	Type	Reset	Name	Description
31:0	rw	0x890702	lower_mac_address	Lower 32 bit of the devices MAC address

2.1224 CONFIG1

Configures the: upper 2 bytes of the devices MAC address, promiscuous flag, MDIO interface - Offset: `0x4` - Reset default: `0x2301` - Reset mask: `0xffffff`

2.1224.1 Fields

{"reg": [{"name": "upper_mac_address", "bits": 16, "attr": ["rw"], "rotate": 0}, {"name": "pro

Bits	Type	Reset	Name	Description
31:20				Reserved
19	rw	0x0	phy_mdio_oe	MDIO output enable
18	rw	0x0	phy_mdio_o	MDIO output
17	rw	0x0	phy_mdclk	MDIO clock
16	rw	0x0	promiscuous	promiscuous flag
15:0	rw	0x2301	upper_mac_address	Upper 16 bit of the devices MAC address

2.1225 CONFIG2

The FCS TX status - Offset: `0x8` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.1225.1 Fields

{"reg": [{"name": "tx_fcs_reg", "bits": 32, "attr": ["ro"], "rotate": 0}], "config": {"lanes":

Bits	Type	Reset	Name	Description
31:0	ro	0x0	tx_fcs_reg	FCS TX status

2.1226 CONFIG3

The FCS RX status - Offset: `0xc` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.1226.1 Fields

{"reg": [{"name": "rx_fcs_reg", "bits": 32, "attr": ["ro"], "rotate": 0}], "config": {"lanes":

Bits	Type	Reset	Name	Description
31:0	ro	0x0	rx_fcs_reg	FCS RX status

2.1227 fp_cluster / doc / registers.md

2.1228 Summary

Name	Offset	Length	Description
spatz_cluster_peripheral.PERF_COUNTER_ENABLE_0	0x0	8	Enable particular performance counter and start tracking.
spatz_cluster_peripheral.PERF_COUNTER_ENABLE_1	0x8	8	Enable particular performance counter and start tracking.
spatz_cluster_peripheral.HART_SELECT0	0x10	8	Select from which hart in the cluster, starting from 0,
spatz_cluster_peripheral.HART_SELECT1	0x18	8	Select from which hart in the cluster, starting from 0,
spatz_cluster_peripheral.PERF_COUNTER_0	0x20	8	Performance counter. Set corresponding PERF_COUNTER_ENABLE bits depending on what
spatz_cluster_peripheral.PERF_COUNTER_1	0x28	8	Performance counter. Set corresponding PERF_COUNTER_ENABLE bits depending on what
spatz_cluster_peripheral.CL_CLINT_SET	0x30	8	Set bits in the cluster-local CLINT. Writing a 1 at location i sets the cluster-local interrupt
spatz_cluster_peripheral.CL_CLINT_CLEAR	0x38	8	Clear bits in the cluster-local CLINT. Writing a 1 at location i clears the cluster-local interrupt
spatz_cluster_peripheral.HW_BARRIER	0x40	8	Hardware barrier register. Loads to this register will block until all cores have
spatz_cluster_peripheral.ICACHE_PREFETCH_ENABLE	0x48	8	Controls prefetching of the instruction cache.
spatz_cluster_peripheral.SPATZ_STATUS	0x50	8	Sets the status of the Spatz cluster.
spatz_cluster_peripheral.CLUSTER_BOOT_CONTROL	0x58	8	Controls the cluster boot process.

2.1229 PERF_COUNTER_ENABLE

Enable particular performance counter and start tracking. - Reset default: `0x0` - Reset mask: `0x7fffffff`

2.1229.1 Instances

Name	Offset
PERF_COUNTER_ENABLE_0	0x0
PERF_COUNTER_ENABLE_1	0x8

2.1229.2 Fields

{"reg": [{"name": "CYCLE", "bits": 1, "attr": ["rw"], "rotate": -90}, {"name": "TCDM_ACCESSED"

Bits	Type	Reset	Name
63:31			Reserved
30	rw	0x0	ICACHE_STALL
29	rw	0x0	ICACHE_DOUBLE_HIT
28	rw	0x0	ICACHE_PREFETCH
27	rw	0x0	ICACHE_HIT
26	rw	0x0	ICACHE_MISS
25	rw	0x0	DMA_BUSY
24	rw	0x0	DMA_B_DONE
23	rw	0x0	DMA_W_BW
22	rw	0x0	DMA_W_DONE
21	rw	0x0	DMA_R_BW
20	rw	0x0	DMA_R_DONE
19	rw	0x0	DMA_AR_BW
18	rw	0x0	DMA_AR_DONE
17	rw	0x0	DMA_AW_BW
16	rw	0x0	DMA_AW_DONE
15	rw	0x0	DMA_BUF_R_STALL
14	rw	0x0	DMA_BUF_W_STALL
13	rw	0x0	DMA_W_STALL
12	rw	0x0	DMA_R_STALL
11	rw	0x0	DMA_AR_STALL
10	rw	0x0	DMA_AW_STALL
9	rw	0x0	RETIRED_ACC
8	rw	0x0	RETIRED_I
7	rw	0x0	RETIRED_LOAD
6	rw	0x0	RETIRED_INSTR
5	rw	0x0	ISSUE_CORE_TO_FPU
4	rw	0x0	ISSUE_FPU_SEQ
3	rw	0x0	ISSUE_FPU
2	rw	0x0	TCDM_CONGESTED
1	rw	0x0	TCDM_ACCESSED
0	rw	0x0	CYCLE

2.1229.3 PERF_COUNTER_ENABLE . ICACHE_STALL

Incremented for instruction cache stalls. *This is a hart-local signal*

2.1229.4 PERF_COUNTER_ENABLE . ICACHE_DOUBLE_HIT

Incremented for instruction cache double hit. *This is a hart-local signal*

2.1229.5 PERF_COUNTER_ENABLE . ICACHE_PREFETCH

Incremented for instruction cache prefetches. *This is a hart-local signal*

2.1229.6 PERF_COUNTER_ENABLE . ICACHE_HIT

Incremented for instruction cache hits. *This is a hart-local signal*

2.1229.7 PERF_COUNTER_ENABLE . ICACHE_MISS

Incremented for instruction cache misses. *This is a hart-local signal*

2.1229.8 PERF_COUNTER_ENABLE . DMA_BUSY

Incremented whenever DMA is busy. *This is a DMA-local signal*

2.1229.9 PERF_COUNTER_ENABLE . DMA_B_DONE

Incremented whenever B handshake occurs. *This is a DMA-local signal*

2.1229.10 PERF_COUNTER_ENABLE . DMA_W_BW

Whenever W handshake occurs, the counter is incremented by the number of bytes transfered in this cycle *This is a DMA-local signal*

2.1229.11 PERF_COUNTER_ENABLE . DMA_W_DONE

Incremented whenvever W handshake occurs. *This is a DMA-local signal*

2.1229.12 PERF_COUNTER_ENABLE . DMA_R_BW

Whenever R handshake occurs, the counter is incremented by the number of bytes transfered in this cycle *This is a DMA-local signal*

2.1229.13 PERF_COUNTER_ENABLE . DMA_R_DONE

Incremented whenever R handshake occurs. *This is a DMA-local signal*

2.1229.14 PERF_COUNTER_ENABLE . DMA_AR_BW

Whenever AR handshake occurs, the counter is incremented by the number of bytes transfered for this transaction *This is a DMA-local signal*

2.1229.15 PERF_COUNTER_ENABLE . DMA_AR_DONE

Incremented whenever AR handshake occurs. *This is a DMA-local signal*

2.1229.16 PERF_COUNTER_ENABLE . DMA_AW_BW

Whenever AW handshake occurs, the counter is incremented by the number of bytes transfered for this transaction *This is a DMA-local signal*

2.1229.17 PERF_COUNTER_ENABLE . DMA_AW_DONE

Incremented whenever AW handshake occurs. *This is a DMA-local signal*

2.1229.18 PERF_COUNTER_ENABLE . DMA_BUF_R_STALL

Incremented whenever r_valid = 1 but r_ready = 0. *This is a DMA-local signal*

2.1229.19 PERF_COUNTER_ENABLE . DMA_BUF_W_STALL

Incremented whenever w_ready = 1 but w_valid = 0. *This is a DMA-local signal*

2.1229.20 PERF_COUNTER_ENABLE . DMA_W_STALL

Incremented whenever w_valid = 1 but w_ready = 0. *This is a DMA-local signal*

2.1229.21 PERF_COUNTER_ENABLE . DMA_R_STALL

Incremented whenever r_ready = 1 but r_valid = 0. *This is a DMA-local signal*

2.1229.22 PERF_COUNTER_ENABLE . DMA_AR_STALL

Incremented whenever ar_valid = 1 but ar_ready = 0. *This is a DMA-local signal*

2.1229.23 PERF_COUNTER_ENABLE . DMA_AW_STALL

Incremented whenever aw_valid = 1 but aw_ready = 0. *This is a DMA-local signal*

2.1229.24 PERF_COUNTER_ENABLE . RETIRED_ACC

Offloaded instructions retired by the core. *This is a hart-local signal.*

2.1229.25 PERF_COUNTER_ENABLE . RETIRED_I

Base instructions retired by the core. *This is a hart-local signal.*

2.1229.26 PERF_COUNTER_ENABLE . RETIRED_LOAD

Load instructions retired by the core. *This is a hart-local signal.*

2.1229.27 PERF_COUNTER_ENABLE . RETIRED_INSTR

Instructions retired by the core. *This is a hart-local signal.*

2.1229.28 PERF_COUNTER_ENABLE . ISSUE_CORE_TO_FPU

Incremented whenever the core issues an FPU instruction. *This is a hart-local signal.*

2.1229.29 PERF_COUNTER_ENABLE . ISSUE_FPU_SEQ

Incremented whenever the FPU Sequencer issues an FPU instruction. Might be non available if the hardware doesn't support FREP. *This is a hart-local signal.*

2.1229.30 PERF_COUNTER_ENABLE . ISSUE_FPU

Core operations performed in the FPU. *This is a hart-local signal.*

2.1229.31 PERF_COUNTER_ENABLE . TCDM_CONGESTED

Incremented whenever an access twoards the TCDM is made but the arbitration logic didn't grant the access (due to congestion). Is strictly less than TCDM_ACCESSED. *This is a cluster-global signal.*

2.1229.32 PERF_COUNTER_ENABLE . TCDM_ACCESSED

Increased whenever the TCDM is accessed. Each individual access is tracked, so if `n` cores access the TCDM, `n` will be added. Accesses are tracked at the TCDM, so it doesn't matter whether the cores or the for example the SSR hardware accesses the TCDM. *This is a cluster-global signal.*

2.1229.33 PERF_COUNTER_ENABLE . CYCLE

Cycle counter. Counts up as long as the cluster is powered.

2.1230 HART_SELECT

Select from which hart in the cluster, starting from `0`, the event should be counted. For each performance counter the cores can be selected individually. If a hart greater than the clusters total hart size is selected the selection will wrap and the hart corresponding to `hart_select % total_harts_in_cluster` will be selected. - Reset default: `0x0` - Reset mask: `0x3ff`

2.1230.1 Instances

Name	Offset
HART_SELECT_0	0x10
HART_SELECT_1	0x18

2.1230.2 Fields

{"reg": [{"name": "HART_SELECT", "bits": 10, "attr": ["rw"], "rotate": -90}, {"bits": 54}], "co

Bits	Type	Reset	Name	Description
63:10				Reserved
9:0	rw	0x0	HART_SELECT	Select source of per-hart performance counter

2.1231 PERF_COUNTER

Performance counter. Set corresponding PERF_COUNTER_ENABLE bits depending on what performance metric you would like to track. - Reset default: `0x0` - Reset mask: `0xffffffffffff`

2.1231.1 Instances

Name	Offset
PERF_COUNTER_0	0x20
PERF_COUNTER_1	0x28

2.1231.2 Fields

{"reg": [{"name": "PERF_COUNTER", "bits": 48, "attr": ["rw"], "rotate": 0}, {"bits": 16}], "co

Bits	Type	Reset	Name	Description
63:48				Reserved
47:0	rw	x	PERF_COUNTER	Performance counter

2.1232 CL_CLINT_SET

Set bits in the cluster-local CLINT. Writing a 1 at location i sets the cluster-local interrupt of hart i, where i is relative to the first hart in the cluster, ignoring the cluster base hart ID. - Offset: `0x30` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.1232.1 Fields

{"reg": [{"name": "CL_CLINT_SET", "bits": 32, "attr": ["wo"], "rotate": 0}, {"bits": 32}], "co

Bits	Type	Reset	Name	Description
63:32				Reserved
31:0	wo	x	CL_CLINT_SET	Set cluster-local interrupt of hart i

2.1233 CL_CLINT_CLEAR

Clear bits in the cluster-local CLINT. Writing a 1 at location i clears the cluster-local interrupt of hart i, where i is relative to the first hart in the cluster, ignoring the cluster base hart ID. - Offset: `0x38` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.1233.1 Fields

{"reg": [{"name": "CL_CLINT_CLEAR", "bits": 32, "attr": ["wo"], "rotate": 0}, {"bits": 32}], "

Bits	Type	Reset	Name	Description
63:32				Reserved
31:0	wo	x	CL_CLINT_CLEAR	Clear cluster-local interrupt of hart i

2.1234 HW_BARRIER

Hardware barrier register. Loads to this register will block until all cores have performed the load. At this stage we know that they reached the same point in the control flow, i.e., the cores are synchronized. - Offset: `0x40` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.1234.1 Fields

{"reg": [{"name": "HW_BARRIER", "bits": 32, "attr": ["ro"], "rotate": 0}, {"bits": 32}], "conf

Bits	Type	Reset	Name	Description
63:32				Reserved
31:0	ro	x	HW_BARRIER	Hardware barrier register.

2.1235 ICACHE_PREFETCH_ENABLE

Controls prefetching of the instruction cache. - Offset: `0x48` - Reset default: `0x1` - Reset mask: `0x1`

2.1235.1 Fields

{"reg": [{"name": "ICACHE_PREFETCH_ENABLE", "bits": 1, "attr": ["wo"], "rotate": -90}, {"bits"

Bits	Type	Reset	Name	Description
63:1				Reserved
0	wo	0x1	ICACHE_PREFETCH_ENABLE	Hardware barrier register.

2.1236 SPATZ_STATUS

Sets the status of the Spatz cluster. - Offset: `0x50` - Reset default: `0x0` - Reset mask: `0x1`

2.1236.1 Fields

{"reg": [{"name": "SPATZ_CLUSTER_PROBE", "bits": 1, "attr": ["wo"], "rotate": -90}, {"bits": 63

Bits	Type	Reset	Name	Description
63:1				Reserved
0	wo	0x0	SPATZ_CLUSTER_PROBE	Indicates the cluster is computing a kernel.

2.1237 CLUSTER_BOOT_CONTROL

Controls the cluster boot process. - Offset: `0x58` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.1237.1 Fields

{"reg": [{"name": "ENTRY_POINT", "bits": 32, "attr": ["rw"], "rotate": 0}, {"bits": 32}], "con

Bits	Type	Reset	Name	Description
63:32				Reserved
31:0	rw	0x0	ENTRY_POINT	Post-bootstrapping entry point.

2.1238 gp_timer1_system_timer / doc / registers.md

2.1239 Summary

Name	Offset	Length	Description
timer_unit.CFG_LO	0x0	4	Timer Low Configuration register.

Name	Offset	Length	Description
timer_unit.CFG_HI	0x4	4	Timer HIGH Configuration register.
timer_unit.CNT_LO	0x8	4	Timer Low counter value register.
timer_unit.CNT_HI	0xc	4	Timer High counter value register.
timer_unit.CMP_LO	0x10	4	Timer Low comparator value register.
timer_unit.CMP_HI	0x14	4	Timer High comparator value register.
timer_unit.START_LO	0x18	4	Start Timer Low counting register.
timer_unit.START_HI	0x1c	4	Start Timer High counting register.
timer_unit.RESET_LO	0x20	4	Reset Timer Low counter register.
timer_unit.RESET_HI	0x24	4	Reset Timer High counter register.

2.1240 CFG_LO

Timer Low Configuration register. - Offset: `0x0` - Reset default: `0x0` - Reset mask: `0x8000ffff`

2.1240.1 Fields


```
{"reg": [{"name": "ENABLE", "bits": 1, "attr": ["rw"], "rotate": -90}, {"name": "RESET", "bits"
```


Bits	Type	Reset	Name	Description
31	rw	0x0	CASC	Timer low + Timer high 64bit cascaded mode configuration bitfield.
30:16				Reserved
15:8	rw	0x0	PVAL	Timer low prescaler value bitfield. Ftimer = Fclk / (1 + PRESC_VAL)
7	rw	0x0	CCFG	Timer low clock source configuration bitfield: - 1'b0: FLL or FLL+Prescaler - 1'b1: Reference clock at 32kHz
6	rw	0x0	PEN	Timer low prescaler enable configuration bitfield: - 1'b0: disabled - 1'b1: enabled
5	rw	0x0	ONE_S	Timer low one shot configuration bitfield: - 1'b0: let Timer low enabled counting when compare match with CMP_LO occurs. - 1'b1: disable Timer low when compare match with CMP_LO occurs.
4	rw	0x0	MODE	Timer low continuous mode configuration bitfield: - 1'b0: Continue mode - continue incrementing Timer low counter when compare match with CMP_LO occurs. - 1'b1: Cycle mode - reset Timer low counter when compare match with CMP_LO occurs.
3	rw	0x0	IEM	Timer low input event mask configuration bitfield: - 1'b0: disabled - 1'b1: enabled
2	rw	0x0	IRQEN	Timer low compare match interrupt enable configuration bitfield: - 1'b0: disabled - 1'b1: enabled
1	rw	0x0	RESET	Timer low counter reset command bitfield. Cleared after Timer Low reset execution.
0	rw	0x0	ENABLE	Timer low enable configuration bitfield: - 1'b0: disabled - 1'b1: enabled

2.1241 CFG_HI

Timer HIGH Configuration register. - Offset: `0x4` - Reset default: `0x0` - Reset mask: `0xff`

2.1241.1 Fields

`{"reg": [{"name": "ENABLE", "bits": 1, "attr": ["rw"], "rotate": -90}, {"name": "RESET", "bits"`

Bits	Type	Reset	Name	Description
31:8				Reserved
7	rw	0x0	CLKCFG	Timer high clock source configuration bitfield: - 1'b0: FLL or FLL+Prescaler - 1'b1: Reference clock at 32kHz
6	rw	0x0	PEN	Timer high prescaler enable configuration bitfield: - 1'b0: disabled - 1'b1: enabled
5	rw	0x0	ONETS	Timer high one shot configuration bitfield: - 1'b0: let Timer high enabled counting when compare match with CMP_HI occurs. - 1'b1: disable Timer high when compare match with CMP_HI occurs.
4	rw	0x0	MODE	Timer high continuous mode configuration bitfield: - 1'b0: Continue mode - continue incrementing Timer high counter when compare match with CMP_HI occurs. - 1'b1: Cycle mode - reset Timer high counter when compare match with CMP_HI occurs.
3	rw	0x0	IEM	Timer high input event mask configuration bitfield: - 1'b0: disabled - 1'b1: enabled
2	rw	0x0	IRQEN	Timer high compare match interrupt enable configuration bitfield: - 1'b0: disabled - 1'b1: enabled
1	wo	0x0	RESET	Timer high counter reset command bitfield. Cleared after Timer high reset execution.
0	rw	0x0	ENABLE	Timer high enable configuration bitfield: - 1'b0: disabled - 1'b1: enabled

2.1242 CNT_LO

Timer Low counter value register. - Offset: `0x8` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.1242.1 Fields

`{"reg": [{"name": "cnt_lo", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "`

Bits	Type	Reset	Name	Description
31:0	rw	0x0	cnt_lo	Timer Low counter value bitfield.

2.1243 CNT_HI

Timer High counter value register. - Offset: `0xc` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.1243.1 Fields

{"reg": [{"name": "cnt_hi", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	cnt_hi	Timer High counter value bitfield.

2.1244 CMP_LO

Timer Low comparator value register. - Offset: `0x10` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.1244.1 Fields

{"reg": [{"name": "cmp_lo", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	cmp_lo	Timer Low comparator value bitfield.

2.1245 CMP_HI

Timer High comparator value register. - Offset: `0x14` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.1245.1 Fields

{"reg": [{"name": "cmp_hi", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	cmp_hi	Timer High comparator value bitfield.

2.1246 START_LO

Start Timer Low counting register. - Offset: `0x18` - Reset default: `0x0` - Reset mask: `0x1`

2.1246.1 Fields

{"reg": [{"name": "strt_lo", "bits": 1, "attr": ["wo"], "rotate": -90}, {"bits": 31}], "config"

Bits	Type	Reset	Name	Description
31:1				Reserved
0	wo	0x0	strt_lo	Timer Low start command bitfield. When executed, CFG_LO.ENABLE is set.

2.1247 START_HI

Start Timer High counting register. - Offset: `0x1c` - Reset default: `0x0` - Reset mask: `0x1`

2.1247.1 Fields


```
{"reg": [{"name": "strt_hi", "bits": 1, "attr": ["wo"], "rotate": -90}, {"bits": 31}], "config"
```


Bits	Type	Reset	Name	Description
31:1				Reserved
0	wo	0x0	strt_hi	Timer High start command bitfield. When executed, CFG_HI.ENABLE is set.

2.1248 RESET_LO

Reset Timer Low counter register. - Offset: `0x20` - Reset default: `0x0` - Reset mask: `0x1`

2.1248.1 Fields


```
{"reg": [{"name": "rst_lo", "bits": 1, "attr": ["wo"], "rotate": -90}, {"bits": 31}], "config"
```


Bits	Type	Reset	Name	Description
31:1				Reserved
0	wo	0x0	rst_lo	Timer Low counter reset command bitfield. When executed, CFG_LO.RESET is set.

2.1249 RESET_HI

Reset Timer High counter register. - Offset: `0x24` - Reset default: `0x0` - Reset mask: `0x1`

2.1249.1 Fields


```
{"reg": [{"name": "rst_hi", "bits": 1, "attr": ["wo"], "rotate": -90}, {"bits": 31}], "config"
```

Bits	Type	Reset	Name	Description
31:1				Reserved
0	wo	0x0	rst_hi	Timer High counter reset command bitfield. When executed, CFG_HI.RESET is set.

2.1250 gp_timer2_advanced_timer / doc / registers.md

2.1251 Summary

Name	Offset	Length	Description
apb_adv_timer.T0_CMD	0x0	4	ADV_TIMER0 command register.
apb_adv_timer.T0_CONFIG	0x4	4	ADV_TIMER0 configuration register.
apb_adv_timer.T0_THRESHOLD	0x8	4	ADV_TIMER0 threshold configuration register.
apb_adv_timer.T0_TH_CHANNEL0	0xc	4	ADV_TIMER0 channel 0 threshold configuration register.
apb_adv_timer.T0_TH_CHANNEL1	0x10	4	ADV_TIMER0 channel 1 threshold configuration register.
apb_adv_timer.T0_TH_CHANNEL2	0x14	4	ADV_TIMER0 channel 2 threshold configuration register.
apb_adv_timer.T0_TH_CHANNEL3	0x18	4	ADV_TIMER0 channel 3 threshold configuration register.
apb_adv_timer.T0_COUNTER	0x1c	4	ADV_TIMER0 counter register.
apb_adv_timer.T1_CMD	0x20	4	ADV_TIMER1 command register.
apb_adv_timer.T1_CONFIG	0x24	4	ADV_TIMER1 configuration register.
apb_adv_timer.T1_THRESHOLD	0x28	4	ADV_TIMER1 threshold configuration register.
apb_adv_timer.T1_TH_CHANNEL0	0x2c	4	ADV_TIMER1 channel 0 threshold configuration register.
apb_adv_timer.T1_TH_CHANNEL1	0x30	4	ADV_TIMER1 channel 1 threshold configuration register.
apb_adv_timer.T1_TH_CHANNEL2	0x34	4	ADV_TIMER1 channel 2 threshold configuration register.
apb_adv_timer.T1_TH_CHANNEL3	0x38	4	ADV_TIMER1 channel 3 threshold configuration register.
apb_adv_timer.T1_COUNTER	0x3c	4	ADV_TIMER1 counter register.
apb_adv_timer.T2_CMD	0x40	4	ADV_TIMER2 command register.
apb_adv_timer.T2_CONFIG	0x44	4	ADV_TIMER2 configuration register.
apb_adv_timer.T2_THRESHOLD	0x48	4	ADV_TIMER2 threshold configuration register.
apb_adv_timer.T2_TH_CHANNEL0	0x4c	4	ADV_TIMER2 channel 0 threshold configuration register.
apb_adv_timer.T2_TH_CHANNEL1	0x50	4	ADV_TIMER2 channel 1 threshold configuration register.

Name	Offset	Length	Description
apb_adv_timer.T2_TH_CHANNEL2	0x54	4	ADV_TIMER2 channel 2 threshold configuration register.
apb_adv_timer.T2_TH_CHANNEL3	0x58	4	ADV_TIMER2 channel 3 threshold configuration register.
apb_adv_timer.T2_COUNTER	0x5c	4	ADV_TIMER2 counter register.
apb_adv_timer.T3_CMD	0x60	4	ADV_TIMER3 command register.
apb_adv_timer.T3_CONFIG	0x64	4	ADV_TIMER3 configuration register.
apb_adv_timer.T3_THRESHOLD	0x68	4	ADV_TIMER3 threshold configuration register.
apb_adv_timer.T3_TH_CHANNEL0	0x6c	4	ADV_TIMER3 channel 0 threshold configuration register.
apb_adv_timer.T3_TH_CHANNEL1	0x70	4	ADV_TIMER3 channel 1 threshold configuration register.
apb_adv_timer.T3_TH_CHANNEL2	0x74	4	ADV_TIMER3 channel 2 threshold configuration register.
apb_adv_timer.T3_TH_CHANNEL3	0x78	4	ADV_TIMER3 channel 3 threshold configuration register.
apb_adv_timer.T3_COUNTER	0x7c	4	ADV_TIMER3 counter register.
apb_adv_timer.EVENT_CFG	0x80	4	ADV_TIMERS events configuration register.
apb_adv_timer.CG	0x84	4	ADV_TIMERS channels clock gating configuration register.

2.1252 T0_CMD

ADV_TIMER0 command register. - Offset: `0x0` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.1252.1 Fields

`{"reg": [{"name": "START", "bits": 1, "attr": ["wo"], "rotate": -90}, {"name": "STOP", "bits":`

Bits	Type	Reset	Name	Description
31:5	wo	0x0	RFU	?
4	wo	0x0	ARM	ADV_TIMER0 arm command bitfield.
3	wo	0x0	RESET	ADV_TIMER0 reset command bitfield.
2	wo	0x0	UPDATE	ADV_TIMER0 update command bitfield.
1	wo	0x0	STOP	ADV_TIMER0 stop command bitfield.
0	wo	0x0	START	ADV_TIMER0 start command bitfield.

2.1253 T0_CONFIG

ADV_TIMER0 configuration register. - Offset: `0x4` - Reset default: `0x1000` - Reset mask: `0xff1fff`

2.1253.1 Fields

{"reg": [{"name": "INSEL", "bits": 8, "attr": ["rw"], "rotate": 0}, {"name": "MODE", "bits": 3

Bits	Type	Reset	Name
31:24			Reserved
23:16	rw	0x0	PRESC
15:13			Reserved
12	rw	0x1	UPDOWNSEL
11	rw	0x0	CLKSEL
10:8	rw	0x0	MODE
7:0	rw	0x0	INSEL

2.1253.2 T0_CONFIG . PRESC

ADV_TIMER0 prescaler value configuration bitfield.

2.1253.3 T0_CONFIG . UPDOWNSEL

ADV_TIMER0 center-aligned mode configuration bitfield: - 1'b0: The counter counts up and down alternatively. - 1'b1: The counter counts up and resets to 0 when reach threshold.

2.1253.4 T0_CONFIG . CLKSEL

ADV_TIMER0 clock source configuration bitfield: - 1'b0: FLL - 1'b1: reference clock at 32kHz

2.1253.5 T0_CONFIG . MODE

ADV_TIMER0 trigger mode configuration bitfield: - 3'h0: trigger event at each clock cycle. - 3'h1: trigger event if input source is 0 - 3'h2: trigger event if input source is 1 - 3'h3: trigger event on input source rising edge - 3'h4: trigger event on input source falling edge - 3'h5: trigger event on input source falling or rising edge - 3'h6: trigger event on input source rising edge when armed - 3'h7: trigger event on input source falling edge when armed

2.1253.6 T0_CONFIG . INSEL

ADV_TIMER0 input source configuration bitfield: - 0-31: GPIO[0] to GPIO[31] - 32-35: Channel 0 to 3 of ADV_TIMER0 - 36-39: Channel 0 to 3 of ADV_TIMER1 - 40-43: Channel 0 to 3 of ADV_TIMER2 - 44-47: Channel 0 to 3 of ADV_TIMER3

2.1254 T0_THRESHOLD

ADV_TIMER0 threshold configuration register. - Offset: `0x8` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.1254.1 Fields

{"reg": [{"name": "TH_LO", "bits": 16, "attr": ["rw"], "rotate": 0}, {"name": "TH_HI", "bits":

Bits	Type	Reset	Name	Description
31:16	rw	0x0	TH_HI	ADV_TIMER0 threshold high part configuration bitfield. It defines end counter value.
15:0	rw	0x0	TH_LO	ADV_TIMER0 threshold low part configuration bitfield. It defines start counter value.

2.1255 T0_TH_CHANNEL0

ADV_TIMER0 channel 0 threshold configuration register. - Offset: `0xc` - Reset default: `0x0` - Reset mask: `0x7ffff`

2.1255.1 Fields

{"reg": [{"name": "TH", "bits": 16, "attr": ["rw"], "rotate": 0}, {"name": "MODE", "bits": 3, "

Bits	Type	Reset	Name
31:19			Reserved
18:16	rw	0x0	MODE
15:0	rw	0x0	TH

2.1255.2 T0_TH_CHANNEL0 . MODE

ADV_TIMER0 channel 0 threshold match action on channel output signal configuration bitfield: - 3'h0: set. - 3'h1: toggle then next threshold match action is clear. - 3'h2: set then next threshold match action is clear. - 3'h3: toggle. - 3'h4: clear. - 3'h5: toggle then next threshold match action is set. - 3'h6: clear then next threshold match action is set.

2.1255.3 T0_TH_CHANNEL0 . TH

ADV_TIMER0 channel 0 threshold configuration bitfield.

2.1256 T0_TH_CHANNEL1

ADV_TIMER0 channel 1 threshold configuration register. - Offset: `0x10` - Reset default: `0x0` - Reset mask: `0x7ffff`

2.1256.1 Fields

{"reg": [{"name": "TH", "bits": 16, "attr": ["rw"], "rotate": 0}, {"name": "MODE", "bits": 3, "

Bits	Type	Reset	Name
31:19			Reserved
18:16	rw	0x0	MODE
15:0	rw	0x0	TH

2.1256.2 T0_TH_CHANNEL1 . MODE

ADV_TIMER0 channel 1 threshold match action on channel output signal configuration bitfield: - 3'h0: set. - 3'h1: toggle then next threshold match action is clear. - 3'h2: set then next threshold match action is clear. - 3'h3: toggle. - 3'h4: clear. - 3'h5: toggle then next threshold match action is set. - 3'h6: clear then next threshold match action is set.

2.1256.3 T0_TH_CHANNEL1 . TH

ADV_TIMER0 channel 1 threshold configuration bitfield.

2.1257 T0_TH_CHANNEL2

ADV_TIMER0 channel 2 threshold configuration register. - Offset: `0x14` - Reset default: `0x0` - Reset mask: `0x7ffff`

2.1257.1 Fields

{"reg": [{"name": "TH", "bits": 16, "attr": ["rw"], "rotate": 0}, {"name": "MODE", "bits": 3, "

Bits	Type	Reset	Name
31:19			Reserved
18:16	rw	0x0	MODE
15:0	rw	0x0	TH

2.1257.2 T0_TH_CHANNEL2 . MODE

ADV_TIMER0 channel 2 threshold match action on channel output signal configuration bitfield: - 3'h0: set. - 3'h1: toggle then next threshold match action is clear. - 3'h2: set then next threshold match action is clear. - 3'h3: toggle. - 3'h4: clear. - 3'h5: toggle then next threshold match action is set. - 3'h6: clear then next threshold match action is set.

2.1257.3 T0_TH_CHANNEL2 . TH

ADV_TIMER0 channel 2 threshold configuration bitfield.

2.1258 T0_TH_CHANNEL3

ADV_TIMER0 channel 3 threshold configuration register. - Offset: `0x18` - Reset default: `0x0` - Reset mask: `0x7ffff`

2.1258.1 Fields


```
{"reg": [{"name": "TH", "bits": 16, "attr": ["rw"], "rotate": 0}, {"name": "MODE", "bits": 3, "
```


Bits	Type	Reset	Name
31:19			Reserved
18:16	rw	0x0	MODE
15:0	rw	0x0	TH

2.1258.2 T0_TH_CHANNEL3 . MODE

ADV_TIMER0 channel 3 threshold match action on channel output signal configuration bitfield: - 3'h0: set. - 3'h1: toggle then next threshold match action is clear. - 3'h2: set then next threshold match action is clear. - 3'h3: toggle. - 3'h4: clear. - 3'h5: toggle then next threshold match action is set. - 3'h6: clear then next threshold match action is set.

2.1258.3 T0_TH_CHANNEL3 . TH

ADV_TIMER0 channel 3 threshold configuration bitfield.

2.1259 T0_COUNTER

ADV_TIMER0 counter register. - Offset: `0x1c` - Reset default: `0x0` - Reset mask: `0xffff`

2.1259.1 Fields


```
{"reg": [{"name": "COUNTER", "bits": 16, "attr": ["ro"], "rotate": 0}, {"bits": 16}], "config"
```


Bits	Type	Reset	Name	Description
31:16				Reserved
15:0	ro	0x0	COUNTER	ADV_TIMER0 counter value.

2.1260 T1_CMD

ADV_TIMER1 command register. - Offset: `0x20` - Reset default: `0x0` - Reset mask: `0x1f`

2.1260.1 Fields

`{"reg": [{"name": "START", "bits": 1, "attr": ["wo"], "rotate": -90}, {"name": "STOP", "bits":`

Bits	Type	Reset	Name	Description
31:5				Reserved
4	wo	0x0	ARM	ADV_TIMER1 arm command bitfield.
3	wo	0x0	RESET	ADV_TIMER1 reset command bitfield.
2	wo	0x0	UPDATE	ADV_TIMER1 update command bitfield.
1	wo	0x0	STOP	ADV_TIMER1 stop command bitfield.
0	wo	0x0	START	ADV_TIMER1 start command bitfield.

2.1261 T1_CONFIG

ADV_TIMER1 configuration register. - Offset: `0x24` - Reset default: `0x1000` - Reset mask: `0xff1fff`

2.1261.1 Fields

`{"reg": [{"name": "INSEL", "bits": 8, "attr": ["rw"], "rotate": 0}, {"name": "MODE", "bits": 3`

Bits	Type	Reset	Name
31:24			Reserved
23:16	rw	0x0	PRESC
15:13			Reserved
12	rw	0x1	UPDOWNSEL
11	rw	0x0	CLKSEL
10:8	rw	0x0	MODE
7:0	rw	0x0	INSEL

2.1261.2 T1_CONFIG . PRESC

ADV_TIMER1 prescaler value configuration bitfield.

2.1261.3 T1_CONFIG . UPDOWNSEL

ADV_TIMER1 center-aligned mode configuration bitfield: - 1'b0: The counter counts up and down alternatively. - 1'b1: The counter counts up and resets to 0 when reach threshold.

2.1261.4 T1_CONFIG . CLKSEL

ADV_TIMER1 clock source configuration bitfield: - 1'b0: FLL - 1'b1: reference clock at 32kHz

2.1261.5 T1_CONFIG . MODE

ADV_TIMER1 trigger mode configuration bitfield: - 3'h0: trigger event at each clock cycle. - 3'h1: trigger event if input source is 0 - 3'h2: trigger event if input source is 1 - 3'h3: trigger event on input source rising edge - 3'h4: trigger event on input source falling edge - 3'h5: trigger event on input source falling or rising edge - 3'h6: trigger event on input source rising edge when armed - 3'h7: trigger event on input source falling edge when armed

2.1261.6 T1_CONFIG . INSEL

ADV_TIMER1 input source configuration bitfield: - 0-31: GPIO[0] to GPIO[31] - 32-35: Channel 0 to 3 of ADV_TIMER0 - 36-39: Channel 0 to 3 of ADV_TIMER1 - 40-43: Channel 0 to 3 of ADV_TIMER2 - 44-47: Channel 0 to 3 of ADV_TIMER3

2.1262 T1_THRESHOLD

ADV_TIMER1 threshold configuration register. - Offset: `0x28` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.1262.1 Fields

`{"reg": [{"name": "TH_LO", "bits": 16, "attr": ["rw"], "rotate": 0}, {"name": "TH_HI", "bits":`

Bits	Type	Reset	Name	Description
31:16	rw	0x0	TH_HI	ADV_TIMER1 threshold high part configuration bitfield. It defines end counter value.
15:0	rw	0x0	TH_LO	ADV_TIMER1 threshold low part configuration bitfield. It defines start counter value.

2.1263 T1_TH_CHANNEL0

ADV_TIMER1 channel 0 threshold configuration register. - Offset: `0x2c` - Reset default: `0x0` - Reset mask: `0x7ffff`

2.1263.1 Fields

`{"reg": [{"name": "TH", "bits": 16, "attr": ["rw"], "rotate": 0}, {"name": "MODE", "bits": 3,`

Bits	Type	Reset	Name
31:19			Reserved
18:16	rw	0x0	MODE
15:0	rw	0x0	TH

2.1263.2 T1_TH_CHANNEL0 . MODE

ADV_TIMER1 channel 0 threshold match action on channel output signal configuration bitfield: - 3'h0: set. - 3'h1: toggle then next threshold match action is clear. - 3'h2: set then next threshold match action is clear. - 3'h3: toggle. - 3'h4: clear. - 3'h5: toggle then next threshold match action is set. - 3'h6: clear then next threshold match action is set.

2.1263.3 T1_TH_CHANNEL0 . TH

ADV_TIMER1 channel 0 threshold configuration bitfield.

2.1264 T1_TH_CHANNEL1

ADV_TIMER1 channel 1 threshold configuration register. - Offset: `0x30` - Reset default: `0x0` - Reset mask: `0x7ffff`

2.1264.1 Fields


```
{"reg": [{"name": "TH", "bits": 16, "attr": ["rw"], "rotate": 0}, {"name": "MODE", "bits": 3, "
```


Bits	Type	Reset	Name
31:19			Reserved
18:16	rw	0x0	MODE
15:0	rw	0x0	TH

2.1264.2 T1_TH_CHANNEL1 . MODE

ADV_TIMER1 channel 1 threshold match action on channel output signal configuration bitfield: - 3'h0: set. - 3'h1: toggle then next threshold match action is clear. - 3'h2: set then next threshold match action is clear. - 3'h3: toggle. - 3'h4: clear. - 3'h5: toggle then next threshold match action is set. - 3'h6: clear then next threshold match action is set.

2.1264.3 T1_TH_CHANNEL1 . TH

ADV_TIMER1 channel 1 threshold configuration bitfield.

2.1265 T1_TH_CHANNEL2

ADV_TIMER1 channel 2 threshold configuration register. - Offset: `0x34` - Reset default: `0x0` - Reset mask: `0x7ffff`

2.1265.1 Fields

{"reg": [{"name": "TH", "bits": 16, "attr": ["rw"], "rotate": 0}, {"name": "MODE", "bits": 3, "

Bits	Type	Reset	Name
31:19			Reserved
18:16	rw	0x0	MODE
15:0	rw	0x0	TH

2.1265.2 T1_TH_CHANNEL2 . MODE

ADV_TIMER1 channel 2 threshold match action on channel output signal configuration bitfield: - 3'h0: set. - 3'h1: toggle then next threshold match action is clear. - 3'h2: set then next threshold match action is clear. - 3'h3: toggle. - 3'h4: clear. - 3'h5: toggle then next threshold match action is set. - 3'h6: clear then next threshold match action is set.

2.1265.3 T1_TH_CHANNEL2 . TH

ADV_TIMER1 channel 2 threshold configuration bitfield.

2.1266 T1_TH_CHANNEL3

ADV_TIMER1 channel 3 threshold configuration register. - Offset: `0x38` - Reset default: `0x0` - Reset mask: `0x7ffff`

2.1266.1 Fields

{"reg": [{"name": "TH", "bits": 16, "attr": ["rw"], "rotate": 0}, {"name": "MODE", "bits": 3, "

Bits	Type	Reset	Name
31:19			Reserved
18:16	rw	0x0	MODE
15:0	rw	0x0	TH

2.1266.2 T1_TH_CHANNEL3 . MODE

ADV_TIMER1 channel 3 threshold match action on channel output signal configuration bitfield: - 3'h0: set. - 3'h1: toggle then next threshold match action is clear. - 3'h2: set then next threshold match action is clear. - 3'h3: toggle. - 3'h4: clear. - 3'h5: toggle then next threshold match action is set. - 3'h6: clear then next threshold match action is set.

2.1266.3 T1_TH_CHANNEL3 . TH

ADV_TIMER1 channel 3 threshold configuration bitfield.

2.1267 T1_COUNTER

ADV_TIMER1 counter register. - Offset: `0x3c` - Reset default: `0x0` - Reset mask: `0xffff`

2.1267.1 Fields

`{"reg": [{"name": "COUNTER", "bits": 16, "attr": ["ro"], "rotate": 0}, {"bits": 16}], "config"`

Bits	Type	Reset	Name	Description
31:16				Reserved
15:0	ro	0x0	COUNTER	ADV_TIMER1 counter value.

2.1268 T2_CMD

ADV_TIMER2 command register. - Offset: `0x40` - Reset default: `0x0` - Reset mask: `0x1f`

2.1268.1 Fields

`{"reg": [{"name": "START", "bits": 1, "attr": ["wo"], "rotate": -90}, {"name": "STOP", "bits":`

Bits	Type	Reset	Name	Description
31:5				Reserved
4	wo	0x0	ARM	ADV_TIMER2 arm command bitfield.
3	wo	0x0	RESET	ADV_TIMER2 reset command bitfield.
2	wo	0x0	UPDATE	ADV_TIMER2 update command bitfield.
1	wo	0x0	STOP	ADV_TIMER2 stop command bitfield.
0	wo	0x0	START	ADV_TIMER2 start command bitfield.

2.1269 T2_CONFIG

ADV_TIMER2 configuration register. - Offset: `0x44` - Reset default: `0x1000` - Reset mask: `0xff1fff`

2.1269.1 Fields

{"reg": [{"name": "INSEL", "bits": 8, "attr": ["rw"], "rotate": 0}, {"name": "MODE", "bits": 3

Bits	Type	Reset	Name
31:24			Reserved
23:16	rw	0x0	PRESC
15:13			Reserved
12	rw	0x1	UPDOWNSEL
11	rw	0x0	CLKSEL
10:8	rw	0x0	MODE
7:0	rw	0x0	INSEL

2.1269.2 T2_CONFIG . PRESC

ADV_TIMER2 prescaler value configuration bitfield.

2.1269.3 T2_CONFIG . UPDOWNSEL

ADV_TIMER2 center-aligned mode configuration bitfield: - 1'b0: The counter counts up and down alternatively. - 1'b1: The counter counts up and resets to 0 when reach threshold.

2.1269.4 T2_CONFIG . CLKSEL

ADV_TIMER2 clock source configuration bitfield: - 1'b0: FLL - 1'b1: reference clock at 32kHz

2.1269.5 T2_CONFIG . MODE

ADV_TIMER2 trigger mode configuration bitfield: - 3'h0: trigger event at each clock cycle. - 3'h1: trigger event if input source is 0 - 3'h2: trigger event if input source is 1 - 3'h3: trigger event on input source rising edge - 3'h4: trigger event on input source falling edge - 3'h5: trigger event on input source falling or rising edge - 3'h6: trigger event on input source rising edge when armed - 3'h7: trigger event on input source falling edge when armed

2.1269.6 T2_CONFIG . INSEL

ADV_TIMER2 input source configuration bitfield: - 0-31: GPIO[0] to GPIO[31] - 32-35: Channel 0 to 3 of ADV_TIMER0 - 36-39: Channel 0 to 3 of ADV_TIMER1 - 40-43: Channel 0 to 3 of ADV_TIMER2 - 44-47: Channel 0 to 3 of ADV_TIMER3

2.1270 T2_THRESHOLD

ADV_TIMER2 threshold configuration register. - Offset: `0x48` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.1270.1 Fields

{"reg": [{"name": "TH_LO", "bits": 16, "attr": ["rw"], "rotate": 0}, {"name": "TH_HI", "bits":

Bits	Type	Reset	Name	Description
31:16	rw	0x0	TH_HI	ADV_TIMER2 threshold high part configuration bitfield. It defines end counter value.
15:0	rw	0x0	TH_LO	ADV_TIMER2 threshold low part configuration bitfield. It defines start counter value.

2.1271 T2_TH_CHANNEL0

ADV_TIMER2 channel 0 threshold configuration register. - Offset: `0x4c` - Reset default: `0x0` - Reset mask: `0x7ffff`

2.1271.1 Fields

{"reg": [{"name": "TH", "bits": 16, "attr": ["rw"], "rotate": 0}, {"name": "MODE", "bits": 3, "

Bits	Type	Reset	Name
31:19			Reserved
18:16	rw	0x0	MODE
15:0	rw	0x0	TH

2.1271.2 T2_TH_CHANNEL0 . MODE

ADV_TIMER2 channel 0 threshold match action on channel output signal configuration bitfield: - 3'h0: set. - 3'h1: toggle then next threshold match action is clear. - 3'h2: set then next threshold match action is clear. - 3'h3: toggle. - 3'h4: clear. - 3'h5: toggle then next threshold match action is set. - 3'h6: clear then next threshold match action is set.

2.1271.3 T2_TH_CHANNEL0 . TH

ADV_TIMER2 channel 0 threshold configuration bitfield.

2.1272 T2_TH_CHANNEL1

ADV_TIMER2 channel 1 threshold configuration register. - Offset: `0x50` - Reset default: `0x0` - Reset mask: `0x7ffff`

2.1272.1 Fields

{"reg": [{"name": "TH", "bits": 16, "attr": ["rw"], "rotate": 0}, {"name": "MODE", "bits": 3, "

Bits	Type	Reset	Name
31:19			Reserved
18:16	rw	0x0	MODE
15:0	rw	0x0	TH

2.1272.2 T2_TH_CHANNEL1 . MODE

ADV_TIMER2 channel 1 threshold match action on channel output signal configuration bitfield: - 3'h0: set. - 3'h1: toggle then next threshold match action is clear. - 3'h2: set then next threshold match action is clear. - 3'h3: toggle. - 3'h4: clear. - 3'h5: toggle then next threshold match action is set. - 3'h6: clear then next threshold match action is set.

2.1272.3 T2_TH_CHANNEL1 . TH

ADV_TIMER2 channel 1 threshold configuration bitfield.

2.1273 T2_TH_CHANNEL2

ADV_TIMER2 channel 2 threshold configuration register. - Offset: `0x54` - Reset default: `0x0` - Reset mask: `0x7ffff`

2.1273.1 Fields

{"reg": [{"name": "TH", "bits": 16, "attr": ["rw"], "rotate": 0}, {"name": "MODE", "bits": 3, "

Bits	Type	Reset	Name
31:19			Reserved
18:16	rw	0x0	MODE
15:0	rw	0x0	TH

2.1273.2 T2_TH_CHANNEL2 . MODE

ADV_TIMER2 channel 2 threshold match action on channel output signal configuration bitfield: - 3'h0: set. - 3'h1: toggle then next threshold match action is clear. - 3'h2: set then next threshold match action is clear. - 3'h3: toggle. - 3'h4: clear. - 3'h5: toggle then next threshold match action is set. - 3'h6: clear then next threshold match action is set.

2.1273.3 T2_TH_CHANNEL2 . TH

ADV_TIMER2 channel 2 threshold configuration bitfield.

2.1274 T2_TH_CHANNEL3

ADV_TIMER2 channel 3 threshold configuration register. - Offset: `0x58` - Reset default: `0x0` - Reset mask: `0x7ffff`

2.1274.1 Fields


```
{"reg": [{"name": "TH", "bits": 16, "attr": ["rw"], "rotate": 0}, {"name": "MODE", "bits": 3, "
```


Bits	Type	Reset	Name
31:19			Reserved
18:16	rw	0x0	MODE
15:0	rw	0x0	TH

2.1274.2 T2_TH_CHANNEL3 . MODE

ADV_TIMER2 channel 3 threshold match action on channel output signal configuration bitfield: - 3'h0: set. - 3'h1: toggle then next threshold match action is clear. - 3'h2: set then next threshold match action is clear. - 3'h3: toggle. - 3'h4: clear. - 3'h5: toggle then next threshold match action is set. - 3'h6: clear then next threshold match action is set.

2.1274.3 T2_TH_CHANNEL3 . TH

ADV_TIMER2 channel 3 threshold configuration bitfield.

2.1275 T2_COUNTER

ADV_TIMER2 counter register. - Offset: `0x5c` - Reset default: `0x0` - Reset mask: `0xffff`

2.1275.1 Fields


```
{"reg": [{"name": "COUNTER", "bits": 16, "attr": ["ro"], "rotate": 0}, {"bits": 16}], "config"
```


Bits	Type	Reset	Name	Description
31:16				Reserved
15:0	ro	0x0	COUNTER	ADV_TIMER2 counter value.

2.1276 T3_CMD

ADV_TIMER3 command register. - Offset: `0x60` - Reset default: `0x0` - Reset mask: `0x1f`

2.1276.1 Fields

`{"reg": [{"name": "START", "bits": 1, "attr": ["wo"], "rotate": -90}, {"name": "STOP", "bits":`

Bits	Type	Reset	Name	Description
31:5				Reserved
4	wo	0x0	ARM	ADV_TIMER3 arm command bitfield.
3	wo	0x0	RESET	ADV_TIMER3 reset command bitfield.
2	wo	0x0	UPDATE	ADV_TIMER3 update command bitfield.
1	wo	0x0	STOP	ADV_TIMER3 stop command bitfield.
0	wo	0x0	START	ADV_TIMER3 start command bitfield.

2.1277 T3_CONFIG

ADV_TIMER3 configuration register. - Offset: `0x64` - Reset default: `0x1000` - Reset mask: `0xff1fff`

2.1277.1 Fields

`{"reg": [{"name": "INSEL", "bits": 8, "attr": ["rw"], "rotate": 0}, {"name": "MODE", "bits": 3`

Bits	Type	Reset	Name
31:24			Reserved
23:16	rw	0x0	PRESC
15:13			Reserved
12	rw	0x1	UPDOWNSEL
11	rw	0x0	CLKSEL
10:8	rw	0x0	MODE
7:0	rw	0x0	INSEL

2.1277.2 T3_CONFIG . PRESC

ADV_TIMER3 prescaler value configuration bitfield.

2.1277.3 T3_CONFIG . UPDOWNSEL

ADV_TIMER3 center-aligned mode configuration bitfield: - 1'b0: The counter counts up and down alternatively. - 1'b1: The counter counts up and resets to 0 when reach threshold.

2.1277.4 T3_CONFIG . CLKSEL

ADV_TIMER3 clock source configuration bitfield: - 1'b0: FLL - 1'b1: reference clock at 32kHz

2.1277.5 T3_CONFIG . MODE

ADV_TIMER3 trigger mode configuration bitfield: - 3'h0: trigger event at each clock cycle. - 3'h1: trigger event if input source is 0 - 3'h2: trigger event if input source is 1 - 3'h3: trigger event on input source rising edge - 3'h4: trigger event on input source falling edge - 3'h5: trigger event on input source falling or rising edge - 3'h6: trigger event on input source rising edge when armed - 3'h7: trigger event on input source falling edge when armed

2.1277.6 T3_CONFIG . INSEL

ADV_TIMER3 input source configuration bitfield: - 0-31: GPIO[0] to GPIO[31] - 32-35: Channel 0 to 3 of ADV_TIMER0 - 36-39: Channel 0 to 3 of ADV_TIMER1 - 40-43: Channel 0 to 3 of ADV_TIMER2 - 44-47: Channel 0 to 3 of ADV_TIMER3

2.1278 T3_THRESHOLD

ADV_TIMER3 threshold configuration register. - Offset: `0x68` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.1278.1 Fields

`{"reg": [{"name": "TH_LO", "bits": 16, "attr": ["rw"], "rotate": 0}, {"name": "TH_HI", "bits":`

Bits	Type	Reset	Name	Description
31:16	rw	0x0	TH_HI	ADV_TIMER3 threshold high part configuration bitfield. It defines end counter value.
15:0	rw	0x0	TH_LO	ADV_TIMER3 threshold low part configuration bitfield. It defines start counter value.

2.1279 T3_TH_CHANNEL0

ADV_TIMER3 channel 0 threshold configuration register. - Offset: `0x6c` - Reset default: `0x0` - Reset mask: `0x7ffff`

2.1279.1 Fields

`{"reg": [{"name": "TH", "bits": 16, "attr": ["rw"], "rotate": 0}, {"name": "MODE", "bits": 3,`

Bits	Type	Reset	Name
31:19			Reserved
18:16	rw	0x0	MODE
15:0	rw	0x0	TH

2.1279.2 T3_TH_CHANNEL0 . MODE

ADV_TIMER3 channel 0 threshold match action on channel output signal configuration bitfield: - 3'h0: set. - 3'h1: toggle then next threshold match action is clear. - 3'h2: set then next threshold match action is clear. - 3'h3: toggle. - 3'h4: clear. - 3'h5: toggle then next threshold match action is set. - 3'h6: clear then next threshold match action is set.

2.1279.3 T3_TH_CHANNEL0 . TH

ADV_TIMER3 channel 0 threshold configuration bitfield.

2.1280 T3_TH_CHANNEL1

ADV_TIMER3 channel 1 threshold configuration register. - Offset: `0x70` - Reset default: `0x0` - Reset mask: `0x7ffff`

2.1280.1 Fields

`{"reg": [{"name": "TH", "bits": 16, "attr": ["rw"], "rotate": 0}, {"name": "MODE", "bits": 3, `

Bits	Type	Reset	Name
31:19			Reserved
18:16	rw	0x0	MODE
15:0	rw	0x0	TH

2.1280.2 T3_TH_CHANNEL1 . MODE

ADV_TIMER3 channel 1 threshold match action on channel output signal configuration bitfield: - 3'h0: set. - 3'h1: toggle then next threshold match action is clear. - 3'h2: set then next threshold match action is clear. - 3'h3: toggle. - 3'h4: clear. - 3'h5: toggle then next threshold match action is set. - 3'h6: clear then next threshold match action is set.

2.1280.3 T3_TH_CHANNEL1 . TH

ADV_TIMER3 channel 1 threshold configuration bitfield.

2.1281 T3_TH_CHANNEL2

ADV_TIMER3 channel 2 threshold configuration register. - Offset: `0x74` - Reset default: `0x0` - Reset mask: `0x7ffff`

2.1281.1 Fields

{"reg": [{"name": "TH", "bits": 16, "attr": ["rw"], "rotate": 0}, {"name": "MODE", "bits": 3, "

Bits	Type	Reset	Name
31:19			Reserved
18:16	rw	0x0	MODE
15:0	rw	0x0	TH

2.1281.2 T3_TH_CHANNEL2 . MODE

ADV_TIMER3 channel 2 threshold match action on channel output signal configuration bitfield: - 3'h0: set. - 3'h1: toggle then next threshold match action is clear. - 3'h2: set then next threshold match action is clear. - 3'h3: toggle. - 3'h4: clear. - 3'h5: toggle then next threshold match action is set. - 3'h6: clear then next threshold match action is set.

2.1281.3 T3_TH_CHANNEL2 . TH

ADV_TIMER3 channel 2 threshold configuration bitfield.

2.1282 T3_TH_CHANNEL3

ADV_TIMER3 channel 3 threshold configuration register. - Offset: `0x78` - Reset default: `0x0` - Reset mask: `0x7ffff`

2.1282.1 Fields

{"reg": [{"name": "TH", "bits": 16, "attr": ["rw"], "rotate": 0}, {"name": "MODE", "bits": 3, "

Bits	Type	Reset	Name
31:19			Reserved
18:16	rw	0x0	MODE
15:0	rw	0x0	TH

2.1282.2 T3_TH_CHANNEL3 . MODE

ADV_TIMER3 channel 3 threshold match action on channel output signal configuration bitfield: - 3'h0: set. - 3'h1: toggle then next threshold match action is clear. - 3'h2: set then next threshold match action is clear. - 3'h3: toggle. - 3'h4: clear. - 3'h5: toggle then next threshold match action is set. - 3'h6: clear then next threshold match action is set.

2.1282.3 T3_TH_CHANNEL3 . TH

ADV_TIMER3 channel 3 threshold configuration bitfield.

2.1283 T3_COUNTER

ADV_TIMER3 counter register. - Offset: `0x7c` - Reset default: `0x0` - Reset mask: `0xffff`

2.1283.1 Fields

`{"reg": [{"name": "COUNTER", "bits": 16, "attr": ["ro"], "rotate": 0}, {"bits": 16}], "config"`

Bits	Type	Reset	Name	Description
31:16				Reserved
15:0	ro	0x0	COUNTER	ADV_TIMER3 counter value.

2.1284 EVENT_CFG

ADV_TIMERS events configuration register. - Offset: `0x80` - Reset default: `0x0` - Reset mask: `0xfffff`

2.1284.1 Fields

`{"reg": [{"name": "SEL0", "bits": 4, "attr": ["rw"], "rotate": 0}, {"name": "SEL1", "bits": 4,`

Bits	Type	Reset	Name
31:20			Reserved
19:16	rw	0x0	ENA
15:12	rw	0x0	SEL3
11:8	rw	0x0	SEL2
7:4	rw	0x0	SEL1
3:0	rw	0x0	SEL0

2.1284.2 EVENT_CFG . ENA

ADV_TIMER output event enable configuration bitfield. ENA[i]=1 enables output event i generation.

2.1284.3 EVENT_CFG . SEL3

ADV_TIMER output event 3 source configuration bitfiled: - 4'h0: ADV_TIMER0 channel 0. - 4'h1: ADV_TIMER0 channel 1. - 4'h2: ADV_TIMER0 channel 2. - 4'h3: ADV_TIMER0 channel 3. - 4'h4: ADV_TIMER1 channel 0. - 4'h5: ADV_TIMER1 channel 1. - 4'h6: ADV_TIMER1 channel 2. - 4'h7: ADV_TIMER1 channel 3. - 4'h8: ADV_TIMER2 channel 0. - 4'h9: ADV_TIMER2 channel 1. - 4'hA: ADV_TIMER2 channel 2. - 4'hB: ADV_TIMER2 channel 3. - 4'hC: ADV_TIMER3 channel 0. - 4'hD: ADV_TIMER3 channel 1. - 4'hE: ADV_TIMER3 channel 2. - 4'hF: ADV_TIMER3 channel 3.

2.1284.4 EVENT_CFG . SEL2

ADV_TIMER output event 2 source configuration bitfiled: - 4'h0: ADV_TIMER0 channel 0. - 4'h1: ADV_TIMER0 channel 1. - 4'h2: ADV_TIMER0 channel 2. - 4'h3: ADV_TIMER0 channel 3. - 4'h4: ADV_TIMER1 channel 0. - 4'h5: ADV_TIMER1 channel 1. - 4'h6: ADV_TIMER1 channel 2. - 4'h7: ADV_TIMER1 channel 3. - 4'h8: ADV_TIMER2 channel 0. - 4'h9: ADV_TIMER2 channel 1. - 4'hA: ADV_TIMER2 channel 2. - 4'hB: ADV_TIMER2 channel 3. - 4'hC: ADV_TIMER3 channel 0. - 4'hD: ADV_TIMER3 channel 1. - 4'hE: ADV_TIMER3 channel 2. - 4'hF: ADV_TIMER3 channel 3.

2.1284.5 EVENT_CFG . SEL1

ADV_TIMER output event 1 source configuration bitfiled: - 4'h0: ADV_TIMER0 channel 0. - 4'h1: ADV_TIMER0 channel 1. - 4'h2: ADV_TIMER0 channel 2. - 4'h3: ADV_TIMER0 channel 3. - 4'h4: ADV_TIMER1 channel 0. - 4'h5: ADV_TIMER1 channel 1. - 4'h6: ADV_TIMER1 channel 2. - 4'h7: ADV_TIMER1 channel 3. - 4'h8: ADV_TIMER2 channel 0. - 4'h9: ADV_TIMER2 channel 1. - 4'hA: ADV_TIMER2 channel 2. - 4'hB: ADV_TIMER2 channel 3. - 4'hC: ADV_TIMER3 channel 0. - 4'hD: ADV_TIMER3 channel 1. - 4'hE: ADV_TIMER3 channel 2. - 4'hF: ADV_TIMER3 channel 3.

2.1284.6 EVENT_CFG . SEL0

ADV_TIMER output event 0 source configuration bitfiled: - 4'h0: ADV_TIMER0 channel 0. - 4'h1: ADV_TIMER0 channel 1. - 4'h2: ADV_TIMER0 channel 2. - 4'h3: ADV_TIMER0 channel 3. - 4'h4: ADV_TIMER1 channel 0. - 4'h5: ADV_TIMER1 channel 1. - 4'h6: ADV_TIMER1 channel 2. - 4'h7: ADV_TIMER1 channel 3. - 4'h8: ADV_TIMER2 channel 0. - 4'h9: ADV_TIMER2 channel 1. - 4'hA: ADV_TIMER2 channel 2. - 4'hB: ADV_TIMER2 channel 3. - 4'hC: ADV_TIMER3 channel 0. - 4'hD: ADV_TIMER3 channel 1. - 4'hE: ADV_TIMER3 channel 2. - 4'hF: ADV_TIMER3 channel 3.

2.1285 CG

ADV_TIMERS channels clock gating configuration register. - Offset: `0x84` - Reset default: `0x0` - Reset mask: `0xf`

2.1285.1 Fields

{"reg": [{"name": "ENA", "bits": 4, "attr": ["rw"], "rotate": 0}, {"bits": 28}], "config": {"la

Bits	Type	Reset	Name	Description
31:4				Reserved
3:0	rw	0x0	ENA	ADV_TIMER clock gating configuration bitfield. - ENA[i]=0: clock gate ADV_TIMERi. - ENA[i]=1: enable ADV_TIMERi.

2.1286 gpio / doc / registers.md

2.1287 Summary

Name	Offset	Length	Description
gpio.INTR_STATE	0x0	4	Interrupt State Register
gpio.INTR_ENABLE	0x4	4	Interrupt Enable Register
gpio.INTR_TEST	0x8	4	Interrupt Test Register
gpio.ALERT_TEST	0xc	4	Alert Test Register
gpio.DATA_IN	0x10	4	GPIO Input data read value
gpio.DIRECT_OUT	0x14	4	GPIO direct output data write value
gpio.MASKED_OUT_LOWER	0x18	4	GPIO write data lower with mask.
gpio.MASKED_OUT_UPPER	0x1c	4	GPIO write data upper with mask.
gpio.DIRECT_OE	0x20	4	GPIO Output Enable.
gpio.MASKED_OE_LOWER	0x24	4	GPIO write Output Enable lower with mask.
gpio.MASKED_OE_UPPER	0x28	4	GPIO write Output Enable upper with mask.
gpio.INTR_CTRL_EN_RISING	0x2c	4	GPIO interrupt enable for GPIO, rising edge.
gpio.INTR_CTRL_EN_FALLING	0x30	4	GPIO interrupt enable for GPIO, falling edge.
gpio.INTR_CTRL_EN_LVLHIGH	0x34	4	GPIO interrupt enable for GPIO, level high.
gpio.INTR_CTRL_EN_LVLLOW	0x38	4	GPIO interrupt enable for GPIO, level low.
gpio.CTRL_EN_INPUT_FILTER	0x3c	4	filter enable for GPIO input bits.

2.1288 INTR_STATE

Interrupt State Register - Offset: `0x0` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.1288.1 Fields

{"reg": [{"name": "gpio", "bits": 32, "attr": ["rw1c"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw1c	0x0	gpio	raised if any of GPIO pin detects configured interrupt mode

2.1289 INTR_ENABLE

Interrupt Enable Register - Offset: `0x4` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.1289.1 Fields

{"reg": [{"name": "gpio", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "f

Bits	Type	Reset	Name	Description
31:0	rw	0x0	gpio	Enable interrupt when corresponding bit in INTR_STATE.gpio is set.

2.1290 INTR_TEST

Interrupt Test Register - Offset: `0x8` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.1290.1 Fields

{"reg": [{"name": "gpio", "bits": 32, "attr": ["wo"], "rotate": 0}], "config": {"lanes": 1, "f

Bits	Type	Reset	Name	Description
31:0	wo	0x0	gpio	Write 1 to force corresponding bit in INTR_STATE.gpio to 1.

2.1291 ALERT_TEST

Alert Test Register - Offset: `0xc` - Reset default: `0x0` - Reset mask: `0x1`

2.1291.1 Fields

{"reg": [{"name": "fatal_fault", "bits": 1, "attr": ["wo"], "rotate": -90}, {"bits": 31}], "co

Bits	Type	Reset	Name	Description
31:1				Reserved
0	wo	0x0	fatal_fault	Write 1 to trigger one alert event of this kind.

2.1292 DATA_IN

GPIO Input data read value - Offset: `0x10` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.1292.1 Fields

{"reg": [{"name": "DATA_IN", "bits": 32, "attr": ["ro"], "rotate": 0}], "config": {"lanes": 1,

Bits	Type	Reset	Name	Description
31:0	ro	x	DATA_IN	

2.1293 DIRECT_OUT

GPIO direct output data write value - Offset: `0x14` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.1293.1 Fields

{"reg": [{"name": "DIRECT_OUT", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes":

Bits	Type	Reset	Name	Description
31:0	rw	x	DIRECT_OUT	

2.1294 MASKED_OUT_LOWER

GPIO write data lower with mask.

Masked write for DATA_OUT[15:0].

Upper 16 bits of this register are used as mask. Writing lower 16 bits of the register changes DATA_OUT[15:0] value if mask bits are set.

Read-back of this register returns upper 16 bits as zero and lower 16 bits as DATA_OUT[15:0]. - Offset: `0x18` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.1294.1 Fields

{"reg": [{"name": "data", "bits": 16, "attr": ["rw"], "rotate": 0}, {"name": "mask", "bits": 16

Bits	Type	Reset	Name	Description
31:16	wo	x	mask	Write data mask[15:0]. A value of 1 in mask[i] allows the updating of DATA_OUT[i], 0 <= i <= 15
15:0	rw	x	data	Write data value[15:0]. Value to write into DATA_OUT[i], valid in the presence of mask[i]==1

2.1295 MASKED_OUT_UPPER

GPIO write data upper with mask.

Masked write for DATA_OUT[31:16].

Upper 16 bits of this register are used as mask. Writing lower 16 bits of the register changes DATA_OUT[31:16] value if mask bits are set.

Read-back of this register returns upper 16 bits as zero and lower 16 bits as DATA_OUT[31:16]. - Offset: `0x1c` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.1295.1 Fields

{"reg": [{"name": "data", "bits": 16, "attr": ["rw"], "rotate": 0}, {"name": "mask", "bits": 16

Bits	Type	Reset	Name	Description
31:16	wo	x	mask	Write data mask[31:16]. A value of 1 in mask[i] allows the updating of DATA_OUT[i], 16 <= i <= 31
15:0	rw	x	data	Write data value[31:16]. Value to write into DATA_OUT[i], valid in the presence of mask[i]==1

2.1296 DIRECT_OE

GPIO Output Enable.

Setting direct_oe[i] to 1 enables output mode for GPIO[i] - Offset: `0x20` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.1296.1 Fields

{"reg": [{"name": "DIRECT_OE", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes":

Bits	Type	Reset	Name	Description
31:0	rw	x	DIRECT_OE	

2.1297 MASKED_OE_LOWER

GPIO write Output Enable lower with mask.

Masked write for DATA_OE[15:0], the register that controls output mode for GPIO pins [15:0].

Upper 16 bits of this register are used as mask. Writing lower 16 bits of the register changes DATA_OE[15:0] value if mask bits are set.

Read-back of this register returns upper 16 bits as zero and lower 16 bits as DATA_OE[15:0]. - Offset: `0x24` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.1297.1 Fields

`{"reg": [{"name": "data", "bits": 16, "attr": ["rw"], "rotate": 0}, {"name": "mask", "bits": 16`

Bits	Type	Reset	Name	Description
31:16	rw	x	mask	Write OE mask[15:0]. A value of 1 in mask[i] allows the updating of DATA_OE[i], 0 <= i <= 15
15:0	rw	x	data	Write OE value[15:0]. Value to write into DATA_OE[i], valid in the presence of mask[i]==1

2.1298 MASKED_OE_UPPER

GPIO write Output Enable upper with mask.

Masked write for DATA_OE[31:16], the register that controls output mode for GPIO pins [31:16].

Upper 16 bits of this register are used as mask. Writing lower 16 bits of the register changes DATA_OE[31:16] value if mask bits are set.

Read-back of this register returns upper 16 bits as zero and lower 16 bits as DATA_OE[31:16]. - Offset: `0x28` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.1298.1 Fields

`{"reg": [{"name": "data", "bits": 16, "attr": ["rw"], "rotate": 0}, {"name": "mask", "bits": 16`

Bits	Type	Reset	Name	Description
31:16	rw	x	mask	Write OE mask[31:16]. A value of 1 in mask[i] allows the updating of DATA_OE[i], 16 <= i <= 31

Bits	Type	Reset	Name	Description
15:0	rw	x	data	Write OE value[31:16]. Value to write into DATA_OE[i], valid in the presence of mask[i]==1

2.1299 INTR_CTRL_EN_RISING

GPIO interrupt enable for GPIO, rising edge.

If INTR_ENABLE[i] is true, a value of 1 on INTR_CTRL_EN_RISING[i] enables rising-edge interrupt detection on GPIO[i]. - Offset: 0x2c - Reset default: 0x0 - Reset mask: 0xffffffff

2.1299.1 Fields

{"reg": [{"name": "INTR_CTRL_EN_RISING", "bits": 32, "attr": ["rw"], "rotate": 0}], "config":

Bits	Type	Reset	Name	Description
31:0	rw	0x0	INTR_CTRL_EN_RISING	

2.1300 INTR_CTRL_EN_FALLING

GPIO interrupt enable for GPIO, falling edge.

If INTR_ENABLE[i] is true, a value of 1 on INTR_CTRL_EN_FALLING[i] enables falling-edge interrupt detection on GPIO[i]. - Offset: 0x30 - Reset default: 0x0 - Reset mask: 0xffffffff

2.1300.1 Fields

{"reg": [{"name": "INTR_CTRL_EN_FALLING", "bits": 32, "attr": ["rw"], "rotate": 0}], "config":

Bits	Type	Reset	Name	Description
31:0	rw	0x0	INTR_CTRL_EN_FALLING	

2.1301 INTR_CTRL_EN_LVLHIGH

GPIO interrupt enable for GPIO, level high.

If INTR_ENABLE[i] is true, a value of 1 on INTR_CTRL_EN_LVLHIGH[i] enables level high interrupt detection on GPIO[i]. - Offset: 0x34 - Reset default: 0x0 - Reset mask: 0xffffffff

2.1301.1 Fields

{"reg": [{"name": "INTR_CTRL_EN_LVLHIGH", "bits": 32, "attr": ["rw"], "rotate": 0}], "config":

Bits	Type	Reset	Name	Description
31:0	rw	0x0	INTR_CTRL_EN_LVLHIGH	

2.1302 INTR_CTRL_EN_LVLLOW

GPIO interrupt enable for GPIO, level low.

If INTR_ENABLE[i] is true, a value of 1 on INTR_CTRL_EN_LVLLOW[i] enables level low interrupt detection on GPIO[i]. - Offset: 0x38 - Reset default: 0x0 - Reset mask: 0xffffffff

2.1302.1 Fields

{"reg": [{"name": "INTR_CTRL_EN_LVLLOW", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": +

Bits	Type	Reset	Name	Description
31:0	rw	0x0	INTR_CTRL_EN_LVLLOW	

2.1303 CTRL_EN_INPUT_FILTER

filter enable for GPIO input bits.

If CTRL_EN_INPUT_FILTER[i] is true, a value of input bit [i] must be stable for 16 cycles before transitioning. - Offset: 0x3c - Reset default: 0x0 - Reset mask: 0xffffffff

2.1303.1 Fields

{"reg": [{"name": "CTRL_EN_INPUT_FILTER", "bits": 32, "attr": ["rw"], "rotate": 0}], "config":

Bits	Type	Reset	Name	Description
31:0	rw	0x0	CTRL_EN_INPUT_FILTER	

2.1304 hyperbus / doc / registers.md

2.1305 Summary

Name	Offset	Length	Description
hyperbus.T_LATENCY_ACCESS	0x0	4	Initial latency
hyperbus.EN_LATENCY_ADDITIONAL	0x4	4	Force 2x Latency count
hyperbus.T_BURST_MAX	0x8	4	Max burst Length between two memory refresh
hyperbus.T_READ_WRITE_RECOVERY	0xc	4	Idle time between transactions
hyperbus.T_RX_CLOCK_DELAY	0x10	4	RX Delay Line
hyperbus.T_TX_CLOCK_DELAY	0x14	4	TX Delay Line
hyperbus.ADDRESS_MASK_MSB	0x18	4	Address Mask MSB
hyperbus.ADDRESS_SPACE	0x1c	4	L2 sleep configuration register
hyperbus.PHYS_IN_USE	0x20	4	Number of PHYs on use
hyperbus.WHICH_PHY	0x24	4	PHY used in single PHY mode
hyperbus.CS0_BASE	0x28	4	CS0 Base address range
hyperbus.CS0_END	0x2c	4	CS0 End address range
hyperbus.CS1_BASE	0x30	4	CS1 Base address range
hyperbus.CS1_END	0x34	4	CS1 End address range
hyperbus.CS2_BASE	0x38	4	CS2 Base address range
hyperbus.CS2_END	0x3c	4	CS2 End address range
hyperbus.CS3_BASE	0x40	4	CS3 Base address range
hyperbus.CS3_END	0x44	4	CS3 End address range

2.1306 T_LATENCY_ACCESS

Initial latency - Offset: `0x0` - Reset default: `0x6` - Reset mask: `0xf`

2.1306.1 Fields

```
{"reg": [{"name": "T_LATENCY_ACCESS", "bits": 4, "attr": ["rw"], "rotate": -90}, {"bits": 28}]
```

Bits	Type	Reset	Name	Description
31:4				Reserved
3:0	rw	0x6	T_LATENCY_ACCESS	Initial latency

2.1307 EN_LATENCY_ADDITIONAL

Force 2x Latency count - Offset: `0x4` - Reset default: `0x0` - Reset mask: `0x1`

2.1307.1 Fields

```
{"reg": [{"name": "EN_LATENCY_ADDITIONAL", "bits": 1, "attr": ["rw"], "rotate": -90}, {"bits":
```

Bits	Type	Reset	Name	Description
31:1				Reserved
0	rw	0x0	EN_LATENCY_ADDITIONAL	Force 2x Latency count

2.1308 T_BURST_MAX

Max burst Length between two memory refresh - Offset: `0x8` - Reset default: `0x15e` - Reset mask: `0xffff`

2.1308.1 Fields

```
{"reg": [{"name": "T_BURST_MAX", "bits": 16, "attr": ["rw"], "rotate": 0}, {"bits": 16}], "con
```

Bits	Type	Reset	Name	Description
31:16				Reserved
15:0	rw	0x15e	T_BURST_MAX	Max burst Length between two memory refresh

2.1309 T_READ_WRITE_RECOVERY

Idle time between transactions - Offset: `0xc` - Reset default: `0x6` - Reset mask: `0xf`

2.1309.1 Fields

```
{"reg": [{"name": "T_READ_WRITE_RECOVERY", "bits": 4, "attr": ["rw"], "rotate": -90}, {"bits":
```

Bits	Type	Reset	Name	Description
31:4				Reserved
3:0	rw	0x6	T_READ_WRITE_RECOVERY	Idle time between transactions

2.1310 T_RX_CLOCK_DELAY

RX Delay Line - Offset: `0x10` - Reset default: `0x8` - Reset mask: `0xf`

2.1310.1 Fields

```
{"reg": [{"name": "T_RX_CLOCK_DELAY", "bits": 4, "attr": ["rw"], "rotate": -90}, {"bits": 28}]
```

Bits	Type	Reset	Name	Description
31:4				Reserved
3:0	rw	0x8	T_RX_CLOCK_DELAY	RX Delay Line

2.1311 T_TX_CLOCK_DELAY

TX Delay Line - Offset: `0x14` - Reset default: `0x8` - Reset mask: `0xf`

2.1311.1 Fields

```
{"reg": [{"name": "T_TX_CLOCK_DELAY", "bits": 4, "attr": ["rw"], "rotate": -90}, {"bits": 28}]
```

Bits	Type	Reset	Name	Description
31:4				Reserved
3:0	rw	0x8	T_TX_CLOCK_DELAY	TX Delay Line

2.1312 ADDRESS_MASK_MSB

Address Mask MSB - Offset: `0x18` - Reset default: `0x19` - Reset mask: `0x7ffff`

2.1312.1 Fields

```
{"reg": [{"name": "ADDRESS_MASK_MSB", "bits": 19, "attr": ["rw"], "rotate": 0}, {"bits": 13}],
```

Bits	Type	Reset	Name	Description
31:19				Reserved
18:0	rw	0x19	ADDRESS_MASK_MSB	Address Mask MSB

2.1313 ADDRESS_SPACE

L2 sleep configuration register - Offset: `0x1c` - Reset default: `0x0` - Reset mask: `0x1`

2.1313.1 Fields

```
{"reg": [{"name": "ADDRESS_SPACE", "bits": 1, "attr": ["rw"], "rotate": -90}, {"bits": 31}], "
```

Bits	Type	Reset	Name	Description
31:1				Reserved

Bits	Type	Reset	Name	Description
0	rw	0x0	ADDRESS_SPACE	L2 sleep configuration register

2.1314 PHYS_IN_USE

Number of PHYs on use - Offset: `0x20` - Reset default: `0x1` - Reset mask: `0x1`

2.1314.1 Fields


```
{"reg": [{"name": "PHYS_IN_USE", "bits": 1, "attr": ["rw"], "rotate": -90}, {"bits": 31}], "co
```


Bits	Type	Reset	Name	Description
31:1				Reserved
0	rw	0x1	PHYS_IN_USE	Number of PHYs on use: - 1'b0: Uses 1 PHY - 1'b1: Uses 2 PHYs

2.1315 WHICH_PHY

PHY used in single PHY mode - Offset: `0x24` - Reset default: `0x1` - Reset mask: `0x1`

2.1315.1 Fields


```
{"reg": [{"name": "WHICH_PHY", "bits": 1, "attr": ["rw"], "rotate": -90}, {"bits": 31}], "conf
```


Bits	Type	Reset	Name	Description
31:1				Reserved
0	rw	0x1	WHICH_PHY	PHY used in single PHY mode: - 1'b0: PHY 0 is used - 1'b1: PHY 1 is used

2.1316 CS0_BASE

CS0 Base address range - Offset: `0x28` - Reset default: `0x80000000` - Reset mask: `0xffffffff`

2.1316.1 Fields


```
{"reg": [{"name": "CS0_BASE", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1
```

Bits	Type	Reset	Name	Description
31:0	rw	0x80000000	CS0_BASE	CS0 Base address range

2.1317 CS0_END

CS0 End address range - Offset: `0x2c` - Reset default: `0x81000000` - Reset mask: `0xffffffff`

2.1317.1 Fields

`{"reg": [{"name": "CS0_END", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1,`

Bits	Type	Reset	Name	Description
31:0	rw	0x81000000	CS0_END	CS0 End address range

2.1318 CS1_BASE

CS1 Base address range - Offset: `0x30` - Reset default: `0x81000000` - Reset mask: `0xffffffff`

2.1318.1 Fields

`{"reg": [{"name": "CS1_BASE", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1`

Bits	Type	Reset	Name	Description
31:0	rw	0x81000000	CS1_BASE	CS1 Base address range

2.1319 CS1_END

CS1 End address range - Offset: `0x34` - Reset default: `0x82000000` - Reset mask: `0xffffffff`

2.1319.1 Fields

`{"reg": [{"name": "CS1_END", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1,`

Bits	Type	Reset	Name	Description
31:0	rw	0x82000000	CS1_END	CS1 End address range

2.1320 CS2_BASE

CS2 Base address range - Offset: `0x38` - Reset default: `0x82000000` - Reset mask: `0xffffffff`

2.1320.1 Fields

{"reg": [{"name": "CS2_BASE", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1

Bits	Type	Reset	Name	Description
31:0	rw	0x82000000	CS2_BASE	CS2 Base address range

2.1321 CS2_END

CS2 End address range - Offset: `0x3c` - Reset default: `0x83000000` - Reset mask: `0xffffffff`

2.1321.1 Fields

{"reg": [{"name": "CS2_END", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1,

Bits	Type	Reset	Name	Description
31:0	rw	0x83000000	CS2_END	CS2 End address range

2.1322 CS3_BASE

CS3 Base address range - Offset: `0x40` - Reset default: `0x83000000` - Reset mask: `0xffffffff`

2.1322.1 Fields

{"reg": [{"name": "CS3_BASE", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1

Bits	Type	Reset	Name	Description
31:0	rw	0x83000000	CS3_BASE	CS3 Base address range

2.1323 CS3_END

CS3 End address range - Offset: `0x44` - Reset default: `0x84000000` - Reset mask: `0xffffffff`

2.1323.1 Fields

{"reg": [{"name": "CS3_END", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1,

Bits	Type	Reset	Name	Description
31:0	rw	0x84000000	CS3_END	CS3 End address range

2.1324 i2c / doc / registers.md

2.1325 Summary

Name	Offset	Length	Description
i2c.INTR_STATE	0x0	4	Interrupt State Register
i2c.INTR_ENABLE	0x4	4	Interrupt Enable Register
i2c.INTR_TEST	0x8	4	Interrupt Test Register
i2c.ALERT_TEST	0xc	4	Alert Test Register
i2c.CTRL	0x10	4	I2C Control Register
i2c.STATUS	0x14	4	I2C Live Status Register for Host and Target modes
i2c.RDATA	0x18	4	I2C Read Data
i2c.FDATA	0x1c	4	I2C Host Format Data
i2c.FIFO_CTRL	0x20	4	I2C FIFO control register
i2c.HOST_FIFO_CONFIG	0x24	4	Host mode FIFO configuration
i2c.TARGET_FIFO_CONFIG	0x28	4	Target mode FIFO configuration
i2c.HOST_FIFO_STATUS	0x2c	4	Host mode FIFO status register
i2c.TARGET_FIFO_STATUS	0x30	4	Target mode FIFO status register
i2c.OVRD	0x34	4	I2C Override Control Register
i2c.VAL	0x38	4	Oversampled RX values
i2c.TIMING0	0x3c	4	Detailed I2C Timings (directly corresponding to table 10 in the I2C Specification).
i2c.TIMING1	0x40	4	Detailed I2C Timings (directly corresponding to table 10 in the I2C Specification).
i2c.TIMING2	0x44	4	Detailed I2C Timings (directly corresponding to table 10 in the I2C Specification).
i2c.TIMING3	0x48	4	Detailed I2C Timings (directly corresponding to table 10, in the I2C Specification).
i2c.TIMING4	0x4c	4	Detailed I2C Timings (directly corresponding to table 10, in the I2C Specification).
i2c.TIMEOUT_CTRL	0x50	4	I2C clock stretching and bus timeout control.
i2c.TARGET_ID	0x54	4	I2C target address and mask pairs
i2c.ACQDATA	0x58	4	I2C target acquired data
i2c.TXDATA	0x5c	4	I2C target transmit data
i2c.HOST_TIMEOUT_CTRL	0x60	4	I2C host clock generation timeout value (in units of input clock frequency).
i2c.TARGET_TIMEOUT_CTRL	0x64	4	I2C target internal stretching timeout control.
i2c.TARGET_NACK_COUNT	0x68	4	Number of times the I2C target has NACK'ed a new transaction since the last read of this register.
i2c.TARGET_ACK_CTRL	0x6c	4	Controls for mid-transfer (N)ACK phase handling

Name	Offset	Length	Description
i2c.ACQ_FIFO_NEXT_DATA	0x70	4	The data byte pending to be written to the ACQ FIFO.
i2c.HOST_NACK_HANDLER_TIMEOUT	0x74	4	Timeout in Host-Mode for an unhandled NACK before hardware automatically ends the transaction.
i2c.CONTROLLER_EVENTS	0x78	4	Latched events that explain why the controller halted.
i2c.TARGET_EVENTS	0x7c	4	Latched events that can cause the target module to stretch the clock at the beginning of a read transfer.

2.1326 INTR_STATE

Interrupt State Register - Offset: `0x0` - Reset default: `0x0` - Reset mask: `0x7fff`

2.1326.1 Fields

{"reg": [{"name": "fmt_threshold", "bits": 1, "attr": ["ro"], "rotate": -90}, {"name": "rx_thre

Bits	Type	Reset	Name	Description
31:15				Reserved
14	rw1c	0x0	host_timeout	target mode interrupt: raised if the host stops sending the clock during an ongoing transaction.
13	rw1c	0x0	unexp_stop	target mode interrupt: raised if STOP is received without a preceding NACK during an external host read.
12	ro	0x0	acq_stretch	target mode interrupt: raised if the target is stretching clocks due to full ACQ FIFO or zero count in TARGET_ACK_CTRL.NBYTES (if enabled). This is a level status interrupt.
11	ro	0x0	tx_threshold	target mode interrupt: asserted whilst the TX FIFO level is below the low threshold. This is a level status interrupt.
10	ro	0x0	tx_stretch	target mode interrupt: raised if the target is stretching clocks for a read command. This is a level status interrupt.
9	rw1c	0x0	cmd_complete	host and target mode interrupt. In host mode, raised if the host issues a repeated START or terminates the transaction by issuing STOP. In target mode, raised if the external host issues a STOP or repeated START.
8	rw1c	0x0	sda_unstable	host mode interrupt: raised if the target does not assert a constant value of SDA during transmission.
7	rw1c	0x0	stretch_timeout	host mode interrupt: raised if target stretches the clock beyond the allowed timeout period
6	rw1c	0x0	sda_interference	host mode interrupt: raised if the SDA line goes low when host is trying to assert high
5	rw1c	0x0	scl_interference	host mode interrupt: raised if the SCL line drops early (not supported without clock synchronization).

Bits	Type	Reset	Name	Description
4	ro	0x0	controller_halt	Host mode interrupt: raised if the controller FSM is halted, such as on an unexpected NACK or lost arbitration. Check CONTROLLER_EVENTS for the reason. The interrupt will be released when the bits in CONTROLLER_EVENTS are cleared.
3	rw1c	0x0	rx_overflow	Host mode interrupt: raised if the RX FIFO has overflowed.
2	ro	0x0	acq_threshold	Host mode interrupt: asserted whilst the ACQ FIFO level is above the high threshold. This is a level status interrupt.
1	ro	0x0	rx_threshold	Host mode interrupt: asserted whilst the RX FIFO level is above the high threshold. This is a level status interrupt.
0	ro	0x0	fmt_threshold	Host mode interrupt: asserted whilst the FMT FIFO level is below the low threshold. This is a level status interrupt.

2.1327 INTR_ENABLE

Interrupt Enable Register - Offset: `0x4` - Reset default: `0x0` - Reset mask: `0x7fff`

2.1327.1 Fields

{"reg": [{"name": "fmt_threshold", "bits": 1, "attr": ["rw"], "rotate": -90}, {"name": "rx_thre

Bits	Type	Reset	Name	Description
31:15				Reserved
14	rw	0x0	host_timeout	Enable interrupt when INTR_STATE.host_timeout is set.
13	rw	0x0	unexp_stop	Enable interrupt when INTR_STATE.unexp_stop is set.
12	rw	0x0	acq_stretch	Enable interrupt when INTR_STATE.acq_stretch is set.
11	rw	0x0	tx_threshold	Enable interrupt when INTR_STATE.tx_threshold is set.
10	rw	0x0	tx_stretch	Enable interrupt when INTR_STATE.tx_stretch is set.
9	rw	0x0	cmd_complete	Enable interrupt when INTR_STATE.cmd_complete is set.
8	rw	0x0	sda_unstable	Enable interrupt when INTR_STATE.sda_unstable is set.
7	rw	0x0	stretch_timeout	Enable interrupt when INTR_STATE.stretch_timeout is set.
6	rw	0x0	sda_interference	Enable interrupt when INTR_STATE.sda_interference is set.
5	rw	0x0	scl_interference	Enable interrupt when INTR_STATE.scl_interference is set.
4	rw	0x0	controller_halt	Enable interrupt when INTR_STATE.controller_halt is set.
3	rw	0x0	rx_overflow	Enable interrupt when INTR_STATE.rx_overflow is set.

Bits	Type	Reset	Name	Description
2	rw	0x0	acq_threshold	Enable interrupt when INTR_STATE.acq_threshold is set.
1	rw	0x0	rx_threshold	Enable interrupt when INTR_STATE.rx_threshold is set.
0	rw	0x0	fmt_threshold	Enable interrupt when INTR_STATE.fmt_threshold is set.

2.1328 INTR_TEST

Interrupt Test Register - Offset: 0x8 - Reset default: 0x0 - Reset mask: 0x7fff

2.1328.1 Fields

{"reg": [{"name": "fmt_threshold", "bits": 1, "attr": ["wo"], "rotate": -90}, {"name": "rx_thre

Bits	Type	Reset	Name	Description
31:15				Reserved
14	wo	0x0	host_timeout	Write 1 to force INTR_STATE.host_timeout to 1.
13	wo	0x0	unexp_stop	Write 1 to force INTR_STATE.unexp_stop to 1.
12	wo	0x0	acq_stretch	Write 1 to force INTR_STATE.acq_stretch to 1.
11	wo	0x0	tx_threshold	Write 1 to force INTR_STATE.tx_threshold to 1.
10	wo	0x0	tx_stretch	Write 1 to force INTR_STATE.tx_stretch to 1.
9	wo	0x0	cmd_complete	Write 1 to force INTR_STATE.cmd_complete to 1.
8	wo	0x0	sda_unstable	Write 1 to force INTR_STATE.sda_unstable to 1.
7	wo	0x0	stretch_timeout	Write 1 to force INTR_STATE.stretch_timeout to 1.
6	wo	0x0	sda_interference	Write 1 to force INTR_STATE.sda_interference to 1.
5	wo	0x0	scl_interference	Write 1 to force INTR_STATE.scl_interference to 1.
4	wo	0x0	controller_halt	Write 1 to force INTR_STATE.controller_halt to 1.
3	wo	0x0	rx_overflow	Write 1 to force INTR_STATE.rx_overflow to 1.
2	wo	0x0	acq_threshold	Write 1 to force INTR_STATE.acq_threshold to 1.
1	wo	0x0	rx_threshold	Write 1 to force INTR_STATE.rx_threshold to 1.
0	wo	0x0	fmt_threshold	Write 1 to force INTR_STATE.fmt_threshold to 1.

2.1329 ALERT_TEST

Alert Test Register - Offset: 0xc - Reset default: 0x0 - Reset mask: 0x1

2.1329.1 Fields

{"reg": [{"name": "fatal_fault", "bits": 1, "attr": ["wo"], "rotate": -90}, {"bits": 31}], "co

Bits	Type	Reset	Name	Description
31:1				Reserved
0	wo	0x0	fatal_fault	Write 1 to trigger one alert event of this kind.

2.1330 CTRL

I2C Control Register - Offset: `0x10` - Reset default: `0x0` - Reset mask: `0x7f`

2.1330.1 Fields

{"reg": [{"name": "ENABLEHOST", "bits": 1, "attr": ["rw"], "rotate": -90}, {"name": "ENABLETARG

Bits	Type	Reset	Name
31:7			Reserved
6	rw	0x0	TX_STRETCH_CTRL_EN
5	rw	0x0	MULTI_CONTROLLER_MONITOR_EN
4	rw	0x0	ACK_CTRL_EN
3	rw	0x0	NACK_ADDR_AFTER_TIMEOUT
2	rw	0x0	LLPBK
1	rw	0x0	ENABLETARGET
0	rw	0x0	ENABLEHOST

2.1330.2 CTRL . TX_STRETCH_CTRL_EN

If set to 1, this bit causes a read transfer addressed to this target to set the corresponding bit in `TARGET_EVENTS.`

While `TARGET_EVENTS.TX_PENDING` is 1, subsequent read transactions will stretch the clock, even if there is data in the TX FIFO.

If enabled, this function allows software to confirm the data in the TX FIFO should be released for the current read. This may be useful for cases where the TX FIFO has data that does not apply to the current transfer. For example, the transaction could've targeted an alternate function via another address.

2.1330.3 CTRL . MULTI_CONTROLLER_MONITOR_EN

Enable the bus monitor in multi-controller mode.

If a 0->1 transition happens while `CTRL.ENABLEHOST` and `CTRL.ENABLETARGET` are both 0, the bus monitor will enable and begin in the "bus busy" state. To transition to a bus free state, `HOST_TIMEOUT_CTRL` must be nonzero, so the bus monitor may count out idle cycles to confirm the freedom to transmit. In addition, the bus monitor will track whether the bus is free based on the enabled timeouts and detected Stop symbols. For multi-controller mode,

ensure CTRL.MULTI_CONTROLLER_MONITOR_EN becomes 1 no later than CTRL.ENABLEHOST or CTRL.ENABLETARGET. This bit can be set at the same time as either or both of the other two, though.

Note that if CTRL.MULTI_CONTROLLER_MONITOR_EN is set after CTRL.ENABLEHOST or CTRL.ENABLETARGET, the bus monitor will begin in the "bus free" state instead. This would violate the proper protocol for a controller to join a multi-controller environment. However, if this controller is known to be the first to join, this ordering will enable skipping the idle wait.

When 0, the bus monitor will report that the bus is always free, so the controller FSM is never blocked from transmitting.

2.1330.4 CTRL . ACK_CTRL_EN

Enable I2C Target ACK Control Mode.

ACK Control Mode works together with TARGET_ACK_CTRL.NBYTES to allow software to control upper-layer protocol (N)ACKing (e.g. as in SMBus). This bit enables the mode when 1, and TARGET_ACK_CTRL.NBYTES limits how many bytes may be automatically ACK'd while the ACQ FIFO has space. If it is 0, the decision to ACK or NACK is made only from stretching timeouts and CTRL.NACK_ADDR_AFTER_TIMEOUT.

2.1330.5 CTRL . NACK_ADDR_AFTER_TIMEOUT

Enable NACKing the address on a stretch timeout.

This is a Target mode feature. If enabled (1), a stretch timeout will cause the device to NACK the address byte. If disabled (0), a stretch timeout will cause the device to ACK the address byte. SMBus requires that devices always ACK their address, even for read commands. However, non-SMBus protocols may have a different approach and can choose to NACK instead.

Note that both cases handle data bytes the same way. For writes, the Target module will NACK all subsequent data bytes until it receives a Stop. For reads, the Target module will release SDA, causing 0xff to be returned for all data bytes until it receives a Stop.

2.1330.6 CTRL . LLPBK

Enable I2C line loopback test If line loopback is enabled, the internal design sees ACQ and RX data as "1"

2.1330.7 CTRL . ENABLETARGET

Enable Target I2C functionality

2.1330.8 CTRL . ENABLEHOST

Enable Host I2C functionality

2.1331 STATUS

I2C Live Status Register for Host and Target modes - Offset: `0x14` - Reset default: `0x33c` - Reset mask: `0x7ff`

2.1331.1 Fields


```
{"reg": [{"name": "FMTFULL", "bits": 1, "attr": ["ro"], "rotate": -90}, {"name": "RXFULL", "bi
```


Bits	Type	Reset	Name	Description
31:11				Reserved
10	ro	x	ACK_CTRL_STRETCH	Target mode stretching at (N)ACK phase due to zero count in TARGET_ACK_CTRL.NBYTES
9	ro	0x1	ACQEMPTY	Target mode receive FIFO is empty
8	ro	0x1	TXEMPTY	Target mode TX FIFO is empty
7	ro	x	ACQFULL	Target mode receive FIFO is full
6	ro	x	TXFULL	Target mode TX FIFO is full
5	ro	0x1	RXEMPTY	Host mode RX FIFO is empty
4	ro	0x1	TARGETIDLE	Target functionality is idle. No Target transaction is in progress
3	ro	0x1	HOSTIDLE	Host functionality is idle. No Host transaction is in progress
2	ro	0x1	FMTEMPTY	Host mode FMT FIFO is empty
1	ro	x	RXFULL	Host mode RX FIFO is full
0	ro	x	FMTFULL	Host mode FMT FIFO is full

2.1332 RDATA

I2C Read Data - Offset: `0x18` - Reset default: `0x0` - Reset mask: `0xff`

2.1332.1 Fields


```
{"reg": [{"name": "RDATA", "bits": 8, "attr": ["ro"], "rotate": 0}, {"bits": 24}], "config": {
```


Bits	Type	Reset	Name	Description
31:8				Reserved
7:0	ro	x	RDATA	

2.1333 FDATA

I2C Host Format Data

Writes to this register are used to define and drive Controller-Mode transactions. - Offset: `0x1c` - Reset default: `0x0` - Reset mask: `0x1fff`

2.1333.1 Fields

{"reg": [{"name": "FBYTE", "bits": 8, "attr": ["wo"], "rotate": 0}, {"name": "START", "bits": 1

Bits	Type	Reset	Name
31:13			Reserved
12	wo	0x0	NAKOK
11	wo	0x0	RCONT
10	wo	0x0	READB
9	wo	0x0	STOP
8	wo	0x0	START
7:0	wo	0x0	FBYTE

2.1333.2 FDATA . NAKOK

For the currrent controller-transmitter byte (WRITE), do not halt via CONTROLLER_EVENTS or assert the 'controller_halt' interrupt if the current byte is not ACK'd.

2.1333.3 FDATA . RCONT

Do not NACK the last byte read, let the read operation continue.

2.1333.4 FDATA . READB

Transfer Direction Indicator.

If unset, this write to FDATA defines a controller-transmitter operation (WRITE). A single byte of data (FBYTE) is written to the bus.

If set, this write to FDATA defines a controller-receiver operation (READ). The value of FBYTE defines the number of bytes read from the bus. (256 if FBYTE==0)" After this number of bytes are read, the final byte will be NACKed to end the transfer unless RCONT is also set.

2.1333.5 FDATA . STOP

Issue a STOP condition after transmitting FBYTE.

2.1333.6 FDATA . START

Issue a START condition before transmitting FBYTE.

2.1333.7 FDATA . FBYTE

Format Byte.

If no flags are set, hardware will transmit this byte directly.

If READB is set, this field becomes the number of bytes hardware will automatically read from the bus.

2.1334 FIFO_CTRL

I2C FIFO control register - Offset: `0x20` - Reset default: `0x0` - Reset mask: `0x183`

2.1334.1 Fields


```
{"reg": [{"name": "RXRST", "bits": 1, "attr": ["wo"], "rotate": -90}, {"name": "FMTRST", "bits"
```


Bits	Type	Reset	Name	Description
31:9				Reserved
8	wo	0x0	TXRST	TX FIFO reset. Write 1 to the register resets it. Read returns 0
7	wo	0x0	ACQRST	ACQ FIFO reset. Write 1 to the register resets it. Read returns 0
6:2				Reserved
1	wo	0x0	FMTRST	FMT fifo reset. Write 1 to the register resets FMT_FIFO. Read returns 0
0	wo	0x0	RXRST	RX fifo reset. Write 1 to the register resets RX_FIFO. Read returns 0

2.1335 HOST_FIFO_CONFIG

Host mode FIFO configuration - Offset: `0x24` - Reset default: `0x0` - Reset mask: `0xfff0fff`

2.1335.1 Fields


```
{"reg": [{"name": "RX_THRESH", "bits": 12, "attr": ["rw"], "rotate": 0}, {"bits": 4}, {"name":
```


Bits	Type	Reset	Name	Description
31:28				Reserved
27:16	rw	0x0	FMT_THRESH	Threshold level for FMT interrupts. Whilst the number of used entries in the FMT FIFO is below this setting, the fmt_threshold interrupt will be asserted.
15:12				Reserved

Bits	Type	Reset	Name	Description
11:0	rw	0x0	RX_THRESH	Threshold level for RX interrupts. Whilst the level of data in the RX FIFO is above this setting, the rx_threshold interrupt will be asserted.

2.1336 TARGET_FIFO_CONFIG

Target mode FIFO configuration - Offset: `0x28` - Reset default: `0x0` - Reset mask: `0xfff0fff`

2.1336.1 Fields

```
{"reg": [{"name": "TX_THRESH", "bits": 12, "attr": ["rw"], "rotate": 0}, {"bits": 4}, {"name":
```

Bits	Type	Reset	Name	Description
31:28				Reserved
27:16	rw	0x0	ACQ_THRESH	Threshold level for ACQ interrupts. Whilst the level of data in the ACQ FIFO is above this setting, the acq_threshold interrupt will be asserted.
15:12				Reserved
11:0	rw	0x0	TX_THRESH	Threshold level for TX interrupts. Whilst the number of used entries in the TX FIFO is below this setting, the tx_threshold interrupt will be asserted.

2.1337 HOST_FIFO_STATUS

Host mode FIFO status register - Offset: `0x2c` - Reset default: `0x0` - Reset mask: `0xfff0fff`

2.1337.1 Fields

```
{"reg": [{"name": "FMTLVL", "bits": 12, "attr": ["ro"], "rotate": 0}, {"bits": 4}, {"name": "RX
```

Bits	Type	Reset	Name	Description
31:28				Reserved
27:16	ro	x	RXLVL	Current fill level of RX fifo
15:12				Reserved
11:0	ro	x	FMTLVL	Current fill level of FMT fifo

2.1338 TARGET_FIFO_STATUS

Target mode FIFO status register - Offset: `0x30` - Reset default: `0x0` - Reset mask: `0xfff0fff`

2.1338.1 Fields

{"reg": [{"name": "TXLVL", "bits": 12, "attr": ["ro"], "rotate": 0}, {"bits": 4}, {"name": "AC

Bits	Type	Reset	Name	Description
31:28				Reserved
27:16	ro	x	ACQLVL	Current fill level of ACQ fifo
15:12				Reserved
11:0	ro	x	TXLVL	Current fill level of TX fifo

2.1339 OVRD

I2C Override Control Register - Offset: `0x34` - Reset default: `0x0` - Reset mask: `0x7`

2.1339.1 Fields

{"reg": [{"name": "TXOVRDEN", "bits": 1, "attr": ["rw"], "rotate": -90}, {"name": "SCLVAL", "bi

Bits	Type	Reset	Name	Description
31:3				Reserved
2	rw	0x0	SDAVAL	Value for SDA Override. Set to 0 to drive TX Low, and set to 1 for high-Z
1	rw	0x0	SCLVAL	Value for SCL Override. Set to 0 to drive TX Low, and set to 1 for high-Z
0	rw	0x0	TXOVRDEN	Override the SDA and SCL TX signals.

2.1340 VAL

Oversampled RX values - Offset: `0x38` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.1340.1 Fields

{"reg": [{"name": "SCL_RX", "bits": 16, "attr": ["ro"], "rotate": 0}, {"name": "SDA_RX", "bits"

Bits	Type	Reset	Name	Description
31:16	ro	x	SDA_RX	Last 16 oversampled values of SDA. Most recent bit is bit 16, oldest 31.
15:0	ro	x	SCL_RX	Last 16 oversampled values of SCL. Most recent bit is bit 0, oldest 15.

2.1341 TIMING0

Detailed I2C Timings (directly corresponding to table 10 in the I2C Specification). All values are expressed in units of the input clock period. These must be greater than 2 in order for the change in SCL to propagate to the input of the FSM so that acknowledgements are detected correctly. - Offset: `0x3c` - Reset default: `0x0` - Reset mask: `0x1fff1fff`

2.1341.1 Fields


```
{"reg": [{"name": "THIGH", "bits": 13, "attr": ["rw"], "rotate": 0}, {"bits": 3}, {"name": "TL
```


Bits	Type	Reset	Name	Description
31:29				Reserved
28:16	rw	0x0	TLOW	The actual time to hold SCL low between any two SCL pulses. This field is sized to have a range of at least Standard Mode's 4.7 us max with a core clock at 1 GHz.
15:13				Reserved
12:0	rw	0x0	THIGH	The actual time to hold SCL high in a given pulse. This field is sized to have a range of at least Standard Mode's 4.0 us max with a core clock at 1 GHz.

2.1342 TIMING1

Detailed I2C Timings (directly corresponding to table 10 in the I2C Specification). All values are expressed in units of the input clock period. - Offset: `0x40` - Reset default: `0x0` - Reset mask: `0x1ff03ff`

2.1342.1 Fields


```
{"reg": [{"name": "T_R", "bits": 10, "attr": ["rw"], "rotate": 0}, {"bits": 6}, {"name": "T_F"
```


Bits	Type	Reset	Name	Description
31:25				Reserved
24:16	rw	0x0	T_F	The nominal fall time to anticipate for the bus (influences SDA hold times). This field is sized to have a range of at least Standard Mode's 300 ns max with a core clock at 1 GHz.
15:10				Reserved
9:0	rw	0x0	T_R	The nominal rise time to anticipate for the bus (depends on capacitance). This field is sized to have a range of at least Standard Mode's 1000 ns max with a core clock at 1 GHz.

2.1343 TIMING2

Detailed I2C Timings (directly corresponding to table 10 in the I2C Specification). All values are expressed in units of the input clock period. - Offset: `0x44` - Reset default: `0x0` - Reset mask: `0x1fff1fff`

2.1343.1 Fields


```
{"reg": [{"name": "TSU_STA", "bits": 13, "attr": ["rw"], "rotate": 0}, {"bits": 3}, {"name": "
```


Bits	Type	Reset	Name	Description
31:29				Reserved
28:16	rw	0x0	THD_STA	Actual hold time for start signals. This field is sized to have a range of at least Standard Mode's 4.0 us max with a core clock at 1 GHz.
15:13				Reserved
12:0	rw	0x0	TSU_STA	Actual setup time for repeated start signals. This field is sized to have a range of at least Standard Mode's 4.7 us max with a core clock at 1 GHz.

2.1344 TIMING3

Detailed I2C Timings (directly corresponding to table 10, in the I2C Specification). All values are expressed in units of the input clock period. - Offset: `0x48` - Reset default: `0x0` - Reset mask: `0x1fff01ff`

2.1344.1 Fields


```
{"reg": [{"name": "TSU_DAT", "bits": 9, "attr": ["rw"], "rotate": 0}, {"bits": 7}, {"name": "TH
```


Bits	Type	Reset	Name
31:29			Reserved
28:16	rw	0x0	THD_DAT
15:9			Reserved
8:0	rw	0x0	TSU_DAT

2.1344.2 TIMING3 . THD_DAT

Actual hold time for data (or ack) bits. (Note, where required, the parameters TVD_DAT is taken to be THD_DAT+T_F) This field is sized to have a range that accommodates Standard Mode's 3.45 us max for TVD_DAT with a core clock at 1 GHz. However, this field is generally expected to represent a time substantially shorter than that. It should be long enough to cover the maximum round-trip latency from output pins, through pads and voltage transitions on the board, and back to the input pins, but it should not be substantially greater.

2.1344.3 TIMING3 . TSU_DAT

Actual setup time for data (or ack) bits. This field is sized to have a range of at least Standard Mode's 250 ns max with a core clock at 1 GHz.

2.1345 TIMING4

Detailed I2C Timings (directly corresponding to table 10, in the I2C Specification). All values are expressed in units of the input clock period. - Offset: `0x4c` - Reset default: `0x0` - Reset mask: `0x1fff1fff`

2.1345.1 Fields


```
{"reg": [{"name": "TSU_STO", "bits": 13, "attr": ["rw"], "rotate": 0}, {"bits": 3}, {"name": "
```


Bits	Type	Reset	Name	Description
31:29				Reserved
28:16	rw	0x0	T_BUF	Actual time between each STOP signal and the following START signal. This field is sized to have a range of at least Standard Mode's 4.7 us max with a core clock at 1 GHz.
15:13				Reserved
12:0	rw	0x0	TSU_STO	Actual setup time for stop signals. This field is sized to have a range of at least Standard Mode's 4.0 us max with a core clock at 1 GHz.

2.1346 TIMEOUT_CTRL

I2C clock stretching and bus timeout control.

This timeout must be enabled by setting `TIMEOUT_CTRL.EN` to 1, and the behavior of this feature depends on the value of `TIMEOUT_CTRL.MODE`.

If the mode is "STRETCH_TIMEOUT", this is used in I2C controller mode to detect whether a connected target is stretching a single low time beyond the timeout value. Configured as such, this timeout is more informative and doesn't do more than assert the "stretch_timeout" interrupt.

If the mode is "BUS_TIMEOUT", it is used to detect whether the clock has been held low for too long instead, inclusive of the controller's clock low time. This is useful for an SMBus context, where the VAL programmed should be tTIMEOUT:MIN. - Offset: `0x50` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.1346.1 Fields


```
{"reg": [{"name": "VAL", "bits": 30, "attr": ["rw"], "rotate": 0}, {"name": "MODE", "bits": 1,
```

Bits	Type	Reset	Name
31	rw	0x0	EN
30	rw	0x0	MODE
29:0	rw	0x0	VAL

2.1346.2 TIMEOUT_CTRL . EN

Enable stretch timeout or bus timeout feature

2.1346.3 TIMEOUT_CTRL . MODE

Selects the timeout mode, between a stretch timeout and a bus timeout.

Between the two modes, the primary difference is how much of the clock low period is counted. For a stretch timeout, only the time that another device holds the clock low will be counted. For a bus timeout, the entire clock low time is counted, consistent with the SMBus tTIMEOUT type.

TIMEOUT_CTRL.EN must be 1 for either of these features to be enabled.

Value	Name	Description
0x0	STRETCH_TIMEOUT	The timeout is a target stretch timeout. The counter will track how long the clock has been stretched by another device while the controller is active.
0x1	BUS_TIMEOUT	The timeout is a clock low timeout. The counter will track how long the clock low period is, inclusive of the controller's ordinary low count. A timeout will set !!CONTROLLER_EVENTS.BUS_TIMEOUT and cause a "controller_halt" interrupt.

2.1346.4 TIMEOUT_CTRL . VAL

Clock stretching timeout value (in units of input clock frequency)

2.1347 TARGET_ID

I2C target address and mask pairs - Offset: 0x54 - Reset default: 0x0 - Reset mask: 0xffffffff

2.1347.1 Fields

{"reg": [{"name": "ADDRESS0", "bits": 7, "attr": ["rw"], "rotate": 0}, {"name": "MASK0", "bits"

Bits	Type	Reset	Name	Description
31:28				Reserved
27:21	rw	0x0	MASK1	I2C target mask number 1. At least one bit in MASK1 must be set to 1 for ADDRESS1 to be used.

Bits	Type	Reset	Name	Description
20:14	rw	0x0	ADDRESS1	I2C target address number 1
13:7	rw	0x0	MASK0	I2C target mask number 0. At least one bit in MASK0 must be set to 1 for ADDRESS0 to be used.
6:0	rw	0x0	ADDRESS0	I2C target address number 0

2.1348 ACQDATA

I2C target acquired data - Offset: `0x58` - Reset default: `0x0` - Reset mask: `0x7ff`

2.1348.1 Fields


```
{"reg": [{"name": "ABYTE", "bits": 8, "attr": ["ro"], "rotate": 0}, {"name": "SIGNAL", "bits":
```


Bits	Type	Reset	Name
31:11			Reserved
10:8	ro	x	SIGNAL
7:0	ro	x	ABYTE

2.1348.2 ACQDATA . SIGNAL

Indicates any control symbols associated with the ABYTE.

For the STOP symbol, a stretch timeout or other unexpected events will cause a NACK_STOP to appear in the ACQ FIFO. If the ACQ FIFO doesn't have enough space to record a START and a STOP, the transaction will be dropped entirely on a stretch timeout. In that case, the START byte will not appear (neither as START nor NACK_START), but a standalone NACK_STOP may, if there was space. Software can discard any standalone NACK_STOP that appears.

See the associated values for more information about the contents.

Value	Name	Description
0x0	NONE	ABYTE contains an ordinary data byte that was received and ACK'd.
0x1	START	A START condition preceded the ABYTE to start a new transaction. ABYTE contains the 7-bit I2C address plus R/W command bit in the order received on the bus, MSB first.
0x2	STOP	A STOP condition was received for a transaction including a transfer that addressed this Target. No transfers addressing this Target in that transaction were NACK'd. ABYTE contains no data.
0x3	RESTART	A repeated START condition preceded the ABYTE, extending the current transaction with a new transfer. ABYTE contains the 7-bit I2C address plus R/W command bit in the order received on the bus, MSB first.
0x4	NACK	ABYTE contains an ordinary data byte that was received and NACK'd.

Value	Name	Description
0x5	NACK_START	A START condition preceded the ABYTE (including repeated START) that was part of a NACK'd transfer. The ABYTE contains the matching I2C address and command bit. The ABYTE was ACK'd, but the rest of the transaction was NACK'ed.
0x6	NACK_STOP	A transaction including a transfer that addressed this Target was ended, but the transaction ended abnormally and/or the transfer was NACK'd. The end can be due to a STOP condition or unexpected events, such as a bus timeout (if enabled). ABYTE contains no data. NACKing can occur for multiple reasons, including a stretch timeout, a SW-directed NACK, or lost arbitration. This signal is a bucket for all these error-type terminations.

Other values are reserved.

2.1348.3 ACQDATA . ABYTE

Address for accepted transaction or acquired byte

2.1349 TXDATA

I2C target transmit data - Offset: `0x5c` - Reset default: `0x0` - Reset mask: `0xff`

2.1349.1 Fields

`{"reg": [{"name": "TXDATA", "bits": 8, "attr": ["wo"], "rotate": 0}, {"bits": 24}], "config": `

Bits	Type	Reset	Name	Description
31:8				Reserved
7:0	wo	0x0	TXDATA	

2.1350 HOST_TIMEOUT_CTRL

I2C host clock generation timeout value (in units of input clock frequency).

In an active transaction in Target-Mode, if the Controller ceases to send SCL pulses for this number of cycles then the "host_timeout" interrupt will be asserted.

In multi-controller monitoring mode, `HOST_TIMEOUT_CTRL` is required to be nonzero to transition out of the initial busy state. Set this CSR to 0 to disable this behaviour. - Offset: `0x60` - Reset default: `0x0` - Reset mask: `0xffffff`

2.1350.1 Fields

{"reg": [{"name": "HOST_TIMEOUT_CTRL", "bits": 20, "attr": ["rw"], "rotate": 0}, {"bits": 12}]

Bits	Type	Reset	Name	Description
31:20				Reserved
19:0	rw	0x0	HOST_TIMEOUT_CTRL	

2.1351 TARGET_TIMEOUT_CTRL

I2C target internal stretching timeout control. When the target has stretched beyond this time it will send a NACK for incoming data bytes or release SDA for outgoing data bytes. The behavior for the address byte is configurable via CTRL.ACK_ADDR_AFTER_TIMEOUT. Note that the count accumulates stretching time over the course of a transaction. In other words, this is equivalent to the SMBus cumulative target clock extension time. - Offset: `0x64` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.1351.1 Fields

{"reg": [{"name": "VAL", "bits": 31, "attr": ["rw"], "rotate": 0}, {"name": "EN", "bits": 1, "a

Bits	Type	Reset	Name	Description
31	rw	0x0	EN	Enable timeout feature and send NACK once the timeout has been reached
30:0	rw	0x0	VAL	Clock stretching timeout value (in units of input clock frequency)

2.1352 TARGET_NACK_COUNT

Number of times the I2C target has NACK'ed a new transaction since the last read of this register. Reading this register clears it. This is useful because when the ACQ FIFO is full the software know that a NACK has occurred, but without this register would not know how many transactions it missed. When it reaches its maximum value it will stay at that value. - Offset: `0x68` - Reset default: `0x0` - Reset mask: `0xff`

2.1352.1 Fields

{"reg": [{"name": "TARGET_NACK_COUNT", "bits": 8, "attr": ["rc"], "rotate": -90}, {"bits": 24}]

Bits	Type	Reset	Name	Description
31:8				Reserved
7:0	rc	0x0	TARGET_NACK_COUNT	

2.1353 TARGET_ACK_CTRL

Controls for mid-transfer (N)ACK phase handling - Offset: `0x6c` - Reset default: `0x0` - Reset mask: `0x800001ff`

2.1353.1 Fields

{"reg": [{"name": "NBYTES", "bits": 9, "attr": ["rw"], "rotate": 0}, {"bits": 22}, {"name": "NA

Bits	Type	Reset	Name
31	wo	x	NACK
30:9			Reserved
8:0	rw	x	NBYTES

2.1353.2 TARGET_ACK_CTRL . NACK

When the Target module stretches on the (N)ACK phase of a Write due to TARGET_ACK_CTRL.NBYTES being 0, writing a 1 here will cause it to send a NACK.

If software chooses to NACK, note that the NACKing behavior is the same as if a stretch timeout occurred. The rest of the transaction will be NACK'd, including subsequent transfers. For the address byte, the (N)ACK phase of subsequent transfers will follow the behavior specified by CTRL.NACK_ADDR_AFTER_TIMEOUT.

Automatically clears to 0.

2.1353.3 TARGET_ACK_CTRL . NBYTES

Remaining number of bytes the Target module may ACK automatically.

If CTRL.ACK_CTRL_EN is set to 1, the Target module will stretch the clock at the (N)ACK phase of a byte if this CSR is 0, awaiting software's instructions.

At the beginning of each Write transfer, this byte count is reset to 0. Writes to this CSR also are only accepted while the Target module is stretching the clock. The Target module will always ACK its address if the ACQ FIFO has space. For data bytes afterwards, it will stop at the (N)ACK phase and stretch the clock when this CSR is 0. For each data byte that is ACK'd in a transaction, the byte count will decrease by 1.

Note that a full ACQ FIFO can still cause the Target module to halt at the beginning of a new byte. The ACK Control Mode provides an additional synchronization point, during the (N)ACK phase

instead of after. For both cases, TARGET_TIMEOUT_CTRL applies, and stretching past the timeout will produce an automatic NACK.

This mode can be used to implement the mid-transfer (N)ACK responses required by various SMBus protocols.

2.1354 ACQ_FIFO_NEXT_DATA

The data byte pending to be written to the ACQ FIFO.

This CSR is only valid while the Target module is stretching in the (N)ACK phase, indicated by STATUS.ACK_CTRL_STRETCH . It is intended to be used with ACK Control Mode, so software may check the current byte. - Offset: 0x70 - Reset default: 0x0 - Reset mask: 0xff

2.1354.1 Fields

{"reg": [{"name": "ACQ_FIFO_NEXT_DATA", "bits": 8, "attr": ["ro"], "rotate": -90}, {"bits": 24

Bits	Type	Reset	Name	Description
31:8				Reserved
7:0	ro	x	ACQ_FIFO_NEXT_DATA	

2.1355 HOST_NACK_HANDLER_TIMEOUT

Timeout in Host-Mode for an unhandled NACK before hardware automatically ends the transaction. (in units of input clock frequency)

If an active Controller-Transmitter transfer receives a NACK from the Target, the CONTROLLER_EVENTS.NACK bit is set. In turn, this causes the Controller FSM to halt awaiting software intervention, and the 'controller_halt' interrupt may assert. Software must clear the CONTROLLER_EVENTS.NACK bit to allow the state machine to continue, typically after clearing out the FMTFIFO to start a new transfer. While halted, the active transaction is not ended (no STOP (P) condition is created), and the block asserts SCL and leaves SDA released.

This timeout can be used to automatically produce a STOP condition, whether as a backstop for slow software responses (longer timeout) or as a convenience (short timeout). If the timeout expires, the Controller FSM will issue a STOP (P) condition on the bus to end the active transaction. Additionally, the CONTROLLER_EVENTS.UNHANDLED_NACK_TIMEOUT bit is set to alert software, and the FSM will return to the idle state and halt until the bit is cleared.

The enable bit must be set for this feature to operate. - Offset: 0x74 - Reset default: 0x0 - Reset mask: 0xffffffff

2.1355.1 Fields

{"reg": [{"name": "VAL", "bits": 31, "attr": ["rw"], "rotate": 0}, {"name": "EN", "bits": 1, "a

Bits	Type	Reset	Name	Description
31	rw	0x0	EN	Timeout enable
30:0	rw	0x0	VAL	Unhandled NAK timeout value (in units of input clock frequency)

2.1356 CONTROLLER_EVENTS

Latched events that explain why the controller halted.

Any bits that are set must be written (with a 1) to clear the CONTROLLER_HALT interrupt. - Offset: `0x78` - Reset default: `0x0` - Reset mask: `0xf`

2.1356.1 Fields


```
{"reg": [{"name": "NACK", "bits": 1, "attr": ["rw1c"], "rotate": -90}, {"name": "UNHANDLED_NAC
```


Bits	Type	Reset	Name	Description
31:4				Reserved
3	rw1c	0x0	ARBITRATION_LOST	A Host-Mode active transaction has terminated due to lost arbitration.
2	rw1c	0x0	BUS_TIMEOUT	A Host-Mode active transaction has terminated due to a bus timeout activated by `TIMEOUT_CTRL`.
1	rw1c	0x0	UNHANDLED_NACK_TIMEOUT	A Host-Mode active transaction has been ended by the `HOST_NACK_HANDLER_TIMEOUT` mechanism.
0	rw1c	0x0	NACK	Received an unexpected NACK

2.1357 TARGET_EVENTS

Latched events that can cause the target module to stretch the clock at the beginning of a read transfer.

These events cause TX FIFO-related stretching even when the TX FIFO has data available. Any bits that are set must be written (with a 1) to clear the tx_stretch interrupt.

This CSR serves as a gate to prevent the Target module from responding to a read command with unrelated, leftover data. - Offset: `0x7c` - Reset default: `0x0` - Reset mask: `0x7`

2.1357.1 Fields


```
{"reg": [{"name": "TX_PENDING", "bits": 1, "attr": ["rw1c"], "rotate": -90}, {"name": "BUS_TIM
```

Bits	Type	Reset	Name
31:3			Reserved
2	rw1c	0x0	ARBITRATION_LOST
1	rw1c	0x0	BUS_TIMEOUT
0	rw1c	0x0	TX_PENDING

2.1357.2 TARGET_EVENTS . ARBITRATION_LOST

A Target-Mode read transfer has terminated due to lost arbitration.

2.1357.3 TARGET_EVENTS . BUS_TIMEOUT

A Target-Mode read transfer has terminated due to a bus timeout activated by TIMEOUT_CTRL.

2.1357.4 TARGET_EVENTS . TX_PENDING

A new Target-Mode read transfer has arrived that addressed this target.

This bit is used by software to confirm the release of the contents in the TX FIFO. If the contents do not apply, software should first reset the TX FIFO, then load it with the correct data, then clear this bit.

Optionally enabled by CTRL.TX_STRETCH_CTRL_EN.

2.1358 integer_cluster / doc / pulp_cluster_peripherals_memory_map.md

2.1359 PULP Cluster Peripheral Memory Map

This document describes the memory-mapped peripheral devices accessible from the PULP cluster through the peripheral interconnect slave port.

2.1360 Base Address

- **Cluster Base Address**: 0x5000_0000
- **Peripheral Offset**: 0x0020_0000
- **External Offset**: 0x0040_0000

Cluster Peripheral Base Address:
0x5020_0000 – 0x5040_0000 (2 MiB region)

2.1361 Peripheral Layout

Peripheral	ID	Offset (from Peripheral Base)	Address Range
EOC	0	0x0000	0x5020_0000 – 0x5020_03FF
Timer	1	0x0400	0x5020_0400 – 0x5020_07FF
Event Unit (also 3)	2/3	0x0800	0x5020_0800 – 0x5020_0FFF
HWPE	4	0x1000	0x5020_1000 – 0x5020_13FF
ICache Controller	5	0x1400	0x5020_1400 – 0x5020_17FF
DMA (Cluster)	6	0x1800	0x5020_1800 – 0x5020_1BFF
DMA (Fabric Ctrl)	7	0x1C00	0x5020_1C00 – 0x5020_1FFF
HMR Unit	8	0x2000	0x5020_2000 – 0x5020_23FF
External	9	0x2400	0x5020_2400 – 0x5020_27FF
Error Unit	10	0x2800	0x5020_2800 – 0x5020_2BFF

2.1362 Address Mapping Summary

Region	Index	Start Address	End Address	Notes
TCDM	0	0x5000_0000	0x5000_0000 + TCDM_SIZE	Tightly Coupled Data Memory
Peripherals	1	0x5020_0000	0x5040_0000	Cluster Peripheral Region
External	2	0x5040_0000	0xFFFF_FFFF	Access beyond cluster
Below Cluster	3	0x0000_0000	0x5000_0000	Not cluster-related

2.1363 irq_router / doc / registers.md

2.1364 Summary

Name	Offset	Length	Description
irq_router.IRQ_TARGET_MASK	0x0	4	Target selection bitmask control register

2.1365 IRQ_TARGET_MASK

Target selection bitmask control register - Offset: 0x0 - Reset default: 0x1 - Reset mask: 0xffffffff

2.1365.1 Fields

{"reg": [{"name": "mask", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "f

Bits	Type	Reset	Name	Description
31:0	rw	0x1	mask	Target selection bitmask control register for single interrupt line. Reflects interrupt line logic level.

2.1366 l2_ecc_config / doc / registers.md

2.1367 Summary

Name	Offset	Length	Description
ECC_manager.mismatch_count	0x0	4	Correctable mismatches caught by ecc on access
ECC_manager.scrub_interval	0x4	4	Interval between scrubs
ECC_manager.scrub_fix_count	0x8	4	Correctable mismatches caught by ecc on scrub
ECC_manager.scrub_uncorrectable_count	0xc	4	Uncorrectable mismatches caught by ecc on scrub
ECC_manager.write_mask_data_n	0x10	4	Testing: Inverted write mask for data bits
ECC_manager.write_mask_ecc_n	0x14	4	Testing: Inverted write mask for ECC bits

2.1368 mismatch_count

Correctable mismatches caught by ecc on access - Offset: `0x0` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.1368.1 Fields

{"reg": [{"name": "correctable_mismatches", "bits": 32, "attr": ["rw0c"], "rotate": 0}], "conf

Bits	Type	Reset	Name	Description
31:0	rw0c	0x0	correctable_mismatches	Correctable mismatches caught by ecc on access

2.1369 scrub_interval

Interval between scrubs - Offset: `0x4` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.1369.1 Fields

{"reg": [{"name": "scrub_interval", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lane

Bits	Type	Reset	Name	Description
31:0	rw	0x0	scrub_interval	Interval between scrubs

2.1370 scrub_fix_count

Correctable mismatches caught by ecc on scrub - Offset: `0x8` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.1370.1 Fields

{"reg": [{"name": "correctable_mismatches", "bits": 32, "attr": ["rw0c"], "rotate": 0}], "confi

Bits	Type	Reset	Name	Description
31:0	rw0c	0x0	correctable_mismatches	Correctable mismatches caught by ecc on scrub

2.1371 scrub_uncorrectable_count

Uncorrectable mismatches caught by ecc on scrub - Offset: `0xc` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.1371.1 Fields

{"reg": [{"name": "uncorrectable_mismatches", "bits": 32, "attr": ["rw0c"], "rotate": 0}], "cor

Bits	Type	Reset	Name	Description
31:0	rw0c	0x0	uncorrectable_mismatches	Uncorrectable mismatches caught by ecc on scrub

2.1372 write_mask_data_n

Testing: Inverted write mask for data bits - Offset: `0x10` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.1372.1 Fields

{"reg": [{"name": "write_mask_data_n", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"

Bits	Type	Reset	Name	Description
31:0	rw	0x0	write_mask_data_n	Testing: Inverted write mask for data bits

2.1373 write_mask_ecc_n

Testing: Inverted write mask for ECC bits - Offset: `0x14` - Reset default: `0x0` - Reset mask: `0x7f`

2.1373.1 Fields

{"reg": [{"name": "write_mask_ecc_n", "bits": 7, "attr": ["rw"], "rotate": -90}, {"bits": 25}]

Bits	Type	Reset	Name	Description
31:7				Reserved
6:0	rw	0x0	write_mask_ecc_n	Testing: Inverted write mask for ECC bits

2.1374 mailbox / doc / registers.md

2.1375 Summary

Name	Offset	Length	Description
mailbox.IRQ_SND_STAT	0x0	4	Sender interrupt status register
mailbox.IRQ_SND_SET	0x4	4	Sender interrupt set register
mailbox.IRQ_SND_CLR	0x8	4	Sender interrupt clear register
mailbox.IRQ_SND_EN	0xc	4	Sender interrupt enable register
mailbox.IRQ_RCV_STAT	0x40	4	Receiver interrupt status register
mailbox.IRQ_RCV_SET	0x44	4	Receiver interrupt set register
mailbox.IRQ_RCV_CLR	0x48	4	Receiver interrupt clear register
mailbox.IRQ_RCV_EN	0x4c	4	Receiver interrupt enable register
mailbox.LETTER0	0x80	4	Memory region 0 to put a message or pointer
mailbox.LETTER1	0x84	4	Memory region 1 to put a message or pointer

2.1376 IRQ_SND_STAT

Sender interrupt status register - Offset: `0x0` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.1376.1 Fields

{"reg": [{"name": "stat", "bits": 1, "attr": ["ro"], "rotate": -90}, {"name": "reserved", "bits

Bits	Type	Reset	Name	Description
31:1	ro	x	reserved	reserved
0	ro	x	stat	Sender side interrupt status. Receiver confirms letter. Reflects interrupt line logic level.

2.1377 IRQ_SND_SET

Sender interrupt set register - Offset: `0x4` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.1377.1 Fields

{"reg": [{"name": "set", "bits": 1, "attr": ["wo"], "rotate": -90}, {"name": "reserved", "bits"

Bits	Type	Reset	Name	Description
31:1	ro	x	reserved	reserved
0	wo	x	set	Sender side interrupt set. Receiver confirms letter.

2.1378 IRQ_SND_CLR

Sender interrupt clear register - Offset: `0x8` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.1378.1 Fields

{"reg": [{"name": "clr", "bits": 1, "attr": ["wo"], "rotate": -90}, {"name": "reserved", "bits"

Bits	Type	Reset	Name	Description
31:1	ro	x	reserved	reserved
0	wo	x	clr	Sender side interrupt clear. Receiver confirms letter.

2.1379 IRQ_SND_EN

Sender interrupt enable register - Offset: `0xc` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.1379.1 Fields

{"reg": [{"name": "en", "bits": 1, "attr": ["rw"], "rotate": -90}, {"name": "reserved", "bits"

Bits	Type	Reset	Name	Description
31:1	ro	0x0	reserved	reserved
0	rw	0x0	en	Sender side interrupt enable. Receiver confirms letter.

2.1380 IRQ_RCV_STAT

Receiver interrupt status register - Offset: `0x40` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.1380.1 Fields

{"reg": [{"name": "stat", "bits": 1, "attr": ["ro"], "rotate": -90}, {"name": "reserved", "bits

Bits	Type	Reset	Name	Description
31:1	ro	x	reserved	reserved
0	ro	x	stat	Receiver side interrupt status. Sender notifies receiver of a new letter arriving. Reflects interrupt line logic level.

2.1381 IRQ_RCV_SET

Receiver interrupt set register - Offset: `0x44` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.1381.1 Fields

{"reg": [{"name": "set", "bits": 1, "attr": ["wo"], "rotate": -90}, {"name": "reserved", "bits"

Bits	Type	Reset	Name	Description
31:1	ro	x	reserved	reserved
0	wo	x	set	Receiver side interrupt set. Sender notifies receiver of a new letter arriving.

2.1382 IRQ_RCV_CLR

Receiver interrupt clear register - Offset: `0x48` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.1382.1 Fields

{"reg": [{"name": "clr", "bits": 1, "attr": ["wo"], "rotate": -90}, {"name": "reserved", "bits"

Bits	Type	Reset	Name	Description
31:1	ro	x	reserved	reserved
0	wo	x	clr	Receiver side interrupt clear. Sender notifies receiver of a new letter arriving.

2.1383 IRQ_RCV_EN

Receiver interrupt enable register - Offset: `0x4c` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.1383.1 Fields

{"reg": [{"name": "en", "bits": 1, "attr": ["rw"], "rotate": -90}, {"name": "reserved", "bits"

Bits	Type	Reset	Name	Description
31:1	ro	0x0	reserved	reserved
0	rw	0x0	en	Receiver side interrupt enable. Sender notifies receiver of a new letter arriving.

2.1384 LETTER0

Memory region 0 to put a message or pointer - Offset: `0x80` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.1384.1 Fields

{"reg": [{"name": "LETTER0", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1,

Bits	Type	Reset	Name	Description
31:0	rw	0x0	LETTER0	

2.1385 LETTER1

Memory region 1 to put a message or pointer - Offset: `0x84` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.1385.1 Fields

{"reg": [{"name": "LETTER1", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1,

Bits	Type	Reset	Name	Description
31:0	rw	0x0	LETTER1	

2.1386 plic / doc / registers.md

2.1387 Summary

Name	Offset	Length	Description
rv_plic.PRIO0	0x0	4	Interrupt Source 0 Priority
rv_plic.PRIO1	0x4	4	Interrupt Source 1 Priority
rv_plic.PRIO2	0x8	4	Interrupt Source 2 Priority
rv_plic.PRIO3	0xc	4	Interrupt Source 3 Priority
rv_plic.PRIO4	0x10	4	Interrupt Source 4 Priority
rv_plic.PRIO5	0x14	4	Interrupt Source 5 Priority
rv_plic.PRIO6	0x18	4	Interrupt Source 6 Priority
rv_plic.PRIO7	0x1c	4	Interrupt Source 7 Priority
rv_plic.PRIO8	0x20	4	Interrupt Source 8 Priority
rv_plic.PRIO9	0x24	4	Interrupt Source 9 Priority
rv_plic.PRIO10	0x28	4	Interrupt Source 10 Priority
rv_plic.PRIO11	0x2c	4	Interrupt Source 11 Priority
rv_plic.PRIO12	0x30	4	Interrupt Source 12 Priority
rv_plic.PRIO13	0x34	4	Interrupt Source 13 Priority
rv_plic.PRIO14	0x38	4	Interrupt Source 14 Priority
rv_plic.PRIO15	0x3c	4	Interrupt Source 15 Priority
rv_plic.PRIO16	0x40	4	Interrupt Source 16 Priority
rv_plic.PRIO17	0x44	4	Interrupt Source 17 Priority
rv_plic.PRIO18	0x48	4	Interrupt Source 18 Priority
rv_plic.PRIO19	0x4c	4	Interrupt Source 19 Priority
rv_plic.PRIO20	0x50	4	Interrupt Source 20 Priority
rv_plic.PRIO21	0x54	4	Interrupt Source 21 Priority
rv_plic.PRIO22	0x58	4	Interrupt Source 22 Priority
rv_plic.PRIO23	0x5c	4	Interrupt Source 23 Priority
rv_plic.PRIO24	0x60	4	Interrupt Source 24 Priority
rv_plic.PRIO25	0x64	4	Interrupt Source 25 Priority
rv_plic.PRIO26	0x68	4	Interrupt Source 26 Priority
rv_plic.PRIO27	0x6c	4	Interrupt Source 27 Priority
rv_plic.PRIO28	0x70	4	Interrupt Source 28 Priority
rv_plic.PRIO29	0x74	4	Interrupt Source 29 Priority
rv_plic.PRIO30	0x78	4	Interrupt Source 30 Priority
rv_plic.PRIO31	0x7c	4	Interrupt Source 31 Priority

Name	Offset	Length	Description
rv_plic.IP	0x1000	4	Interrupt Pending
rv_plic.IE0	0x2000	4	Interrupt Enable for Target 0
rv_plic.THRESHOLD0	0x200000	4	Threshold of priority for Target 0
rv_plic.CC0	0x200004	4	Claim interrupt by read, complete interrupt by write for Target 0.
rv_plic.MSIP0	0x4000000	4	msip for Hart 0.
rv_plic.ALERT_TEST	0x4004000	4	Alert Test Register.

2.1388 PRIO0

Interrupt Source 0 Priority - Offset: `0x0` - Reset default: `0x0` - Reset mask: `0x7`

2.1388.1 Fields


```
{"reg": [{"name": "PRIO0", "bits": 3, "attr": ["rw"], "rotate": -90}, {"bits": 29}], "config":
```


Bits	Type	Reset	Name	Description
31:3				Reserved
2:0	rw	0x0	PRIO0	

2.1389 PRIO1

Interrupt Source 1 Priority - Offset: `0x4` - Reset default: `0x0` - Reset mask: `0x7`

2.1389.1 Fields


```
{"reg": [{"name": "PRIO1", "bits": 3, "attr": ["rw"], "rotate": -90}, {"bits": 29}], "config":
```


Bits	Type	Reset	Name	Description
31:3				Reserved
2:0	rw	0x0	PRIO1	

2.1390 PRIO2

Interrupt Source 2 Priority - Offset: `0x8` - Reset default: `0x0` - Reset mask: `0x7`

2.1390.1 Fields

{"reg": [{"name": "PRIO2", "bits": 3, "attr": ["rw"], "rotate": -90}, {"bits": 29}], "config":

Bits	Type	Reset	Name	Description
31:3				Reserved
2:0	rw	0x0	PRIO2	

2.1391 PRIO3

Interrupt Source 3 Priority - Offset: `0xc` - Reset default: `0x0` - Reset mask: `0x7`

2.1391.1 Fields

{"reg": [{"name": "PRIO3", "bits": 3, "attr": ["rw"], "rotate": -90}, {"bits": 29}], "config":

Bits	Type	Reset	Name	Description
31:3				Reserved
2:0	rw	0x0	PRIO3	

2.1392 PRIO4

Interrupt Source 4 Priority - Offset: `0x10` - Reset default: `0x0` - Reset mask: `0x7`

2.1392.1 Fields

{"reg": [{"name": "PRIO4", "bits": 3, "attr": ["rw"], "rotate": -90}, {"bits": 29}], "config":

Bits	Type	Reset	Name	Description
31:3				Reserved
2:0	rw	0x0	PRIO4	

2.1393 PRIO5

Interrupt Source 5 Priority - Offset: `0x14` - Reset default: `0x0` - Reset mask: `0x7`

2.1393.1 Fields

{"reg": [{"name": "PRIO5", "bits": 3, "attr": ["rw"], "rotate": -90}, {"bits": 29}], "config":

Bits	Type	Reset	Name	Description
31:3				Reserved
2:0	rw	0x0	PRIO5	

2.1394 PRIO6

Interrupt Source 6 Priority - Offset: `0x18` - Reset default: `0x0` - Reset mask: `0x7`

2.1394.1 Fields

{"reg": [{"name": "PRIO6", "bits": 3, "attr": ["rw"], "rotate": -90}, {"bits": 29}], "config":

Bits	Type	Reset	Name	Description
31:3				Reserved
2:0	rw	0x0	PRIO6	

2.1395 PRIO7

Interrupt Source 7 Priority - Offset: `0x1c` - Reset default: `0x0` - Reset mask: `0x7`

2.1395.1 Fields

{"reg": [{"name": "PRIO7", "bits": 3, "attr": ["rw"], "rotate": -90}, {"bits": 29}], "config":

Bits	Type	Reset	Name	Description
31:3				Reserved
2:0	rw	0x0	PRIO7	

2.1396 PRIO8

Interrupt Source 8 Priority - Offset: `0x20` - Reset default: `0x0` - Reset mask: `0x7`

2.1396.1 Fields

{"reg": [{"name": "PRIO8", "bits": 3, "attr": ["rw"], "rotate": -90}, {"bits": 29}], "config":

Bits	Type	Reset	Name	Description
31:3				Reserved
2:0	rw	0x0	PRIO8	

2.1397 PRIO9

Interrupt Source 9 Priority - Offset: `0x24` - Reset default: `0x0` - Reset mask: `0x7`

2.1397.1 Fields

{"reg": [{"name": "PRIO9", "bits": 3, "attr": ["rw"], "rotate": -90}, {"bits": 29}], "config":

Bits	Type	Reset	Name	Description
31:3				Reserved
2:0	rw	0x0	PRIO9	

2.1398 PRIO10

Interrupt Source 10 Priority - Offset: `0x28` - Reset default: `0x0` - Reset mask: `0x7`

2.1398.1 Fields

{"reg": [{"name": "PRIO10", "bits": 3, "attr": ["rw"], "rotate": -90}, {"bits": 29}], "config"

Bits	Type	Reset	Name	Description
31:3				Reserved
2:0	rw	0x0	PRIO10	

2.1399 PRIO11

Interrupt Source 11 Priority - Offset: `0x2c` - Reset default: `0x0` - Reset mask: `0x7`

2.1399.1 Fields

{"reg": [{"name": "PRIO11", "bits": 3, "attr": ["rw"], "rotate": -90}, {"bits": 29}], "config"

Bits	Type	Reset	Name	Description
31:3				Reserved
2:0	rw	0x0	PRIO11	

2.1400 PRIO12

Interrupt Source 12 Priority - Offset: `0x30` - Reset default: `0x0` - Reset mask: `0x7`

2.1400.1 Fields

{"reg": [{"name": "PRIO12", "bits": 3, "attr": ["rw"], "rotate": -90}, {"bits": 29}], "config"

Bits	Type	Reset	Name	Description
31:3				Reserved
2:0	rw	0x0	PRIO12	

2.1401 PRIO13

Interrupt Source 13 Priority - Offset: `0x34` - Reset default: `0x0` - Reset mask: `0x7`

2.1401.1 Fields

{"reg": [{"name": "PRIO13", "bits": 3, "attr": ["rw"], "rotate": -90}, {"bits": 29}], "config"

Bits	Type	Reset	Name	Description
31:3				Reserved
2:0	rw	0x0	PRIO13	

2.1402 PRIO14

Interrupt Source 14 Priority - Offset: `0x38` - Reset default: `0x0` - Reset mask: `0x7`

2.1402.1 Fields

{"reg": [{"name": "PRIO14", "bits": 3, "attr": ["rw"], "rotate": -90}, {"bits": 29}], "config"

Bits	Type	Reset	Name	Description
31:3				Reserved
2:0	rw	0x0	PRIO14	

2.1403 PRIO15

Interrupt Source 15 Priority - Offset: `0x3c` - Reset default: `0x0` - Reset mask: `0x7`

2.1403.1 Fields

{"reg": [{"name": "PRIO15", "bits": 3, "attr": ["rw"], "rotate": -90}, {"bits": 29}], "config"

Bits	Type	Reset	Name	Description
31:3				Reserved
2:0	rw	0x0	PRIO15	

2.1404 PRIO16

Interrupt Source 16 Priority - Offset: `0x40` - Reset default: `0x0` - Reset mask: `0x7`

2.1404.1 Fields

{"reg": [{"name": "PRIO16", "bits": 3, "attr": ["rw"], "rotate": -90}, {"bits": 29}], "config"

Bits	Type	Reset	Name	Description
31:3				Reserved
2:0	rw	0x0	PRIO16	

2.1405 PRIO17

Interrupt Source 17 Priority - Offset: `0x44` - Reset default: `0x0` - Reset mask: `0x7`

2.1405.1 Fields

{"reg": [{"name": "PRIO17", "bits": 3, "attr": ["rw"], "rotate": -90}, {"bits": 29}], "config"

Bits	Type	Reset	Name	Description
31:3				Reserved
2:0	rw	0x0	PRIO17	

2.1406 PRIO18

Interrupt Source 18 Priority - Offset: `0x48` - Reset default: `0x0` - Reset mask: `0x7`

2.1406.1 Fields

{"reg": [{"name": "PRIO18", "bits": 3, "attr": ["rw"], "rotate": -90}, {"bits": 29}], "config"

Bits	Type	Reset	Name	Description
31:3				Reserved
2:0	rw	0x0	PRIO18	

2.1407 PRIO19

Interrupt Source 19 Priority - Offset: `0x4c` - Reset default: `0x0` - Reset mask: `0x7`

2.1407.1 Fields

{"reg": [{"name": "PRIO19", "bits": 3, "attr": ["rw"], "rotate": -90}, {"bits": 29}], "config"

Bits	Type	Reset	Name	Description
31:3				Reserved
2:0	rw	0x0	PRIO19	

2.1408 PRIO20

Interrupt Source 20 Priority - Offset: `0x50` - Reset default: `0x0` - Reset mask: `0x7`

2.1408.1 Fields

{"reg": [{"name": "PRIO20", "bits": 3, "attr": ["rw"], "rotate": -90}, {"bits": 29}], "config"

Bits	Type	Reset	Name	Description
31:3				Reserved
2:0	rw	0x0	PRIO20	

2.1409 PRIO21

Interrupt Source 21 Priority - Offset: `0x54` - Reset default: `0x0` - Reset mask: `0x7`

2.1409.1 Fields

{"reg": [{"name": "PRIO21", "bits": 3, "attr": ["rw"], "rotate": -90}, {"bits": 29}], "config"

Bits	Type	Reset	Name	Description
31:3				Reserved
2:0	rw	0x0	PRIO21	

2.1410 PRIO22

Interrupt Source 22 Priority - Offset: `0x58` - Reset default: `0x0` - Reset mask: `0x7`

2.1410.1 Fields

{"reg": [{"name": "PRIO22", "bits": 3, "attr": ["rw"], "rotate": -90}, {"bits": 29}], "config"

Bits	Type	Reset	Name	Description
31:3				Reserved
2:0	rw	0x0	PRIO22	

2.1411 PRIO23

Interrupt Source 23 Priority - Offset: `0x5c` - Reset default: `0x0` - Reset mask: `0x7`

2.1411.1 Fields

{"reg": [{"name": "PRIO23", "bits": 3, "attr": ["rw"], "rotate": -90}, {"bits": 29}], "config"

Bits	Type	Reset	Name	Description
31:3				Reserved
2:0	rw	0x0	PRIO23	

2.1412 PRIO24

Interrupt Source 24 Priority - Offset: `0x60` - Reset default: `0x0` - Reset mask: `0x7`

2.1412.1 Fields

{"reg": [{"name": "PRIO24", "bits": 3, "attr": ["rw"], "rotate": -90}, {"bits": 29}], "config"

Bits	Type	Reset	Name	Description
31:3				Reserved
2:0	rw	0x0	PRIO24	

2.1413 PRIO25

Interrupt Source 25 Priority - Offset: `0x64` - Reset default: `0x0` - Reset mask: `0x7`

2.1413.1 Fields

{"reg": [{"name": "PRIO25", "bits": 3, "attr": ["rw"], "rotate": -90}, {"bits": 29}], "config"

Bits	Type	Reset	Name	Description
31:3				Reserved
2:0	rw	0x0	PRIO25	

2.1414 PRIO26

Interrupt Source 26 Priority - Offset: `0x68` - Reset default: `0x0` - Reset mask: `0x7`

2.1414.1 Fields

{"reg": [{"name": "PRIO26", "bits": 3, "attr": ["rw"], "rotate": -90}, {"bits": 29}], "config"

Bits	Type	Reset	Name	Description
31:3				Reserved
2:0	rw	0x0	PRIO26	

2.1415 PRIO27

Interrupt Source 27 Priority - Offset: `0x6c` - Reset default: `0x0` - Reset mask: `0x7`

2.1415.1 Fields

{"reg": [{"name": "PRIO27", "bits": 3, "attr": ["rw"], "rotate": -90}, {"bits": 29}], "config"

Bits	Type	Reset	Name	Description
31:3				Reserved
2:0	rw	0x0	PRIO27	

2.1416 PRIO28

Interrupt Source 28 Priority - Offset: `0x70` - Reset default: `0x0` - Reset mask: `0x7`

2.1416.1 Fields

{"reg": [{"name": "PRIO28", "bits": 3, "attr": ["rw"], "rotate": -90}, {"bits": 29}], "config"

Bits	Type	Reset	Name	Description
31:3				Reserved
2:0	rw	0x0	PRIO28	

2.1417 PRIO29

Interrupt Source 29 Priority - Offset: `0x74` - Reset default: `0x0` - Reset mask: `0x7`

2.1417.1 Fields

{"reg": [{"name": "PRIO29", "bits": 3, "attr": ["rw"], "rotate": -90}, {"bits": 29}], "config"

Bits	Type	Reset	Name	Description
31:3				Reserved
2:0	rw	0x0	PRIO29	

2.1418 PRIO30

Interrupt Source 30 Priority - Offset: `0x78` - Reset default: `0x0` - Reset mask: `0x7`

2.1418.1 Fields

{"reg": [{"name": "PRIO30", "bits": 3, "attr": ["rw"], "rotate": -90}, {"bits": 29}], "config"

Bits	Type	Reset	Name	Description
31:3				Reserved
2:0	rw	0x0	PRIO30	

2.1419 PRIO31

Interrupt Source 31 Priority - Offset: `0x7c` - Reset default: `0x0` - Reset mask: `0x7`

2.1419.1 Fields

{"reg": [{"name": "PRIO31", "bits": 3, "attr": ["rw"], "rotate": -90}, {"bits": 29}], "config"

Bits	Type	Reset	Name	Description
31:3				Reserved
2:0	rw	0x0	PRIO31	

2.1420 IP

Interrupt Pending - Offset: `0x1000` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.1420.1 Fields

{"reg": [{"name": "P_0", "bits": 1, "attr": ["ro"], "rotate": -90}, {"name": "P_1", "bits": 1,

Bits	Type	Reset	Name	Description
31	ro	0x0	P_31	Interrupt Pending of Source
30	ro	0x0	P_30	Interrupt Pending of Source
29	ro	0x0	P_29	Interrupt Pending of Source
28	ro	0x0	P_28	Interrupt Pending of Source
27	ro	0x0	P_27	Interrupt Pending of Source
26	ro	0x0	P_26	Interrupt Pending of Source
25	ro	0x0	P_25	Interrupt Pending of Source
24	ro	0x0	P_24	Interrupt Pending of Source
23	ro	0x0	P_23	Interrupt Pending of Source
22	ro	0x0	P_22	Interrupt Pending of Source
21	ro	0x0	P_21	Interrupt Pending of Source
20	ro	0x0	P_20	Interrupt Pending of Source
19	ro	0x0	P_19	Interrupt Pending of Source
18	ro	0x0	P_18	Interrupt Pending of Source
17	ro	0x0	P_17	Interrupt Pending of Source
16	ro	0x0	P_16	Interrupt Pending of Source
15	ro	0x0	P_15	Interrupt Pending of Source
14	ro	0x0	P_14	Interrupt Pending of Source
13	ro	0x0	P_13	Interrupt Pending of Source
12	ro	0x0	P_12	Interrupt Pending of Source
11	ro	0x0	P_11	Interrupt Pending of Source
10	ro	0x0	P_10	Interrupt Pending of Source
9	ro	0x0	P_9	Interrupt Pending of Source
8	ro	0x0	P_8	Interrupt Pending of Source
7	ro	0x0	P_7	Interrupt Pending of Source
6	ro	0x0	P_6	Interrupt Pending of Source
5	ro	0x0	P_5	Interrupt Pending of Source
4	ro	0x0	P_4	Interrupt Pending of Source
3	ro	0x0	P_3	Interrupt Pending of Source
2	ro	0x0	P_2	Interrupt Pending of Source
1	ro	0x0	P_1	Interrupt Pending of Source
0	ro	0x0	P_0	Interrupt Pending of Source

2.1421 IE0

Interrupt Enable for Target 0 - Offset: `0x2000` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.1421.1 Fields

{"reg": [{"name": "E_0", "bits": 1, "attr": ["rw"], "rotate": -90}, {"name": "E_1", "bits": 1,

Bits	Type	Reset	Name	Description
31	rw	0x0	E_31	Interrupt Enable of Source
30	rw	0x0	E_30	Interrupt Enable of Source
29	rw	0x0	E_29	Interrupt Enable of Source
28	rw	0x0	E_28	Interrupt Enable of Source
27	rw	0x0	E_27	Interrupt Enable of Source
26	rw	0x0	E_26	Interrupt Enable of Source
25	rw	0x0	E_25	Interrupt Enable of Source
24	rw	0x0	E_24	Interrupt Enable of Source
23	rw	0x0	E_23	Interrupt Enable of Source
22	rw	0x0	E_22	Interrupt Enable of Source
21	rw	0x0	E_21	Interrupt Enable of Source
20	rw	0x0	E_20	Interrupt Enable of Source
19	rw	0x0	E_19	Interrupt Enable of Source
18	rw	0x0	E_18	Interrupt Enable of Source
17	rw	0x0	E_17	Interrupt Enable of Source
16	rw	0x0	E_16	Interrupt Enable of Source
15	rw	0x0	E_15	Interrupt Enable of Source
14	rw	0x0	E_14	Interrupt Enable of Source
13	rw	0x0	E_13	Interrupt Enable of Source
12	rw	0x0	E_12	Interrupt Enable of Source
11	rw	0x0	E_11	Interrupt Enable of Source
10	rw	0x0	E_10	Interrupt Enable of Source
9	rw	0x0	E_9	Interrupt Enable of Source
8	rw	0x0	E_8	Interrupt Enable of Source
7	rw	0x0	E_7	Interrupt Enable of Source
6	rw	0x0	E_6	Interrupt Enable of Source
5	rw	0x0	E_5	Interrupt Enable of Source
4	rw	0x0	E_4	Interrupt Enable of Source
3	rw	0x0	E_3	Interrupt Enable of Source
2	rw	0x0	E_2	Interrupt Enable of Source
1	rw	0x0	E_1	Interrupt Enable of Source
0	rw	0x0	E_0	Interrupt Enable of Source

2.1422 THRESHOLD0

Threshold of priority for Target 0 - Offset: `0x200000` - Reset default: `0x0` - Reset mask: `0x7`

2.1422.1 Fields


```
{"reg": [{"name": "THRESHOLD0", "bits": 3, "attr": ["rw"], "rotate": -90}, {"bits": 29}], "con
```


Bits	Type	Reset	Name	Description
31:3				Reserved

Bits	Type	Reset	Name	Description
2:0	rw	0x0	THRESHOLD0	

2.1423 CC0

Claim interrupt by read, complete interrupt by write for Target 0. Value read/written is interrupt ID. Reading a value of 0 means no pending interrupts. - Offset: `0x200004` - Reset default: `0x0` - Reset mask: `0x1f`

2.1423.1 Fields


```
{"reg": [{"name": "CC0", "bits": 5, "attr": ["rw"], "rotate": 0}, {"bits": 27}], "config": {"la
```


Bits	Type	Reset	Name	Description
31:5				Reserved
4:0	rw	x	CC0	

2.1424 MSIP0

msip for Hart 0. Write 1 to here asserts software interrupt for Hart msip_o[0], write 0 to clear. - Offset: `0x4000000` - Reset default: `0x0` - Reset mask: `0x1`

2.1424.1 Fields


```
{"reg": [{"name": "MSIP0", "bits": 1, "attr": ["rw"], "rotate": -90}, {"bits": 31}], "config":
```


Bits	Type	Reset	Name	Description
31:1				Reserved
0	rw	0x0	MSIP0	Software Interrupt Pending register

2.1425 ALERT_TEST

Alert Test Register. - Offset: `0x4004000` - Reset default: `0x0` - Reset mask: `0x1`

2.1425.1 Fields


```
{"reg": [{"name": "fatal_fault", "bits": 1, "attr": ["wo"], "rotate": -90}, {"bits": 31}], "co
```

Bits	Type	Reset	Name	Description
31:1				Reserved
0	wo	x	fatal_fault	'Write 1 to trigger one alert event of this kind.'

2.1426 safety_island / doc / registers.md

2.1427 Summary

Name	Offset	Length	Description
safety_soc_ctrl.bootaddr	0x0	4	Core Boot Address
safety_soc_ctrl.fetchen	0x4	4	Core Fetch Enable
safety_soc_ctrl.corestatus	0x8	4	Core Return Status (return value, EOC)
safety_soc_ctrl.bootmode	0xc	4	Core Boot Mode

2.1428 bootaddr

Core Boot Address - Offset: `0x0` - Reset default: `0x1a000000` - Reset mask: `0xffffffff`

2.1428.1 Fields

{"reg": [{"name": "bootaddr", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1

Bits	Type	Reset	Name	Description
31:0	rw	0x1a000000	bootaddr	Boot Address

2.1429 fetchen

Core Fetch Enable - Offset: `0x4` - Reset default: `0x0` - Reset mask: `0x1`

2.1429.1 Fields

{"reg": [{"name": "fetchen", "bits": 1, "attr": ["rw"], "rotate": -90}, {"bits": 31}], "config

Bits	Type	Reset	Name	Description
31:1				Reserved
0	rw	0x0	fetchen	Fetch Enable

2.1430 corestatus

Core Return Status (return value, EOC) - Offset: `0x8` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.1430.1 Fields

{"reg": [{"name": "core_status", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes"

Bits	Type	Reset	Name	Description
31:0	rw	0x0	core_status	Core Return Status (EOC(bit[31]) and status(bit[30:0]))

2.1431 bootmode

Core Boot Mode - Offset: `0xc` - Reset default: `0x0` - Reset mask: `0x3`

2.1431.1 Fields

{"reg": [{"name": "bootmode", "bits": 2, "attr": ["rw"], "rotate": -90}, {"bits": 30}], "confi

Bits	Type	Reset	Name	Description
31:2				Reserved
1:0	rw	0x0	bootmode	Boot Mode

2.1432 serial_link / doc / registers.md

2.1433 Summary

Name	Offset	Length	Description
serial_link.CTRL	0x0	4	Global clock, isolation and reset control configuration
serial_link.ISOLATED	0x4	4	Isolation status of AXI ports
serial_link.TX_PHY_CLK_DIV_0	0x8	4	Holds clock divider factor for forwarded clock of the TX Phys
serial_link.TX_PHY_CLK_DIV_1	0xc	4	Holds clock divider factor for forwarded clock of the TX Phys
serial_link.TX_PHY_CLK_DIV_2	0x10	4	Holds clock divider factor for forwarded clock of the TX Phys
serial_link.TX_PHY_CLK_DIV_3	0x14	4	Holds clock divider factor for forwarded clock of the TX Phys

Name	Offset	Length	Description
serial_link.TX_PHY_CLK_DIV_4	0x18	4	Holds clock divider factor for forwarded clock of the TX Phys
serial_link.TX_PHY_CLK_DIV_5	0x1c	4	Holds clock divider factor for forwarded clock of the TX Phys
serial_link.TX_PHY_CLK_DIV_6	0x20	4	Holds clock divider factor for forwarded clock of the TX Phys
serial_link.TX_PHY_CLK_DIV_7	0x24	4	Holds clock divider factor for forwarded clock of the TX Phys
serial_link.TX_PHY_CLK_DIV_8	0x28	4	Holds clock divider factor for forwarded clock of the TX Phys
serial_link.TX_PHY_CLK_DIV_9	0x2c	4	Holds clock divider factor for forwarded clock of the TX Phys
serial_link.TX_PHY_CLK_DIV_10	0x30	4	Holds clock divider factor for forwarded clock of the TX Phys
serial_link.TX_PHY_CLK_DIV_11	0x34	4	Holds clock divider factor for forwarded clock of the TX Phys
serial_link.TX_PHY_CLK_DIV_12	0x38	4	Holds clock divider factor for forwarded clock of the TX Phys
serial_link.TX_PHY_CLK_DIV_13	0x3c	4	Holds clock divider factor for forwarded clock of the TX Phys
serial_link.TX_PHY_CLK_DIV_14	0x40	4	Holds clock divider factor for forwarded clock of the TX Phys
serial_link.TX_PHY_CLK_DIV_15	0x44	4	Holds clock divider factor for forwarded clock of the TX Phys
serial_link.TX_PHY_CLK_DIV_16	0x48	4	Holds clock divider factor for forwarded clock of the TX Phys
serial_link.TX_PHY_CLK_DIV_17	0x4c	4	Holds clock divider factor for forwarded clock of the TX Phys
serial_link.TX_PHY_CLK_DIV_18	0x50	4	Holds clock divider factor for forwarded clock of the TX Phys
serial_link.TX_PHY_CLK_DIV_19	0x54	4	Holds clock divider factor for forwarded clock of the TX Phys
serial_link.TX_PHY_CLK_DIV_20	0x58	4	Holds clock divider factor for forwarded clock of the TX Phys
serial_link.TX_PHY_CLK_DIV_21	0x5c	4	Holds clock divider factor for forwarded clock of the TX Phys
serial_link.TX_PHY_CLK_DIV_22	0x60	4	Holds clock divider factor for forwarded clock of the TX Phys
serial_link.TX_PHY_CLK_DIV_23	0x64	4	Holds clock divider factor for forwarded clock of the TX Phys
serial_link.TX_PHY_CLK_DIV_24	0x68	4	Holds clock divider factor for forwarded clock of the TX Phys
serial_link.TX_PHY_CLK_DIV_25	0x6c	4	Holds clock divider factor for forwarded clock of the TX Phys
serial_link.TX_PHY_CLK_DIV_26	0x70	4	Holds clock divider factor for forwarded clock of the TX Phys

Name	Offset	Length	Description
serial_link.TX_PHY_CLK_DIV_27	0x74	4	Holds clock divider factor for forwarded clock of the TX Phys
serial_link.TX_PHY_CLK_DIV_28	0x78	4	Holds clock divider factor for forwarded clock of the TX Phys
serial_link.TX_PHY_CLK_DIV_29	0x7c	4	Holds clock divider factor for forwarded clock of the TX Phys
serial_link.TX_PHY_CLK_DIV_30	0x80	4	Holds clock divider factor for forwarded clock of the TX Phys
serial_link.TX_PHY_CLK_DIV_31	0x84	4	Holds clock divider factor for forwarded clock of the TX Phys
serial_link.TX_PHY_CLK_DIV_32	0x88	4	Holds clock divider factor for forwarded clock of the TX Phys
serial_link.TX_PHY_CLK_DIV_33	0x8c	4	Holds clock divider factor for forwarded clock of the TX Phys
serial_link.TX_PHY_CLK_DIV_34	0x90	4	Holds clock divider factor for forwarded clock of the TX Phys
serial_link.TX_PHY_CLK_DIV_35	0x94	4	Holds clock divider factor for forwarded clock of the TX Phys
serial_link.TX_PHY_CLK_DIV_36	0x98	4	Holds clock divider factor for forwarded clock of the TX Phys
serial_link.TX_PHY_CLK_DIV_37	0x9c	4	Holds clock divider factor for forwarded clock of the TX Phys
serial_link.TX_PHY_CLK_START_0	0xa0	4	Controls duty cycle and phase of rising edge in TX Phys
serial_link.TX_PHY_CLK_START_1	0xa4	4	Controls duty cycle and phase of rising edge in TX Phys
serial_link.TX_PHY_CLK_START_2	0xa8	4	Controls duty cycle and phase of rising edge in TX Phys
serial_link.TX_PHY_CLK_START_3	0xac	4	Controls duty cycle and phase of rising edge in TX Phys
serial_link.TX_PHY_CLK_START_4	0xb0	4	Controls duty cycle and phase of rising edge in TX Phys
serial_link.TX_PHY_CLK_START_5	0xb4	4	Controls duty cycle and phase of rising edge in TX Phys
serial_link.TX_PHY_CLK_START_6	0xb8	4	Controls duty cycle and phase of rising edge in TX Phys
serial_link.TX_PHY_CLK_START_7	0xbc	4	Controls duty cycle and phase of rising edge in TX Phys
serial_link.TX_PHY_CLK_START_8	0xc0	4	Controls duty cycle and phase of rising edge in TX Phys
serial_link.TX_PHY_CLK_START_9	0xc4	4	Controls duty cycle and phase of rising edge in TX Phys
serial_link.TX_PHY_CLK_START_10	0xc8	4	Controls duty cycle and phase of rising edge in TX Phys
serial_link.TX_PHY_CLK_START_11	0xcc	4	Controls duty cycle and phase of rising edge in TX Phys

Name	Offset	Length	Description
serial_link.TX_PHY_CLK_START_12	0xd0	4	Controls duty cycle and phase of rising edge in TX Phys
serial_link.TX_PHY_CLK_START_13	0xd4	4	Controls duty cycle and phase of rising edge in TX Phys
serial_link.TX_PHY_CLK_START_14	0xd8	4	Controls duty cycle and phase of rising edge in TX Phys
serial_link.TX_PHY_CLK_START_15	0xdc	4	Controls duty cycle and phase of rising edge in TX Phys
serial_link.TX_PHY_CLK_START_16	0xe0	4	Controls duty cycle and phase of rising edge in TX Phys
serial_link.TX_PHY_CLK_START_17	0xe4	4	Controls duty cycle and phase of rising edge in TX Phys
serial_link.TX_PHY_CLK_START_18	0xe8	4	Controls duty cycle and phase of rising edge in TX Phys
serial_link.TX_PHY_CLK_START_19	0xec	4	Controls duty cycle and phase of rising edge in TX Phys
serial_link.TX_PHY_CLK_START_20	0xf0	4	Controls duty cycle and phase of rising edge in TX Phys
serial_link.TX_PHY_CLK_START_21	0xf4	4	Controls duty cycle and phase of rising edge in TX Phys
serial_link.TX_PHY_CLK_START_22	0xf8	4	Controls duty cycle and phase of rising edge in TX Phys
serial_link.TX_PHY_CLK_START_23	0xfc	4	Controls duty cycle and phase of rising edge in TX Phys
serial_link.TX_PHY_CLK_START_24	0x100	4	Controls duty cycle and phase of rising edge in TX Phys
serial_link.TX_PHY_CLK_START_25	0x104	4	Controls duty cycle and phase of rising edge in TX Phys
serial_link.TX_PHY_CLK_START_26	0x108	4	Controls duty cycle and phase of rising edge in TX Phys
serial_link.TX_PHY_CLK_START_27	0x10c	4	Controls duty cycle and phase of rising edge in TX Phys
serial_link.TX_PHY_CLK_START_28	0x110	4	Controls duty cycle and phase of rising edge in TX Phys
serial_link.TX_PHY_CLK_START_29	0x114	4	Controls duty cycle and phase of rising edge in TX Phys
serial_link.TX_PHY_CLK_START_30	0x118	4	Controls duty cycle and phase of rising edge in TX Phys
serial_link.TX_PHY_CLK_START_31	0x11c	4	Controls duty cycle and phase of rising edge in TX Phys
serial_link.TX_PHY_CLK_START_32	0x120	4	Controls duty cycle and phase of rising edge in TX Phys
serial_link.TX_PHY_CLK_START_33	0x124	4	Controls duty cycle and phase of rising edge in TX Phys
serial_link.TX_PHY_CLK_START_34	0x128	4	Controls duty cycle and phase of rising edge in TX Phys

Name	Offset	Length	Description
serial_link.TX_PHY_CLK_START_35	0x12c	4	Controls duty cycle and phase of rising edge in TX Phys
serial_link.TX_PHY_CLK_START_36	0x130	4	Controls duty cycle and phase of rising edge in TX Phys
serial_link.TX_PHY_CLK_START_37	0x134	4	Controls duty cycle and phase of rising edge in TX Phys
serial_link.TX_PHY_CLK_END_0	0x138	4	Controls duty cycle and phase of falling edge in TX Phys
serial_link.TX_PHY_CLK_END_1	0x13c	4	Controls duty cycle and phase of falling edge in TX Phys
serial_link.TX_PHY_CLK_END_2	0x140	4	Controls duty cycle and phase of falling edge in TX Phys
serial_link.TX_PHY_CLK_END_3	0x144	4	Controls duty cycle and phase of falling edge in TX Phys
serial_link.TX_PHY_CLK_END_4	0x148	4	Controls duty cycle and phase of falling edge in TX Phys
serial_link.TX_PHY_CLK_END_5	0x14c	4	Controls duty cycle and phase of falling edge in TX Phys
serial_link.TX_PHY_CLK_END_6	0x150	4	Controls duty cycle and phase of falling edge in TX Phys
serial_link.TX_PHY_CLK_END_7	0x154	4	Controls duty cycle and phase of falling edge in TX Phys
serial_link.TX_PHY_CLK_END_8	0x158	4	Controls duty cycle and phase of falling edge in TX Phys
serial_link.TX_PHY_CLK_END_9	0x15c	4	Controls duty cycle and phase of falling edge in TX Phys
serial_link.TX_PHY_CLK_END_10	0x160	4	Controls duty cycle and phase of falling edge in TX Phys
serial_link.TX_PHY_CLK_END_11	0x164	4	Controls duty cycle and phase of falling edge in TX Phys
serial_link.TX_PHY_CLK_END_12	0x168	4	Controls duty cycle and phase of falling edge in TX Phys
serial_link.TX_PHY_CLK_END_13	0x16c	4	Controls duty cycle and phase of falling edge in TX Phys
serial_link.TX_PHY_CLK_END_14	0x170	4	Controls duty cycle and phase of falling edge in TX Phys
serial_link.TX_PHY_CLK_END_15	0x174	4	Controls duty cycle and phase of falling edge in TX Phys
serial_link.TX_PHY_CLK_END_16	0x178	4	Controls duty cycle and phase of falling edge in TX Phys
serial_link.TX_PHY_CLK_END_17	0x17c	4	Controls duty cycle and phase of falling edge in TX Phys
serial_link.TX_PHY_CLK_END_18	0x180	4	Controls duty cycle and phase of falling edge in TX Phys
serial_link.TX_PHY_CLK_END_19	0x184	4	Controls duty cycle and phase of falling edge in TX Phys

Name	Offset	Length	Description
serial_link.TX_PHY_CLK_END_20	0x188	4	Controls duty cycle and phase of falling edge in TX Phys
serial_link.TX_PHY_CLK_END_21	0x18c	4	Controls duty cycle and phase of falling edge in TX Phys
serial_link.TX_PHY_CLK_END_22	0x190	4	Controls duty cycle and phase of falling edge in TX Phys
serial_link.TX_PHY_CLK_END_23	0x194	4	Controls duty cycle and phase of falling edge in TX Phys
serial_link.TX_PHY_CLK_END_24	0x198	4	Controls duty cycle and phase of falling edge in TX Phys
serial_link.TX_PHY_CLK_END_25	0x19c	4	Controls duty cycle and phase of falling edge in TX Phys
serial_link.TX_PHY_CLK_END_26	0x1a0	4	Controls duty cycle and phase of falling edge in TX Phys
serial_link.TX_PHY_CLK_END_27	0x1a4	4	Controls duty cycle and phase of falling edge in TX Phys
serial_link.TX_PHY_CLK_END_28	0x1a8	4	Controls duty cycle and phase of falling edge in TX Phys
serial_link.TX_PHY_CLK_END_29	0x1ac	4	Controls duty cycle and phase of falling edge in TX Phys
serial_link.TX_PHY_CLK_END_30	0x1b0	4	Controls duty cycle and phase of falling edge in TX Phys
serial_link.TX_PHY_CLK_END_31	0x1b4	4	Controls duty cycle and phase of falling edge in TX Phys
serial_link.TX_PHY_CLK_END_32	0x1b8	4	Controls duty cycle and phase of falling edge in TX Phys
serial_link.TX_PHY_CLK_END_33	0x1bc	4	Controls duty cycle and phase of falling edge in TX Phys
serial_link.TX_PHY_CLK_END_34	0x1c0	4	Controls duty cycle and phase of falling edge in TX Phys
serial_link.TX_PHY_CLK_END_35	0x1c4	4	Controls duty cycle and phase of falling edge in TX Phys
serial_link.TX_PHY_CLK_END_36	0x1c8	4	Controls duty cycle and phase of falling edge in TX Phys
serial_link.TX_PHY_CLK_END_37	0x1cc	4	Controls duty cycle and phase of falling edge in TX Phys
serial_link.RAW_MODE_EN	0x1d0	4	Enables Raw mode
serial_link.RAW_MODE_IN_CH_SEL	0x1d4	4	Receive channel select in RAW mode
serial_link.RAW_MODE_IN_DATA_VALID_0	0x1d8	4	Mask for valid data in RX FIFOs during RAW mode.
serial_link.RAW_MODE_IN_DATA_VALID_1	0x1dc	4	Mask for valid data in RX FIFOs during RAW mode.
serial_link.RAW_MODE_IN_DATA	0x1e0	4	Data received by the selected channel in RAW mode

Name	Offset	Length	Description
serial_link.RAW_MODE_OUT_CH_MASK_0	0x1e4	4	Selects channels to send out data in RAW mode, '1 corresponds to broadcasting
serial_link.RAW_MODE_OUT_CH_MASK_1	0x1e8	4	Selects channels to send out data in RAW mode, '1 corresponds to broadcasting
serial_link.RAW_MODE_OUT_DATA_FIFO	0x1ec	4	Data that will be pushed to the RAW mode output FIFO
serial_link.RAW_MODE_OUT_DATA_FIFO_CTRL	0x1f0	4	Status and control register for the RAW mode data out FIFO
serial_link.RAW_MODE_OUT_EN	0x1f4	4	Enable transmission of data currently hold in the output FIFO
serial_link.FLOW_CONTROL_FIFO_CLEAR	0x1f8	4	Clears the flow control Fifo
serial_link.CHANNEL_ALLOC_TX_CFG	0x1fc	4	Configuration settings for the TX side in the channel allocator
serial_link.CHANNEL_ALLOC_TX_CH_EN_0	0x200	4	Channel enable mask for the TX side.
serial_link.CHANNEL_ALLOC_TX_CH_EN_1	0x204	4	Channel enable mask for the TX side.
serial_link.CHANNEL_ALLOC_TX_CTRL	0x208	4	Soft clear or force flush the TX side of the channel allocator
serial_link.CHANNEL_ALLOC_RX_CFG	0x20c	4	Configuration settings for the RX side in the channel allocator
serial_link.CHANNEL_ALLOC_RX_CTRL	0x210	4	Soft clear the RX side of the channel allocator
serial_link.CHANNEL_ALLOC_RX_CH_EN_0	0x214	4	Channel enable mask for the RX side.
serial_link.CHANNEL_ALLOC_RX_CH_EN_1	0x218	4	Channel enable mask for the RX side.

2.1434 CTRL

Global clock, isolation and reset control configuration - Offset: `0x0` - Reset default: `0x302` - Reset mask: `0x303`

2.1434.1 Fields


```
{"reg": [{"name": "clk_ena", "bits": 1, "attr": ["rw"], "rotate": -90}, {"name": "reset_n", "bi
```


Bits	Type	Reset	Name	Description
31:10				Reserved
9	rw	0x1	axi_out_isolate	Isolate AXI master out port. (active-high)
8	rw	0x1	axi_in_isolate	Isolate AXI slave in port. (active-high)
7:2				Reserved
1	rw	0x1	reset_n	SW controlled synchronous reset. (active-low)
0	rw	0x0	clk_ena	Clock gate enable for network, link, physical layer. (active-high)

2.1435 ISOLATED

Isolation status of AXI ports - Offset: `0x4` - Reset default: `0x3` - Reset mask: `0x3`

2.1435.1 Fields


```
{"reg": [{"name": "axi_in", "bits": 1, "attr": ["ro"], "rotate": -90}, {"name": "axi_out", "bit
```


Bits	Type	Reset	Name	Description
31:2				Reserved
1	ro	0x1	axi_out	master out isolation status
0	ro	0x1	axi_in	slave in isolation status

2.1436 TX_PHY_CLK_DIV

Holds clock divider factor for forwarded clock of the TX Phys - Reset default: `0x8` - Reset mask: `0x7ff`

2.1436.1 Instances

Name	Offset
TX_PHY_CLK_DIV_0	0x8
TX_PHY_CLK_DIV_1	0xc
TX_PHY_CLK_DIV_2	0x10
TX_PHY_CLK_DIV_3	0x14
TX_PHY_CLK_DIV_4	0x18
TX_PHY_CLK_DIV_5	0x1c
TX_PHY_CLK_DIV_6	0x20
TX_PHY_CLK_DIV_7	0x24
TX_PHY_CLK_DIV_8	0x28
TX_PHY_CLK_DIV_9	0x2c
TX_PHY_CLK_DIV_10	0x30
TX_PHY_CLK_DIV_11	0x34
TX_PHY_CLK_DIV_12	0x38
TX_PHY_CLK_DIV_13	0x3c
TX_PHY_CLK_DIV_14	0x40
TX_PHY_CLK_DIV_15	0x44
TX_PHY_CLK_DIV_16	0x48
TX_PHY_CLK_DIV_17	0x4c
TX_PHY_CLK_DIV_18	0x50
TX_PHY_CLK_DIV_19	0x54
TX_PHY_CLK_DIV_20	0x58
TX_PHY_CLK_DIV_21	0x5c

Name	Offset
TX_PHY_CLK_DIV_22	0x60
TX_PHY_CLK_DIV_23	0x64
TX_PHY_CLK_DIV_24	0x68
TX_PHY_CLK_DIV_25	0x6c
TX_PHY_CLK_DIV_26	0x70
TX_PHY_CLK_DIV_27	0x74
TX_PHY_CLK_DIV_28	0x78
TX_PHY_CLK_DIV_29	0x7c
TX_PHY_CLK_DIV_30	0x80
TX_PHY_CLK_DIV_31	0x84
TX_PHY_CLK_DIV_32	0x88
TX_PHY_CLK_DIV_33	0x8c
TX_PHY_CLK_DIV_34	0x90
TX_PHY_CLK_DIV_35	0x94
TX_PHY_CLK_DIV_36	0x98
TX_PHY_CLK_DIV_37	0x9c

2.1436.2 Fields

{"reg": [{"name": "clk_divs", "bits": 11, "attr": ["rw"], "rotate": 0}, {"bits": 21}], "config

Bits	Type	Reset	Name	Description
31:11				Reserved
10:0	rw	0x8	clk_divs	Clock division factor of TX clock

2.1437 TX_PHY_CLK_START

Controls duty cycle and phase of rising edge in TX Phys - Reset default: `0x2` - Reset mask: `0x7ff`

2.1437.1 Instances

Name	Offset
TX_PHY_CLK_START_0	0xa0
TX_PHY_CLK_START_1	0xa4
TX_PHY_CLK_START_2	0xa8
TX_PHY_CLK_START_3	0xac
TX_PHY_CLK_START_4	0xb0
TX_PHY_CLK_START_5	0xb4
TX_PHY_CLK_START_6	0xb8
TX_PHY_CLK_START_7	0xbc
TX_PHY_CLK_START_8	0xc0

Name	Offset
TX_PHY_CLK_START_9	0xc4
TX_PHY_CLK_START_10	0xc8
TX_PHY_CLK_START_11	0xcc
TX_PHY_CLK_START_12	0xd0
TX_PHY_CLK_START_13	0xd4
TX_PHY_CLK_START_14	0xd8
TX_PHY_CLK_START_15	0xdc
TX_PHY_CLK_START_16	0xe0
TX_PHY_CLK_START_17	0xe4
TX_PHY_CLK_START_18	0xe8
TX_PHY_CLK_START_19	0xec
TX_PHY_CLK_START_20	0xf0
TX_PHY_CLK_START_21	0xf4
TX_PHY_CLK_START_22	0xf8
TX_PHY_CLK_START_23	0xfc
TX_PHY_CLK_START_24	0x100
TX_PHY_CLK_START_25	0x104
TX_PHY_CLK_START_26	0x108
TX_PHY_CLK_START_27	0x10c
TX_PHY_CLK_START_28	0x110
TX_PHY_CLK_START_29	0x114
TX_PHY_CLK_START_30	0x118
TX_PHY_CLK_START_31	0x11c
TX_PHY_CLK_START_32	0x120
TX_PHY_CLK_START_33	0x124
TX_PHY_CLK_START_34	0x128
TX_PHY_CLK_START_35	0x12c
TX_PHY_CLK_START_36	0x130
TX_PHY_CLK_START_37	0x134

2.1437.2 Fields

{"reg": [{"name": "clk_shift_start", "bits": 11, "attr": ["rw"], "rotate": 0}, {"bits": 21}], "

Bits	Type	Reset	Name	Description
31:11				Reserved
10:0	rw	0x2	clk_shift_start	Positive Edge of divided, shifted clock

2.1438 TX_PHY_CLK_END

Controls duty cycle and phase of falling edge in TX Phys - Reset default: `0x6` - Reset mask: `0x7ff`

2.1438.1 Instances

Name	Offset
TX_PHY_CLK_END_0	0x138
TX_PHY_CLK_END_1	0x13c
TX_PHY_CLK_END_2	0x140
TX_PHY_CLK_END_3	0x144
TX_PHY_CLK_END_4	0x148
TX_PHY_CLK_END_5	0x14c
TX_PHY_CLK_END_6	0x150
TX_PHY_CLK_END_7	0x154
TX_PHY_CLK_END_8	0x158
TX_PHY_CLK_END_9	0x15c
TX_PHY_CLK_END_10	0x160
TX_PHY_CLK_END_11	0x164
TX_PHY_CLK_END_12	0x168
TX_PHY_CLK_END_13	0x16c
TX_PHY_CLK_END_14	0x170
TX_PHY_CLK_END_15	0x174
TX_PHY_CLK_END_16	0x178
TX_PHY_CLK_END_17	0x17c
TX_PHY_CLK_END_18	0x180
TX_PHY_CLK_END_19	0x184
TX_PHY_CLK_END_20	0x188
TX_PHY_CLK_END_21	0x18c
TX_PHY_CLK_END_22	0x190
TX_PHY_CLK_END_23	0x194
TX_PHY_CLK_END_24	0x198
TX_PHY_CLK_END_25	0x19c
TX_PHY_CLK_END_26	0x1a0
TX_PHY_CLK_END_27	0x1a4
TX_PHY_CLK_END_28	0x1a8
TX_PHY_CLK_END_29	0x1ac
TX_PHY_CLK_END_30	0x1b0
TX_PHY_CLK_END_31	0x1b4
TX_PHY_CLK_END_32	0x1b8
TX_PHY_CLK_END_33	0x1bc
TX_PHY_CLK_END_34	0x1c0
TX_PHY_CLK_END_35	0x1c4
TX_PHY_CLK_END_36	0x1c8
TX_PHY_CLK_END_37	0x1cc

2.1438.2 Fields

{"reg": [{"name": "clk_shift_end", "bits": 11, "attr": ["rw"], "rotate": 0}, {"bits": 21}], "c

Bits	Type	Reset	Name	Description
31:11				Reserved
10:0	rw	0x6	clk_shift_end	Negative Edge of divided, shifted clock

2.1439 RAW_MODE_EN

Enables Raw mode - Offset: `0x1d0` - Reset default: `0x0` - Reset mask: `0x1`

2.1439.1 Fields

`{"reg": [{"name": "RAW_MODE_EN", "bits": 1, "attr": ["wo"], "rotate": -90}, {"bits": 31}], "co`

Bits	Type	Reset	Name	Description
31:1				Reserved
0	wo	0x0	RAW_MODE_EN	

2.1440 RAW_MODE_IN_CH_SEL

Receive channel select in RAW mode - Offset: `0x1d4` - Reset default: `0x0` - Reset mask: `0x3f`

2.1440.1 Fields

`{"reg": [{"name": "RAW_MODE_IN_CH_SEL", "bits": 6, "attr": ["wo"], "rotate": -90}, {"bits": 26`

Bits	Type	Reset	Name	Description
31:6				Reserved
5:0	wo	0x0	RAW_MODE_IN_CH_SEL	

2.1441 RAW_MODE_IN_DATA_VALID_0

Mask for valid data in RX FIFOs during RAW mode. - Offset: `0x1d8` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.1441.1 Fields

`{"reg": [{"name": "RAW_MODE_IN_DATA_VALID_0", "bits": 1, "attr": ["ro"], "rotate": -90}, {"name`

Bits	Type	Reset	Name	Description
31	ro	x	RAW_MODE_IN_DATA_VALID_31	
30	ro	x	RAW_MODE_IN_DATA_VALID_30	
29	ro	x	RAW_MODE_IN_DATA_VALID_29	
28	ro	x	RAW_MODE_IN_DATA_VALID_28	
27	ro	x	RAW_MODE_IN_DATA_VALID_27	
26	ro	x	RAW_MODE_IN_DATA_VALID_26	
25	ro	x	RAW_MODE_IN_DATA_VALID_25	
24	ro	x	RAW_MODE_IN_DATA_VALID_24	
23	ro	x	RAW_MODE_IN_DATA_VALID_23	
22	ro	x	RAW_MODE_IN_DATA_VALID_22	
21	ro	x	RAW_MODE_IN_DATA_VALID_21	
20	ro	x	RAW_MODE_IN_DATA_VALID_20	
19	ro	x	RAW_MODE_IN_DATA_VALID_19	
18	ro	x	RAW_MODE_IN_DATA_VALID_18	
17	ro	x	RAW_MODE_IN_DATA_VALID_17	
16	ro	x	RAW_MODE_IN_DATA_VALID_16	
15	ro	x	RAW_MODE_IN_DATA_VALID_15	
14	ro	x	RAW_MODE_IN_DATA_VALID_14	
13	ro	x	RAW_MODE_IN_DATA_VALID_13	
12	ro	x	RAW_MODE_IN_DATA_VALID_12	
11	ro	x	RAW_MODE_IN_DATA_VALID_11	
10	ro	x	RAW_MODE_IN_DATA_VALID_10	
9	ro	x	RAW_MODE_IN_DATA_VALID_9	
8	ro	x	RAW_MODE_IN_DATA_VALID_8	
7	ro	x	RAW_MODE_IN_DATA_VALID_7	
6	ro	x	RAW_MODE_IN_DATA_VALID_6	
5	ro	x	RAW_MODE_IN_DATA_VALID_5	
4	ro	x	RAW_MODE_IN_DATA_VALID_4	
3	ro	x	RAW_MODE_IN_DATA_VALID_3	
2	ro	x	RAW_MODE_IN_DATA_VALID_2	
1	ro	x	RAW_MODE_IN_DATA_VALID_1	
0	ro	x	RAW_MODE_IN_DATA_VALID_0	

2.1442 RAW_MODE_IN_DATA_VALID_1

Mask for valid data in RX FIFOs during RAW mode. - Offset: `0x1dc` - Reset default: `0x0` - Reset mask: `0x3f`

2.1442.1 Fields

{"reg": [{"name": "RAW_MODE_IN_DATA_VALID_32", "bits": 1, "attr": ["ro"], "rotate": -90}, {"nar

Bits	Type	Reset	Name	Description
31:6				Reserved
5	ro	x	RAW_MODE_IN_DATA_VALID_37	RAW_MODE_IN_DATA_VALID1
4	ro	x	RAW_MODE_IN_DATA_VALID_36	RAW_MODE_IN_DATA_VALID1
3	ro	x	RAW_MODE_IN_DATA_VALID_35	RAW_MODE_IN_DATA_VALID1
2	ro	x	RAW_MODE_IN_DATA_VALID_34	RAW_MODE_IN_DATA_VALID1
1	ro	x	RAW_MODE_IN_DATA_VALID_33	RAW_MODE_IN_DATA_VALID1
0	ro	x	RAW_MODE_IN_DATA_VALID_32	RAW_MODE_IN_DATA_VALID1

2.1443 RAW_MODE_IN_DATA

Data received by the selected channel in RAW mode - Offset: `0x1e0` - Reset default: `0x0` - Reset mask: `0xffff`

2.1443.1 Fields


```
{"reg": [{"name": "RAW_MODE_IN_DATA", "bits": 16, "attr": ["ro"], "rotate": 0}, {"bits": 16}],
```


Bits	Type	Reset	Name	Description
31:16				Reserved
15:0	ro	x	RAW_MODE_IN_DATA	

2.1444 RAW_MODE_OUT_CH_MASK_0

Selects channels to send out data in RAW mode, '1 corresponds to broadcasting - Offset: `0x1e4` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.1444.1 Fields


```
{"reg": [{"name": "RAW_MODE_OUT_CH_MASK_0", "bits": 1, "attr": ["wo"], "rotate": -90}, {"name"
```


Bits	Type	Reset	Name	Description
31	wo	0x0	RAW_MODE_OUT_CH_MASK_31	
30	wo	0x0	RAW_MODE_OUT_CH_MASK_30	
29	wo	0x0	RAW_MODE_OUT_CH_MASK_29	

Bits	Type	Reset	Name	Description
28	wo	0x0	RAW_MODE_OUT_CH_MASK_28	
27	wo	0x0	RAW_MODE_OUT_CH_MASK_27	
26	wo	0x0	RAW_MODE_OUT_CH_MASK_26	
25	wo	0x0	RAW_MODE_OUT_CH_MASK_25	
24	wo	0x0	RAW_MODE_OUT_CH_MASK_24	
23	wo	0x0	RAW_MODE_OUT_CH_MASK_23	
22	wo	0x0	RAW_MODE_OUT_CH_MASK_22	
21	wo	0x0	RAW_MODE_OUT_CH_MASK_21	
20	wo	0x0	RAW_MODE_OUT_CH_MASK_20	
19	wo	0x0	RAW_MODE_OUT_CH_MASK_19	
18	wo	0x0	RAW_MODE_OUT_CH_MASK_18	
17	wo	0x0	RAW_MODE_OUT_CH_MASK_17	
16	wo	0x0	RAW_MODE_OUT_CH_MASK_16	
15	wo	0x0	RAW_MODE_OUT_CH_MASK_15	
14	wo	0x0	RAW_MODE_OUT_CH_MASK_14	
13	wo	0x0	RAW_MODE_OUT_CH_MASK_13	
12	wo	0x0	RAW_MODE_OUT_CH_MASK_12	
11	wo	0x0	RAW_MODE_OUT_CH_MASK_11	
10	wo	0x0	RAW_MODE_OUT_CH_MASK_10	
9	wo	0x0	RAW_MODE_OUT_CH_MASK_9	
8	wo	0x0	RAW_MODE_OUT_CH_MASK_8	
7	wo	0x0	RAW_MODE_OUT_CH_MASK_7	
6	wo	0x0	RAW_MODE_OUT_CH_MASK_6	
5	wo	0x0	RAW_MODE_OUT_CH_MASK_5	
4	wo	0x0	RAW_MODE_OUT_CH_MASK_4	
3	wo	0x0	RAW_MODE_OUT_CH_MASK_3	
2	wo	0x0	RAW_MODE_OUT_CH_MASK_2	
1	wo	0x0	RAW_MODE_OUT_CH_MASK_1	
0	wo	0x0	RAW_MODE_OUT_CH_MASK_0	

2.1445 RAW_MODE_OUT_CH_MASK_1

Selects channels to send out data in RAW mode, '1 corresponds to broadcasting - Offset: `0x1e8` - Reset default: `0x0` - Reset mask: `0x3f`

2.1445.1 Fields

`{"reg": [{"name": "RAW_MODE_OUT_CH_MASK_32", "bits": 1, "attr": ["wo"], "rotate": -90}, {"name"`

Bits	Type	Reset	Name	Description
31:6				Reserved
5	wo	0x0	RAW_MODE_OUT_CH_MASK_37	RAW_MODE_OUT_CH_MASK1

Bits	Type	Reset	Name	Description
4	wo	0x0	RAW_MODE_OUT_CH_MASK_36	Mask RAW_MODE_OUT_CH_MASK1
3	wo	0x0	RAW_MODE_OUT_CH_MASK_35	Mask RAW_MODE_OUT_CH_MASK1
2	wo	0x0	RAW_MODE_OUT_CH_MASK_34	Mask RAW_MODE_OUT_CH_MASK1
1	wo	0x0	RAW_MODE_OUT_CH_MASK_33	Mask RAW_MODE_OUT_CH_MASK1
0	wo	0x0	RAW_MODE_OUT_CH_MASK_32	Mask RAW_MODE_OUT_CH_MASK1

2.1446 RAW_MODE_OUT_DATA_FIFO

Data that will be pushed to the RAW mode output FIFO - Offset: `0x1ec` - Reset default: `0x0` - Reset mask: `0xffff`

2.1446.1 Fields


```
{"reg": [{"name": "RAW_MODE_OUT_DATA_FIFO", "bits": 16, "attr": ["wo"], "rotate": 0}, {"bits":
```


Bits	Type	Reset	Name	Description
31:16				Reserved
15:0	wo	0x0	RAW_MODE_OUT_DATA_FIFO	

2.1447 RAW_MODE_OUT_DATA_FIFO_CTRL

Status and control register for the RAW mode data out FIFO - Offset: `0x1f0` - Reset default: `0x0` - Reset mask: `0x80000701`

2.1447.1 Fields


```
{"reg": [{"name": "clear", "bits": 1, "attr": ["wo"], "rotate": -90}, {"bits": 7}, {"name": "f
```


Bits	Type	Reset	Name	Description
31	ro	0x0	is_full	If '1' the FIFO is full and does not accept any more items. Any additional write to the data fill register will be ignored until there is sufficient space again.
30:11				Reserved
10:8	ro	0x0	fill_state	The number of elements currently stored in the RAW mode TX FIFO that are ready to be sent.

Bits	Type	Reset	Name	Description
7:1				Reserved
0	wo	x	clear	Clears the raw mode TX FIFO.

2.1448 RAW_MODE_OUT_EN

Enable transmission of data currently hold in the output FIFO - Offset: `0x1f4` - Reset default: `0x0` - Reset mask: `0x1`

2.1448.1 Fields


```
{"reg": [{"name": "RAW_MODE_OUT_EN", "bits": 1, "attr": ["rw"], "rotate": -90}, {"bits": 31}],
```


Bits	Type	Reset	Name	Description
31:1				Reserved
0	rw	0x0	RAW_MODE_OUT_EN	

2.1449 FLOW_CONTROL_FIFO_CLEAR

Clears the flow control Fifo - Offset: `0x1f8` - Reset default: `0x0` - Reset mask: `0x1`

2.1449.1 Fields


```
{"reg": [{"name": "FLOW_CONTROL_FIFO_CLEAR", "bits": 1, "attr": ["wo"], "rotate": -90}, {"bits"
```


Bits	Type	Reset	Name	Description
31:1				Reserved
0	wo	0x0	FLOW_CONTROL_FIFO_CLEAR	

2.1450 CHANNEL_ALLOC_TX_CFG

Configuration settings for the TX side in the channel allocator - Offset: `0x1fc` - Reset default: `0x203` - Reset mask: `0xff03`

2.1450.1 Fields


```
{"reg": [{"name": "bypass_en", "bits": 1, "attr": ["rw"], "rotate": -90}, {"name": "auto_flush
```

Bits	Type	Reset	Name	Description
31:16				Reserved
15:8	rw	0x2	auto_flush_cou	The number of cycles to wait before auto flushing (sending) packets in the channel allocator
7:2				Reserved
1	rw	0x1	auto_flush_en	Enable the auto-flush feature of the TX side in the channel allocator
0	rw	0x1	bypass_en	Enable bypassing the TX channel allocator

2.1451 CHANNEL_ALLOC_TX_CH_EN_0

Channel enable mask for the TX side. - Offset: `0x200` - Reset default: `0xffffffff` - Reset mask: `0xffffffff`

2.1451.1 Fields

`{"reg": [{"name": "CHANNEL_ALLOC_TX_CH_EN_0", "bits": 1, "attr": ["rw"], "rotate": -90}, {"name`

Bits	Type	Reset	Name	Description
31	rw	0x1	CHANNEL_ALLOC_TX_CH_EN_31	
30	rw	0x1	CHANNEL_ALLOC_TX_CH_EN_30	
29	rw	0x1	CHANNEL_ALLOC_TX_CH_EN_29	
28	rw	0x1	CHANNEL_ALLOC_TX_CH_EN_28	
27	rw	0x1	CHANNEL_ALLOC_TX_CH_EN_27	
26	rw	0x1	CHANNEL_ALLOC_TX_CH_EN_26	
25	rw	0x1	CHANNEL_ALLOC_TX_CH_EN_25	
24	rw	0x1	CHANNEL_ALLOC_TX_CH_EN_24	
23	rw	0x1	CHANNEL_ALLOC_TX_CH_EN_23	
22	rw	0x1	CHANNEL_ALLOC_TX_CH_EN_22	
21	rw	0x1	CHANNEL_ALLOC_TX_CH_EN_21	
20	rw	0x1	CHANNEL_ALLOC_TX_CH_EN_20	
19	rw	0x1	CHANNEL_ALLOC_TX_CH_EN_19	
18	rw	0x1	CHANNEL_ALLOC_TX_CH_EN_18	
17	rw	0x1	CHANNEL_ALLOC_TX_CH_EN_17	
16	rw	0x1	CHANNEL_ALLOC_TX_CH_EN_16	
15	rw	0x1	CHANNEL_ALLOC_TX_CH_EN_15	
14	rw	0x1	CHANNEL_ALLOC_TX_CH_EN_14	
13	rw	0x1	CHANNEL_ALLOC_TX_CH_EN_13	
12	rw	0x1	CHANNEL_ALLOC_TX_CH_EN_12	
11	rw	0x1	CHANNEL_ALLOC_TX_CH_EN_11	
10	rw	0x1	CHANNEL_ALLOC_TX_CH_EN_10	
9	rw	0x1	CHANNEL_ALLOC_TX_CH_EN_9	
8	rw	0x1	CHANNEL_ALLOC_TX_CH_EN_8	
7	rw	0x1	CHANNEL_ALLOC_TX_CH_EN_7	

Bits	Type	Reset	Name	Description
6	rw	0x1	CHANNEL_ALLOC_TX_CH_EN_6	
5	rw	0x1	CHANNEL_ALLOC_TX_CH_EN_5	
4	rw	0x1	CHANNEL_ALLOC_TX_CH_EN_4	
3	rw	0x1	CHANNEL_ALLOC_TX_CH_EN_3	
2	rw	0x1	CHANNEL_ALLOC_TX_CH_EN_2	
1	rw	0x1	CHANNEL_ALLOC_TX_CH_EN_1	
0	rw	0x1	CHANNEL_ALLOC_TX_CH_EN_0	

2.1452 CHANNEL_ALLOC_TX_CH_EN_1

Channel enable mask for the TX side. - Offset: `0x204` - Reset default: `0x3f` - Reset mask: `0x3f`

2.1452.1 Fields


```
{"reg": [{"name": "CHANNEL_ALLOC_TX_CH_EN_32", "bits": 1, "attr": ["rw"], "rotate": -90}, {"nam
```


Bits	Type	Reset	Name	Description
31:6				Reserved
5	rw	0x1	CHANNEL_ALLOC_TX_CH_EN_37	FEN CHAN-NEL_ALLOC_TX_CH_EN1
4	rw	0x1	CHANNEL_ALLOC_TX_CH_EN_36	FEN CHAN-NEL_ALLOC_TX_CH_EN1
3	rw	0x1	CHANNEL_ALLOC_TX_CH_EN_35	FEN CHAN-NEL_ALLOC_TX_CH_EN1
2	rw	0x1	CHANNEL_ALLOC_TX_CH_EN_34	FEN CHAN-NEL_ALLOC_TX_CH_EN1
1	rw	0x1	CHANNEL_ALLOC_TX_CH_EN_33	FEN CHAN-NEL_ALLOC_TX_CH_EN1
0	rw	0x1	CHANNEL_ALLOC_TX_CH_EN_32	FEN CHAN-NEL_ALLOC_TX_CH_EN1

2.1453 CHANNEL_ALLOC_TX_CTRL

Soft clear or force flush the TX side of the channel allocator - Offset: `0x208` - Reset default: `0x0` - Reset mask: `0x3`

2.1453.1 Fields


```
{"reg": [{"name": "clear", "bits": 1, "attr": ["wo"], "rotate": -90}, {"name": "flush", "bits"
```

Bits	Type	Reset	Name	Description
31:2				Reserved
1	wo	x	flush	Flush (transmit remaining data) in the TX side of the channel allocator.
0	wo	x	clear	Software clear the TX side of the channel allocator

2.1454 CHANNEL_ALLOC_RX_CFG

Configuration settings for the RX side in the channel allocator - Offset: `0x20c` - Reset default: `0x10203` - Reset mask: `0x1ff03`

2.1454.1 Fields

`{"reg": [{"name": "bypass_en", "bits": 1, "attr": ["rw"], "rotate": -90}, {"name": "auto_flush_`

Bits	Type	Reset	Name	Description
31:17				Reserved
16	rw	0x1	sync_en	Enable (1) or disable (0) the synchronization barrier between the channels (needs to be disabled in raw mode).
15:8	rw	0x2	auto_flush_count	The number of cycles to wait before synchronizing on partial packets on the RX side
7:2				Reserved
1	rw	0x1	auto_flush_en	Enable the auto-flush feature of the RX side in the channel allocator
0	rw	0x1	bypass_en	Enable bypassing the RX channel allocator

2.1455 CHANNEL_ALLOC_RX_CTRL

Soft clear the RX side of the channel allocator - Offset: `0x210` - Reset default: `0x0` - Reset mask: `0x1`

2.1455.1 Fields

`{"reg": [{"name": "clear", "bits": 1, "attr": ["wo"], "rotate": -90}, {"bits": 31}], "config":`

Bits	Type	Reset	Name	Description
31:1				Reserved
0	wo	x	clear	Software clear the TX side of the channel allocator

2.1456 CHANNEL_ALLOC_RX_CH_EN_0

Channel enable mask for the RX side. - Offset: `0x214` - Reset default: `0xffffffff` - Reset mask: `0xffffffff`

2.1456.1 Fields

{"reg": [{"name": "CHANNEL_ALLOC_RX_CH_EN_0", "bits": 1, "attr": ["rw"], "rotate": -90}, {"name

Bits	Type	Reset	Name	Description
31	rw	0x1	CHANNEL_ALLOC_RX_CH_EN_31	
30	rw	0x1	CHANNEL_ALLOC_RX_CH_EN_30	
29	rw	0x1	CHANNEL_ALLOC_RX_CH_EN_29	
28	rw	0x1	CHANNEL_ALLOC_RX_CH_EN_28	
27	rw	0x1	CHANNEL_ALLOC_RX_CH_EN_27	
26	rw	0x1	CHANNEL_ALLOC_RX_CH_EN_26	
25	rw	0x1	CHANNEL_ALLOC_RX_CH_EN_25	
24	rw	0x1	CHANNEL_ALLOC_RX_CH_EN_24	
23	rw	0x1	CHANNEL_ALLOC_RX_CH_EN_23	
22	rw	0x1	CHANNEL_ALLOC_RX_CH_EN_22	
21	rw	0x1	CHANNEL_ALLOC_RX_CH_EN_21	
20	rw	0x1	CHANNEL_ALLOC_RX_CH_EN_20	
19	rw	0x1	CHANNEL_ALLOC_RX_CH_EN_19	
18	rw	0x1	CHANNEL_ALLOC_RX_CH_EN_18	
17	rw	0x1	CHANNEL_ALLOC_RX_CH_EN_17	
16	rw	0x1	CHANNEL_ALLOC_RX_CH_EN_16	
15	rw	0x1	CHANNEL_ALLOC_RX_CH_EN_15	
14	rw	0x1	CHANNEL_ALLOC_RX_CH_EN_14	
13	rw	0x1	CHANNEL_ALLOC_RX_CH_EN_13	
12	rw	0x1	CHANNEL_ALLOC_RX_CH_EN_12	
11	rw	0x1	CHANNEL_ALLOC_RX_CH_EN_11	
10	rw	0x1	CHANNEL_ALLOC_RX_CH_EN_10	
9	rw	0x1	CHANNEL_ALLOC_RX_CH_EN_9	
8	rw	0x1	CHANNEL_ALLOC_RX_CH_EN_8	
7	rw	0x1	CHANNEL_ALLOC_RX_CH_EN_7	
6	rw	0x1	CHANNEL_ALLOC_RX_CH_EN_6	
5	rw	0x1	CHANNEL_ALLOC_RX_CH_EN_5	
4	rw	0x1	CHANNEL_ALLOC_RX_CH_EN_4	
3	rw	0x1	CHANNEL_ALLOC_RX_CH_EN_3	
2	rw	0x1	CHANNEL_ALLOC_RX_CH_EN_2	
1	rw	0x1	CHANNEL_ALLOC_RX_CH_EN_1	
0	rw	0x1	CHANNEL_ALLOC_RX_CH_EN_0	

2.1457 CHANNEL_ALLOC_RX_CH_EN_1

Channel enable mask for the RX side. - Offset: `0x218` - Reset default: `0x3f` - Reset mask: `0x3f`

2.1457.1 Fields

{"reg": [{"name": "CHANNEL_ALLOC_RX_CH_EN_32", "bits": 1, "attr": ["rw"], "rotate": -90}, {"na

Bits	Type	Reset	Name	Description
31:6				Reserved
5	rw	0x1	CHANNEL_ALLOC_RX_CH_EN_37	CHANNEL_ALLOC_RX_CH_EN1
4	rw	0x1	CHANNEL_ALLOC_RX_CH_EN_36	CHANNEL_ALLOC_RX_CH_EN1
3	rw	0x1	CHANNEL_ALLOC_RX_CH_EN_35	CHANNEL_ALLOC_RX_CH_EN1
2	rw	0x1	CHANNEL_ALLOC_RX_CH_EN_34	CHANNEL_ALLOC_RX_CH_EN1
1	rw	0x1	CHANNEL_ALLOC_RX_CH_EN_33	CHANNEL_ALLOC_RX_CH_EN1
0	rw	0x1	CHANNEL_ALLOC_RX_CH_EN_32	CHANNEL_ALLOC_RX_CH_EN1

2.1458 spim / doc / registers.md

2.1459 Summary

Name	Offset	Length	Description
spi_host.INTR_STATE	0x0	4	Interrupt State Register
spi_host.INTR_ENABLE	0x4	4	Interrupt Enable Register
spi_host.INTR_TEST	0x8	4	Interrupt Test Register
spi_host.ALERT_TEST	0xc	4	Alert Test Register
spi_host.CONTROL	0x10	4	Control register
spi_host.STATUS	0x14	4	Status register
spi_host.CONFIGOPTS	0x18	4	Configuration options register.
spi_host.CSID	0x1c	4	Chip-Select ID
spi_host.COMMAND	0x20	4	Command Register
spi_host.RXDATA	0x24	4	SPI Receive Data.
spi_host.TXDATA	0x28	4	SPI Transmit Data.
spi_host.ERROR_ENABLE	0x2c	4	Controls which classes of errors raise an interrupt.
spi_host.ERROR_STATUS	0x30	4	Indicates that any errors that have occurred.
spi_host.EVENT_ENABLE	0x34	4	Controls which classes of SPI events raise an interrupt.

2.1460 INTR_STATE

Interrupt State Register - Offset: `0x0` - Reset default: `0x0` - Reset mask: `0x3`

2.1460.1 Fields

{"reg": [{"name": "error", "bits": 1, "attr": ["rw1c"], "rotate": -90}, {"name": "spi_event", "

Bits	Type	Reset	Name	Description
31:2				Reserved
1	ro	0x0	spi_event	Event-related interrupts, see EVENT_ENABLE register for more information.
0	rw1c	0x0	error	Error-related interrupts, see ERROR_ENABLE register for more information.

2.1461 INTR_ENABLE

Interrupt Enable Register - Offset: 0x4 - Reset default: 0x0 - Reset mask: 0x3

2.1461.1 Fields

{"reg": [{"name": "error", "bits": 1, "attr": ["rw"], "rotate": -90}, {"name": "spi_event", "bi

Bits	Type	Reset	Name	Description
31:2				Reserved
1	rw	0x0	spi_event	Enable interrupt when INTR_STATE.spi_event is set.
0	rw	0x0	error	Enable interrupt when INTR_STATE.error is set.

2.1462 INTR_TEST

Interrupt Test Register - Offset: 0x8 - Reset default: 0x0 - Reset mask: 0x3

2.1462.1 Fields

{"reg": [{"name": "error", "bits": 1, "attr": ["wo"], "rotate": -90}, {"name": "spi_event", "bi

Bits	Type	Reset	Name	Description
31:2				Reserved
1	wo	0x0	spi_event	Write 1 to force INTR_STATE.spi_event to 1.
0	wo	0x0	error	Write 1 to force INTR_STATE.error to 1.

2.1463 ALERT_TEST

Alert Test Register - Offset: 0xc - Reset default: 0x0 - Reset mask: 0x1

2.1463.1 Fields

{"reg": [{"name": "fatal_fault", "bits": 1, "attr": ["wo"], "rotate": -90}, {"bits": 31}], "co

Bits	Type	Reset	Name	Description
31:1				Reserved
0	wo	0x0	fatal_fault	Write 1 to trigger one alert event of this kind.

2.1464 CONTROL

Control register - Offset: `0x10` - Reset default: `0x7f` - Reset mask: `0xe000ffff`

2.1464.1 Fields

{"reg": [{"name": "RX_WATERMARK", "bits": 8, "attr": ["rw"], "rotate": 0}, {"name": "TX_WATERM

Bits	Type	Reset	Name
31	rw	0x0	SPIEN
30	rw	0x0	SW_RST
29	rw	0x0	OUTPUT_EN
28:16			Reserved
15:8	rw	0x0	TX_WATERMARK
7:0	rw	0x7f	RX_WATERMARK

2.1464.2 CONTROL . SPIEN

Enables the SPI host. On reset, this field is 0, meaning that no transactions can proceed.

2.1464.3 CONTROL . SW_RST

Clears the internal state (not registers) to the reset state when set to 1, including the FIFOs, the CDC's, the core state machine and the shift register. In the current implementation, the CDC FIFOs are drained not reset. Therefore software must confirm that both FIFO's empty before releasing the IP from reset.

2.1464.4 CONTROL . OUTPUT_EN

Enable the SPI host output buffers for the sck, csb, and sd lines. This allows the SPI_HOST IP to connect to the same bus as other SPI controllers without interference.

2.1464.5 CONTROL . TX_WATERMARK

If EVENT_ENABLE.TXWM is set, the IP will send an interrupt when the depth of the TX FIFO drops below TX_WATERMARK words (32b each).

2.1464.6 CONTROL . RX_WATERMARK

If EVENT_ENABLE.RXWM is set, the IP will send an interrupt when the depth of the RX FIFO reaches RX_WATERMARK words (32b each).

2.1465 STATUS

Status register - Offset: 0x14 - Reset default: 0x0 - Reset mask: 0xffdfffff

2.1465.1 Fields

{"reg": [{"name": "TXQD", "bits": 8, "attr": ["ro"], "rotate": 0}, {"name": "RXQD", "bits": 8,

Bits	Type	Reset	Name	Description
31	ro	0x0	READY	When high, indicates the SPI host is ready to receive commands. Writing to COMMAND when READY is low is an error, and will trigger an interrupt.
30	ro	0x0	ACTIVE	When high, indicates the SPI host is processing a previously issued command.
29	ro	0x0	TXFULL	When high, indicates that the transmit data fifo is full. Any further writes to TXDATA will create an error interrupt.
28	ro	0x0	TXEMPTY	When high, indicates that the transmit data fifo is empty.
27	ro	0x0	TXSTALL	If high, signifies that an ongoing transaction has stalled due to lack of data in the TX FIFO
26	ro	0x0	TXWM	If high, the amount of data in the TX FIFO has fallen below the level of CONTROL.TX_WATERMARK words (32b each).
25	ro	0x0	RXFULL	When high, indicates that the receive fifo is full. Any ongoing transactions will stall until firmware reads some data from RXDATA.
24	ro	0x0	RXEMPTY	When high, indicates that the receive fifo is empty. Any reads from RX FIFO will cause an error interrupt.
23	ro	0x0	RXSTALL	If high, signifies that an ongoing transaction has stalled due to lack of available space in the RX FIFO
22	ro	0x0	BYTEORDER	The value of the ByteOrder parameter, provided so that firmware can confirm proper IP configuration.
21				Reserved
20	ro	0x0	RXWM	If high, the number of 32-bits in the RX FIFO now exceeds the CONTROL.RX_WATERMARK entries (32b each).
19:16	ro	0x0	CMDQD	Command queue depth. Indicates how many unread 32-bit words are currently in the command segment queue.

Bits	Type	Reset	Name	Description
15:8	ro	0x0	RXQD	Receive queue depth. Indicates how many unread 32-bit words are currently in the RX FIFO. When active, this result may an underestimate due to synchronization delays.
7:0	ro	0x0	TXQD	Transmit queue depth. Indicates how many unsent 32-bit words are currently in the TX FIFO. When active, this result may be an overestimate due to synchronization delays.

2.1466 CONFIGOPTS

Configuration options register.

Contains options for controlling the current peripheral. Firmware needs to configure the options before the transfer. - Offset: `0x18` - Reset default: `0x0` - Reset mask: `0xeffffffff`

2.1466.1 Fields

{"reg": [{"name": "CLKDIV", "bits": 16, "attr": ["rw"], "rotate": 0}, {"name": "CSNIDLE", "bits

Bits	Type	Reset	Name
31	rw	0x0	CPOL
30	rw	0x0	CPHA
29	rw	0x0	FULLCYC
28			Reserved
27:24	rw	0x0	CSNLEAD
23:20	rw	0x0	CSNTRAIL
19:16	rw	0x0	CSNIDLE
15:0	rw	0x0	CLKDIV

2.1466.2 CONFIGOPTS . CPOL

The polarity of the sck clock signal. When CPOL is 0, sck is low when idle, and emits high pulses. When CPOL is 1, sck is high when idle, and emits a series of low pulses.

2.1466.3 CONFIGOPTS . CPHA

The phase of the sck clock signal relative to the data. When CPHA = 0, the data changes on the trailing edge of sck and is typically sampled on the leading edge. Conversely if CPHA = 1 high, data lines change on the leading edge of sck and are typically sampled on the trailing edge. CPHA should be chosen to match the phase of the selected device. The sampling behavior is modified by the `CONFIGOPTS.FULLCYC` bit.

2.1466.4 CONFIGOPTS . FULLCYC

Full cycle. Modifies the CPHA sampling behaviour to allow for longer device logic setup times. Rather than sampling the SD bus a half cycle after shifting out data, the data is sampled a full cycle after shifting data out. This means that if CPHA = 0, data is shifted out on the trailing edge, and sampled a full cycle later. If CPHA = 1, data is shifted and sampled with the trailing edge, also separated by a full cycle.

2.1466.5 CONFIGOPTS . CSNLEAD

CS_N Leading Time. Indicates the number of half sck cycles, CSNLEAD+1, to leave between the falling edge of cs_n and the first edge of sck. Setting this register to zero corresponds to the minimum delay of one-half sck cycle

2.1466.6 CONFIGOPTS . CSNTRAIL

CS_N Trailing Time. Indicates the number of half sck cycles, CSNTRAIL+1, to leave between last edge of sck and the rising edge of cs_n. Setting this register to zero corresponds to the minimum delay of one-half sck cycle.

2.1466.7 CONFIGOPTS . CSNIDLE

Minimum idle time between commands. Indicates the minimum number of sck half-cycles to hold cs_n high between commands. Setting this register to zero creates a minimally-wide CS_N-high pulse of one-half sck cycle.

2.1466.8 CONFIGOPTS . CLKDIV

Core clock divider. Slows down subsequent SPI transactions by a factor of (CLKDIV+1) relative to the core clock frequency. The period of sck, T(sck) then becomes `2*(CLK_DIV+1)*T(core)`

2.1467 CSID

Chip-Select ID

Controls which device to target with the next command. This register is passed to the core whenever `COMMAND` is written. The core then asserts cio_csb_o[`CSID`] during the execution of the command. - Offset: `0x1c` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.1467.1 Fields

{"reg": [{"name": "CSID", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "f

Bits	Type	Reset	Name	Description
31:0	rw	0x0	CSID	Chip Select ID

2.1468 COMMAND

Command Register

Parameters specific to each command segment. Unlike the CONFIGOPTS multi-register, there is only one command register for controlling all attached SPI devices - Offset: 0x20 - Reset default: 0x0 - Reset mask: 0x1fffffff

2.1468.1 Fields

{"reg": [{"name": "CSAAT", "bits": 1, "attr": ["wo"], "rotate": -90}, {"name": "SPEED", "bits"

Bits	Type	Reset	Name
31:25			Reserved
24:5	wo	0x0	LEN
4:3	wo	0x0	DIRECTION
2:1	wo	0x0	SPEED
0	wo	0x0	CSAAT

2.1468.2 COMMAND . LEN

Segment Length.

For read or write segments, this field controls the number of 1-byte bursts to transmit and or receive in this command segment. The number of cyles required to send or received a byte will depend on COMMAND.SPEED. For dummy segments, (COMMAND.DIRECTION == 0), this register controls the number of dummy cycles to issue. The number of bytes (or dummy cycles) in the segment will be equal to COMMAND.LEN + 1.

2.1468.3 COMMAND . DIRECTION

The direction for the following command: “0” = Dummy cycles (no TX/RX). “1” = Rx only, “2” = Tx only, “3” = Bidirectional Tx/Rx (Standard SPI mode only).

2.1468.4 COMMAND . SPEED

The speed for this command segment: “0” = Standard SPI. “1” = Dual SPI. “2”=Quad SPI, “3”: RESERVED.

2.1468.5 COMMAND . CSAAT

Chip **S**elect **A**ctive **A**fter **T**ransaction. If `COMMAND.CSAAT` = 0, the chip select line is raised immediately at the end of the command segment. If `COMMAND.CSAAT` = 1, the chip select line is left low at the end of the current transaction segment. This allows the creation of longer, more complete SPI transactions, consisting of several separate segments for issuing instructions, pausing for dummy cycles, and transmitting or receiving data from the device.

2.1469 RXDATA

SPI Receive Data.

Reads from this window pull data from the RXFIFO.

The serial order of bit transmission is chosen to match SPI flash devices. Individual bytes are always transmitted with the most significant bit first. Only four-byte reads are supported. If ByteOrder = 0, the first byte received is packed in the MSB of !!RXDATA. For some processor architectures, this could lead to shuffling of flash data as compared to how it is written in memory. In which case, choosing ByteOrder = 1 can reverse the byte-order of each data read, causing the first byte received to be packed into the LSB of !!RXDATA. (Though within each byte the most significant bit is always pulled from the bus first.)

- Word Aligned Offset Range: `0x24`to`0x24`
- Size (words): `1`
- Access: `ro`
- Byte writes are *not* supported.

2.1470 TXDATA

SPI Transmit Data.

Data written to this window is placed into the TXFIFO. Byte-enables are supported for writes.

The serial order of bit transmission is chosen to match SPI flash devices. Individual bytes are always transmitted with the most significant bit first. Multi-byte writes are also supported, and if ByteOrder = 0, the bits of !!TXDATA are transmitted strictly in order of decreasing signficance (i.e. most signicant bit first). For some processor architectures, this could lead to shuffling of flash data as compared to how it is written in memory. In which case, choosing ByteOrder = 1 can reverse the byte-order of multi-byte data writes. (Though within each byte the most significant bit is always sent first.)

- Word Aligned Offset Range: `0x28`to`0x28`
- Size (words): `1`
- Access: `wo`
- Byte writes are supported.

2.1471 ERROR_ENABLE

Controls which classes of errors raise an interrupt. - Offset: `0x2c` - Reset default: `0x1f` - Reset mask: `0x1f`

2.1471.1 Fields

{"reg": [{"name": "CMDBUSY", "bits": 1, "attr": ["rw"], "rotate": -90}, {"name": "OVERFLOW", "

Bits	Type	Reset	Name	Description
31:5				Reserved
4	rw	0x1	CSIDINVAL	Invalid CSID: If this bit is set, the block sends an error interrupt whenever a command is submitted, but CSID exceeds NumCS.
3	rw	0x1	CMDINVAL	Invalid Command Errors: If this bit is set, the block sends an error interrupt whenever a command is sent with invalid values for COMMAND.SPEED or COMMAND.DIRECTION.
2	rw	0x1	UNDERFLOW	Underflow Errors: If this bit is set, the block sends an error interrupt whenever there is a read from RXDATA but the RX FIFO is empty.
1	rw	0x1	OVERFLOW	Overflow Errors: If this bit is set, the block sends an error interrupt whenever the TX FIFO overflows.
0	rw	0x1	CMDBUSY	Command Error: If this bit is set, the block sends an error interrupt whenever a command is issued while busy (i.e. a 1 is when STATUS.READY is not asserted.)

2.1472 ERROR_STATUS

Indicates that any errors that have occurred. When an error occurs, the corresponding bit must be cleared here before issuing any further commands. - Offset: 0x30 - Reset default: 0x0 - Reset mask: 0x3f

2.1472.1 Fields

{"reg": [{"name": "CMDBUSY", "bits": 1, "attr": ["rw1c"], "rotate": -90}, {"name": "OVERFLOW",

Bits	Type	Reset	Name	Description
31:6				Reserved
5	rw1c	0x0	ACCESSINVAL	Indicates that TLUL attempted to write to TXDATA with no bytes enabled. Such 'zero byte' writes are not supported.
4	rw1c	0x0	CSIDINVAL	Indicates a command was attempted with an invalid value for CSID.
3	rw1c	0x0	CMDINVAL	Indicates an invalid command segment, meaning either an invalid value of COMMAND.SPEED or a request for bidirectional data transfer at dual or quad speed
2	rw1c	0x0	UNDERFLOW	Indicates that firmware has attempted to read from RXDATA when the RX FIFO is empty.
1	rw1c	0x0	OVERFLOW	Indicates that firmware has overflowed the TX FIFO
0	rw1c	0x0	CMDBUSY	Indicates a write to COMMAND when STATUS.READY = 0.

2.1473 EVENT_ENABLE

Controls which classes of SPI events raise an interrupt. - Offset: `0x34` - Reset default: `0x0` - Reset mask: `0x3f`

2.1473.1 Fields

{"reg": [{"name": "RXFULL", "bits": 1, "attr": ["rw"], "rotate": -90}, {"name": "TXEMPTY", "bi

Bits	Type	Reset	Name
31:6			Reserved
5	rw	0x0	IDLE
4	rw	0x0	READY
3	rw	0x0	TXWM
2	rw	0x0	RXWM
1	rw	0x0	TXEMPTY
0	rw	0x0	RXFULL

2.1473.2 EVENT_ENABLE . IDLE

Assert to send a spi_event interrupt whenever `STATUS.ACTIVE` goes low

2.1473.3 EVENT_ENABLE . READY

Assert to send a spi_event interrupt whenever `STATUS.READY` goes high

2.1473.4 EVENT_ENABLE . TXWM

Assert to send a spi_event interrupt whenever the number of 32-bit words in the TX FIFO is less than `CONTROL.TX_WATERMARK.` To prevent the reassertion of this interrupt add more data to the TX FIFO, or reduce `CONTROL.TX_WATERMARK.`

2.1473.5 EVENT_ENABLE . RXWM

Assert to send a spi_event interrupt whenever the number of 32-bit words in the RX FIFO is greater than `CONTROL.RX_WATERMARK.` To prevent the reassertion of this interrupt, read more data from the RX FIFO, or increase `CONTROL.RX_WATERMARK.`

2.1473.6 EVENT_ENABLE . TXEMPTY

Assert to send a spi_event interrupt whenever `STATUS.TXEMPTY` goes high

2.1473.7 EVENT_ENABLE . RXFULL

Assert to send a spi_event interrupt whenever STATUS.RXFULL goes high

2.1474 tagger / doc / registers.md

2.1475 Summary

Name	Offset	Length	Description
tagger_reg.PAT_COMMIT	0x0	4	Partition configuration commit register
tagger_reg.PAT_ADDR_0	0x4	4	Partition address
tagger_reg.PAT_ADDR_1	0x8	4	Partition address
tagger_reg.PAT_ADDR_2	0xc	4	Partition address
tagger_reg.PAT_ADDR_3	0x10	4	Partition address
tagger_reg.PAT_ADDR_4	0x14	4	Partition address
tagger_reg.PAT_ADDR_5	0x18	4	Partition address
tagger_reg.PAT_ADDR_6	0x1c	4	Partition address
tagger_reg.PAT_ADDR_7	0x20	4	Partition address
tagger_reg.PAT_ADDR_8	0x24	4	Partition address
tagger_reg.PAT_ADDR_9	0x28	4	Partition address
tagger_reg.PAT_ADDR_10	0x2c	4	Partition address
tagger_reg.PAT_ADDR_11	0x30	4	Partition address
tagger_reg.PAT_ADDR_12	0x34	4	Partition address
tagger_reg.PAT_ADDR_13	0x38	4	Partition address
tagger_reg.PAT_ADDR_14	0x3c	4	Partition address
tagger_reg.PAT_ADDR_15	0x40	4	Partition address
tagger_reg.PATID_0	0x44	4	Partition ID
tagger_reg.PATID_1	0x48	4	Partition ID
tagger_reg.PATID_2	0x4c	4	Partition ID
tagger_reg.ADDR_CONF	0x50	4	Address encoding mode switch register

2.1476 PAT_COMMIT

Partition configuration commit register - Offset: `0x0` - Reset default: `0x0` - Reset mask: `0x1`

2.1476.1 Fields

{"reg": [{"name": "commit_0", "bits": 1, "attr": ["rw"], "rotate": -90}, {"bits": 31}], "confi

Bits	Type	Reset	Name	Description
31:1				Reserved

Bits	Type	Reset	Name	Description
0	rw	0x0	commit_0	commit changes of partition configuration

2.1477 PAT_ADDR

Partition address - Reset default: `0x0` - Reset mask: `0xffffffff`

2.1477.1 Instances

Name	Offset
PAT_ADDR_0	0x4
PAT_ADDR_1	0x8
PAT_ADDR_2	0xc
PAT_ADDR_3	0x10
PAT_ADDR_4	0x14
PAT_ADDR_5	0x18
PAT_ADDR_6	0x1c
PAT_ADDR_7	0x20
PAT_ADDR_8	0x24
PAT_ADDR_9	0x28
PAT_ADDR_10	0x2c
PAT_ADDR_11	0x30
PAT_ADDR_12	0x34
PAT_ADDR_13	0x38
PAT_ADDR_14	0x3c
PAT_ADDR_15	0x40

2.1477.2 Fields

{"reg": [{"name": "PAT_ADDR", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1

Bits	Type	Reset	Name	Description
31:0	rw	0x0	PAT_ADDR	Single partition configurations: address

2.1478 PATID

Partition ID - Reset default: `0x0` - Reset mask: `0xffffffff`

2.1478.1 Instances

Name	Offset
PATID_0	0x44
PATID_1	0x48
PATID_2	0x4c

2.1478.2 Fields

{"reg": [{"name": "PATID", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	PATID	Partition ID (PatID) for each partition, length determined by params

2.1479 ADDR_CONF

Address encoding mode switch register - Reset default: `0x0` - Reset mask: `0xffffffff`

2.1479.1 Instances

Name	Offset
ADDR_CONF	0x50

2.1479.2 Fields

{"reg": [{"name": "addr_conf", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes":

Bits	Type	Reset	Name	Description
31:0	rw	0x0	addr_conf	2 bits configuration for each partition. 2'b00: OFF, 2'b01: TOR, 2'b10: NA4

2.1480 uart / doc / registers.md

2.1481 Summary

Name	Offset	Length	Description
uart.INTR_STATE	0x0	4	Interrupt State Register
uart.INTR_ENABLE	0x4	4	Interrupt Enable Register
uart.INTR_TEST	0x8	4	Interrupt Test Register

Name	Offset	Length	Description
uart.ALERT_TEST	0xc	4	Alert Test Register
uart.CTRL	0x10	4	UART control register
uart.STATUS	0x14	4	UART live status register
uart.RDATA	0x18	4	UART read data
uart.WDATA	0x1c	4	UART write data
uart.FIFO_CTRL	0x20	4	UART FIFO control register
uart.FIFO_STATUS	0x24	4	UART FIFO status register
uart.OVRD	0x28	4	TX pin override control. Gives direct SW control over TX pin state
uart.VAL	0x2c	4	UART oversampled values
uart.TIMEOUT_CTRL	0x30	4	UART RX timeout control

2.1482 INTR_STATE

Interrupt State Register - Offset: `0x0` - Reset default: `0x101` - Reset mask: `0x1ff`

2.1482.1 Fields


```
{"reg": [{"name": "tx_watermark", "bits": 1, "attr": ["ro"], "rotate": -90}, {"name": "rx_wate
```


Bits	Type	Reset	Name	Description
31:9				Reserved
8	ro	0x1	tx_empty	raised if the transmit FIFO is empty.
7	rw1c	0x0	rx_parity_err	raised if the receiver has detected a parity error.
6	rw1c	0x0	rx_timeout	raised if RX FIFO has characters remaining in the FIFO without being retrieved for the programmed time period.
5	rw1c	0x0	rx_break_err	raised if break condition has been detected on receive.
4	rw1c	0x0	rx_frame_err	raised if a framing error has been detected on receive.
3	rw1c	0x0	rx_overflow	raised if the receive FIFO has overflowed.
2	rw1c	0x0	tx_done	raised if the transmit FIFO has emptied and no transmit is ongoing.
1	ro	0x0	rx_watermark	raised if the receive FIFO is past the high-water mark.
0	ro	0x1	tx_watermark	raised if the transmit FIFO is past the high-water mark.

2.1483 INTR_ENABLE

Interrupt Enable Register - Offset: `0x4` - Reset default: `0x0` - Reset mask: `0x1ff`

2.1483.1 Fields


```
{"reg": [{"name": "tx_watermark", "bits": 1, "attr": ["rw"], "rotate": -90}, {"name": "rx_wate
```

Bits	Type	Reset	Name	Description
31:9				Reserved
8	rw	0x0	tx_empty	Enable interrupt when INTR_STATE.tx_empty is set.
7	rw	0x0	rx_parity_err	Enable interrupt when INTR_STATE.rx_parity_err is set.
6	rw	0x0	rx_timeout	Enable interrupt when INTR_STATE.rx_timeout is set.
5	rw	0x0	rx_break_err	Enable interrupt when INTR_STATE.rx_break_err is set.
4	rw	0x0	rx_frame_err	Enable interrupt when INTR_STATE.rx_frame_err is set.
3	rw	0x0	rx_overflow	Enable interrupt when INTR_STATE.rx_overflow is set.
2	rw	0x0	tx_done	Enable interrupt when INTR_STATE.tx_done is set.
1	rw	0x0	rx_watermark	Enable interrupt when INTR_STATE.rx_watermark is set.
0	rw	0x0	tx_watermark	Enable interrupt when INTR_STATE.tx_watermark is set.

2.1484 INTR_TEST

Interrupt Test Register - Offset: `0x8` - Reset default: `0x0` - Reset mask: `0x1ff`

2.1484.1 Fields

{"reg": [{"name": "tx_watermark", "bits": 1, "attr": ["wo"], "rotate": -90}, {"name": "rx_wate

Bits	Type	Reset	Name	Description
31:9				Reserved
8	wo	0x0	tx_empty	Write 1 to force INTR_STATE.tx_empty to 1.
7	wo	0x0	rx_parity_err	Write 1 to force INTR_STATE.rx_parity_err to 1.
6	wo	0x0	rx_timeout	Write 1 to force INTR_STATE.rx_timeout to 1.
5	wo	0x0	rx_break_err	Write 1 to force INTR_STATE.rx_break_err to 1.
4	wo	0x0	rx_frame_err	Write 1 to force INTR_STATE.rx_frame_err to 1.
3	wo	0x0	rx_overflow	Write 1 to force INTR_STATE.rx_overflow to 1.
2	wo	0x0	tx_done	Write 1 to force INTR_STATE.tx_done to 1.
1	wo	0x0	rx_watermark	Write 1 to force INTR_STATE.rx_watermark to 1.
0	wo	0x0	tx_watermark	Write 1 to force INTR_STATE.tx_watermark to 1.

2.1485 ALERT_TEST

Alert Test Register - Offset: `0xc` - Reset default: `0x0` - Reset mask: `0x1`

2.1485.1 Fields

{"reg": [{"name": "fatal_fault", "bits": 1, "attr": ["wo"], "rotate": -90}, {"bits": 31}], "co

Bits	Type	Reset	Name	Description
31:1				Reserved
0	wo	0x0	fatal_fault	Write 1 to trigger one alert event of this kind.

2.1486 CTRL

UART control register - Offset: `0x10` - Reset default: `0x0` - Reset mask: `0xffff03f7`

2.1486.1 Fields

{"reg": [{"name": "TX", "bits": 1, "attr": ["rw"], "rotate": -90}, {"name": "RX", "bits": 1, "a

Bits	Type	Reset	Name
31:16	rw	0x0	NCO
15:10			Reserved
9:8	rw	0x0	RXBLVL
7	rw	0x0	PARITY_ODD
6	rw	0x0	PARITY_EN
5	rw	0x0	LLPBK
4	rw	0x0	SLPBK
3			Reserved
2	rw	0x0	NF
1	rw	0x0	RX
0	rw	0x0	TX

2.1486.2 CTRL . NCO

BAUD clock rate control.

2.1486.3 CTRL . RXBLVL

Trigger level for RX break detection. Sets the number of character times the line must be low to detect a break.

Value	Name	Description
0x0	break2	2 characters
0x1	break4	4 characters

Value	Name	Description
0x2	break8	8 characters
0x3	break16	16 characters

2.1486.4 CTRL . PARITY_ODD

If PARITY_EN is true, this determines the type, 1 for odd parity, 0 for even.

2.1486.5 CTRL . PARITY_EN

If true, parity is enabled in both RX and TX directions.

2.1486.6 CTRL . LLPBK

Line loopback enable.

If this bit is turned on, incoming bits are forwarded to TX for testing purpose. See Block Diagram. Note that the internal design sees RX value as 1 always if line loopback is enabled.

2.1486.7 CTRL . SLPBK

System loopback enable.

If this bit is turned on, any outgoing bits to TX are received through RX. See Block Diagram. Note that the TX line goes 1 if System loopback is enabled.

2.1486.8 CTRL . NF

RX noise filter enable. If the noise filter is enabled, RX line goes through the 3-tap repetition code. It ignores single IP clock period noise.

2.1486.9 CTRL . RX

RX enable

2.1486.10 CTRL . TX

TX enable

2.1487 STATUS

UART live status register - Offset: `0x14` - Reset default: `0x3c` - Reset mask: `0x3f`

2.1487.1 Fields

{"reg": [{"name": "TXFULL", "bits": 1, "attr": ["ro"], "rotate": -90}, {"name": "RXFULL", "bits

Bits	Type	Reset	Name	Description
31:6				Reserved
5	ro	0x1	RXEMPTY	RX FIFO is empty
4	ro	0x1	RXIDLE	RX is idle
3	ro	0x1	TXIDLE	TX FIFO is empty and all bits have been transmitted
2	ro	0x1	TXEMPTY	TX FIFO is empty
1	ro	x	RXFULL	RX buffer is full
0	ro	x	TXFULL	TX buffer is full

2.1488 RDATA

UART read data - Offset: `0x18` - Reset default: `0x0` - Reset mask: `0xff`

2.1488.1 Fields

{"reg": [{"name": "RDATA", "bits": 8, "attr": ["ro"], "rotate": 0}, {"bits": 24}], "config": {

Bits	Type	Reset	Name	Description
31:8				Reserved
7:0	ro	x	RDATA	

2.1489 WDATA

UART write data - Offset: `0x1c` - Reset default: `0x0` - Reset mask: `0xff`

2.1489.1 Fields

{"reg": [{"name": "WDATA", "bits": 8, "attr": ["wo"], "rotate": 0}, {"bits": 24}], "config": {

Bits	Type	Reset	Name	Description
31:8				Reserved
7:0	wo	0x0	WDATA	

2.1490 FIFO_CTRL

UART FIFO control register - Offset: `0x20` - Reset default: `0x0` - Reset mask: `0xff`

2.1490.1 Fields

{"reg": [{"name": "RXRST", "bits": 1, "attr": ["wo"], "rotate": -90}, {"name": "TXRST", "bits"

Bits	Type	Reset	Name
31:8			Reserved
7:5	rw	0x0	TXILVL
4:2	rw	0x0	RXILVL
1	wo	0x0	TXRST
0	wo	0x0	RXRST

2.1490.2 FIFO_CTRL . TXILVL

Trigger level for TX interrupts. If the FIFO depth is less than the setting, it raises tx_watermark interrupt.

Value	Name	Description
0x0	txlvl1	1 character
0x1	txlvl2	2 characters
0x2	txlvl4	4 characters
0x3	txlvl8	8 characters
0x4	txlvl16	16 characters

Other values are reserved.

2.1490.3 FIFO_CTRL . RXILVL

Trigger level for RX interrupts. If the FIFO depth is greater than or equal to the setting, it raises rx_watermark interrupt.

Value	Name	Description
0x0	rxlvl1	1 character
0x1	rxlvl2	2 characters
0x2	rxlvl4	4 characters
0x3	rxlvl8	8 characters
0x4	rxlvl16	16 characters
0x5	rxlvl32	32 characters
0x6	rxlvl62	62 characters

Other values are reserved.

2.1490.4 FIFO_CTRL . TXRST

TX fifo reset. Write 1 to the register resets TX_FIFO. Read returns 0

2.1490.5 FIFO_CTRL . RXRST

RX fifo reset. Write 1 to the register resets RX_FIFO. Read returns 0

2.1491 FIFO_STATUS

UART FIFO status register - Offset: `0x24` - Reset default: `0x0` - Reset mask: `0xff00ff`

2.1491.1 Fields


```
{"reg": [{"name": "TXLVL", "bits": 8, "attr": ["ro"], "rotate": 0}, {"bits": 8}, {"name": "RXL
```


Bits	Type	Reset	Name	Description
31:24				Reserved
23:16	ro	x	RXLVL	Current fill level of RX fifo
15:8				Reserved
7:0	ro	x	TXLVL	Current fill level of TX fifo

2.1492 OVRD

TX pin override control. Gives direct SW control over TX pin state - Offset: `0x28` - Reset default: `0x0` - Reset mask: `0x3`

2.1492.1 Fields


```
{"reg": [{"name": "TXEN", "bits": 1, "attr": ["rw"], "rotate": -90}, {"name": "TXVAL", "bits":
```


Bits	Type	Reset	Name	Description
31:2				Reserved
1	rw	0x0	TXVAL	Write to set the value of the TX pin
0	rw	0x0	TXEN	Enable TX pin override control

2.1493 VAL

UART oversampled values - Offset: `0x2c` - Reset default: `0x0` - Reset mask: `0xffff`

2.1493.1 Fields


```
{"reg": [{"name": "RX", "bits": 16, "attr": ["ro"], "rotate": 0}, {"bits": 16}], "config": {"la
```

Bits	Type	Reset	Name	Description
31:16				Reserved
15:0	ro	x	RX	Last 16 oversampled values of RX. Most recent bit is bit 0, oldest 15.

2.1494 TIMEOUT_CTRL

UART RX timeout control - Offset: `0x30` - Reset default: `0x0` - Reset mask: `0x80ffffff`

2.1494.1 Fields


```
{"reg": [{"name": "VAL", "bits": 24, "attr": ["rw"], "rotate": 0}, {"bits": 7}, {"name": "EN",
```


Bits	Type	Reset	Name	Description
31	rw	0x0	EN	Enable RX timeout feature
30:24				Reserved
23:0	rw	0x0	VAL	RX timeout value in UART bit times

2.1495 unbent / doc / registers.md

2.1496 Summary

Name	Offset	Length	Description
bus_err_unit.err_addr	0x0	4	Address of the bus error
bus_err_unit.err_addr_top	0x4	4	Top of the address of the bus error
bus_err_unit.err_code	0x8	4	Error code of the bus error
bus_err_unit.meta	0xc	4	Meta information of the bus error

2.1497 err_addr

Address of the bus error - Offset: `0x0` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.1497.1 Fields


```
{"reg": [{"name": "err_addr", "bits": 32, "attr": ["ro"], "rotate": 0}], "config": {"lanes": 1
```

Bits	Type	Reset	Name	Description
31:0	ro	x	err_addr	Address of the bus error

2.1498 err_addr_top

Top of the address of the bus error - Offset: `0x4` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.1498.1 Fields


```
{"reg": [{"name": "err_addr", "bits": 32, "attr": ["ro"], "rotate": 0}], "config": {"lanes": 1
```


Bits	Type	Reset	Name	Description
31:0	ro	x	err_addr	Address of the bus error

2.1499 err_code

Error code of the bus error - Offset: `0x8` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.1499.1 Fields


```
{"reg": [{"name": "err_code", "bits": 32, "attr": ["ro"], "rotate": 0}], "config": {"lanes": 1
```


Bits	Type	Reset	Name	Description
31:0	ro	x	err_code	Error code of the bus error

2.1500 meta

Meta information of the bus error - Offset: `0xc` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.1500.1 Fields


```
{"reg": [{"name": "meta", "bits": 32, "attr": ["ro"], "rotate": 0}], "config": {"lanes": 1, "f
```


Bits	Type	Reset	Name	Description
31:0	ro	x	meta	Meta information of the bus error

2.1501 vga / doc / registers.md

2.1502 Summary

Name	Offset	Length	Description
axi_vga.CONTROL	0x0	4	Control register
axi_vga.CLK_DIV	0x4	4	Clock divider
axi_vga.HORI_VISIBLE_SIZE	0x8	4	Size of horizontal visible area
axi_vga.HORI_FRONT_PORCH_SIZE	0xc	4	Size of horizontal front porch
axi_vga.HORI_SYNC_SIZE	0x10	4	Size of horizontal sync area
axi_vga.HORI_BACK_PORCH_SIZE	0x14	4	Size of horizontal back porch
axi_vga.VERT_VISIBLE_SIZE	0x18	4	Size of vertical visible area
axi_vga.VERT_FRONT_PORCH_SIZE	0x1c	4	Size of vertical front porch
axi_vga.VERT_SYNC_SIZE	0x20	4	Size of vertical sync area
axi_vga.VERT_BACK_PORCH_SIZE	0x24	4	Size of vertical back porch
axi_vga.START_ADDR_LOW	0x28	4	Low end of start address of frame buffer
axi_vga.START_ADDR_HIGH	0x2c	4	High end of start address of frame buffer
axi_vga.FRAME_SIZE	0x30	4	Size of whole frame
axi_vga.BURST_LEN	0x34	4	Number of beats in a burst

2.1503 CONTROL

Control register - Offset: `0x0` - Reset default: `0x6` - Reset mask: `0x7`

2.1503.1 Fields

`{"reg": [{"name": "enable", "bits": 1, "attr": ["rw"], "rotate": -90}, {"name": "hsync_pol", "`

Bits	Type	Reset	Name	Description
31:3				Reserved
2	rw	0x1	vsync_pol	Sets polarity for VSYNC 0 - Active Low 1 - Active High
1	rw	0x1	hsync_pol	Sets polarity for HSYNC 0 - Active Low 1 - Active High
0	rw	0x0	enable	Enables FSM.

2.1504 CLK_DIV

Clock divider - Offset: `0x4` - Reset default: `0x1` - Reset mask: `0xff`

2.1504.1 Fields

{"reg": [{"name": "clk_div", "bits": 8, "attr": ["rw"], "rotate": 0}, {"bits": 24}], "config":

Bits	Type	Reset	Name	Description
31:8				Reserved
7:0	rw	0x1	clk_div	Clock divider.

2.1505 HORI_VISIBLE_SIZE

Size of horizontal visible area - Offset: `0x8` - Reset default: `0x1` - Reset mask: `0xffffffff`

2.1505.1 Fields

{"reg": [{"name": "hori_visible_size", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"

Bits	Type	Reset	Name	Description
31:0	rw	0x1	hori_visible_size	Size of horizontal visible area.

2.1506 HORI_FRONT_PORCH_SIZE

Size of horizontal front porch - Offset: `0xc` - Reset default: `0x1` - Reset mask: `0xffffffff`

2.1506.1 Fields

{"reg": [{"name": "hori_front_porch_size", "bits": 32, "attr": ["rw"], "rotate": 0}], "config"

Bits	Type	Reset	Name	Description
31:0	rw	0x1	hori_front_porch_size	Size of horizontal front porch.

2.1507 HORI_SYNC_SIZE

Size of horizontal sync area - Offset: `0x10` - Reset default: `0x1` - Reset mask: `0xffffffff`

2.1507.1 Fields

{"reg": [{"name": "hori_sync_size", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lan

Bits	Type	Reset	Name	Description
31:0	rw	0x1	hori_sync_size	Size of horizontal sync area.

2.1508 HORI_BACK_PORCH_SIZE

Size of horizontal back porch - Offset: `0x14` - Reset default: `0x1` - Reset mask: `0xffffffff`

2.1508.1 Fields


```
{"reg": [{"name": "hori_back_porch_size", "bits": 32, "attr": ["rw"], "rotate": 0}], "config":
```


Bits	Type	Reset	Name	Description
31:0	rw	0x1	hori_back_porch_size	Size of horizontal back porch.

2.1509 VERT_VISIBLE_SIZE

Size of vertical visible area - Offset: `0x18` - Reset default: `0x1` - Reset mask: `0xffffffff`

2.1509.1 Fields


```
{"reg": [{"name": "vert_visible_size", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"
```


Bits	Type	Reset	Name	Description
31:0	rw	0x1	vert_visible_size	Size of vertical visible area.

2.1510 VERT_FRONT_PORCH_SIZE

Size of vertical front porch - Offset: `0x1c` - Reset default: `0x1` - Reset mask: `0xffffffff`

2.1510.1 Fields


```
{"reg": [{"name": "vert_front_porch_size", "bits": 32, "attr": ["rw"], "rotate": 0}], "config"
```


Bits	Type	Reset	Name	Description
31:0	rw	0x1	vert_front_porch_size	Size of vertical front porch.

2.1511 VERT_SYNC_SIZE

Size of vertical sync area - Offset: `0x20` - Reset default: `0x1` - Reset mask: `0xffffffff`

2.1511.1 Fields

{"reg": [{"name": "vert_sync_size", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lan

Bits	Type	Reset	Name	Description
31:0	rw	0x1	vert_sync_size	Size of vertical sync area.

2.1512 VERT_BACK_PORCH_SIZE

Size of vertical back porch - Offset: `0x24` - Reset default: `0x1` - Reset mask: `0xffffffff`

2.1512.1 Fields

{"reg": [{"name": "vert_back_porch_size", "bits": 32, "attr": ["rw"], "rotate": 0}], "config":

Bits	Type	Reset	Name	Description
31:0	rw	0x1	vert_back_porch_size	Size of vertical back porch.

2.1513 START_ADDR_LOW

Low end of start address of frame buffer - Offset: `0x28` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.1513.1 Fields

{"reg": [{"name": "start_addr_low", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lan

Bits	Type	Reset	Name	Description
31:0	rw	0x0	start_addr_low	Low end of start address of frame buffer.

2.1514 START_ADDR_HIGH

High end of start address of frame buffer - Offset: `0x2c` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.1514.1 Fields

{"reg": [{"name": "start_addr_high", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"la

Bits	Type	Reset	Name	Description
31:0	rw	0x0	start_addr_high	High end of start address of frame buffer.

2.1515 FRAME_SIZE

Size of whole frame - Offset: `0x30` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.1515.1 Fields

{"reg": [{"name": "frame_size", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes":

Bits	Type	Reset	Name	Description
31:0	rw	0x0	frame_size	Size of whole frame.

2.1516 BURST_LEN

Number of beats in a burst - Offset: `0x34` - Reset default: `0x0` - Reset mask: `0xff`

2.1516.1 Fields

{"reg": [{"name": "burst_len", "bits": 8, "attr": ["rw"], "rotate": 0}, {"bits": 24}], "config

Bits	Type	Reset	Name	Description
31:8				Reserved
7:0	rw	0x0	burst_len	Number of beats in a burst.

2.1517 watchdog_timer / doc / registers.md

2.1518 Summary

Name	Offset	Length	Description
aon_timer.ALERT_TEST	0x0	4	Alert Test Register
aon_timer.WKUP_CTRL	0x4	4	Wakeup Timer Control register

Name	Offset	Length	Description
aon_timer.WKUP_THOLD	0x8	4	Wakeup Timer Threshold Register
aon_timer.WKUP_COUNT	0xc	4	Wakeup Timer Count Register
aon_timer.WDOG_REGWEN	0x10	4	Watchdog Timer Write Enable Register
aon_timer.WDOG_CTRL	0x14	4	Watchdog Timer Control register
aon_timer.WDOG_BARK_THOLD	0x18	4	Watchdog Timer Bark Threshold Register
aon_timer.WDOG_BITE_THOLD	0x1c	4	Watchdog Timer Bite Threshold Register
aon_timer.WDOG_COUNT	0x20	4	Watchdog Timer Count Register
aon_timer.INTR_STATE	0x24	4	Interrupt State Register
aon_timer.INTR_TEST	0x28	4	Interrupt Test Register
aon_timer.WKUP_CAUSE	0x2c	4	Wakeup request status

2.1519 ALERT_TEST

Alert Test Register - Offset: `0x0` - Reset default: `0x0` - Reset mask: `0x1`

2.1519.1 Fields


```
{"reg": [{"name": "fatal_fault", "bits": 1, "attr": ["wo"], "rotate": -90}, {"bits": 31}], "co
```


Bits	Type	Reset	Name	Description
31:1				Reserved
0	wo	0x0	fatal_fault	Write 1 to trigger one alert event of this kind.

2.1520 WKUP_CTRL

Wakeup Timer Control register - Offset: `0x4` - Reset default: `0x0` - Reset mask: `0x1fff`

2.1520.1 Fields


```
{"reg": [{"name": "enable", "bits": 1, "attr": ["rw"], "rotate": -90}, {"name": "prescaler", "
```


Bits	Type	Reset	Name	Description
31:13				Reserved
12:1	rw	0x0	prescaler	Pre-scaler value for wakeup timer count
0	rw	0x0	enable	When set to 1, the wakeup timer will count

2.1521 WKUP_THOLD

Wakeup Timer Threshold Register - Offset: `0x8` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.1521.1 Fields


```
{"reg": [{"name": "threshold", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 
```


Bits	Type	Reset	Name	Description
31:0	rw	0x0	threshold	The count at which a wakeup interrupt should be generated

2.1522 WKUP_COUNT

Wakeup Timer Count Register - Offset: `0xc` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.1522.1 Fields


```
{"reg": [{"name": "count", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "
```


Bits	Type	Reset	Name	Description
31:0	rw	0x0	count	The current wakeup counter value

2.1523 WDOG_REGWEN

Watchdog Timer Write Enable Register - Offset: `0x10` - Reset default: `0x1` - Reset mask: `0x1`

2.1523.1 Fields


```
{"reg": [{"name": "regwen", "bits": 1, "attr": ["rw0c"], "rotate": -90}, {"bits": 31}], "confi
```


Bits	Type	Reset	Name	Description
31:1				Reserved
0	rw0c	0x1	regwen	Once cleared, the watchdog configuration will be locked until the next reset

2.1524 WDOG_CTRL

Watchdog Timer Control register - Offset: `0x14` - Reset default: `0x0` - Reset mask: `0x3` - Register enable: `WDOG_REGWEN`

2.1524.1 Fields

{"reg": [{"name": "enable", "bits": 1, "attr": ["rw"], "rotate": -90}, {"name": "pause_in_slee

Bits	Type	Reset	Name	Description
31:2				Reserved
1	rw	0x0	pause_in_sleep	When set to 1, the watchdog timer will not count during sleep
0	rw	0x0	enable	When set to 1, the watchdog timer will count

2.1525 WDOG_BARK_THOLD

Watchdog Timer Bark Threshold Register - Offset: `0x18` - Reset default: `0x0` - Reset mask: `0xffffffff` - Register enable: `WDOG_REGWEN`

2.1525.1 Fields

{"reg": [{"name": "threshold", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes":

Bits	Type	Reset	Name	Description
31:0	rw	0x0	threshold	The count at which a watchdog bark interrupt should be generated

2.1526 WDOG_BITE_THOLD

Watchdog Timer Bite Threshold Register - Offset: `0x1c` - Reset default: `0x0` - Reset mask: `0xffffffff` - Register enable: `WDOG_REGWEN`

2.1526.1 Fields

{"reg": [{"name": "threshold", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes":

Bits	Type	Reset	Name	Description
31:0	rw	0x0	threshold	The count at which a watchdog bite reset should be generated

2.1527 WDOG_COUNT

Watchdog Timer Count Register - Offset: `0x20` - Reset default: `0x0` - Reset mask: `0xffffffff`

2.1527.1 Fields

{"reg": [{"name": "count", "bits": 32, "attr": ["rw"], "rotate": 0}], "config": {"lanes": 1, "

Bits	Type	Reset	Name	Description
31:0	rw	0x0	count	The current watchdog counter value

2.1528 INTR_STATE

Interrupt State Register - Offset: `0x24` - Reset default: `0x0` - Reset mask: `0x3`

2.1528.1 Fields

{"reg": [{"name": "wkup_timer_expired", "bits": 1, "attr": ["rw1c"], "rotate": -90}, {"name": "

Bits	Type	Reset	Name	Description
31:2				Reserved
1	rw1c	0x0	wdog_timer_bark	Raised if the watchdog timer has hit the bark threshold
0	rw1c	0x0	wkup_timer_expired	Raised if the wakeup timer has hit the specified threshold

2.1529 INTR_TEST

Interrupt Test Register - Offset: `0x28` - Reset default: `0x0` - Reset mask: `0x3`

2.1529.1 Fields

{"reg": [{"name": "wkup_timer_expired", "bits": 1, "attr": ["wo"], "rotate": -90}, {"name": "wo

Bits	Type	Reset	Name	Description
31:2				Reserved
1	wo	x	wdog_timer_bark	Write 1 to force wdog_timer_bark interrupt
0	wo	x	wkup_timer_expired	Write 1 to force wkup_timer_expired interrupt

2.1530 WKUP_CAUSE

Wakeup request status - Offset: `0x2c` - Reset default: `0x0` - Reset mask: `0x1`

2.1530.1 Fields

{"reg": [{"name": "cause", "bits": 1, "attr": ["rw0c"], "rotate": -90}, {"bits": 31}], "config

Bits	Type	Reset	Name	Description
31:1				Reserved
0	rw0c	0x0	cause	AON timer requested wakeup, write 0 to clear