Content Indexing

01.Index
02.Change List
03.Block Diagram
04.Power tree
05.System Power
06.RK3368 Power
07.RK3368 OSC/PMUIO Controler
08.RK3368 DDR Controler
09.RK3368 FLASH/SDMMC Controler
10.RK3368 USB/ADC/HUB Controler
11.RK3368 SDIO/UART/I2S/DVP/CSI
12.RK3368 Display Interface
13.RK3368 GMAC/GPIO | eMMC
14.LPDDR3
15.eDP+TP
16.USB/TF Port
17.HDMI Port
18.WIFI+BT
19.RJ45
20.FAN/LED/IR
21.Edge-Fingers

Power by Geekbuying.com			
Project:	Geekbox		
File:	Index		
Date:	Wednesday, November 18, 2015	Rev:	V1.23
Designed by:	Lu	Sheet:	1 of 21

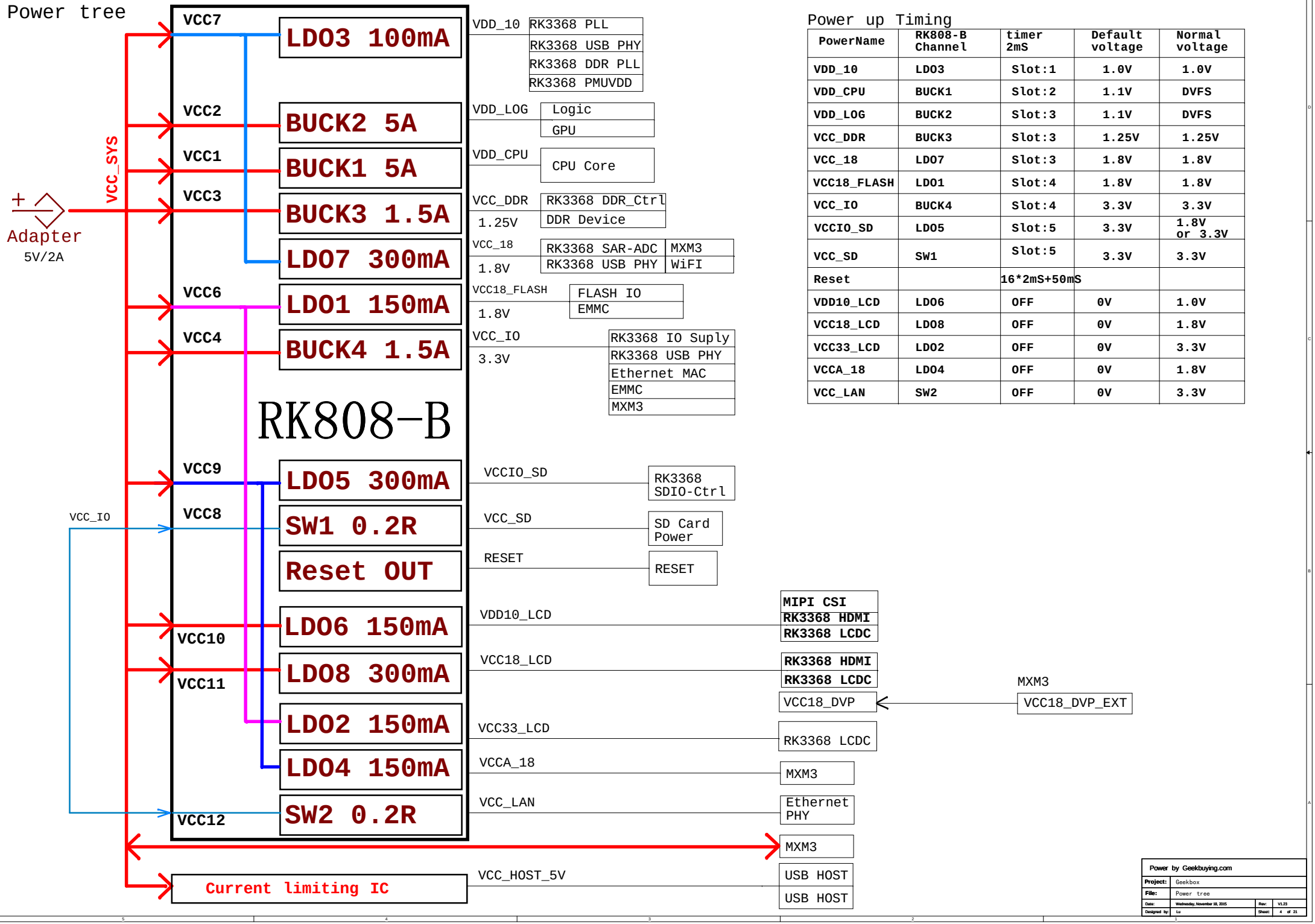
Version	Date	Author	Change Note	Approved
V0.1	20150710	Lu	First edit	gouwa
V1.23	20150929	Lu	1. Use RK808-B PMIC as power solution 2. Redefine the edge-fingers, MXM3.1 as the reference 3. Add the HDMI CEC support	gouwa

Power by Geekbuying.com			
Project:	Geekbox		
File:	Change List		
Date:	Wednesday, November 18, 2015	Rev:	V1.23
Designed by:	Lu	Sheet:	2 of 21

geekbox.tv

Power by Geekbuying.com			
Project:	Geekbox		
File:	Block Diagram		
Date:	Wednesday, November 18, 2015	Rev:	V1.23
Designed by:	Lu	Sheet:	3 of 21

Power tree

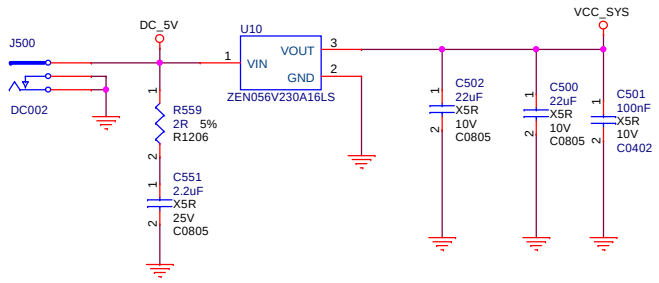


Power up Timing

PowerName	RK808-B Channel	timer 2mS	Default voltage	Normal voltage
VDD_10	LDO3	Slot:1	1.0V	1.0V
VDD_CPU	BUCK1	Slot:2	1.1V	DVFS
VDD_LOG	BUCK2	Slot:3	1.1V	DVFS
VCC_DDR	BUCK3	Slot:3	1.25V	1.25V
VCC_18	LDO7	Slot:3	1.8V	1.8V
VCC18_FLASH	LDO1	Slot:4	1.8V	1.8V
VCC_IO	BUCK4	Slot:4	3.3V	3.3V
VCCIO_SD	LDO5	Slot:5	3.3V	1.8V or 3.3V
VCC_SD	SW1	Slot:5	3.3V	3.3V
Reset		16*2mS+50mS		
VDD10_LCD	LDO6	OFF	0V	1.0V
VCC18_LCD	LDO8	OFF	0V	1.8V
VCC33_LCD	LDO2	OFF	0V	3.3V
VCCA_18	LDO4	OFF	0V	1.8V
VCC_LAN	SW2	OFF	0V	3.3V

Power by Geekbuying.com

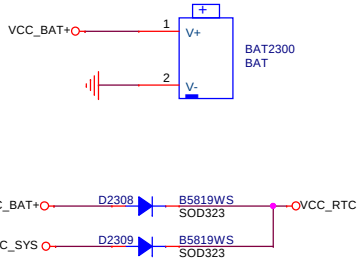
Project:	Geekbox
File:	Power tree
Date:	Wednesday, November 18, 2015
Rev:	V1.23
Designed by:	Lu
Sheet:	4 of 21



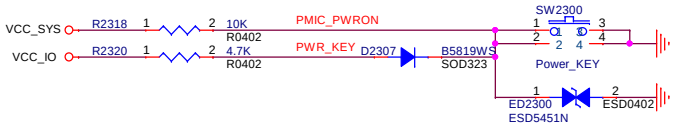
4.8V-5.3V

DC IN

Battery



Power KEY(Power on/off)



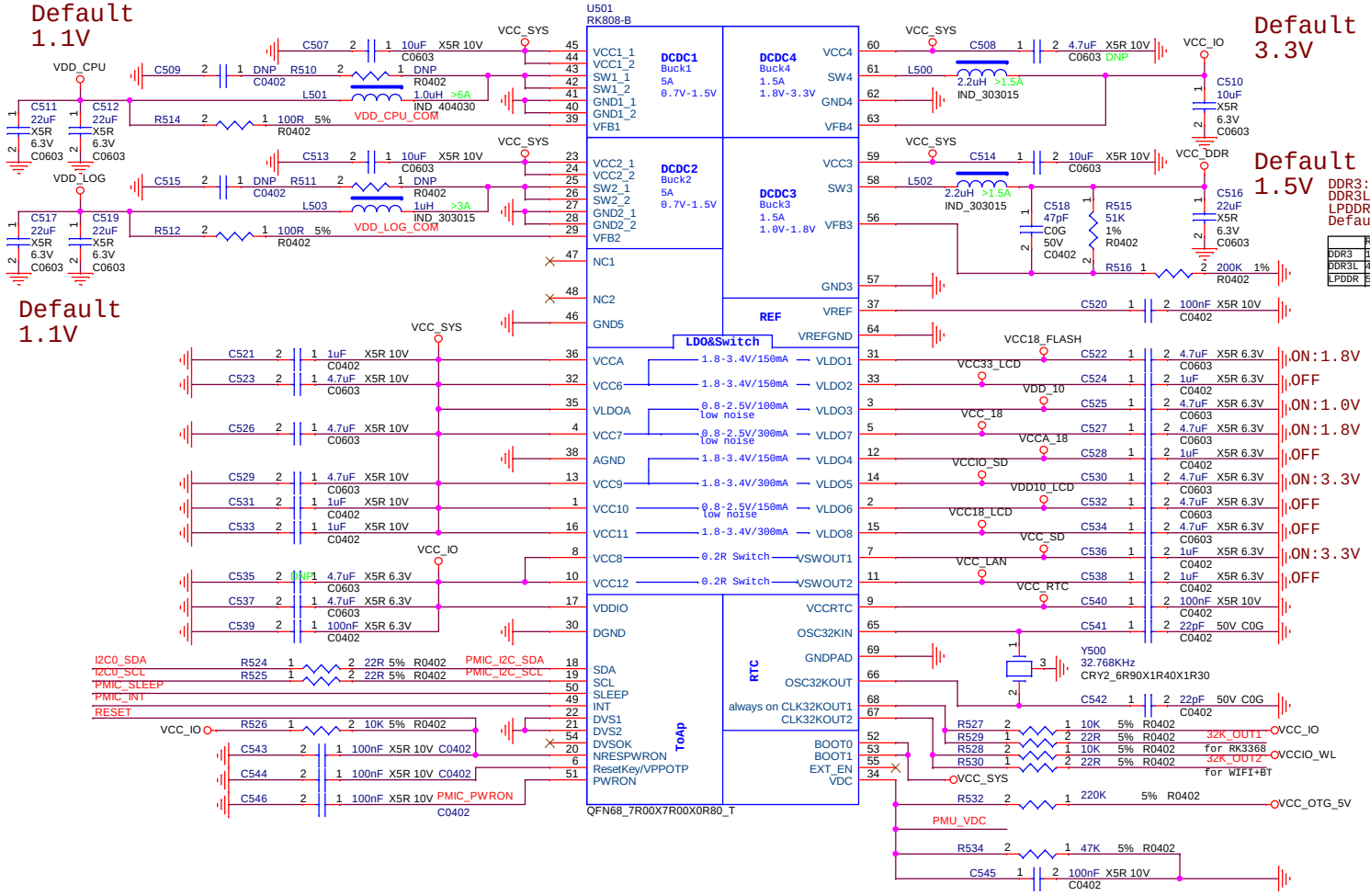
Default
1.1V

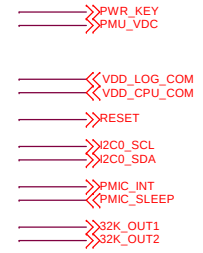
Default
1.1V

Default
3.3V

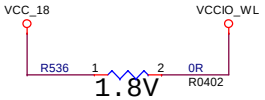
Default
1.5V
DDR3:1.5V
DDR3L:1.35V
LPDDR:1.25V
Default:LPDDR3

	R515	R516
DDR3	100K	200K
DDR3L	43K	120K
LPDDR	51K	200K

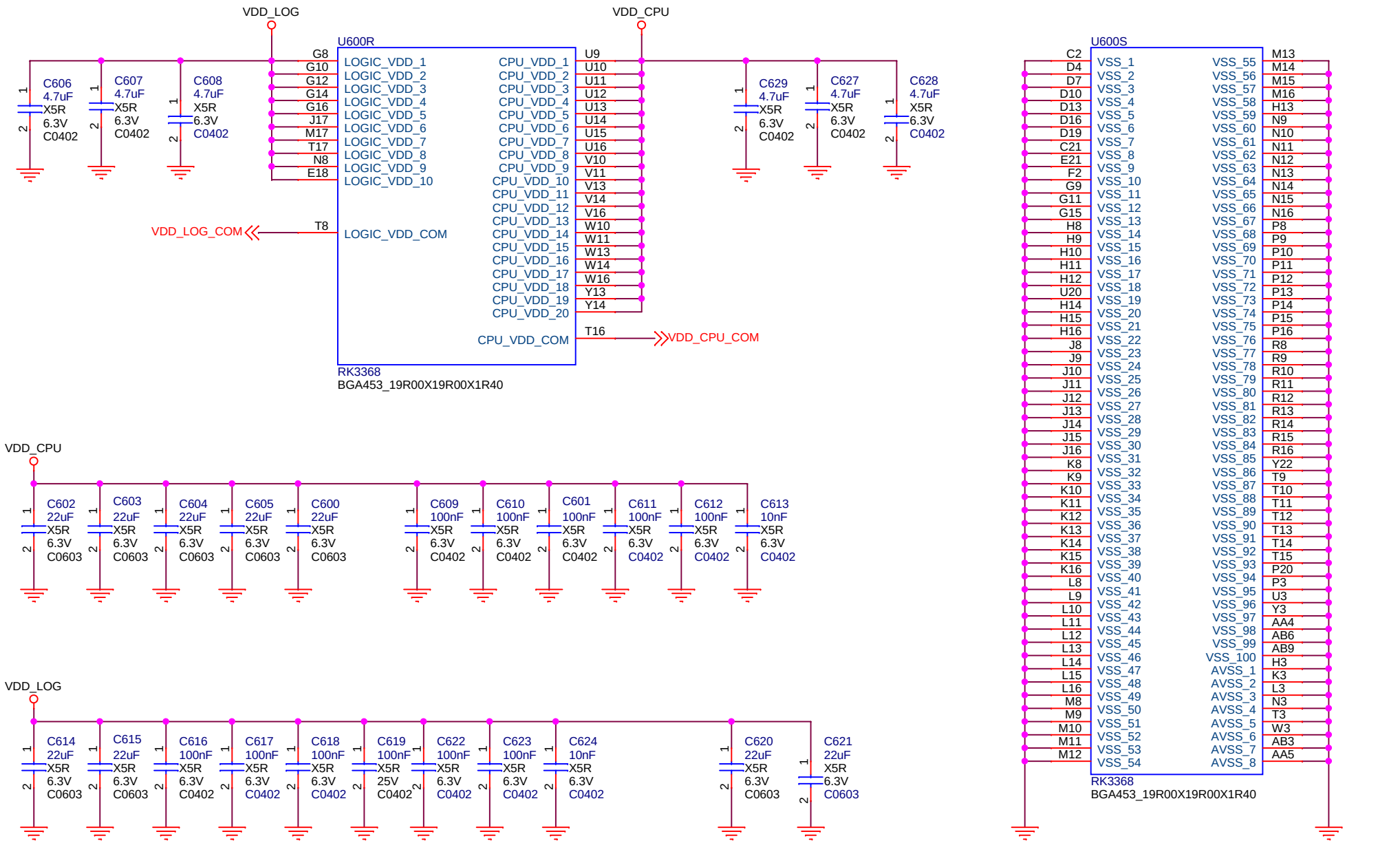




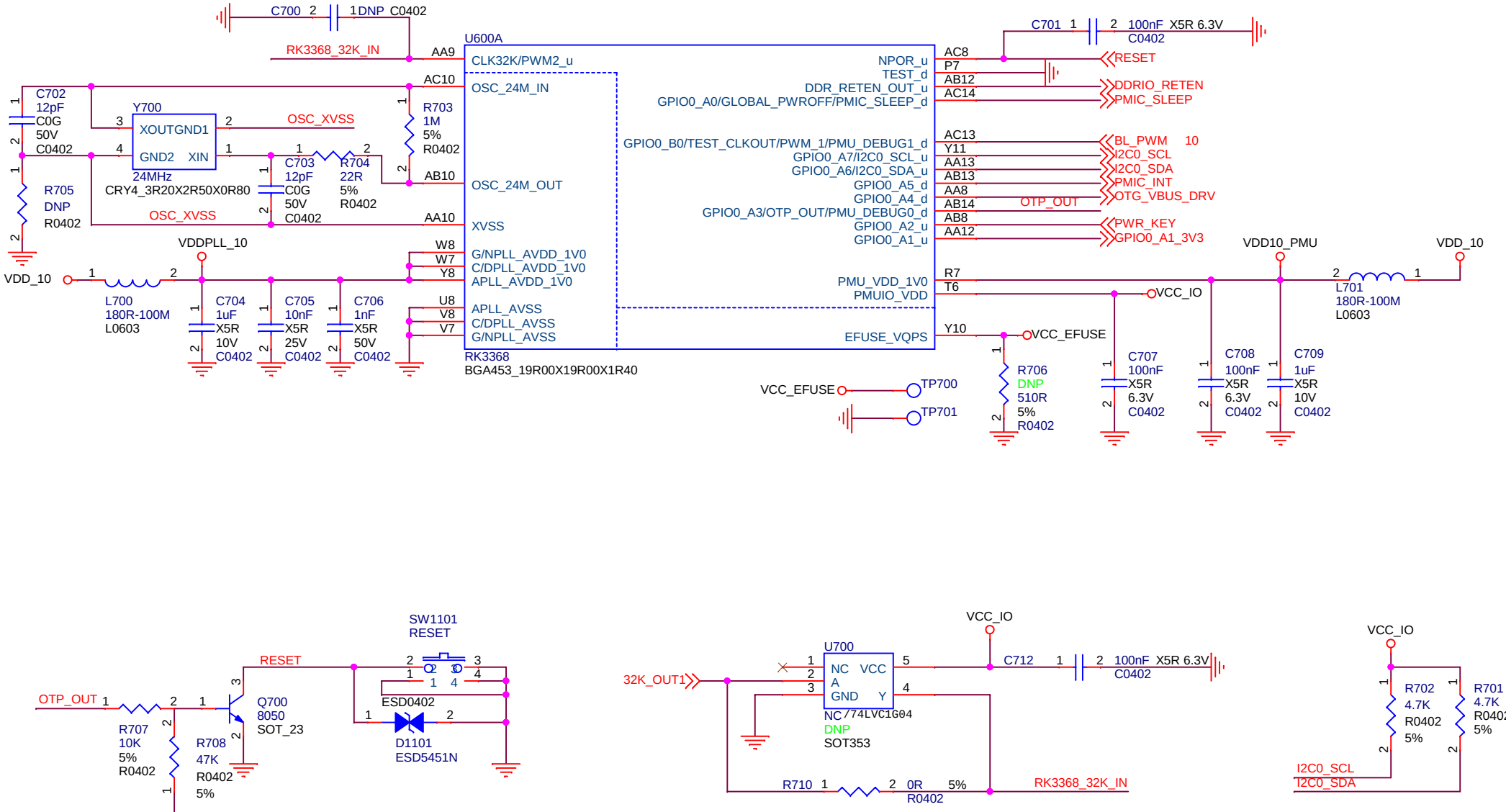
VCCIO_WL



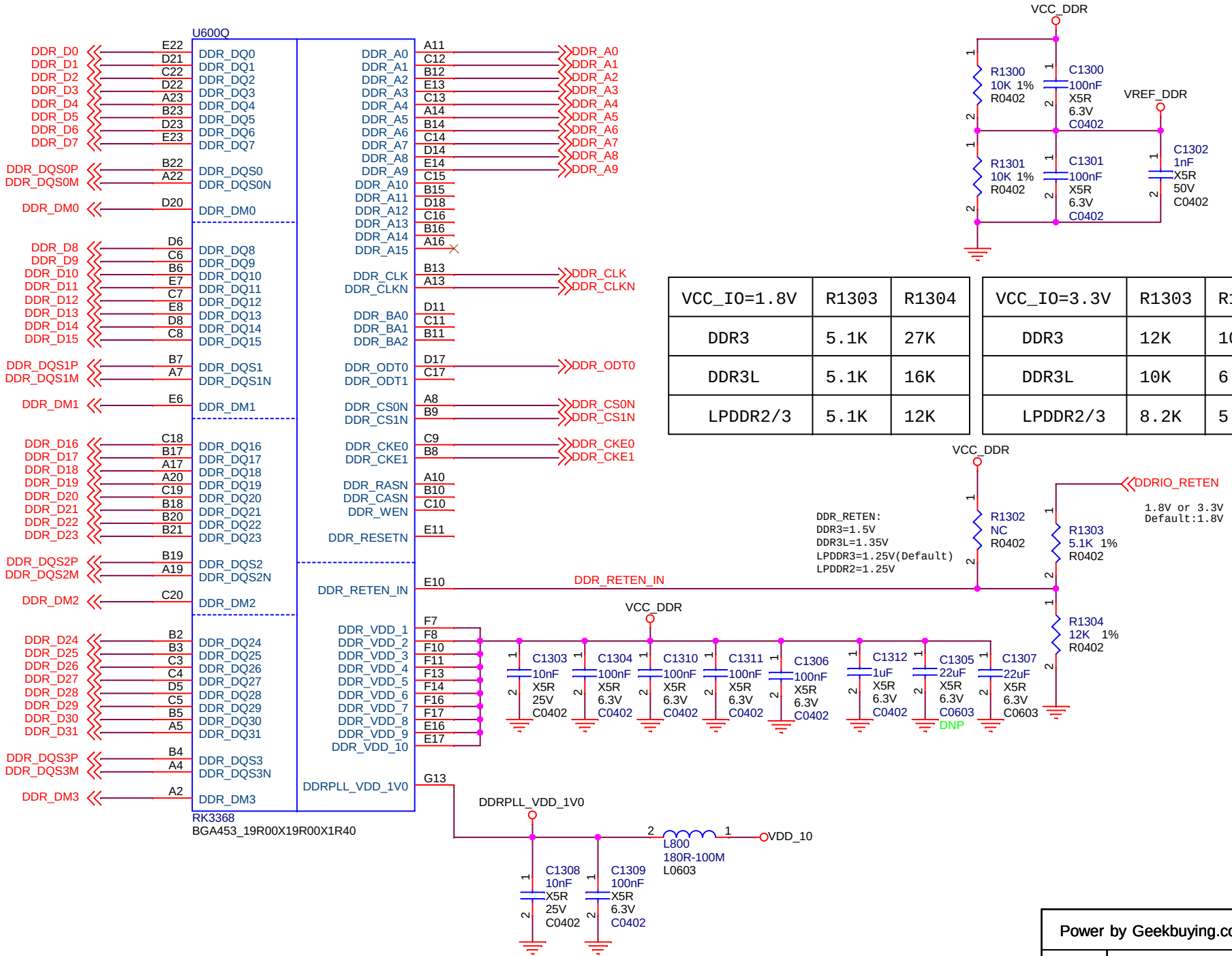
Power by Geekbuying.com	
Project:	Geekbox
File:	System Power
Date:	Wednesday, November 18, 2015
Rev:	V1.23
Designed by:	Lu
Sheet:	5 of 21

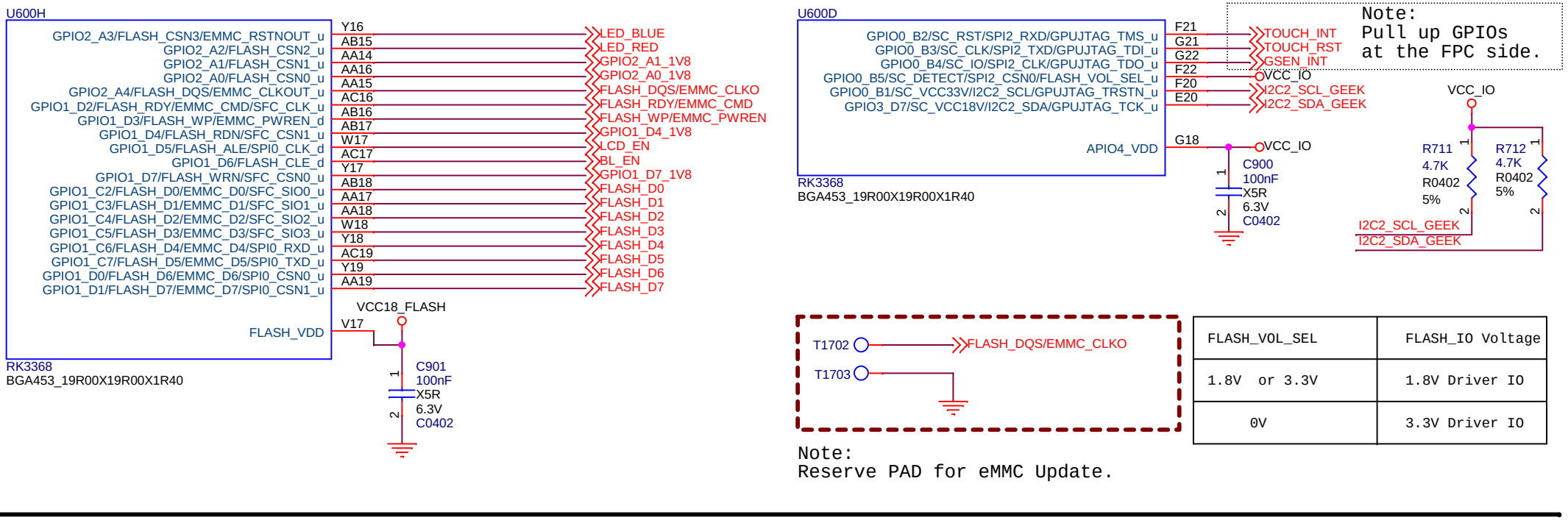


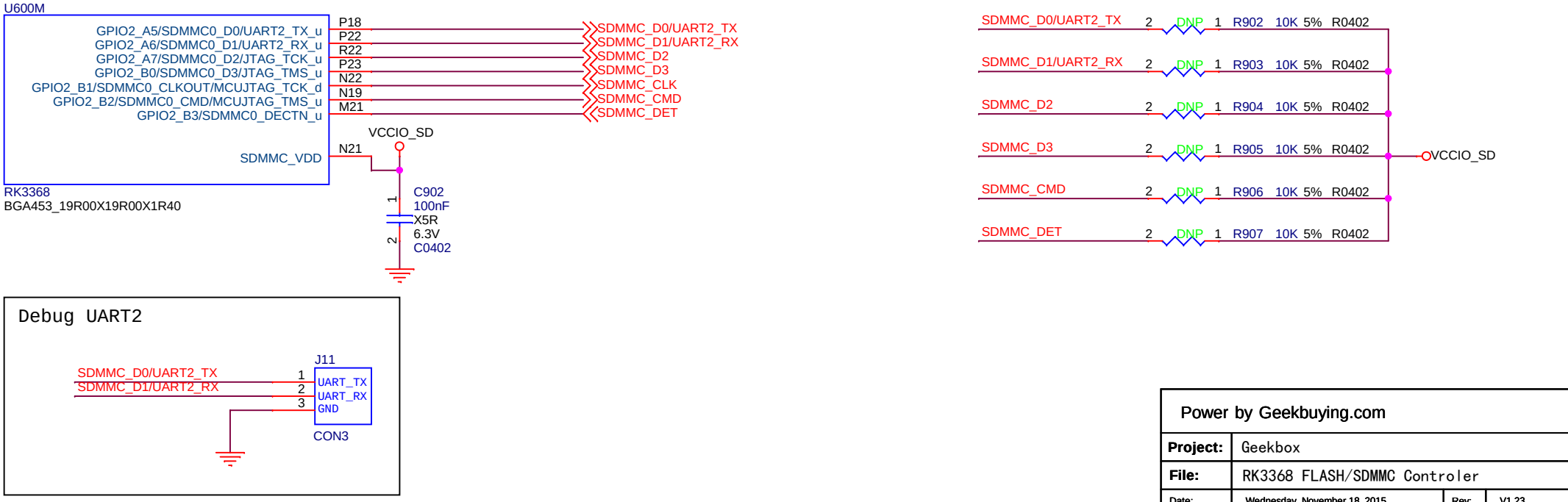
Power by Geekbuying.com			
Project:	Geekbox		
File:	RK3368 Power		
Date:	Wednesday, November 18, 2015	Rev:	V1.23
Designed by:	Lu	Sheet:	6 of 21



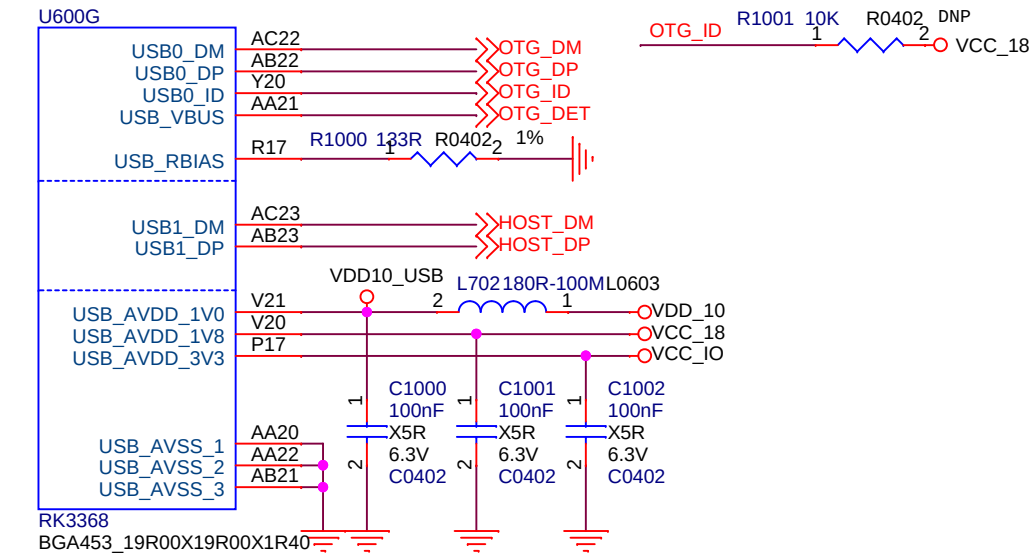
Power by Geekbuying.com			
Project:	Geekbox		
File:	RK3368 OST/PMUIO Controler		
Date:	Wednesday, November 18, 2015	Rev:	V1.23
Designed by:	Lu	Sheet:	7 of 21

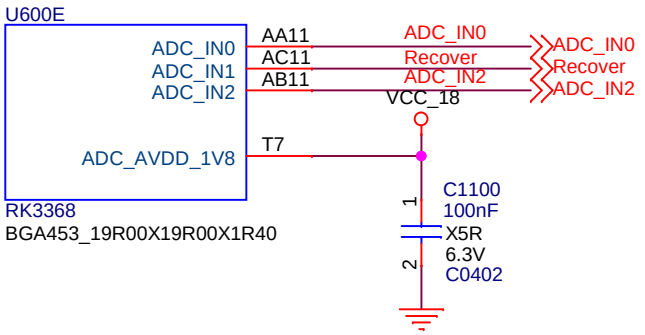

U600Q
RK3368
BGA453_19R00X19R00X1R40
DDR_D0
DDR_D1
DDR_D2
DDR_D3
DDR_D4
DDR_D5
DDR_D6
DDR_D7
DDR_DQS0P
DDR_DQS0M
DDR_DM0
DDR_D8
DDR_D9
DDR_D10
DDR_D11
DDR_D12
DDR_D13
DDR_D14
DDR_D15
DDR_DQS1P
DDR_DQS1M
DDR_DM1
DDR_D16
DDR_D17
DDR_D18
DDR_D19
DDR_D20
DDR_D21
DDR_D22
DDR_D23
DDR_DQS2P
DDR_DQS2M
DDR_DM2
DDR_D24
DDR_D25
DDR_D26
DDR_D27
DDR_D28
DDR_D29
DDR_D30
DDR_D31
DDR_DQS3P
DDR_DQS3M
DDR_DM3
DDR_DQ0
DDR_DQ1
DDR_DQ2
DDR_DQ3
DDR_DQ4
DDR_DQ5
DDR_DQ6
DDR_DQ7
DDR_DQS0
DDR_DQS0N
DDR_DM0
DDR_DQ8
DDR_DQ9
DDR_DQ10
DDR_DQ11
DDR_DQ12
DDR_DQ13
DDR_DQ14
DDR_DQ15
DDR_DQS1
DDR_DQS1N
DDR_DM1
DDR_DQ16
DDR_DQ17
DDR_DQ18
DDR_DQ19
DDR_DQ20
DDR_DQ21
DDR_DQ22
DDR_DQ23
DDR_DQS2
DDR_DQS2N
DDR_DM2
DDR_DQ24
DDR_DQ25
DDR_DQ26
DDR_DQ27
DDR_DQ28
DDR_DQ29
DDR_DQ30
DDR_DQ31
DDR_DQS3
DDR_DQS3N
DDR_DM3
DDR_A0
DDR_A1
DDR_A2
DDR_A3
DDR_A4
DDR_A5
DDR_A6
DDR_A7
DDR_A8
DDR_A9
DDR_A10
DDR_A11
DDR_A12
DDR_A13
DDR_A14
DDR_A15
DDR_CLK
DDR_CLKN
DDR_BA0
DDR_BA1
DDR_BA2
DDR_ODT0
DDR_ODT1
DDR_CS0N
DDR_CS1N
DDR_CKE0
DDR_CKE1
DDR_RASN
DDR_CASN
DDR_WEN
DDR_RESETN
DDR_RETEN_IN
DDR_VDD_1
DDR_VDD_2
DDR_VDD_3
DDR_VDD_4
DDR_VDD_5
DDR_VDD_6
DDR_VDD_7
DDR_VDD_8
DDR_VDD_9
DDR_VDD_10
DDRPLL_VDD_1V0
E22 D21 C22 D22 A23 B23 D23 E23
B22 A22
D20
D6 C6 B6 E7 C7 E8 D8 C8
B7 A7
E6
C18 B17 A17 A20 C19 B18 B20 B21
B19 A19
C20
B2 B3 C3 C4 D5 C5 B5 A5
B4 A4
A2
A11 C12 B12 E13 C13 A14 B14 C14 D14 E14 C15 B15 D18 C16 B16 A16
B13 A13
D11 C11 B11
D17 C17
A8 B9
C9 B8
A10 B10 C10
E11
E10
F7 F8 F10 F11 F13 F14 F16 F17 E16 E17
G13
VCC_DDR
R1300 10K 1% R0402
C1300 100nF X5R 6.3V C0402
VREF_DDR
C1302 1nF X5R 50V C0402
R1301 10K 1% R0402
C1301 100nF X5R 6.3V C0402
VCC_IO=1.8V | R1303 | R1304
DDR3 | 5.1K | 27K
DDR3L | 5.1K | 16K
LPDDR2/3 | 5.1K | 12K
VCC_IO=3.3V | R1303 | R1304
DDR3 | 12K | 10K
DDR3L | 10K | 6.8K
LPDDR2/3 | 8.2K | 5.1K
DDR_RETEN:
DDR3=1.5V
DDR3L=1.35V
LPDDR3=1.25V(Default)
LPDDR2=1.25V
R1302 NC R0402
DDRIO_RETEN
1.8V or 3.3V
Default:1.8V
R1303 5.1K 1% R0402
R1304 12K 1% R0402
C1303 10nF X5R 25V C0402
C1304 100nF X5R 6.3V C0402
C1310 100nF X5R 6.3V C0402
C1311 100nF X5R 6.3V C0402
C1306 100nF X5R 6.3V C0402
C1312 1uF X5R 6.3V C0402
C1305 22uF X5R 6.3V C0603
DNP
C1307 22uF X5R 6.3V C0603
L800 180R-100M L0603
VDD_10
C1308 10nF X5R 25V C0402
C1309 100nF X5R 6.3V C0402
Power by Geekbuying.com
Project: Geekbox
File: RK3368 DDR Controler
Date: Wednesday, November 18, 2015
Rev: V1.23
Designed by: Lu
Sheet: 8 of 21

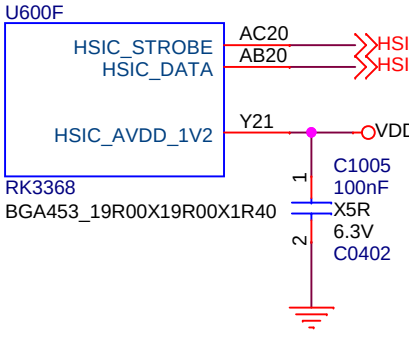


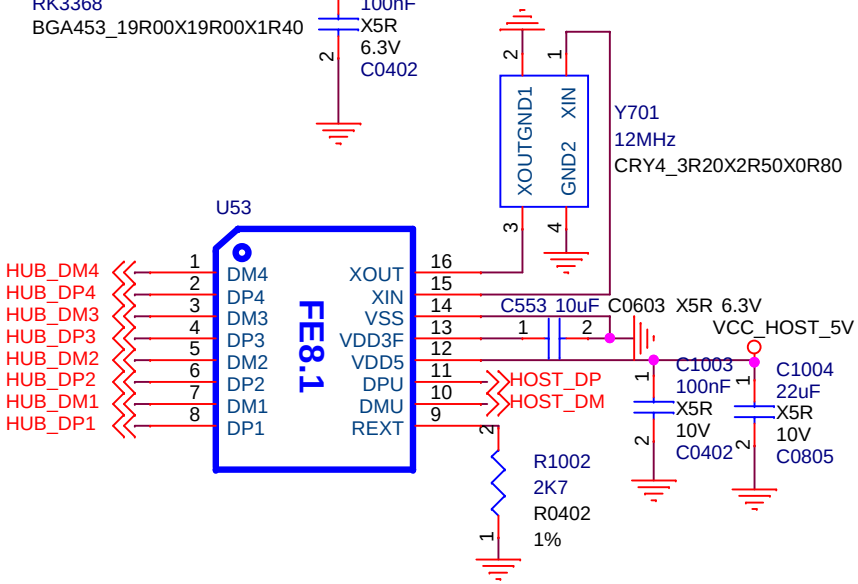


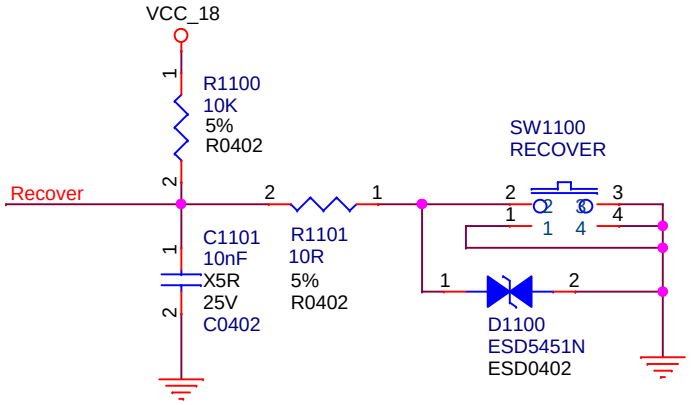
Power by Geekbuying.com	
Project:	Geekbox
File:	RK3368 FLASH/SDMMC Controler
Date: Wednesday, November 18, 2015	Rev: V1.23
Designed by: Lu	Sheet: 9 of 21





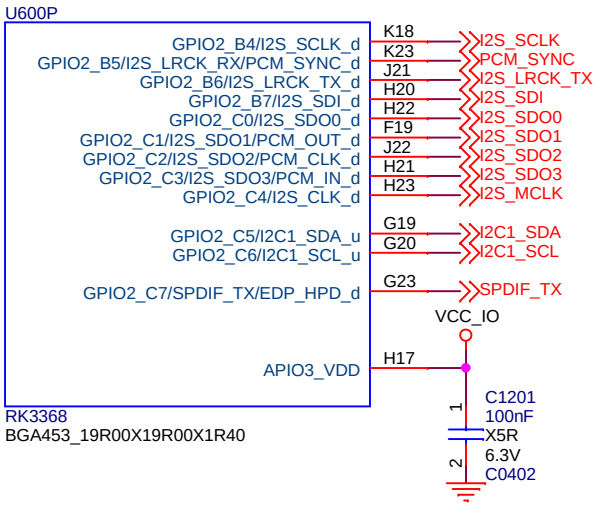


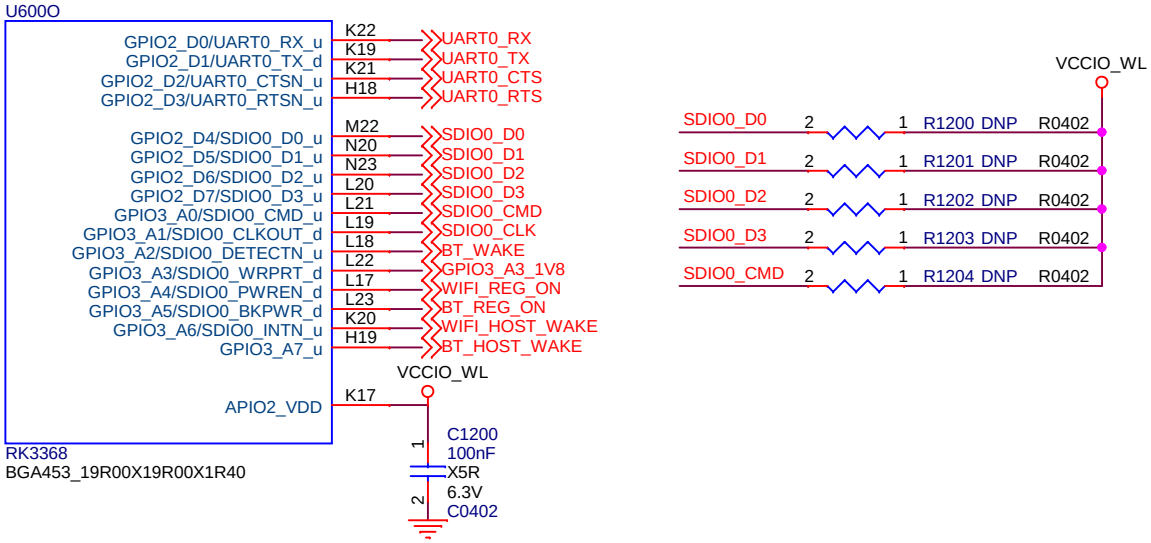




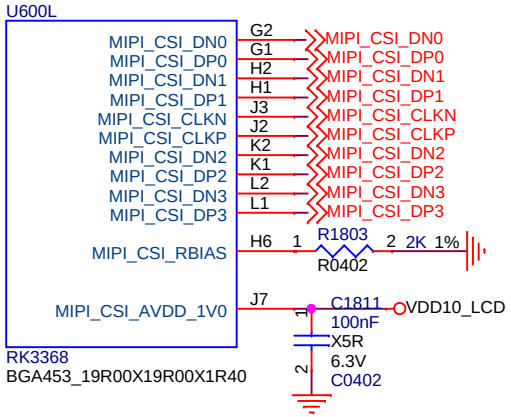
Power by Geekbuying.com

Project:	Geekbox		
File:	RK3368 USB/HSIC/ADC-HUB		
Date:	Wednesday, November 18, 2015	Rev:	V1.23
Designed by:	Lu	Sheet:	10 of 21

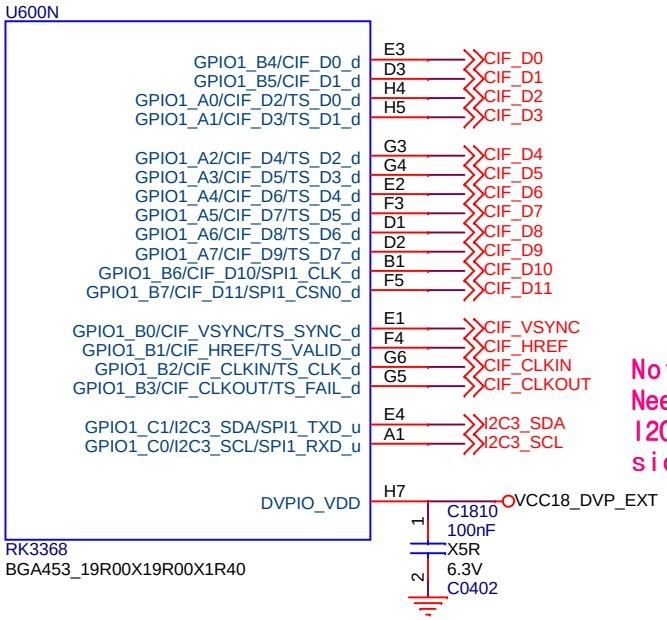




MIPI CSI

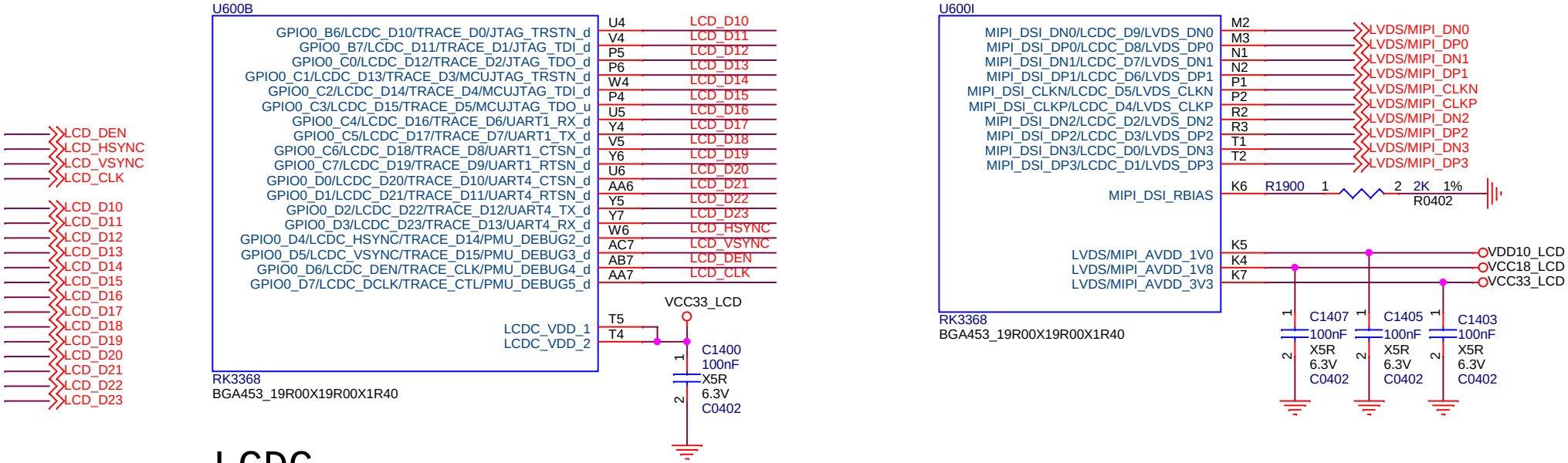


CIF

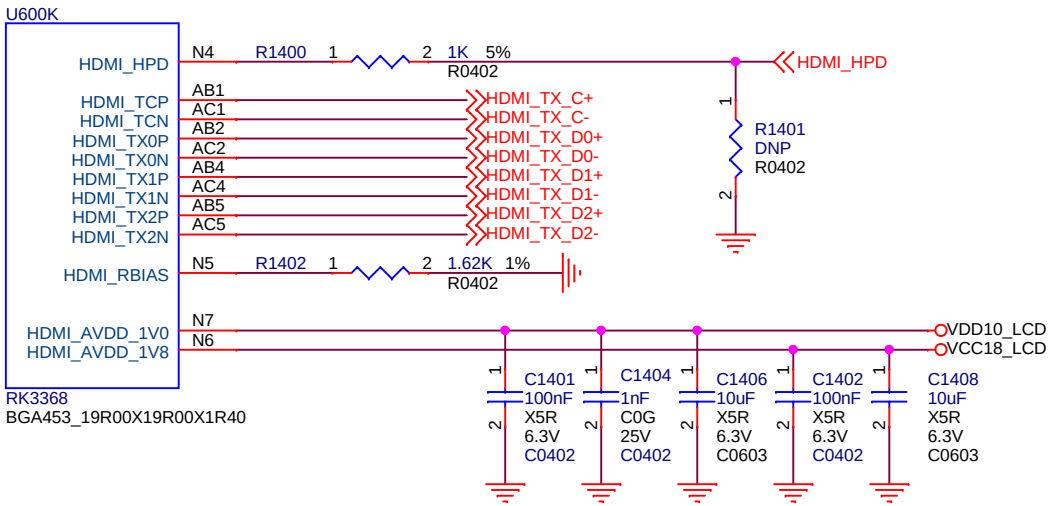


Note:
Need to pull up the I2C Bus at the FPC side.

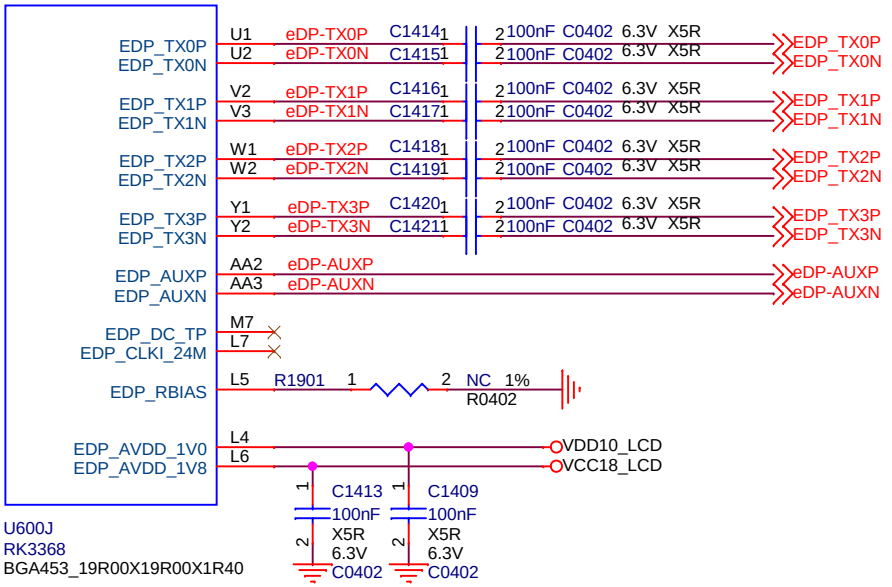
Power by Geekbuying.com	
Project:	Geekbox
File:	RK3368 SDIO0/UART0/I2S/MIPI CSI/CIF
Date: Wednesday, November 18, 2015	Rev: V1.23
Designed by: Lu	Sheet: 11 of 21



LCDC

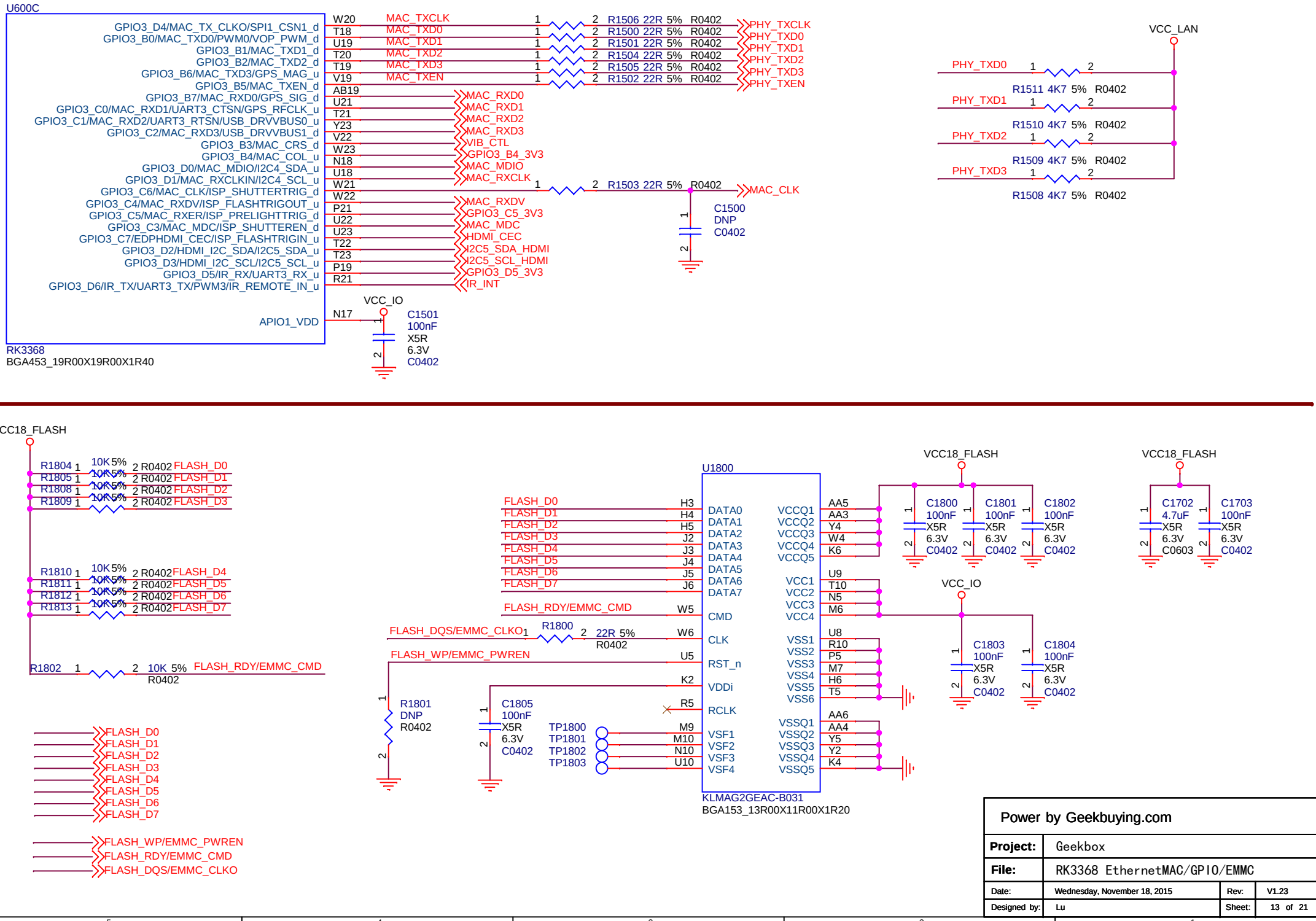


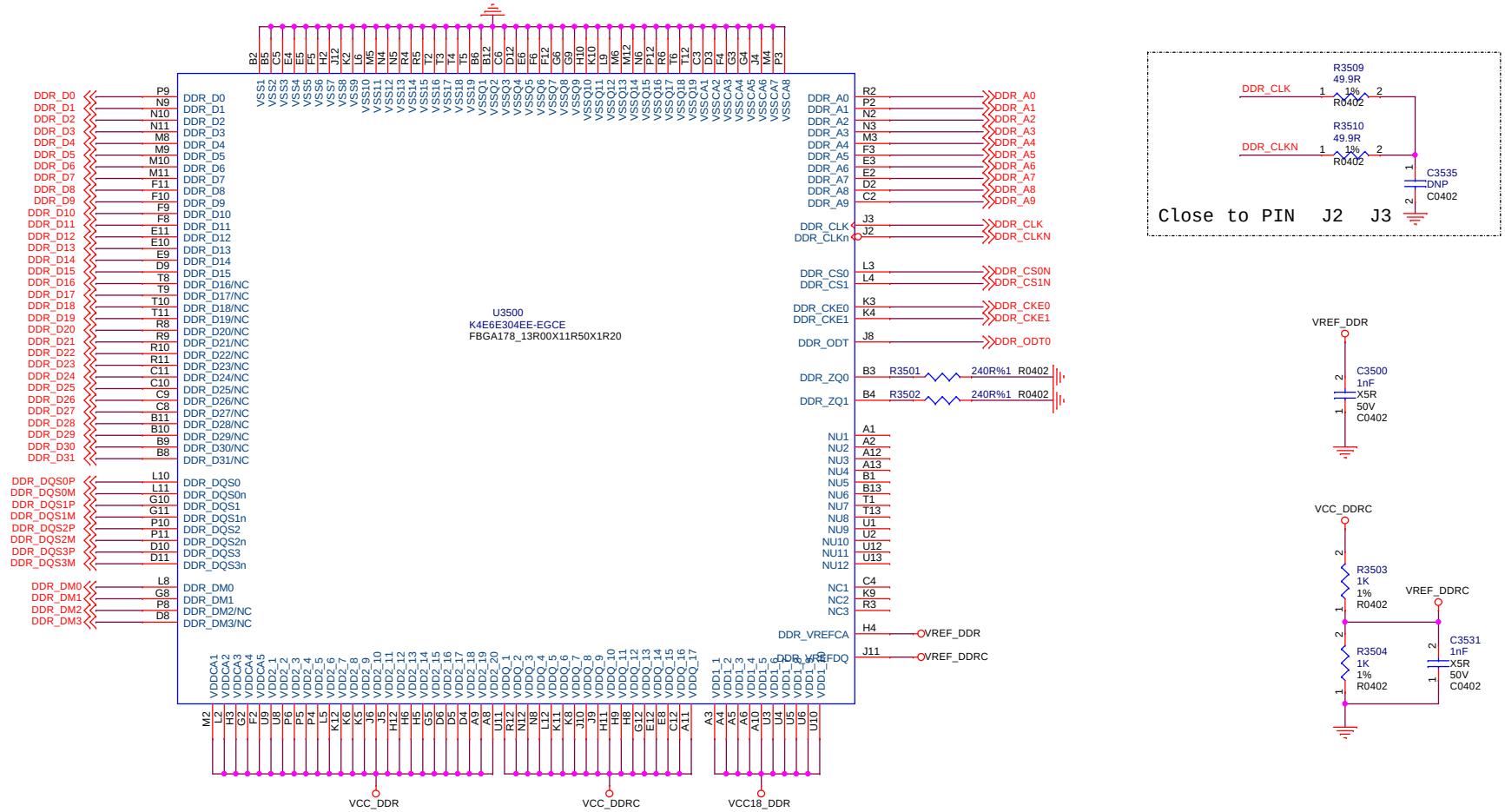
HDMI OUT



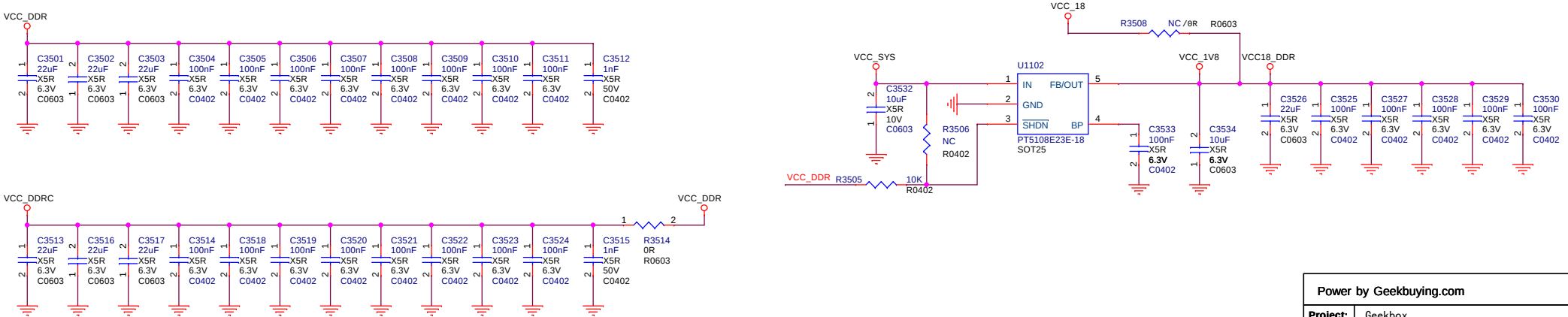
EDP

Power by Geekbuying.com			
Project:	Geekbox		
File:	RK3368 Display Interface		
Date:	Wednesday, November 18, 2015	Rev:	V1.23
Designed by:	Lu	Sheet:	12 of 21

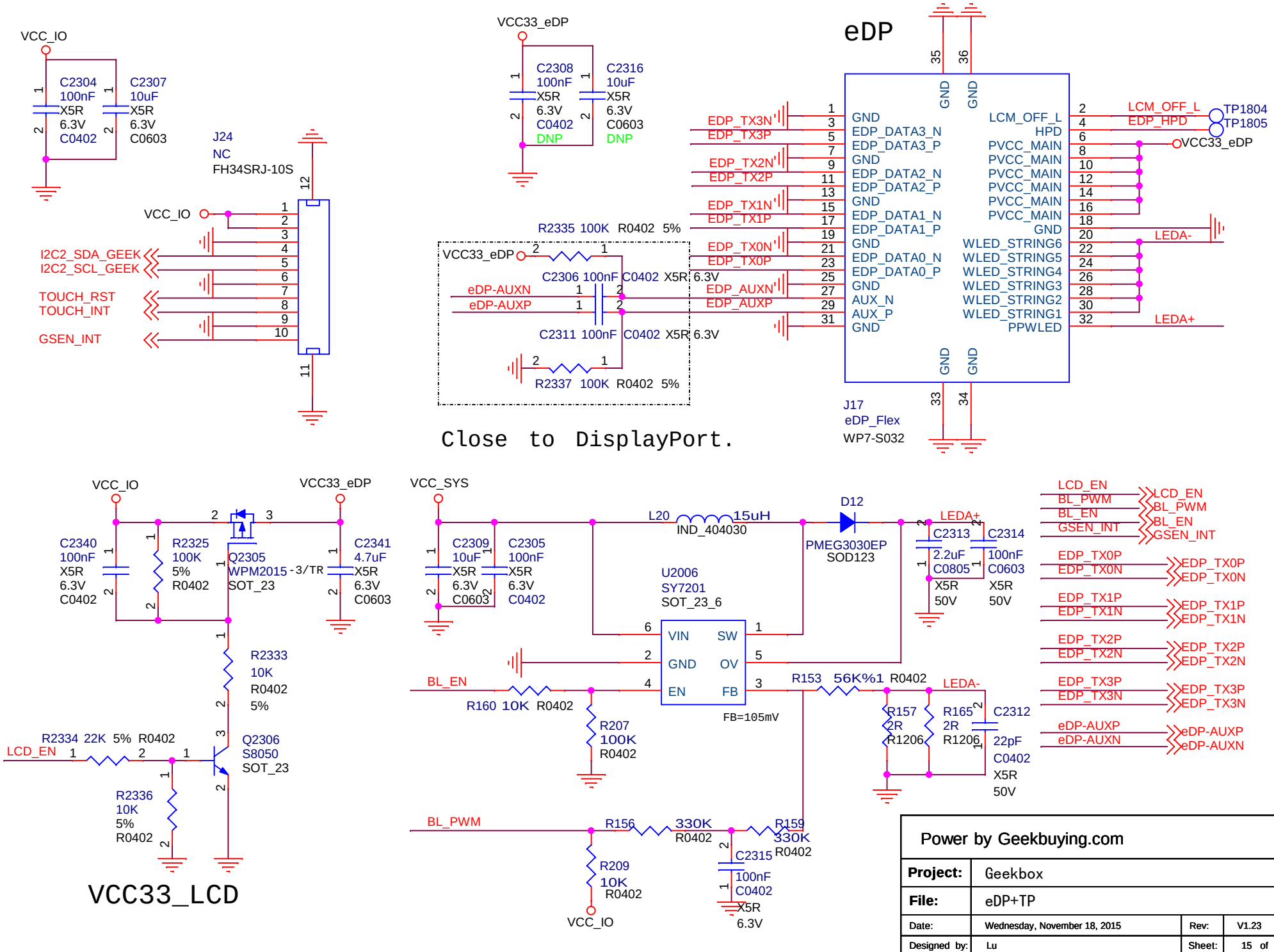

U600C
GPIO3_D4/MAC_TX_CLKO/SPI1_CSN1_d
GPIO3_B0/MAC_TXD0/PWM0/VOP_PWM_d
GPIO3_B1/MAC_TXD1_d
GPIO3_B2/MAC_TXD2_d
GPIO3_B6/MAC_TXD3/GPS_MAG_u
GPIO3_B5/MAC_TXEN_d
GPIO3_B7/MAC_RXD0/GPS_SIG_d
GPIO3_C0/MAC_RXD1/UART3_CTSN/GPS_RFCLK_u
GPIO3_C1/MAC_RXD2/UART3_RTSN/USB_DRVVBUS0_u
GPIO3_C2/MAC_RXD3/USB_DRVVBUS1_d
GPIO3_B3/MAC_CRS_d
GPIO3_B4/MAC_COL_u
GPIO3_D0/MAC_MDIO/I2C4_SDA_u
GPIO3_D1/MAC_RXCLKIN/I2C4_SCL_u
GPIO3_C6/MAC_CLK/ISP_SHUTTERTRIG_d
GPIO3_C4/MAC_RXDV/ISP_FLASHTRIGOUT_u
GPIO3_C5/MAC_RXER/ISP_PRELIGHTTRIG_d
GPIO3_C3/MAC_MDC/ISP_SHUTTEREN_d
GPIO3_C7/EDPHDMI_CEC/ISP_FLASHTRIGIN_u
GPIO3_D2/HDMI_I2C_SDA/I2C5_SDA_u
GPIO3_D3/HDMI_I2C_SCL/I2C5_SCL_u
GPIO3_D5/IR_RX/UART3_RX_u
GPIO3_D6/IR_TX/UART3_TX/PWM3/IR_REMOTE_IN_u
APIO1_VDD
RK3368
BGA453_19R00X19R00X1R40
W20 MAC_TXCLK
T18 MAC_TXD0
U19 MAC_TXD1
T20 MAC_TXD2
T19 MAC_TXD3
V19 MAC_TXEN
R1506 22R 5% R0402
R1500 22R 5% R0402
R1501 22R 5% R0402
R1504 22R 5% R0402
R1505 22R 5% R0402
R1502 22R 5% R0402
PHY_TXCLK
PHY_TXD0
PHY_TXD1
PHY_TXD2
PHY_TXD3
PHY_TXEN
AB19 MAC_RXD0
U21 MAC_RXD1
T21 MAC_RXD2
Y23 MAC_RXD3
V22 VIB_CTL
W23 GPIO3_B4_3V3
N18 MAC_MDIO
U18 MAC_RXCLK
W21
R1503 22R 5% R0402
MAC_CLK
C1500
DNP
C0402
W22 MAC_RXDV
P21 GPIO3_C5_3V3
U22 MAC_MDC
U23 HDMI_CEC
T22 I2C5_SDA_HDMI
T23 I2C5_SCL_HDMI
P19 GPIO3_D5_3V3
R21 IR_INT
VCC_IO
N17
C1501
100nF
X5R
6.3V
C0402
VCC_LAN
PHY_TXD0
R1511 4K7 5% R0402
PHY_TXD1
R1510 4K7 5% R0402
PHY_TXD2
R1509 4K7 5% R0402
PHY_TXD3
R1508 4K7 5% R0402
VCC18_FLASH
R1804 10K 5% R0402 FLASH_D0
R1805 10K 5% R0402 FLASH_D1
R1808 10K 5% R0402 FLASH_D2
R1809 10K 5% R0402 FLASH_D3
R1810 10K 5% R0402 FLASH_D4
R1811 10K 5% R0402 FLASH_D5
R1812 10K 5% R0402 FLASH_D6
R1813 10K 5% R0402 FLASH_D7
R1802 10K 5% R0402 FLASH_RDY/EMMC_CMD
FLASH_D0
FLASH_D1
FLASH_D2
FLASH_D3
FLASH_D4
FLASH_D5
FLASH_D6
FLASH_D7
FLASH_WP/EMMC_PWREN
FLASH_RDY/EMMC_CMD
FLASH_DQS/EMMC_CLKO
U1800
FLASH_D0 H3 DATA0
FLASH_D1 H4 DATA1
FLASH_D2 H5 DATA2
FLASH_D3 J2 DATA3
FLASH_D4 J3 DATA4
FLASH_D5 J4 DATA5
FLASH_D6 J5 DATA6
FLASH_D7 J6 DATA7
FLASH_RDY/EMMC_CMD W5 CMD
FLASH_DQS/EMMC_CLKO R1800 22R 5% R0402 W6 CLK
FLASH_WP/EMMC_PWREN U5 RST_n
K2 VDDi
R5 RCLK
R1801 DNP R0402
C1805 100nF X5R 6.3V C0402
TP1800 M9 VSF1
TP1801 M10 VSF2
TP1802 N10 VSF3
TP1803 U10 VSF4
VCCQ1 AA5
VCCQ2 AA3
VCCQ3 Y4
VCCQ4 W4
VCCQ5 K6
VCC1 U9
VCC2 T10
VCC3 N5
VCC4 M6
VSS1 U8
VSS2 R10
VSS3 P5
VSS4 M7
VSS5 H6
VSS6 T5
VSSQ1 AA6
VSSQ2 AA4
VSSQ3 Y5
VSSQ4 Y2
VSSQ5 K4
KLMAG2GEAC-B031
BGA153_13R00X11R00X1R20
VCC18_FLASH
C1800 100nF X5R 6.3V C0402
C1801 100nF X5R 6.3V C0402
C1802 100nF X5R 6.3V C0402
VCC_IO
C1803 100nF X5R 6.3V C0402
C1804 100nF X5R 6.3V C0402
VCC18_FLASH
C1702 4.7uF X5R 6.3V C0603
C1703 100nF X5R 6.3V C0402
Power by Geekbuying.com
Project: Geekbox
File: RK3368 EthernetMAC/GPIO/EMMC
Date: Wednesday, November 18, 2015
Rev: V1.23
Designed by: Lu
Sheet: 13 of 21



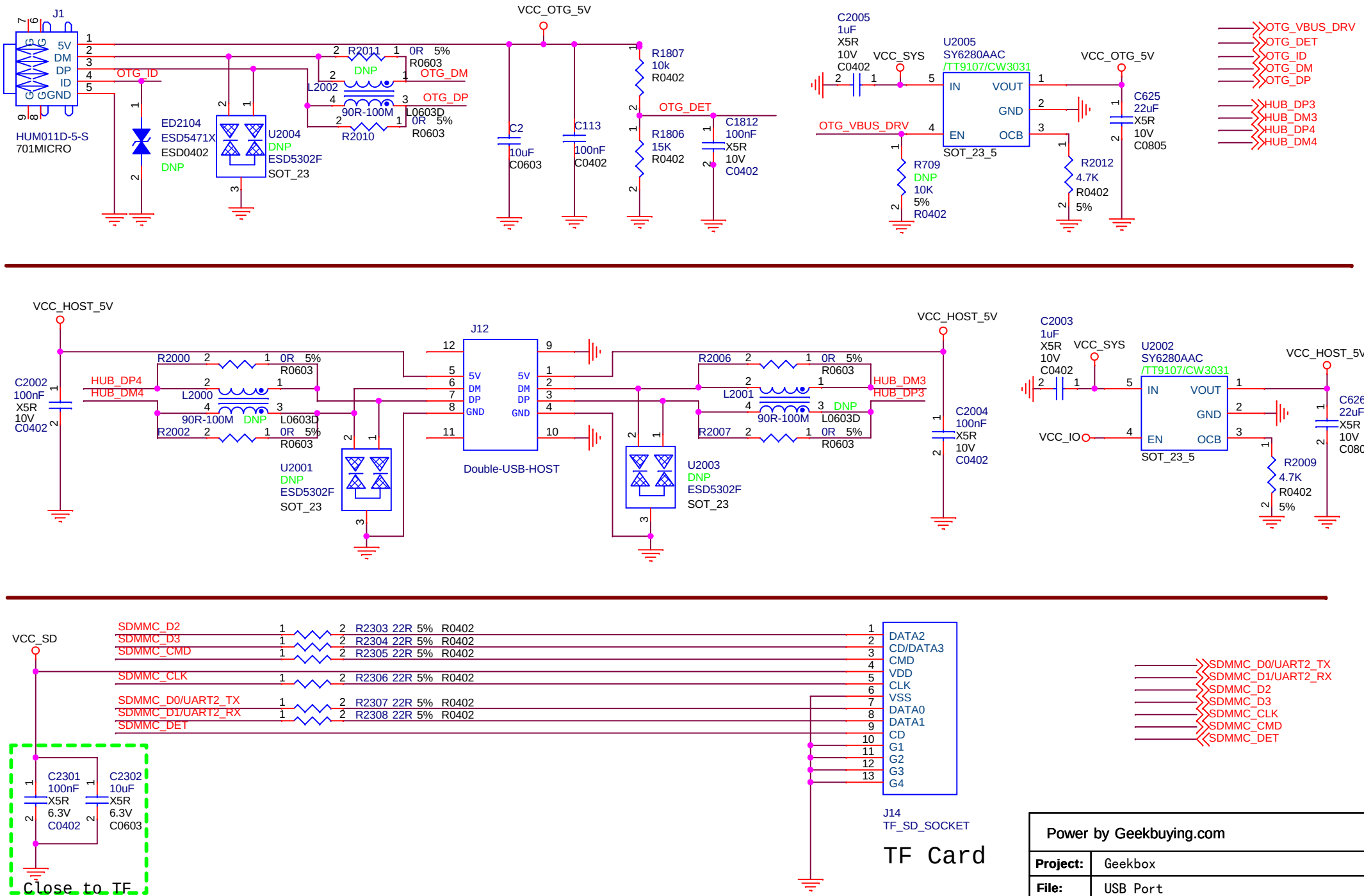
LPDDR3 FILTER



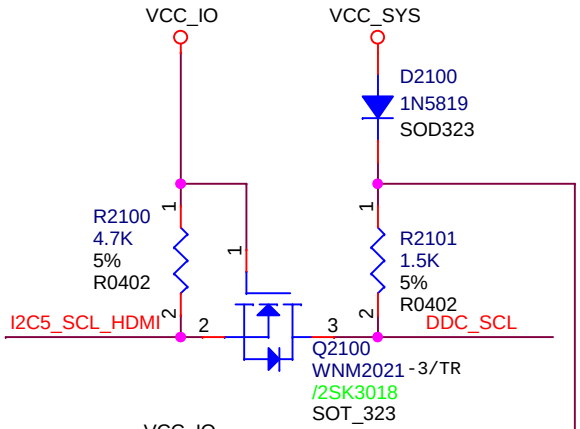
Power by Geekbuying.com			
Project:	Geekbox		
File:	LPDDR3		
Date:	Wednesday, November 18, 2015	Rev:	V1.23
Designed by:	Lu	Sheet:	14 of 21

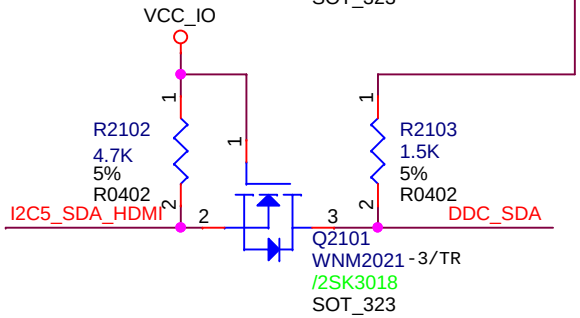


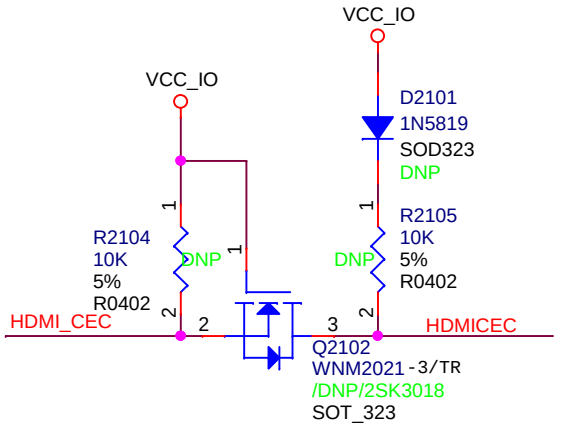
Power by Geekbuying.com			
Project:	Geekbox		
File:	eDP+TP		
Date:	Wednesday, November 18, 2015	Rev:	V1.23
Designed by:	Lu	Sheet:	15 of 21

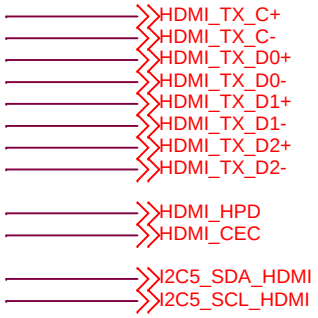


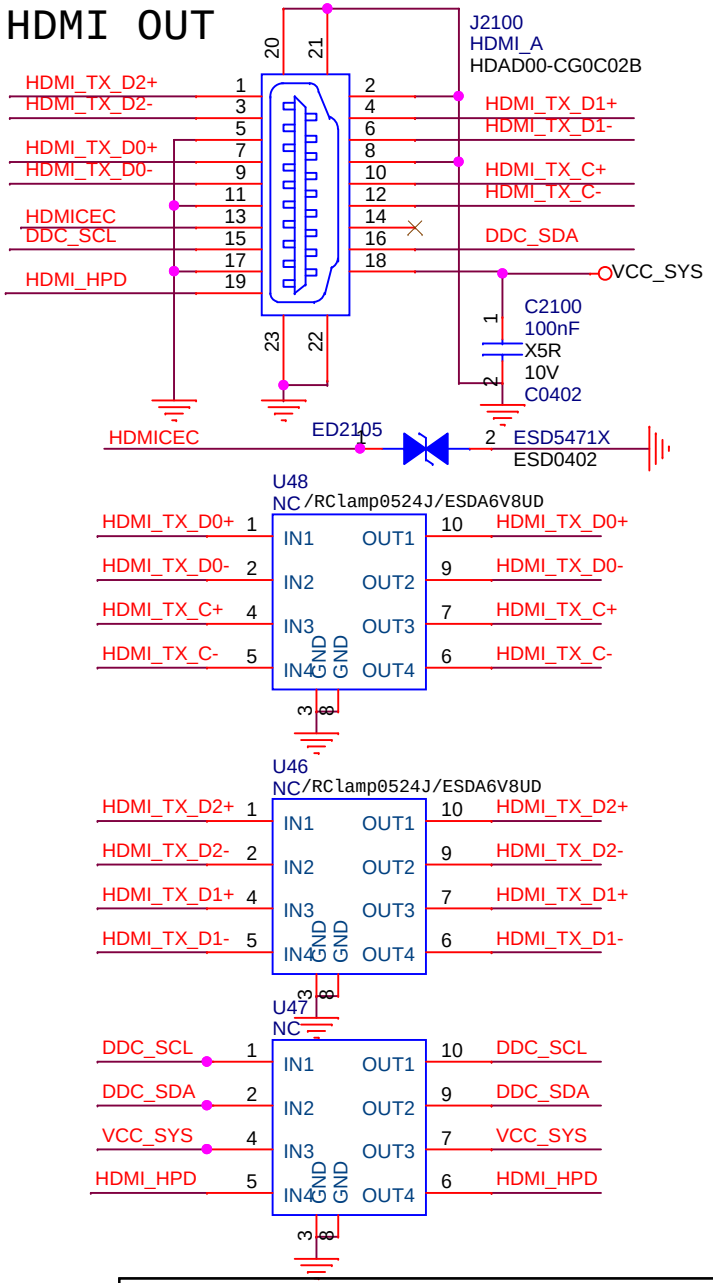
Power by Geekbuying.com	
Project:	Geekbox
File:	USB Port
Date:	Wednesday, November 18, 2015
Rev:	V1.23
Designed by:	Lu
Sheet:	16 of 21



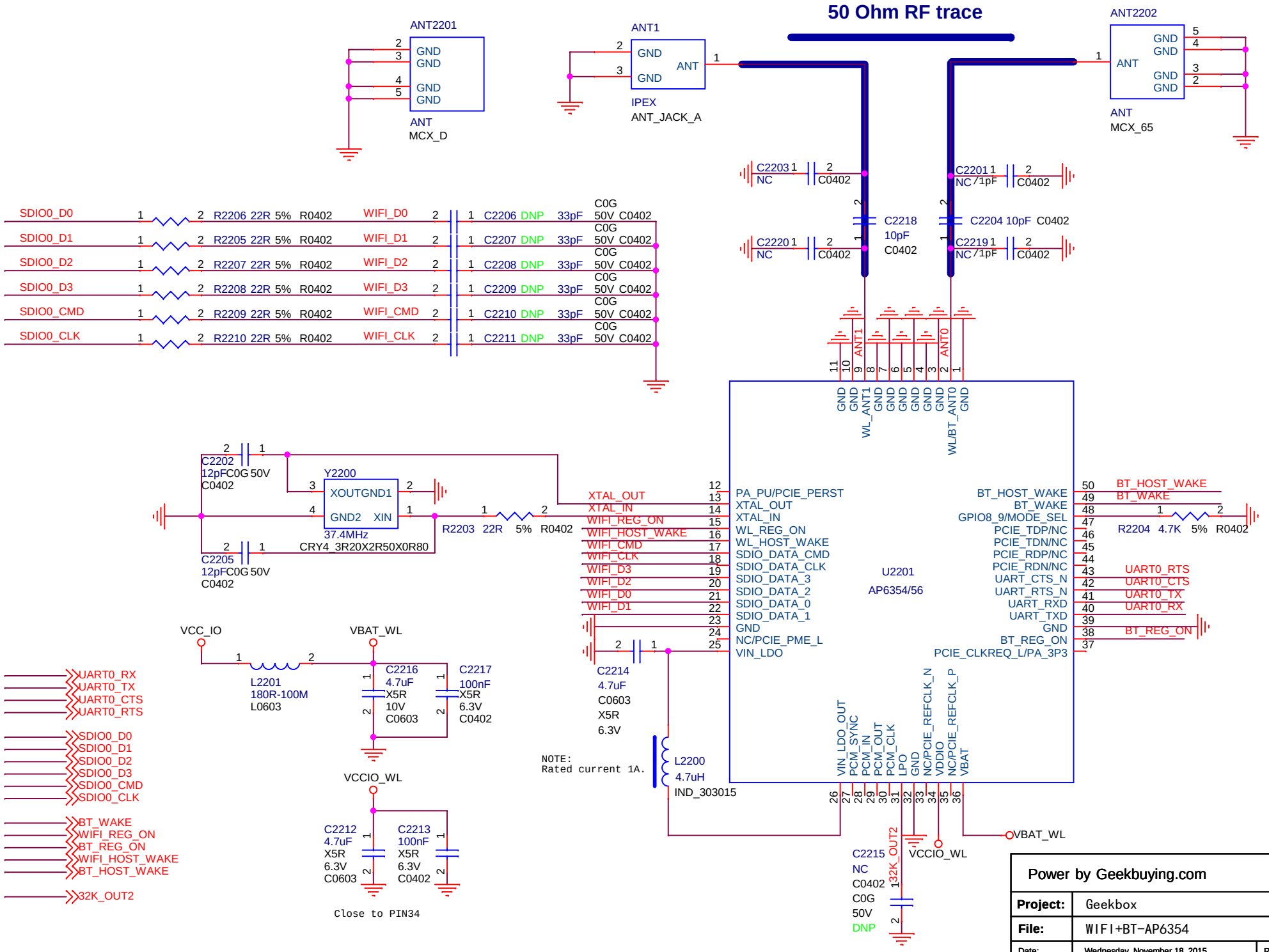


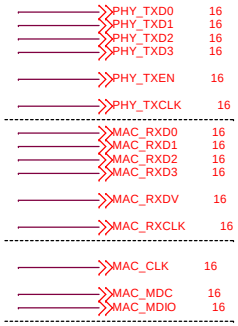


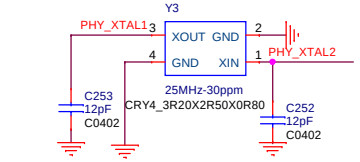




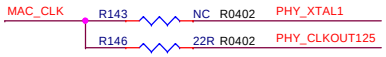
Power by Geekbuying.com			
Project:	Geekbox		
File:	HDMI Out Port		
Date:	Wednesday, November 18, 2015	Rev:	V1.23
Designed by:	Lu	Sheet:	17 of 21

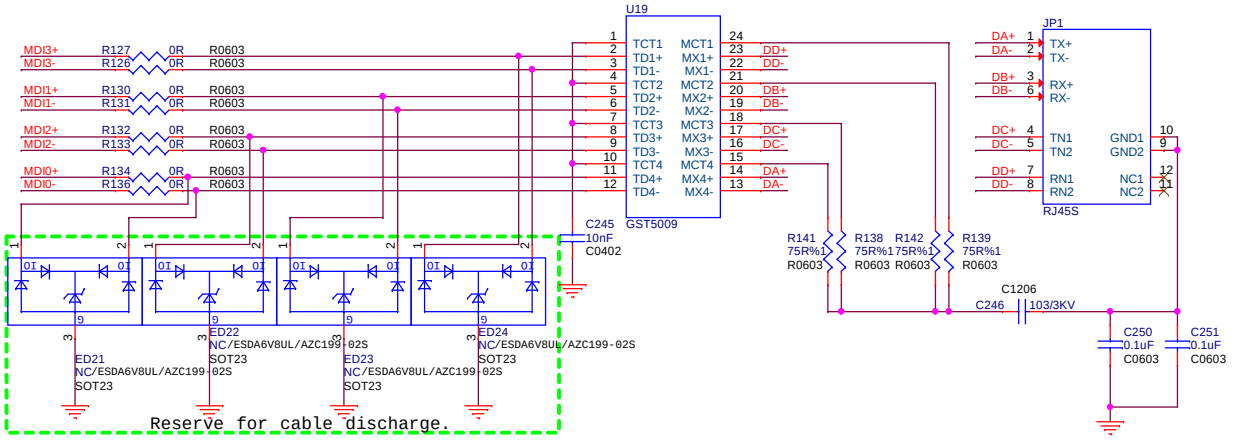

50 Ohm RF trace
ANT2201
GND
GND
GND
GND
ANT
MCX_D
ANT1
GND
GND
ANT
IPEX
ANT_JACK_A
ANT2202
GND
GND
GND
GND
ANT
ANT
MCX_65
C2203 NC C0402
C2201 NC/1pF C0402
C2218 10pF C0402
C2204 10pF C0402
C2220 NC C0402
C2219 NC/1pF C0402
SDIO0_D0
SDIO0_D1
SDIO0_D2
SDIO0_D3
SDIO0_CMD
SDIO0_CLK
R2206 22R 5% R0402
R2205 22R 5% R0402
R2207 22R 5% R0402
R2208 22R 5% R0402
R2209 22R 5% R0402
R2210 22R 5% R0402
WIFI_D0
WIFI_D1
WIFI_D2
WIFI_D3
WIFI_CMD
WIFI_CLK
C2206 DNP 33pF C0G 50V C0402
C2207 DNP 33pF C0G 50V C0402
C2208 DNP 33pF C0G 50V C0402
C2209 DNP 33pF C0G 50V C0402
C2210 DNP 33pF C0G 50V C0402
C2211 DNP 33pF C0G 50V C0402
GND GND WL_ANT1 GND GND GND GND GND GND WL/BT_ANT0 GND
C2202 12pF C0G 50V C0402
Y2200
XOUT GND1
GND2 XIN
37.4MHz
CRY4_3R20X2R50X0R80
C2205 12pF C0G 50V C0402
R2203 22R 5% R0402
XTAL_OUT
XTAL_IN
WIFI_REG_ON
WIFI_HOST_WAKE
WIFI_CMD
WIFI_CLK
WIFI_D3
WIFI_D2
WIFI_D0
WIFI_D1
PA_PU/PCIE_PERST
XTAL_OUT
XTAL_IN
WL_REG_ON
WL_HOST_WAKE
SDIO_DATA_CMD
SDIO_DATA_CLK
SDIO_DATA_3
SDIO_DATA_2
SDIO_DATA_0
SDIO_DATA_1
GND
NC/PCIE_PME_L
VIN_LDO
U2201
AP6354/56
BT_HOST_WAKE
BT_WAKE
GPIO8_9/MODE_SEL
PCIE_TDP/NC
PCIE_TDN/NC
PCIE_RDP/NC
PCIE_RDN/NC
UART_CTS_N
UART_RTS_N
UART_RXD
UART_TXD
GND
BT_REG_ON
PCIE_CLKREQ_L/PA_3P3
R2204 4.7K 5% R0402
UART0_RTS
UART0_CTS
UART0_TX
UART0_RX
BT_REG_ON
VCC_IO
VBAT_WL
L2201 180R-100M L0603
C2216 4.7uF X5R 10V C0603
C2217 100nF X5R 6.3V C0402
C2214 4.7uF C0603 X5R 6.3V
NOTE: Rated current 1A.
L2200 4.7uH IND_303015
VIN_LDO_OUT
PCM_SYNC
PCM_IN
PCM_OUT
PCM_CLK
LPO
GND
NC/PCIE_REFCLK_N
VDDIO
NC/PCIE_REFCLK_P
VBAT
VBAT_WL
UART0_RX
UART0_TX
UART0_CTS
UART0_RTS
SDIO0_D0
SDIO0_D1
SDIO0_D2
SDIO0_D3
SDIO0_CMD
SDIO0_CLK
BT_WAKE
WIFI_REG_ON
BT_REG_ON
WIFI_HOST_WAKE
BT_HOST_WAKE
32K_OUT2
VCCIO_WL
C2212 4.7uF X5R 6.3V C0603
C2213 100nF X5R 6.3V C0402
Close to PIN34
C2215 NC C0402 C0G 50V DNP
32K_OUT2
VCCIO_WL
Power by Geekbuying.com
Project: Geekbox
File: WIFI+BT-AP6354
Date: Wednesday, November 18, 2015
Rev: V1.23
Designed by: Lu
Sheet: 18 of 21



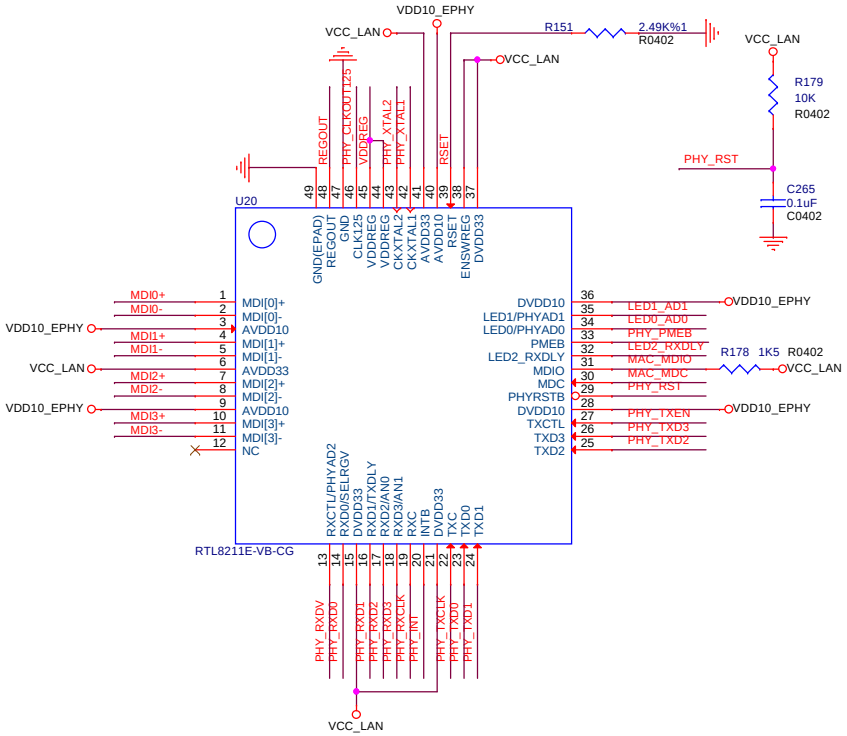


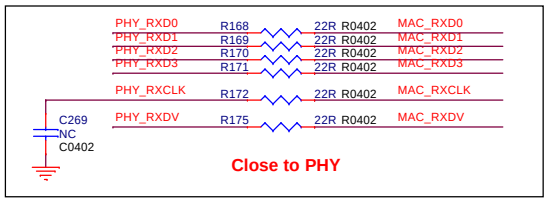
If use external clock
then the XTAL2 need
connect to GND for RTL8211E.



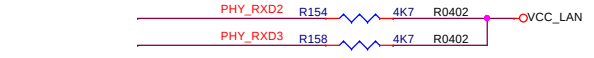


Pin38: Connect ENSWREG to AVDD33 to enable
Switching regulator or connect ENSWREG
to GND to disable Switching regulator.

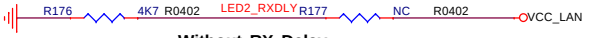




PHY Address=001(RTL8211E)

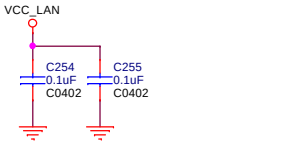


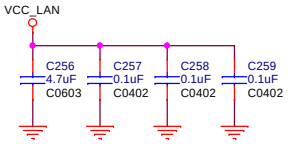
Config for all capability



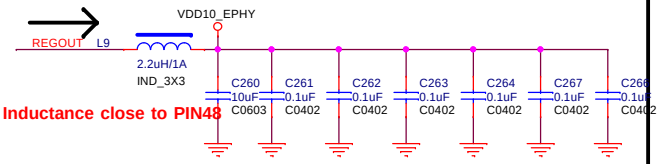
Without RX Delay

Without TX Delay

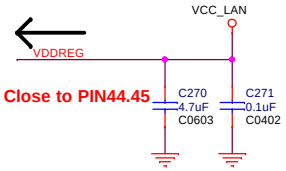




Pull up for 3.3V RGMII (RTL8211D/8211E)

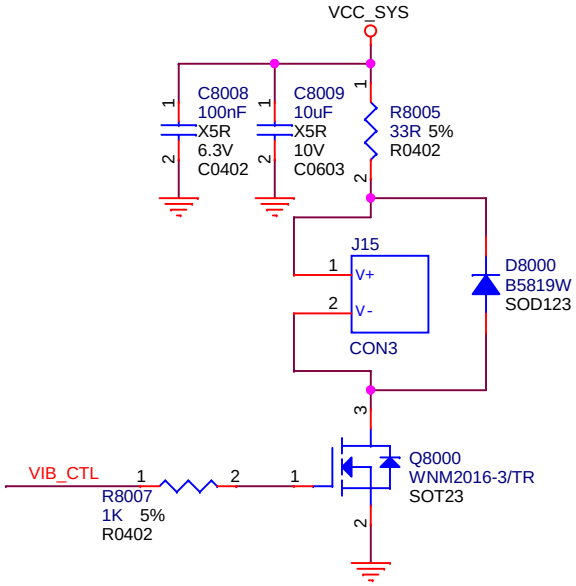


Inductance close to PIN48

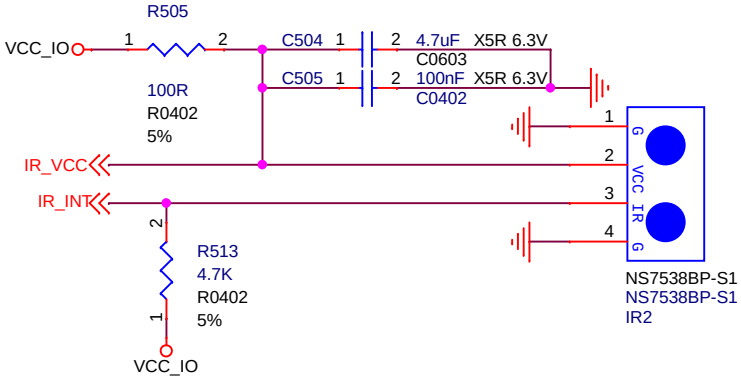


Close to PIN44.45

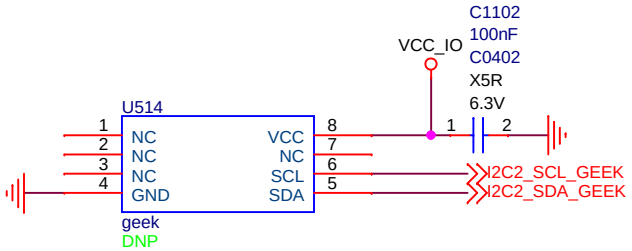
Power by Geekbuying.com			
Project:	Geekbox		
File:	RJ45-10/100/1000M		
Date:	Wednesday, November 18, 2015	Rev:	V1.23
Designed by:	Lu	Sheet:	19 of 21

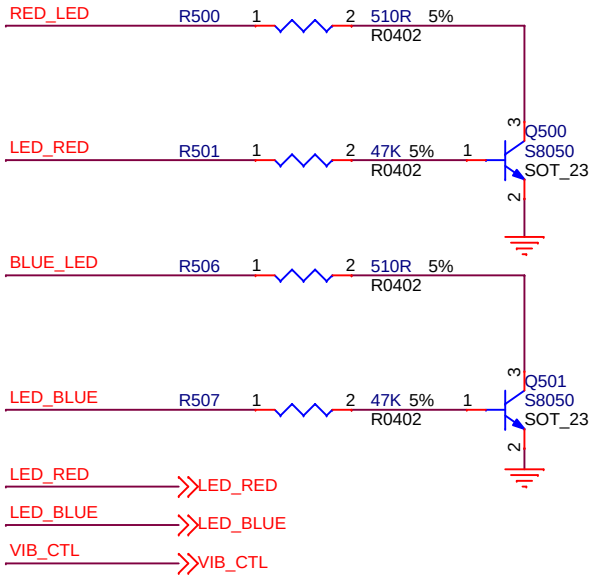


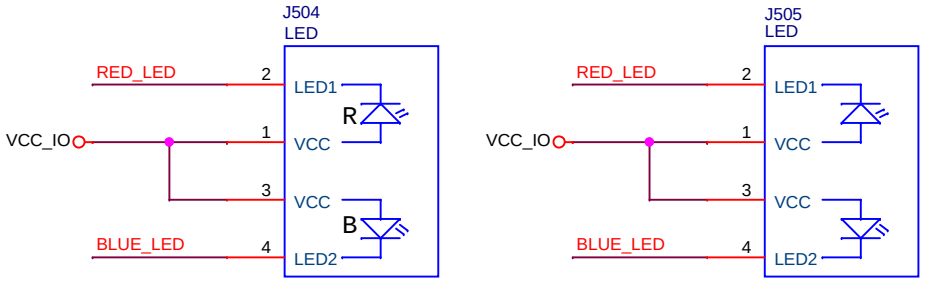
FAN



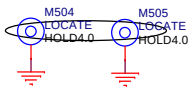
IR Receiver







Power by Geekbuying.com			
Project:	Geekbox		
File:	FAN/LED/IR		
Date:	Wednesday, November 18, 2015	Rev:	V1.23
Designed by:	Lu	Sheet:	20 of 21



Power by Geekbuying.com

Project:	Geekbox		
File:	Edge-Fingers		
Date:	Wednesday, November 18, 2015	Rev:	V1.23
Designed by:	Lu	Sheet:	21 of 21