Syllabus

<table>
<tr><td>Course code</td><td>ECE 358</td><td>Course name</td><td colspan="2">Digital System Design</td><td>credits</td><td>3</td></tr>
<tr><td rowspan="3">Instructor</td><td colspan="3">Name : Hyokeun Lee</td><td colspan="3">Homepage : https://relacslab.github.io/</td></tr>
<tr><td colspan="3">E-Mail : hyokeunlee@ajou.ac.kr</td><td colspan="3">Office : 원천관 403</td></tr>
<tr><td colspan="6">Office hour : appointment is recommended</td></tr>
<tr><td>1. Goals</td><td colspan="6">In this course, we will study and use Verilog HDL -- the most popular HDL today. Further, we will also explore various advanced design methodologies (e.g., FSM, ASM, pipeline) that are essential design components in computer systems.</td></tr>
<tr><td>2. Textbooks</td><td colspan="6">Ming-Bo Lin, "Digital System Designs and Practices : Using Verilog HDL and FPGAs"</td></tr>
<tr><td>3. Prerequisites</td><td colspan="6">▪ Logic Design
▪ Electronic Circuit</td></tr>
<tr><td rowspan="2">4. Ratings (%)</td><td>Attendance</td><td>Homework</td><td>Mid-term</td><td>Final-term</td><td>Project</td><td>Others</td><td>Overall</td></tr>
<tr><td>10</td><td>20</td><td>35</td><td>35</td><td>0</td><td>0</td><td>100</td></tr>
<tr><td rowspan="16">5. Agenda</td><td>Week</td><td colspan="5">Contents</td></tr>
<tr><td>1</td><td colspan="5">Introduction to Digital System Design</td></tr>
<tr><td>2</td><td colspan="5">Verilog HDL and FPGA</td></tr>
<tr><td>3</td><td colspan="5">Basic Combinational Logic in Verilog</td></tr>
<tr><td>4</td><td colspan="5">Advanced Design: Arithmetic Units (1)</td></tr>
<tr><td>5</td><td colspan="5">Advanced Design: Arithmetic Units (2)</td></tr>
<tr><td>6</td><td colspan="5">Basic Sequential Logic in Verilog</td></tr>
<tr><td>7</td><td colspan="5">Advanced Design: Finite State Machines (1)</td></tr>
<tr><td>8</td><td colspan="5">Mid-Term Exam</td></tr>
<tr><td>9</td><td colspan="5">Advanced Design: Finite State Machines (2) and ASM Charts</td></tr>
<tr><td>10</td><td colspan="5">Sequential Logic Use Cases: Counters and Shift Registers</td></tr>
<tr><td>11</td><td colspan="5">Synchronous Designs & Design Issues</td></tr>
<tr><td>12</td><td colspan="5">Memory Technologies: ROM and RAMs</td></tr>
<tr><td>13</td><td colspan="5">New Memory Technologies</td></tr>
<tr><td>14</td><td colspan="5">Architecture-level Simulation</td></tr>
<tr><td>15</td><td colspan="5">Final-Term Exam</td></tr>
<tr><td>6. Notes for students</td><td colspan="6">▪ F will be given if cheating is caught no matter what case is
▪ One grade lower if not taking either mid-term or final-term exam
▪ This class has Verilog homework assignments, please refrain from taking this class if you have not taken "Digital System Design" class</td></tr>
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