Syllabus

Course code	ECE 358	Course name	Digital System Design	credits	3
Instructor	Name : Hyokeun Lee		Homepage : https://relacslab.github.io/		
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	Office hour : appointment is recommended				
1. Goals	In this course, we will study and use Verilog HDL -- the most popular HDL today. Further, we will also explore various advanced design methodologies (e.g., FSM, ASM, pipeline) that are essential to modern digital designs.				
2. Textbooks	Ming-Bo Lin, "Digital System Designs and Practices : Using Verilog HDL and FPGAs"				
3. Prerequisites	▪ Logic Design ▪ Electronic Circuit				

4. Ratings (%)	Attendance	Homework	Mid-term	Final-term	Project	Others	Overall
	5	10	30	30	25	0	100

5. Agenda	Week	Contents
	1	Introduction to Digital System Design
	2	Verilog HDL and FPGA
	3	Basic Combinational Logic in Verilog
	4	Advanced Design: Arithmetic Units (1)
	5	Advanced Design: Arithmetic Units (2)
	6	Basic Sequential Logic in Verilog
	7	Advanced Design: Finite State Machines (1)
	8	Mid-Term Exam
	9	Advanced Design: Finite State Machines (2) and ASM Charts
	10	Sequential Logic Use Cases: Counters and Shift Registers
	11	Synchronous Designs & Design Issues
	12	Memory Technologies: ROM and RAMs
	13	New Memory Technologies
	14	Architecture-level Simulation
	15	Final-Term Exam

6. Notes for students	▪ F will be given if cheating is caught no matter what case is ▪ One grade lower if not taking either mid-term or final-term exam