

Syllabus

Course code	CSE 305	Course name	Computer Architecture				credits	3
Instructor	Name : Hyokeun Lee				Homepage : https://relacslab.github.io/			
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	Office hour : appointment is required							
1. Goals	Like skyscrapers, well-architecting a system that incorporates delicate, bleeding-edge technologies is pressing. This lecture covers the basics of computer architecture, including pipeline designs, memory managements, and some issues related to caches (e.g., policies and coherence). There will be <i>two</i> term projects based on an RTL design and an architecture simulator.							
2. Textbooks	Main: Patterson and Hennessy, "Computer Organization and Design (MIPS Edition)" Sub: Research Papers							
3. Prerequisites	<ul style="list-style-type: none">Logic Design (e.g., gates, flip-flops...)Digital System Design (e.g., Verilog HDL)C/C++ programming-related classes							
4. Ratings (%)	Attendance	Homework	Mid-term	Final-term	Project	Others	Overall	
	5	0	30	35	30	0	100	
5. Agenda	Week	Contents						
	1	Introduction to Computer Architecture						
	2	Instruction Set Architecture (1)						
	3	Instruction Set Architecture (2)						
	4	Single- & Multi-Cycle Microarchitectures						
	5	Pipelined Microarchitecture: Introduction						
	6	Pipelined Microarchitecture: Data Hazard and its Handling						
	7	Pipelined Microarchitecture: Control Hazard and its Handling						
	8	Mid-Term Exam						
	9	Advanced Microarchitectures						
	10	Memory Systems: Cache (1)						
	11	Memory Systems: Cache (2)						
	12	Memory Systems: Cache (3)						
	13	Memory Systems: Virtual Memory						
	14	IO Devices and Managements						
	15	Final-Term Exam						
6. Notes for students	<ul style="list-style-type: none">F will be given if cheating is caught no matter what the case isOne grade lower if not taking either mid-term or final-term examThis class has a Verilog project							