Hyokeun Lee
Ph.D.

Assistant Professor

Department of Electrical and Computer Engineering

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RESEARCH INTERESTS

- Disaggregated memory, disaggregation, SoC security, Compute-Express Link (CXL), non-volatile memory, memory system, computer architecture

WORK EXPERIENCE

•**Department of Electrical and Computer Engineering, Ajou University**   *Mar. 2024 - Present*

Assistant Professor   Gyeonggi, South Korea

•**Secure and Advanced Computer Architecture Group, North Carolina State University**   *Feb. 2023 - Jan. 2024*

Postdoctoral researcher   Raleigh

– Mentor: Dr. Amro Awad

•**Inter-university Research Center, Seoul National University**   *Sep. 2021 - Feb. 2023*

Postdoctoral researcher   Seoul, South Korea

– Mentor: Dr. Hyuk-Jae Lee

– I also served the mandatory military service as a Technical Research Personnel.

EDUCATION

•**Seoul National University, Seoul, South Korea**   *Sep. 2016-Aug. 2021*

Ph.D. Electrical and Computer Engineering

– Advisor: Dr. Hyuk-Jae Lee; Co-advisor: Dr. Hyun Kim

– Dissertation: Mitigating Disturbance Errors and Enhancing RMW Performance for PCM

•**Seoul National University, Seoul, South Korea**   *Sep. 2011 - Aug. 2016*

B.S. Electrical and Computer Engineering

RESEARCH PROJECTS

•**Enabling Secure and Efficient Sharing of Accelerators in Expeditionary Systems**

Sponsor: Office of Naval Research, United States

– Mar. 2023 - Jan. 2024

– Development of secure hardware in an accelerator-rich architecture

– Development of secure GPU with CXL memory expansion

– Mentoring students research

•**Towards Secure, Crash Recoverable and High-Performance Memory Systems in Future Expeditionary Tactical Systems**

Sponsor: Office of Naval Research, United States

– Mar. 2023 - Jan. 2024

– Development of user-transparent secure compiler

– Mentoring students research

•**Parallel Architecture for Native Data-Graph Analytics Operation**

Sponsor: AMD Research, United States

– Mar. 2023 - Jan. 2024

– Development of high-performance and secure access control in disaggregated memory systems

– Mentoring students research

•**Optimization of Type-3 Compute Express Link (CXL) Add-In Card (AIC) Memory**

Sponsor: SK Hynix

– Feb. 2022 - Jan. 2023

– Developed an in-house simulation platform for CXL memory devices

– Broke down the performance of the CXL-attached system under various scenarios

– Optimization of memory-centric workloads (e.g., NLP) on the CXL-attached system

- **Development of Open Convergence Memory Solution and Platform for Next-Generation Memories**

  Sponsor: Ministry of Trade, Industry & Energy (MOTIE), South Korea
  - April. 2020 - Dec. 2022
  - Developed a high-performance and low-power PCM-based computer architecture for CNN inference
  - Developed reliable PCM-based systems

- **DRAM/PRAM Heterogeneous Memory Architecture and Controller IC Design Technology R&D**

  Sponsor: Ministry of Trade, Industry & Energy (MOTIE), South Korea
  - July. 2017 - Dec. 2021
  - Constructed reliable PRAM technologies concerning endurance and write/read disturbance errors
  - Developed an FPGA-based heterogeneous memory system emulation platform

- **Architecture Exploration of a Hardwired PCM Controller**

  Sponsor: SK Hynix
  - July. 2020 - June. 2021
  - Characterized the performance of the in-house PCM controller simulator developed in the previous year
  - Minimized the performance overhead of accessing the DRAM-based address translation table in the PCM controller

- **PRAM Memory Scheduler Modeling and its Verification against RTL**

  Sponsor: SK Hynix
  - July. 2019 - June. 2020
  - Developed an in-house, functional- and cycle-accurate PCM controller simulator
  - Validated functionality and cycle accuracy against the industrial RTL simulation trace

- **Schemes for Managing Metadata in PCRAM Software Wear-leveling**

  Sponsor: SK Hynix
  - July. 2017 - June. 2018
  - Developed a PCRAM simulation environment using NVMain and gem5
  - Minimized the performance overhead of the read-modify-write module in a PCRAM system
  - Enhanced the lifetime of PCRAM with the table-based and static wear-leveling

- **Management on Non-volatile Memory Systems**

  Sponsor: SK Hynix
  - Sep. 2016 - June. 2017
  - Developed a hot address-based wear-leveling for PRAM

- **Development of Parallel Processing Techniques for Computational Imaging**

  Sponsor: Korea Electrotechnology Research Institute (KERI), South Korea
  - Sep. 2016 - Nov. 2017
  - Developed an algorithm for improving the image quality under surgery environment
  - Accelerated the above algorithm using FPGA

PUBLICATIONS

#: co-first author; *: (co-)corresponding author

- **Conference**

  - Jihoon Jang, Hyokeun Lee*, Hyun Kim*, "*EDeN: Enabling Low-Power CNN Inference on Edge Devices Using Prefetcher-Assisted NVM Systems*," ACM/IEEE International Symposium on Lower Power Electronics and Design (ISLPED), Aug. 2024.
  - Debpratim Adak, Hyokeun Lee, Ben Feinberg, Gwendolyn Voskuilen, Clayton Hughes, Huiyang Zhou, Amro Awad, "*SEFsim: A Statistically-Guided Fast DRAM Simulator*," IEEE International Symposium on Performance Analysis of Systems and Software (ISPASS), May. 2024 (Poster).
  - Rahaf Abdullah, Hyokeun Lee, Huiyang Zhou, Amro Awad, "*Salus: Efficient Security Support for CXL-Expanded GPU Memory*," International Symposium on High-Performance Computer Architecture (HPCA), Mar. 2024.
  - Faiz Alam#, Hyokeun Lee#, Abhishek Bhattacharjee, Amro Awad, "*CryptoMMU: Enabling Scalable and Secure Access Control of Third-Party Accelerators*," IEEE/ACM International Symposium on Microarchitecture (MICRO), Oct-Nov. 2023 (**Best Paper Candidate**).
  - Hyokeun Lee, Kwanseok Choi, Hyuk-Jae Lee, Jaewoong Sim, "*SDM: Sharing-enabled Disaggregated Memory System with Cache Coherent Compute Express Link*," International Conference on Parallel Architectures and Compilation Techniques (PACT), Oct. 2023.
  - Shubham Nema, Shiva Kaushik Chunduru, Charan Kodigal, Gwendolyn Voskuilen, Scott Hmmert, Hyokeun Lee, Amro Awad, Clayton Hughes, "*ERAS: A Flexible and Scalable Framework for Seamless Integration of RTL models with Structural Simulation Toolkit*," IEEE International Symposium on Workload Characterization (IISWC), Oct. 2023 (Poster).

- <u>Hyokeun Lee</u>, Hyungsuk Kim, Seokbo Shim, Seungyong Lee, Dosun Hong, Hyuk-Jae Lee, Hyun Kim, "*PCMCsim: An Accurate Phase-Change Memory Controller Simulator and its Performance Analysis*," IEEE International Symposium on Performance Analysis of Systems and Software (ISPASS), May. 2022.
- Hyeong Gi Seong, <u>Hyokeun Lee</u>, Hyun Kim, Hyuk-Jae Lee, "*Analysis of Hardware Prefetchers Suitable for CNN Applications*," IEEE/IEIE International Conference on Consumer Electronics-Asia (ICCE-Asia), Nov. 2021.
- <u>Hyokeun Lee</u>, Seungyong Lee, Moonsoo Kim, Hyun Kim, Hyuk-Jae Lee, "*IMDB: A Low-Cost In-Module Disturbance Barrier for Mitigating Write Disturbance Errors in Phase-Change Memory*," Design Automation Conference (DAC, *work-in-progress session*), July. 2020.
- <u>Hyokeun Lee</u>, Donghyeon Lee, Hyuk-Jae Lee, "*A Predictive Initialization of Hidden State Parameters in a Hidden Markov Model for Hand Gesture Recognition*," IEEE/IEIE International Conference on Consumer Electronics-Asia (ICCE-Asia), June. 2018.

•**Journal**

- <u>Hyokeun Lee</u>, Seungyong Lee, Byeongki Song, Moonsoo Kim, Seokbo Shim, Hyuk-Jae Lee, Hyun Kim, "*An In-Module Disturbance Barrier for Mitigating Write Disturbance in Phase-Change Memory*," IEEE Transactions on Computers, April. 2023.
- <u>Hyokeun Lee</u>, Hyuk-Jae Lee, Hyun Kim, "*A Read Disturbance Tolerant Phase Change Memory System for CNN Inference Workloads*," Journal of Semiconductor Technology and Science, Aug. 2022.
- Moonsoo Kim, <u>Hyokeun Lee</u>, Hyun Kim, Hyuk-Jae Lee, "*WL-WD: Wear-Leveling Solution to Mitigate Write Disturbance Errors for Phase-Change Memory*," IEEE Access, Feb. 2022.
- Seungyong Lee, <u>Hyokeun Lee</u>, Hyuk-Jae Lee, Hyun Kim, "*Evaluation of Various Workloads in Filebench Suitable for Phase-change Memory*," IEIE Transactions on Smart Processing & Computing, April. 2021.
- <u>Hyokeun Lee</u>, Hyunmin Jung, Hyuk-Jae Lee, Hyun Kim, "*Bit-width Reduction in Write Counters for Wear Leveling in a Phase-change Memory System*," IEIE Transactions on Smart Processing & Computing, Oct. 2020.
- Jinwoo Park, <u>Hyokeun Lee</u>, Boyeal Kim, Dong-Goo Kang, Seung Oh Jin, Hyun Kim, Hyuk-Jae Lee, "*A Low-Cost and High-Throughput FPGA Implementation of the Retinex Algorithm for Real-Time Video Enhancement*," IEEE Transactions on Very Large Scale Integration Systems, Jan. 2020.
- <u>Hyokeun Lee</u>, Moonsoo Kim, Hyunchul Kim, Hyun Kim, Hyuk-Jae Lee, "*Integration and Boost of a Read-Modify-Write Module in Phase Change Memory System*," IEEE Transactions on Computers, Dec. 2019.
- Sunwoong Kim, Hyunmin Jung, Woojae Shin, <u>Hyokeun Lee</u>, Hyuk-Jae Lee, "*HAD-TWL: Hot Address Detection-based Wear Leveling for Phase-Change Memory Systems with Low Latency*," IEEE Computer Architecture Letters, July. 2019.

•**Patents**

- "*Mitigating Write Disturbance Errors of Phase-Change Memory Module*," US Patent, No. 11462266, Oct. 2022. (Granted)
- "*Semiconductor Memory Device Performing Command Merging and Operating Method Thereof*," US Patent, No. 11055025, July. 2021. (Granted)
- "*Semiconductor Device for Managing Cold Addresses of Nonvolatile Memory Device*," US Patent, No. 10877698, Dec. 2020. (Granted)
- "*Semiconductor Device for Managing Wear Leveling Operation of a Nonvolatile Memory Device*," US Patent, No. 10713159, July. 2020. (Granted)

PROFESSIONAL ACTIVITIES

•**2025**
- Reviewer, IEEE Transactions on Dependable and Secure Computing
- Program Committee, IEEE International Parallel & Distributed Processing Symposium (IPDPS)

•**2024**
- Reviewer, IEEE Transactions on Computers
- Reviewer, ACM Transactions on Architecture and Code Optimization
- Reviewer, Springer The Journal of Supercomputing
- Program Committee, The 42nd IEEE International Conference on Computer Design (ICCD)
- Program Committee, Great Lakes Symposium on VLSI (GLSVLSI)
- Reviewer, International Conference on Electronics, Information, and Communication (ICEIC)

•**2023**
- Program Committee, The 41st IEEE International Conference on Computer Design (ICCD)
- Reviewer, IEEE Conference on Artificial Intelligence Circuits and Systems (AICAS)
- Reviewer, IEIE Transactions on Smart Processing and Computing

- **2022**
  - Session Chair, The 40th IEEE International Conference on Computer Design (ICCD)
  - Program Committee, The 40th IEEE International Conference on Computer Design (ICCD)
  - Reviewer, Elsevier Microelectronics Journal
  - Reviewer, IEEE Conference on Artificial Intelligence Circuits and Systems (AICAS)

- **2021**
  - Reviewer, Material Research Bulletin, Journal, Elsevier
  - Technical Program Committee, IEEE /IEIE International Conference on Consumer Electronics Asia (ICCE-ASIA)
  - Reviewer, IEIE Transactions on Smart Processing and Computing

LECTURES & INVITED TALKS

- "*Towards Large-Scale Computing Systems via Resource Disaggregation*," Seoul National University of Science and Technology, South Korea, Dec. 2024
- "*Disaggregation and its Security for Large-Scale Computing Systems*," Korea University, South Korea, Aug. 2023.
- "*CXL-enabled Sharing in a Multi-Host Disaggregated Memory System*," Seoul National University GoGE Workshop: Future Generation Security Computing Systems, Aug. 2023.
- "*Introduction to Computer Architecture Simulators and Use of Gem5*," North Carolina State University (ECE 096), United States, Mar. 2023.
- "*Bitwidth Reduction of Write Counters of Wear Leveling in a Phase-Change Memory System*," KSPC, South Korea, Sep. 2022.
- "*Introduction to Computer Architecture Simulators and their Examples*," University of Seoul, South Korea, Jun. 2022.

TECHNICAL SKILLS

Programming: C++, C, Verilog, Python
Architecture Simulators: NVMain, PCMCsim, DRAMsim3, McSimA+, MacSim, gem5
Commercial Software: ModelSim, Vivado, Quartus
Hardware Interface (Transaction Level): AXI-Lite/-Full/-Stream, CXL, PCIe, I2C, JEDEC DDRx
Languages: English (Professional working proficiency), Korean (Native), Chinese (Bilingual)