Syllabus

<table>
<tr><td>Course code</td><td>ECE 352</td><td>Course name</td><td>Computer Organization and Architecture</td><td>credits</td><td>3</td></tr>
<tr><td rowspan="3">Instructor</td><td colspan="3">Name : Hyokeun Lee</td><td colspan="2">Homepage : https://relacslab.github.io/</td></tr>
<tr><td colspan="3">E-Mail : hyokeunlee@ajou.ac.kr</td><td colspan="2">Office : 원천관 403</td></tr>
<tr><td colspan="5">Office hour : appointment is recommended</td></tr>
<tr><td>1. Goals</td><td colspan="5">Similar to skyscrapers, well-architecting a system that incorporates delicate, bleeding-edge technologies is pressing. In this lecture, we will learn the basics of computer architecture, including pipeline designs, memory managements, and some issues related to caches (e.g., policies and coherence). There will be two term projects based on an RTL design and an architecture simulator.</td></tr>
<tr><td>2. Textbooks</td><td colspan="5">Main: Patterson and Hennessy, "Computer Organization and Design (MIPS Edition)"
Sub: (1) Patterson et al., "Computer Architecture: A Quantitative Approach" (2) Research Papers</td></tr>
<tr><td>3. Prerequisites</td><td colspan="5">▪ Logic Design
▪ Digital System Design
▪ C/C++ programming-related classes</td></tr>
<tr><td>4. Ratings (%)</td><td colspan="5"><table>
<tr><td>Attendance</td><td>Homework</td><td>Mid-term</td><td>Final-term</td><td>Project</td><td>Others</td><td>Overall</td></tr>
<tr><td>5</td><td>0</td><td>35</td><td>35</td><td>25</td><td>0</td><td>100</td></tr>
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<tr><td>5. Agenda</td><td colspan="5"><table>
<tr><th>Week</th><th>Contents</th></tr>
<tr><td>1</td><td>Introduction to Computer Architecture</td></tr>
<tr><td>2</td><td>Instruction Set Architecture (1)</td></tr>
<tr><td>3</td><td>Instruction Set Architecture (2)</td></tr>
<tr><td>4</td><td>Single- & Multi-Cycle Microarchitectures</td></tr>
<tr><td>5</td><td>Pipelined Microarchitecture: Introduction</td></tr>
<tr><td>6</td><td>Pipelined Microarchitecture: Data Hazard and its Handling</td></tr>
<tr><td>7</td><td>Pipelined Microarchitecture: Control Hazard and its Handling</td></tr>
<tr><td>8</td><td>Mid-Term Exam</td></tr>
<tr><td>9</td><td>Advanced Microarchitecture: Out-of-Order, Superscalar</td></tr>
<tr><td>10</td><td>Advanced Microarchitecture: Multithreading</td></tr>
<tr><td>11</td><td>Memory Systems: Cache (1)</td></tr>
<tr><td>12</td><td>Memory Systems: Cache (2)</td></tr>
<tr><td>13</td><td>Memory Systems: Virtual Memory</td></tr>
<tr><td>14</td><td>IO Devices and Managements</td></tr>
<tr><td>15</td><td>Final-Term Exam</td></tr>
</table></td></tr>
<tr><td>6. Notes for students</td><td colspan="5">▪ F will be given if cheating is caught no matter what case is
▪ One grade lower if not taking either mid-term or final-term exam
▪ This class has a Verilog project, please refrain from taking this class if you have not taken "Digital System Design" class</td></tr>
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