EE 382M-14: Final Project
Fully-Differential Folded-Cascode Amplifier

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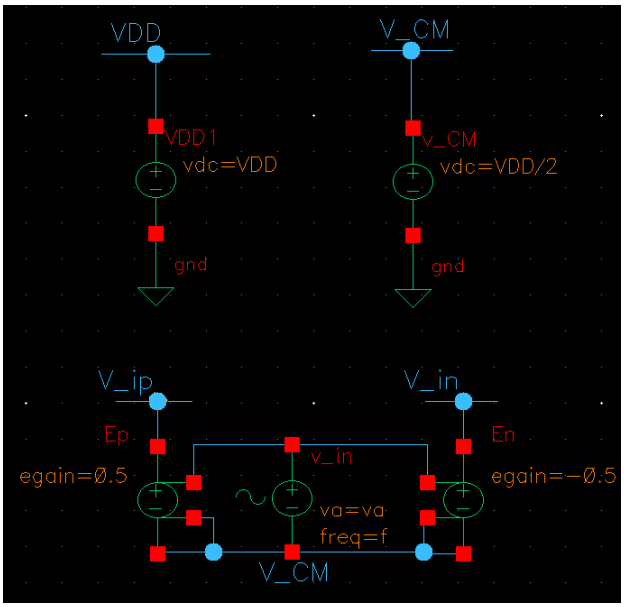
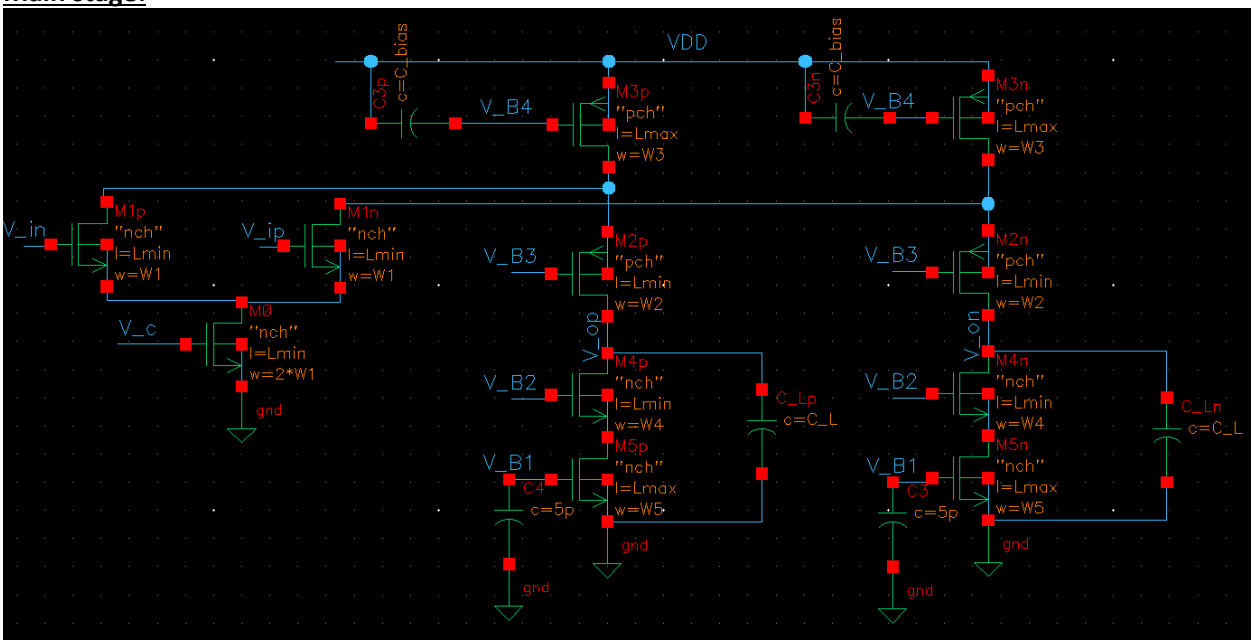
Design Schematic

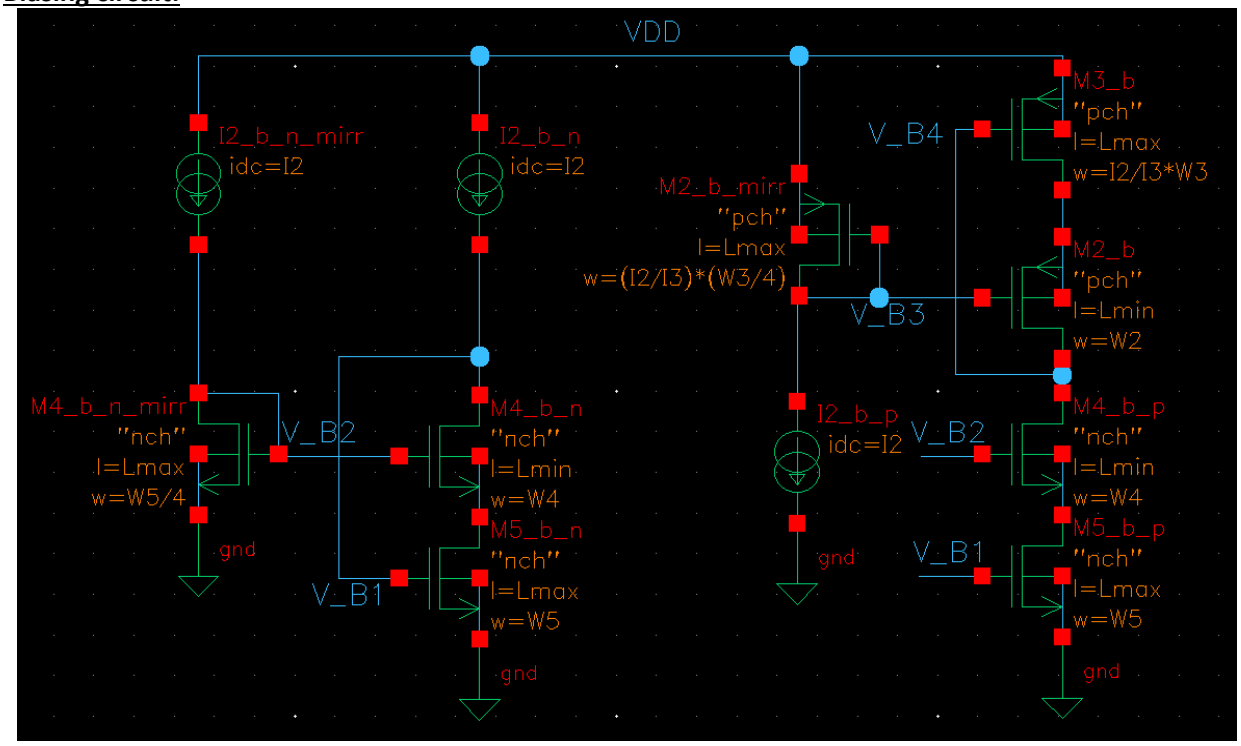
Input Sources:



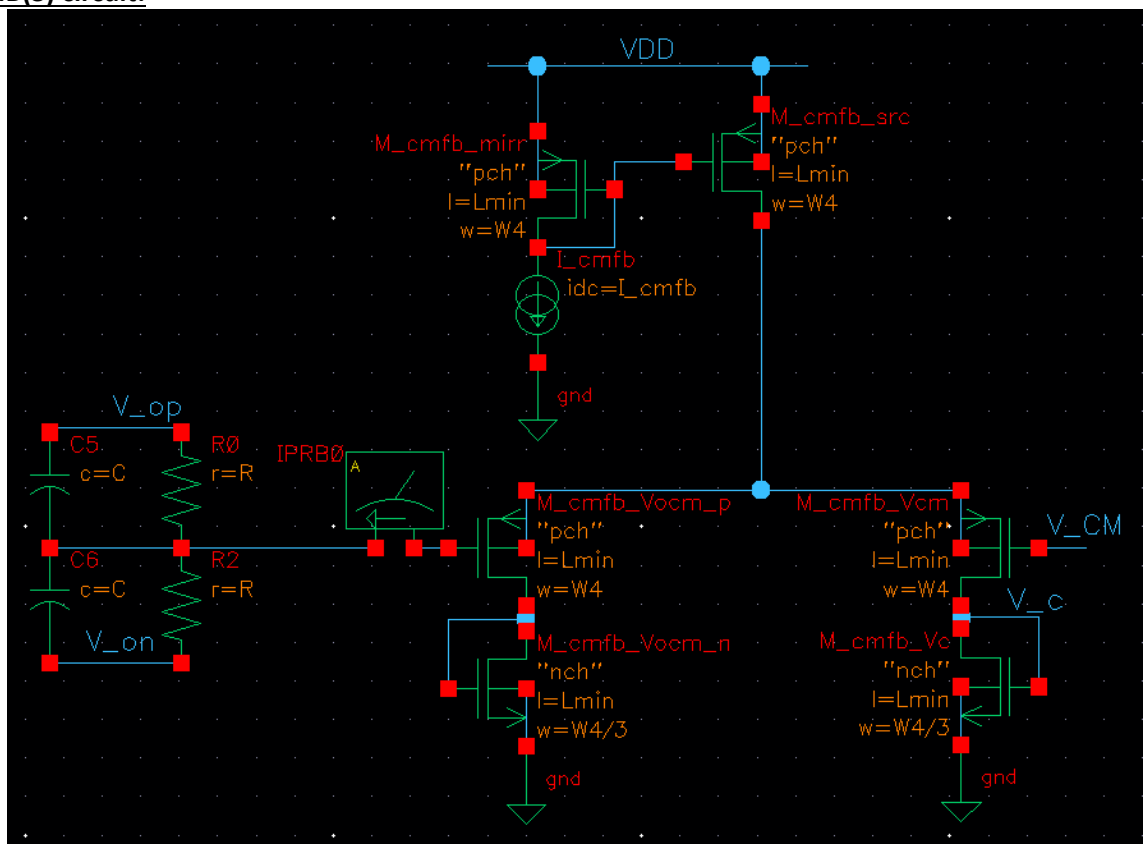
Main stage:



Biasing circuit:



CFMB(3) circuit:



Design Variables:

	Name	Value
1	va	810u
2	I_cmfb	66u
3	I1	220u
4	I2	50u
5	I3	270u
6	W1	36u
7	W2	40u
8	W3	138u
9	W4	12u
10	W5	9u
11	Lmin	180n
12	Lmax	500n
13	R	1M
14	C	15f
15	C_bias	5p
16	VDD	1.8
17	f	10K
18	C_L	5p

Calculations and Analysis

1. **Overdrive voltages:**

$$\Delta V_{o,pk-pk} = 1.4\,V$$
$$V_{DD} = 1.8\,V$$

$$|V_{ov_2}| + |V_{ov_3}| = V_{ov_4} + V_{ov_5} = \frac{V_{DD} - \Delta V_{o,pk-pk}}{2} = \frac{1.8 - 1.4}{2} = 0.2\,V$$

$$|V_{ov_2}| < |V_{ov_3}| \Rightarrow \boldsymbol{|V_{ov_2}|} = \mathbf{0.05\,V}\ (cascode)\ and\ \boldsymbol{|V_{ov_3}|} = 0.2 - 0.05 = \mathbf{0.15\,V}\ (main)\ [assume]$$

$$V_{ov_4} < V_{ov_5} \Rightarrow \boldsymbol{V_{ov_4}} = \mathbf{0.05\,V}\ (cascode)\ and\ \boldsymbol{V_{ov_5}} = 0.2 - 0.05 = \mathbf{0.15\,V}\ (main)\ [assume]$$

$$\boldsymbol{V_{ov_1}} = |V_{ov_2}| = V_{ov_4} = \mathbf{0.1\,V}\ (input)\ [assume]$$

2. **Device sizes:**

$$g_{m_1} \geq 2\pi f_{ugb} C_L = 2\pi(100 * 10^6)(5 * 10^{-9}) \Rightarrow \boldsymbol{g_{m_1}} \geq \mathbf{3.1\,mS}$$
$$\frac{2I_1}{V_{ov,1}} = g_{m_1} \Rightarrow I_1 = \frac{3.1 * 10^{-3} * 0.1}{2} = 157\,\mu A$$

$$Let\ us\ assume\ \boldsymbol{L_1} = \mathbf{0.18\,\mu m}\ (input)$$
$$NMOS\ I_D\ versus\ V_{ov}\ plot{:}\ current\ is\ 44.73\,\mu A\ for\ a\ 10\,\mu m\ wide\ device\ at\ V_{ov} = 0.05\,V$$
$$\boldsymbol{W_1} = \left\lceil \frac{157}{44.73} * 10 \right\rceil = \mathbf{36\,\mu m}$$

$$Let\ us\ assume\ \boldsymbol{I_2 = I_4 = I_5 = 50\mu A} \sim \frac{I_1}{3}$$

$$Let\ us\ assume\ \boldsymbol{L_2 = 0.18\ \mu m}\ (cascode)$$
$$PMOS\ I_D\ versus\ V_{ov}\ plot\text{: }current\ is\ 12.68\ \mu A\ for\ a\ 10\ \mu m\ wide\ device\ at\ |V_{ov}| = 0.05\ V$$
$$\boldsymbol{W_2} = \left\lceil \frac{50}{12.68} * 10 \right\rceil = \boldsymbol{40\ \mu m}$$
$$I_3 = I_1 + I_2 = 207\ \mu A$$

$$Let\ us\ assume\ L_3 = 0.25\ \mu m\ (main)$$
$$PMOS\ I_D\ versus\ V_{ov}\ plot\text{: }current\ is\ 37.25\ \mu A\ for\ a\ 10\ \mu m\ wide\ device\ at\ |V_{ov}| = 0.15\ V$$
$$W_3 = \left\lceil \frac{207}{37.25} * 10 \right\rceil = 56\ \mu m$$

$$Let\ us\ assume\ \boldsymbol{L_4 = 0.18\ \mu m}\ (cascode)$$
$$NMOS\ I_D\ versus\ V_{ov}\ plot\text{: }current\ is\ 44.73\ \mu A\ for\ a\ 10\ \mu m\ wide\ device\ at\ V_{ov} = 0.05\ V$$
$$\boldsymbol{W_4} = \left\lceil \frac{50}{44.73} * 10 \right\rceil = \boldsymbol{12\ \mu m}$$

$$Let\ us\ assume\ L_5 = 0.25\ \mu m\ (main)$$
$$NMOS\ I_D\ versus\ V_{ov}\ plot\text{: }current\ is\ 131\ \mu A\ for\ a\ 10\ \mu m\ wide\ device\ at\ V_{ov} = 0.15\ V$$
$$W_5 = \left\lceil \frac{50}{131} * 10 \right\rceil = 4\ \mu m$$

3. <u>CMFB Compensation Parameters & Device Resizing:</u>

$$For\ CMFB(3)\text{: }f_p = \frac{1}{R_L' C_L'}\ where\ R_L' = R||R_L\ and\ C_L' = C + C_L.$$
$$Therefore, R\ should\ be\ maximized\ and\ C\ should\ be\ minimized.$$
$$\boldsymbol{R = 1M\Omega}\ and\ \boldsymbol{C = 15\ fF}\ (assume)$$

$$Gain\ of\ CMFB\ stage\text{: }A_{o,CMFB} = \frac{\boldsymbol{g_{m_{CMFB_1}}}}{\boldsymbol{g_{m_{CMFB_3}}}} \sim \boldsymbol{3}\ (assume)$$
$$To\ achieve\ this, L_{CMFB_1} = L_{CMFB_3}\ and\ W_{CMFB_1} = 3W_{CMFB_3} = W_4\ (assume)$$

$$This\ CMFB\ design\ does\ not\ give\ enough\ f_{ugb}.$$
$$To\ increase\ f_{ugb}\ and\ f_p, we\ should\ increase\ R_L\ because\ C_L' \sim C_L\ which\ is\ given.$$
$$R_L\ can\ be\ increased\ by\ increasing\ L_3\ and\ L_5.$$

$$Let\ us\ assume\ \boldsymbol{L_3 = 0.5\ \mu m}\ (main)$$
$$PMOS\ I_D\ versus\ V_{ov}\ plot\text{: }current\ is\ 15.08\ \mu A\ for\ a\ 10\ \mu m\ wide\ device\ at\ |V_{ov}| = 0.15\ V$$
$$\boldsymbol{W_3} = \left\lceil \frac{207}{15.08} * 10 \right\rceil = \boldsymbol{138\ \mu m}$$

$$Let\ us\ assume\ \boldsymbol{L_5 = 0.5\ \mu m}\ (main)$$
$$NMOS\ I_D\ versus\ V_{ov}\ plot\text{: }current\ is\ 57.27\ \mu A\ for\ a\ 10\ \mu m\ wide\ device\ at\ V_{ov} = 0.15\ V$$
$$\boldsymbol{W_5} = \left\lceil \frac{50}{57.27} * 10 \right\rceil = \boldsymbol{9\ \mu m}$$

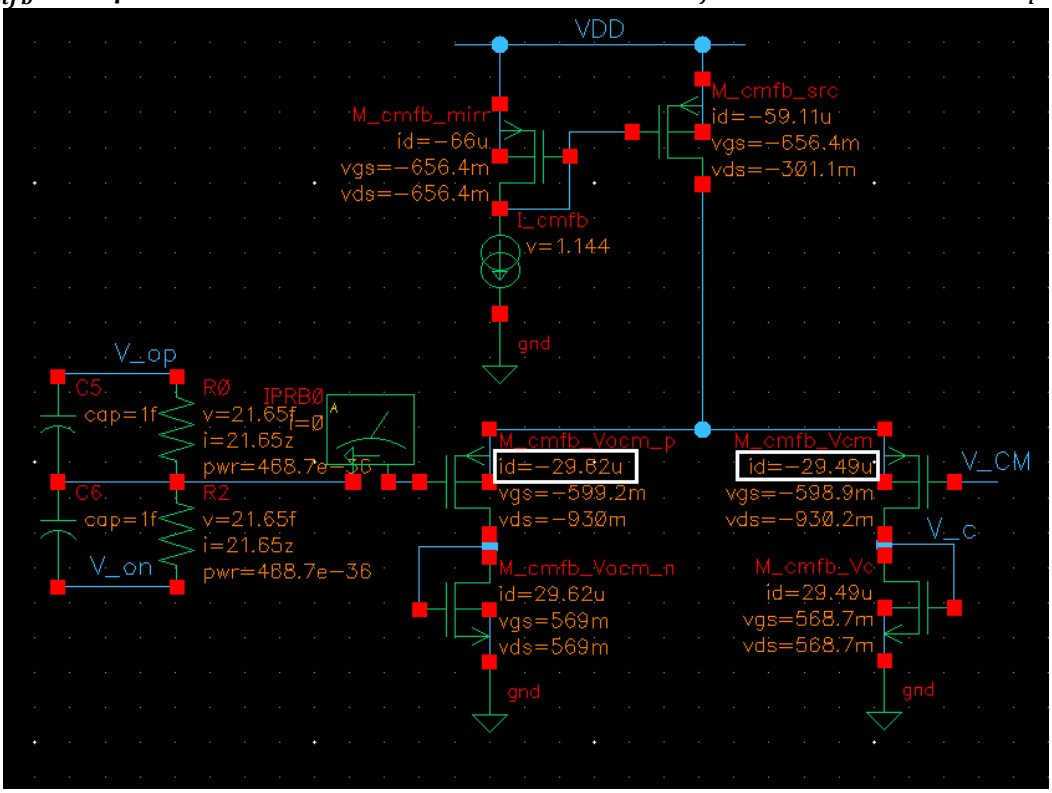
4. DC Current Adjustment & Biasing Circuit Device Resizing:

Using the above device sizes and CMFB stage parameters, we do not get sufficient gain. Therefore, dc currents should be increased by changing the device sizes in the biasing circuit.

$$\boldsymbol{I_1 = 220\ \mu A}, I_2 = 50\mu A \text{ and } \boldsymbol{I_3 = 270\ \mu A} \text{ are set as the new dc currents.}$$

5. CMFB Current Adjustment:

$\boldsymbol{I_{cmfb} = 66\ \mu A}$ *is set so that currents in both branches of the CMFB circuit are equal.*



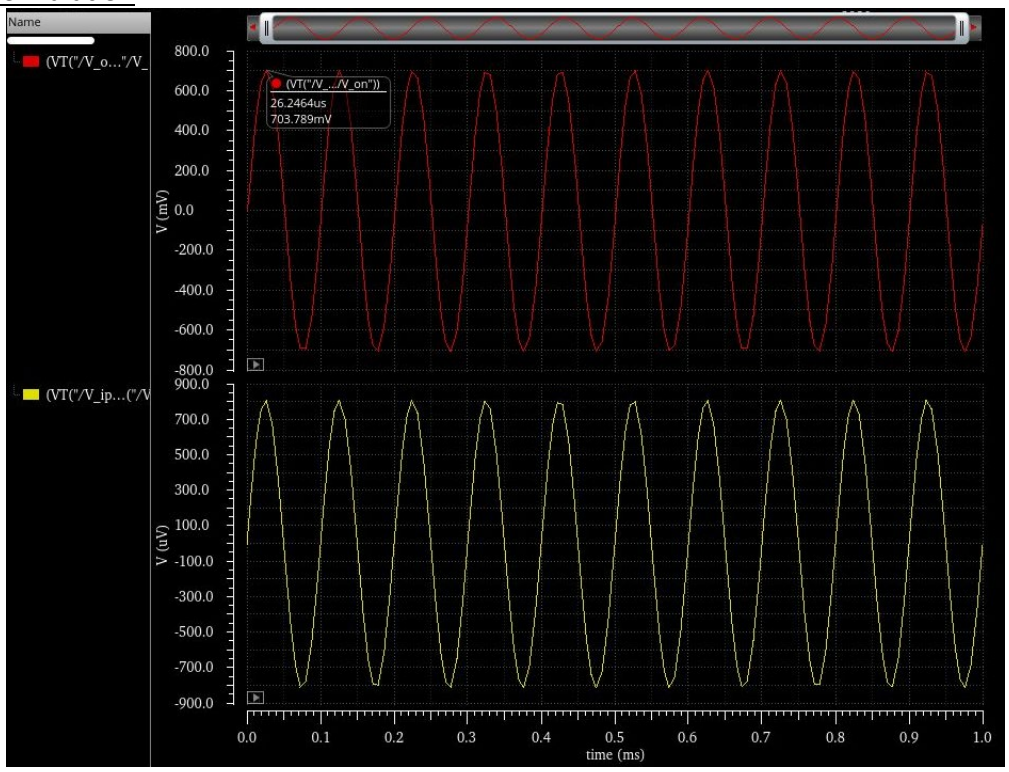
This ensures that V_{OCM} *tracks* $V_{CM} = 900\ mV$.

6. Input Voltage AC Amplitude Adjustment

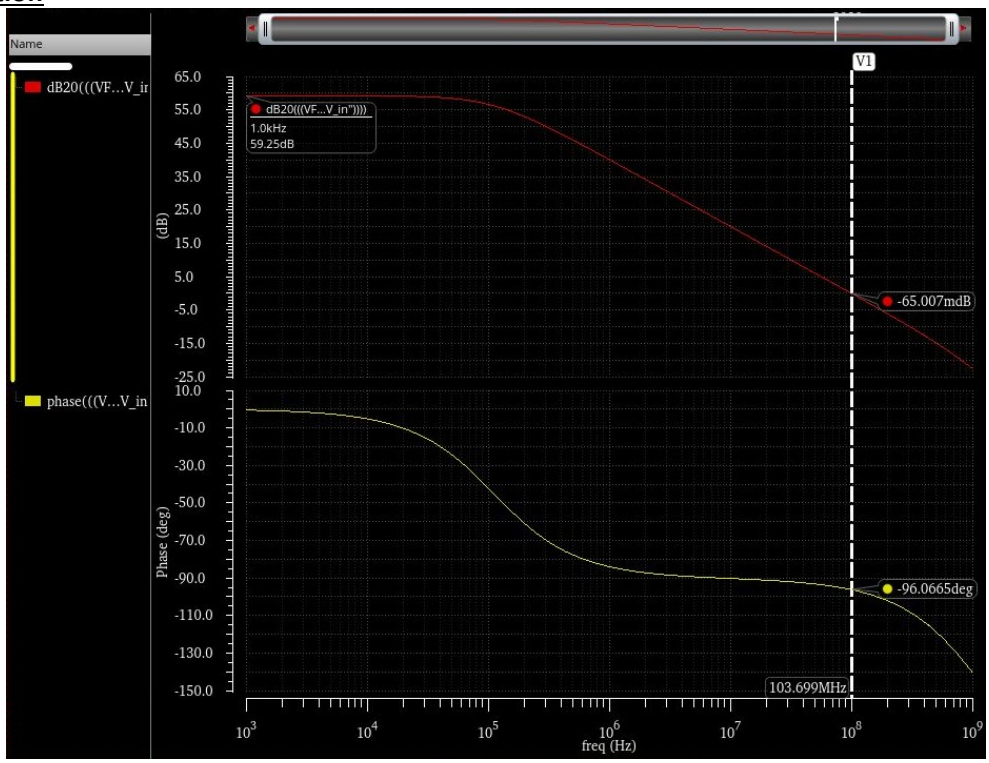
$\boldsymbol{v_a = 810\ \mu V}$ *is set so as to achieve* $\Delta V_{o,pk-pk}$ *close to* $1.4\ V$.

Results

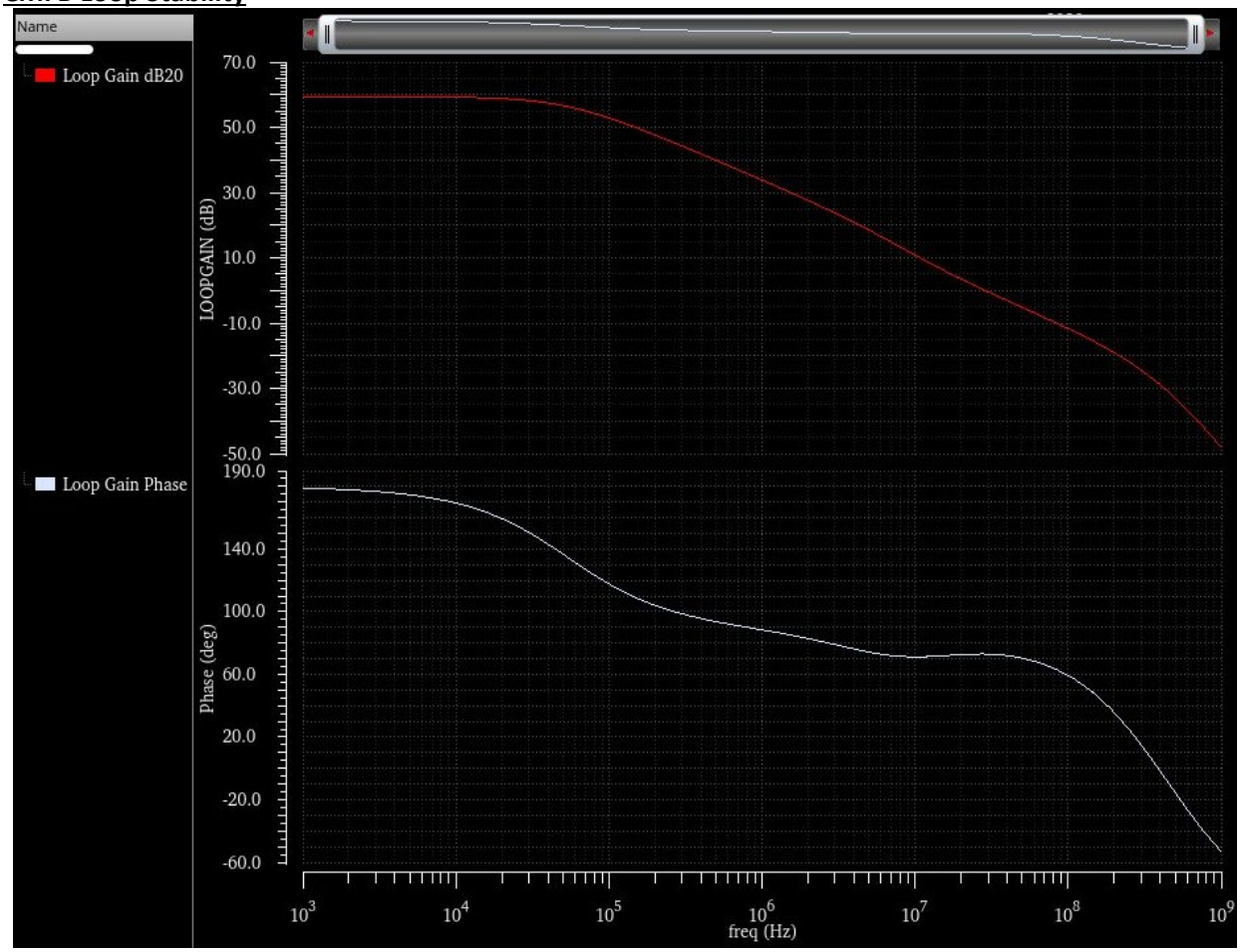
Transient Simulation



AC Simulation



CMFB Loop Stability



Stability Summary - circuit "fd_folded_cascode_cmfb3" with loop probe "IPRB0"

PM(deg)	@Freq(Hz)	GM(dB)	@Freq(Hz)
73.384	29.39M	28.245	392.14M

Transient Operating Points:

signal	OPT("/M1p" "??")
gm	3.923m

signal	OPT("/M3p" "??")
gm	2.956m

signal	OPT("/M5p" "??")
gm	615.5u

Thermal Noise Analysis:

$$P_{sig} = \frac{V_{peak,FD}^2}{2} = \frac{(1.4\ V)^2}{2} = 0.98\ V^2$$

$$From\ simulations:$$
$$g_{m_1} = 3.923\ mS$$
$$g_{m_3} = 2.956\ mS = \frac{2.956}{3.923} g_{m_1} = 0.754 g_{m_1}$$
$$g_{m_5} = 615.5\ \mu s = \frac{615.5}{3923} g_{m_1} = 0.157 g_{m_1}$$
$$\Rightarrow g_{m_1} + g_{m_2} + g_{m_3} = g_{m1} + 0.754 g_{m_1} + 0.157 g_{m_1} = 1.911 g_{m_1}$$
$$In\ the\ presence\ of\ biasing\ capacitors\ (to\ attenuate\ noise\ from\ biasing\ current\ mirrors):$$
$$P_{out,n} = \overline{v_{o,n,tot}^2} = \frac{2kT}{C_L}\gamma\left(g_{m_1} + g_{m_3} + g_{m_5}\right)R_o = \frac{2kT}{C_L}\gamma \times 1.911 g_{m_1} R_o$$
$$Assume\ \gamma = \frac{2}{3}$$

$$From\ simulations: |A_{DC}| = 2 g_{m_1} R_o = 10^{\frac{59.25}{20}} = 917.28 \Rightarrow g_{m_1} R_o = \frac{917.29}{2} = 458.64$$
$$\Rightarrow P_{out,n} = \frac{2 \times 1.38 * 10^{-23}\ m^2 kg\ s^{-2}\ K^{-1} \times 300K}{5 * 10^{-12} F} \times \frac{2}{3} \times 1.911 \times 458.64$$
$$= 96763.41 * 10^{-11}\ V^2$$

$$SNR = 10 \log_{10} \frac{P_{sig}}{P_{out,n}} = 10 \log_{10} \frac{0.98}{96763.41 * 10^{-11}} = 10 \log_{10} 1012779.52 = \mathbf{60.055\ dB}$$

Summary

Parameter	Specification	Achieved
FD DC Gain	> 400	$10^{\frac{59.25}{20}}$ = **917.28** ✓ **(2x+)**
Load Cap	5 pF	**5 pF** ✓
Output FD signal	1.4 V	0.7038*2 = **1.408 V** ✓
VDD	1.8 V	**1.8 V** ✓
UGB Frequency	100 MHz	**103.699 MHz** ✓
PM	> 70°	-96.067°-(-180°) = **83.93°** ✓
SNR	> 60 dB	**60.055 dB** ✓