

Graph Based Analysis of 2-D FPGA Routing

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Abstract—In this paper, we study the two-dimensional FPGA, Xilinx-like routing architectures and present the first known computational complexity results for them. The routing problem is formulated as a two-dimensional interval packing problem and is proved to be NP-complete with or without doglegs. Next, we consider other routing structures obtained from the industrial one by arbitrarily changing switch box connection topology while maintaining the same connection flexibility. There is an exponentially large number of such routing structures. We further prove that there does not exist a better routing architecture among the members of this large domain. In addition, we prove that there is no constant bound on the mapping ratio of a track number required by a detailed routing to a global routing channel density for the studied architectures. Finally, we show two directions of changing the routing architectures which yield polynomial time mapping solutions and constant bounded mapping ratios. Our theoretical analysis is intended to give some insight to, and understanding of this new routing problem's fundamental properties.

I. INTRODUCTION

FPGA's (Field Programmable Gate Arrays) are arrays of pre-fabricated logic blocks and wire segments with user-programmable logic and routing resources. Because of their attractive manufacturing cost for low volume production, FPGA usage has grown rapidly for ASIC implementations. FPGA technologies are commonly classified into three major categories: (a) Look-Up-Table (LUT), SRAM based (e.g., Xilinx [12, 21]), (b) multiplexer, channel organized, anti-fuse based (e.g., Actel [1]) and (c) PLD, EPROM based (e.g., Altera [2]). In this paper we study routability of a general two-dimensional (2-D) architecture. This architecture is a LUT and SRAM technology-based. The routing architecture of an industrial product of this type is described in [7], [12] [18], [20], [22] and shown in Figs. 1 and 2.

Routability is one of the major concerns in current FPGA technology. This is because the wire delay and routing resources are the dominating factors in circuit performance and chip area. The problem has been addressed at different phases of the design process. For example, there have been research on technology mapping algorithms to improve routability [3], [19], and on deleting unroutable wires through incremental restructuring in logic domain [8].

Many of the existing FPGA routers follow a two-step global and detailed routing scheme, where a global router is typically

Manuscript received August 1, 1994; revised September 22, 1995. This work was supported in part by NSF under Grant MIP 3117328. This paper was recommended by Associate Editor M. Sarrafzadeh.

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Publisher Item Identifier S 0278-0070(96)00697-5.

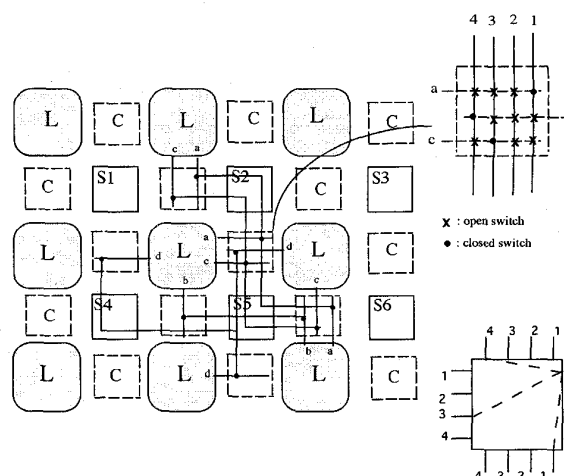


Fig. 1. (a) The routing model. (b) The C-box. (c) The S-box.

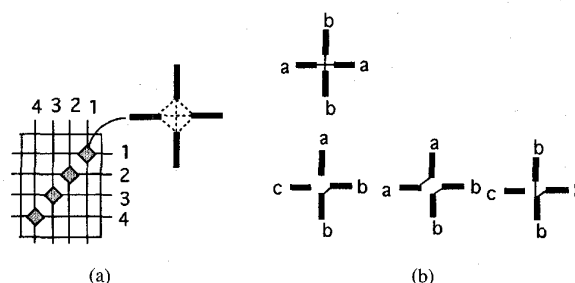


Fig. 2. (a) The diagonal S box architecture. (b) The diagonal S box connection examples (at each intersection point).

tuned to balance channel density across the chip, and is followed by a detailed router which finds feasible tracks for each net. The final success of routing depends on the feasibility of finding detailed routes for the globally routed nets. Thus it is reasonable to measure the routability of an FPGA architecture through the mappability of a global routing of all nets with arbitrary topologies, to a feasible detailed routing. Intuitively, an architecture with a better mappability should be more likely to yield an efficient routing algorithm and produce a higher routing completion rate. The two-step routing scheme is not the only alternative in designing routers. However, since a routing with just a couple of unrouted nets is as bad as any other failed routing, such a global view reflects the desired 100% routing completion rate. Furthermore, in the growing FPGA real-time reconfigurable circuit applications, a fast routing algorithm predicting 100% routing rate would be more desirable or even vital. The mappability of a routing architecture can be

formulated as a *routing decision problem*: Can the decision whether an arbitrary global route can be mapped to a feasible detailed route be made in a polynomial time?

The mappability view in justifying routabilities of wiring architectures has been used to analyze the one-dimensional (1-D) routing architectures. The channel routing problem is one of this kind. It is known that a mapping of global routing of a given density to detailed routing with the same number of tracks is always feasible and solvable in polynomial time for a channel routing problem with no vertical constraints [11]. This classical mapping problem can be considered to be a *1-D interval packing problem (1-D IPP)*. With the generalization of this model into a 2-D structure, the mapping problem of Xc4000 type routing architecture can be viewed as a special case of the *2-D interval packing problem (2-D IPP)* [24]. Here we analyze the computational complexity issues for a 2-D FPGA routing model and its variants with the same flexibility of routing resources.

We first show that all the possible variants of the routing architecture with the same switch box hardware resources can be classified into two major classes: disjoint and overlapped. The Xc4000 type architecture belongs to the class of disjoint architecture.

The (routing decision problem of) 2-D IPP for a disjoint architecture can be shown to be equivalent to the chromatic number problem for an arbitrary graph. Additionally, it can be shown that for both of the two classes (disjoint and overlapped) with fixed switch box of flexibility 3, doglegs allowed or disallowed, the computational complexity of this routing problem remains NP-complete [25] and the worst case mapping ratio of a required number of tracks to complete detailed routing over a global route channel densities is not bounded by a constant. This also implies that the routability of this 2-D FPGA routing architecture cannot be rudimentary improved through re-permuting of the possible interconnection patterns of the routing switch boxes. Finally, we show that by applying properties of perfect graphs [9], [10] we can change the routing architecture to yield polynomial time mapping solutions and constant bounded mapping ratios.

This paper is organized as follows: In Section II we discuss the routing architecture and introduce the basic terminology. In Section III, we give an overview of the previous work. In Section IV we show the 2-D interval packing problem formulation and in Section V we discuss its computational complexity. In Section VI, we show how this intractable routing problem can be improved by changing the routing architecture. We make conclusions in Section VII.

II. ROUTING ARCHITECTURE AND TERMINOLOGY

The studied architecture is depicted in Fig. 1(a). It is a two-dimensional array of logic cells and routing resources. Each logic cell is marked L and can be configured to be an LUT, flip-flop, ..., etc. [12]. Wire segments for connecting pins of logic cells run between the cells in vertical and horizontal channels and are aligned into tracks. Therefore, a vertical (horizontal) channel is a set of tracks between two consecutive columns (rows) of cells. Since wire segments are

prefabricated, personalization of routing resources is achieved through a proper programming of switches. Routing switches are grouped into the connection (C) boxes and switch (S) boxes (Figs. 1(b) and 2). The C boxes contain routing switches that can be programmed to connect logic cell pins to wire segments. The termination points of wire segments are inside switch boxes and the S boxes contain switches that allow one wire segment to be connected to another. In this paper we assume that all wire segments are of single-length (that is, every wire segment spans only one C box, or alternatively, that its end points are in the neighboring S boxes). In the following, we will simply call this architecture a *2-D (array) FPGA*.

We assume that all vertical and horizontal channels have the same number of tracks and denote it by W . The tracks in each horizontal channel are numbered from top to bottom and in each vertical channel are numbered from right to left. A number assigned to each track is referred to as *track id*. The flexibility of a C box, F_c is defined to be the number of tracks a logic pin can connect to. For example, in Fig. 1(b), there are three logic pins in the C box. The pin a can be connected to wire segment in track 2 or to wire segment in track 4. Similarly, pin b can connect to tracks 1 or 3, and pin c can connect to 2 or 4. Each pin in this C box can connect to 2 tracks; therefore the flexibility of this C box is 2. The flexibility of S box, F_s is the number of wire segments that each segment can connect to. For example, consider Fig. 1(c). It shows all possible connections of the right wire segment on track 1. It can be connected to the top segment on track 4, or bottom segment on track 1, or left segment on track 3. Suppose that all other wire segments adjacent to this S box can also connect to 3 other wire segments. Therefore its flexibility is 3.

In the definition of the S box's flexibility, we did not make any assumptions about the location of the wire segments to which each wire segment connects. Suppose now that an S box has $F_s = 3$ and additionally each wire segment can connect to exactly one wire segment in each of the remaining channels adjacent to this S box. We will call such an S box a *basic flexibility S box*. Fig. 2 shows an example of a basic flexibility S box. There an exact position of switch points and their possible interconnection patterns are shown.

The 2-D FPGA we are studying here has a full ($F_c = W$) flexibility of C boxes and the basic flexibility of S boxes.

We define the *identity S box* as the one which allows all segments with the same track *id* to be connected, and which has the basic flexibility. The *diagonal S box* (Fig. 2(a)) used in Xc4000 is of this kind.

A *net* is a set of pins assigned the same signal that are to be connected by wire segments. A *detailed route* of a net is a set of wire segments and switches with appropriate programming used for connecting pins and segments of the net. A detailed route of a net is *simple* if every pin of the net connects to exactly one track (and hence, the route contains at most one wire segment of a track in a C box). A detailed route of a net is a *dogleg route* if there exists a pin of the net which connects to two or more different tracks. Dogleg routing increases delay and should be avoided.

A *global router* decides for each net through which S boxes and C boxes the detailed route of the net will pass. A *detailed router* determines a detailed route for each net while maintaining the topology of the global route of the net. Namely, for each net a detailed router assigns wire segments following the topology specified by the global route such that no overlapping among detailed routes of different nets occurs. When a pin is connected to a wire segment in a C box, this wire segment cannot be accessed from any other pin in the same C box, so we can consider global route to originate and terminate in C boxes. Hence, a *global route* of a net can be viewed as a set of C boxes and S boxes.

Given a 2-D FPGA and global routes of all nets, the nets are said to be routable without doglegs in the FPGA, if all the nets have simple detailed routes not overlapping each other which follow the specified global routes and the number of required tracks does not exceed W . The nets are said to be routable with doglegs in W tracks if all the nets have detailed routes not overlapping each other, each of which is simple or dogleg route and follows the specified global route. We consider in this paper a routing problem of deciding if global to detail routing mapping exists and how to find detailed routes of nets when their global routes are specified. We also consider a new 2-D wiring architecture which makes this routing problem easier.

A channel density resulting from a global routing, W_g , is the maximum number of global routes which run in parallel in any channel. A channel density resulting from a detailed routing, W_d , is the minimum number of tracks W needed for given net topologies to be routable. Note, that the number of tracks W is fixed for a particular chip and W_d depends on global routing. If $W_d > W$, then routing can not be completed. A *mapping ratio* is the value of W_d/W_g .

A wire segment x in C box X is said to be *connectable* to a wire segment y in C box Y (may be the same as X), if there exists a sequence $\langle x = t_0, t_1, t_2, \dots, t_n = y \rangle$ of wire segments such that for every $i (0 < i \leq n)$, a wire segment t_{i-1} is connected to a wire segment t_i , inside some S box. We define a *track domain* as a maximal set of wire segments such that any two segments of the set are connectable. The routing structures with basic flexibility of S box can be divided into two major classes: disjoint and overlapped architectures. A *disjoint routing architecture* is a structure with all wire segments of the whole chip (disjointedly) partitioned into W equal size track domains such that each domain contains exactly one wire segment in each C box. Otherwise, it is an *overlapped routing architecture*.

III. PREVIOUS WORK

Routability was studied experimentally [7], [18], [20], [22] and was defined as the percentage of routed nets. It was shown that if F_c was high enough, relatively low values of F_s can achieve 100% routability. In other words, the F_s value larger than 3 seemed to be not improving routability significantly when connection boxes were of full flexibility. However, F_s less than 3 brought sharp routability degradation regardless increased F_c . The experimental results suggested a full flexibility F_c and F_s value of 3 as reasonable flexibility of

routing resources. In the stochastic model shown in [4], [5], routability was expressed as the likelihood that a net can be connected. More thorough discussion of the previous strategies developed for 2-D FPGA routing architectures can be found in [4], [6], [17].

In [7] and [13], a maze router based, general routing approach for the array type FPGA's was proposed. A global router adapted from standard cell environment was used [16]. This global router divides multi-pin nets into two-pin nets and routes them in minimum length paths. The main objective is to keep all channel densities as even as possible. Based on the global router result, a sequence of wire segments, called the coarse route, is assigned to each connection. Graph representation of the coarse route is called the coarse graph.

After the global routes of all the nets are decided, the Coarse Graph Expansion (CGE) detailed router decides specific wire segments implementing particular connections. In the first phase of CGE, an expanded graph is generated for each net by examining the routing switches and wire segments along the path described by the coarse graph. The alternative detailed routes are recorded in the expanded graph.

In the second phase, CGE places all paths from all the expanded graphs into a single path list. The router then selects paths from the list based on a cost function. Each selected path defines the detailed route of its corresponding connection.

This approach is general enough to cover all kinds of array-type FPGA's. We will give an interpretation of this heuristic for array-type FPGA's with $F_s = 3$ in terms of graph coloring. The results produced by this router have been shown in [13] to be superior to that produced by a conventional maze router, which is net ordering dependent.

IV. TWO-DIMENSIONAL INTERVAL PACKING PROBLEM (2-D IPP)

A. Two-Dimensional Intervals

To identify the disjoint and overlapped routing architecture we characterize the switch-structure (topology) of an S box by its unique connection patterns, which comprise 6 pairs of connection relations between the wire segments adjacent to it. In the case of a basic flexibility S box, each of these 6 connection relations becomes a one-to-one permutation mapping [14].

The permutation mappings ($P_1 \sim P_6$) are shown in Fig. 3. For example, P_5 denotes a connection relation between horizontal wire segments on the left and right sides on an S box. Suppose that $P_5 = \begin{pmatrix} 1234 \\ 4231 \end{pmatrix}$. It means that horizontal wire segment on track 1 on the left side is connected to a wire segment on track 4 on the right side, a wire segment on track 2 on the left to wire segment on track 2 on the right side, and so on.

In a 2-D FPGA architecture with diagonal S box (Xc4000 type) a wire segment on a given track on one side of the S box can only be connected to wire segments on tracks with the same track *id* on the other sides. Therefore this architecture is disjoint and all tracks with the same *id*'s form the track domains.

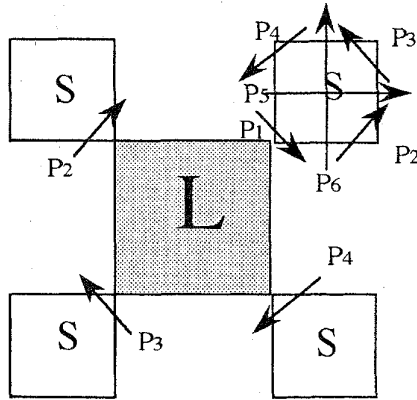


Fig. 3. Track permutation mappings.

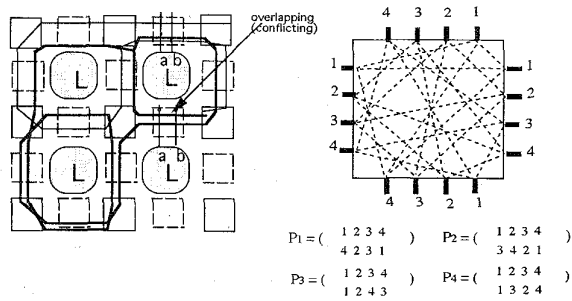
Fig. 4. An overlapped routing architecture (only partial connectable wire are shown. Here, net *a* and net *b* may overlap at some *C*-boxes).

Fig. 4 shows an overlapped routing architecture, where boldfaced tracks and solid line tracks are in the same domain. Note that a detailed route of a net must be contained in a track domain, and in the case of disjoint routing architecture, detailed routes of two nets with global routes in the same *C* box cannot be assigned to the same domain. Otherwise, they may share a track domain.

Given a permutation P_k and a track *id* *t*, $P_k(t)$ denotes a track *id* mapped from *t* by this permutation, and given two permutations P_k and P_h , $P_k P_h$ is a permutation mapping *t* into $P_k(P_h(t))$. The following theorem characterizes the disjoint and overlapped routing architectures.

Theorem 1: Let *I* be the identity permutation $\begin{bmatrix} 1234 \dots n \\ 1234 \dots n \end{bmatrix}$. The routing structure is a disjoint routing architecture, if and only if the permutations defining *S* box topology satisfy the following conditions:

- (1) $P_2 P_3 P_4 P_1 = I$, and
- (2) $P_4 P_3 P_2 P_1 = I$, and
- (3) $P_3 P_2 = P_6$.

The proof is shown in the Appendix.

In all disjoint routing architectures, the detailed routes of any two nets can use a common track domain, if and only if their global routes do not overlap in any *C* box. Therefore, by regarding each track domain as a bin into which global routes are packed, the routing problem can be considered as a two-dimensional interval packing problem (2-D IPP), which is a 2-D generalization of the classical channel routing (1-D

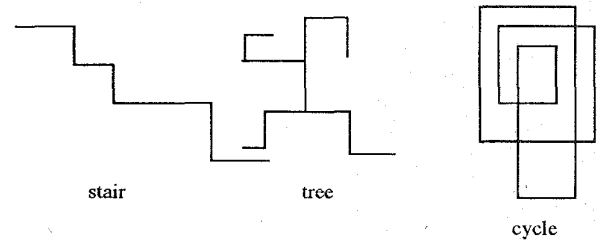


Fig. 5. Examples of 2-D intervals.

interval packing problem). In a classical channel routing, a 1-D interval is a continuous (connected) run of horizontal segments; similarly, a 2-D interval is a continuous run of segments on a 2-D Manhattan grid. In Fig. 5, examples of 2-D intervals are shown. They can be viewed as global routes of some 2-pin or multipin nets.

B. 2-D Interval Packing Problem as a Model of Simple Routing

The 2-D interval packing problem of disjoint routing architecture is an extension of the classical channel routing without vertical constraints. Since every pin adjacent to a *C* box has its own pin line, there are no vertical constraints between pins adjacent to the same *C* box.

The routability decision problem can be stated as follows:

2-D IPP without Dogleg: Given a set of 2-D intervals and a 2-D FPGA with a disjoint routing architecture (2-D bins), can the FPGA accommodate all the 2-D intervals without changing their topology?

This problem can be reduced to a graph coloring problem of an undirected graph G_c constructed in such a way that each vertex corresponds to a 2-D interval and there is an edge between two vertices if and only if the two corresponding 2-D intervals pass through a common *C* box. The graph coloring problem is as follows.

Graph Coloring: Given an undirected graph $G = (V, E)$ and an integer *W*, can we color the vertices by *W* colors such that no adjacent vertices in *G* are colored the same?

For a graph *G*, the least number of colors sufficient to color the vertices of *G* in this way is the chromatic number of a graph *G*, and is denoted by $X(G)$.

Theorem 2: 2-D IPP without dogleg problem is polynomial time reducible to [Graph Coloring] problem, and $W_d = X(G_c)$.

It is not difficult to see this, so the proof is omitted.

C. 2-D Interval Packing Problem as a Model of Routing with Doglegs

Suppose now that for a multi-pin net, doglegs are allowed at all pin locations. For a given net topology the choice of doglegs induces a decomposition of the net into a set of subnets. The routability decision problem is stated as follows.

2-D IPP with Doglegs: Given a set of 2-D intervals and a 2-D FPGA with disjoint routing architecture, can all 2-D intervals be packed into the track domains following global routing topologies? Each 2-D interval can be split at a *C* box if its pin is present there.

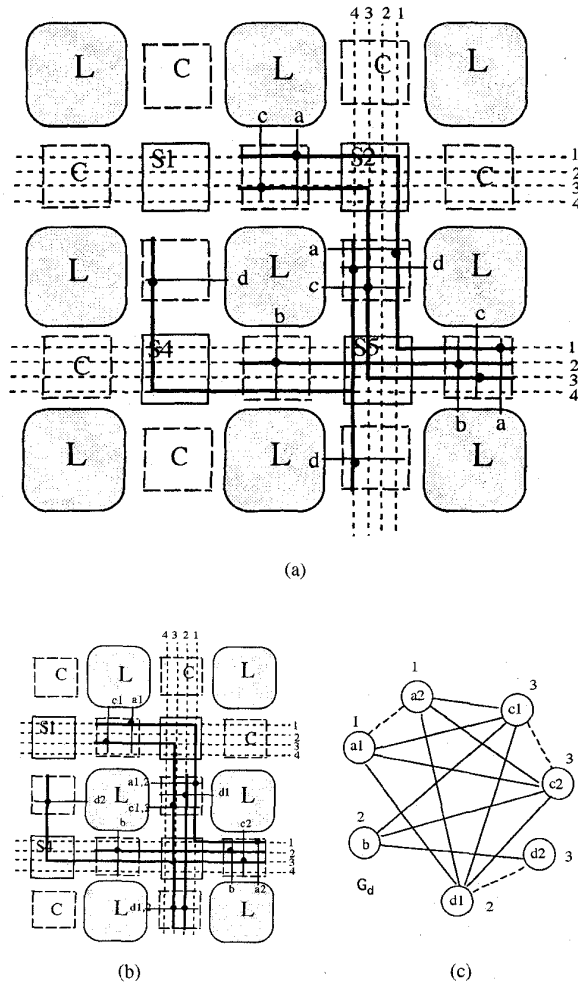


Fig. 6. (a) A routing example. (b) A dogleg routing example for the same circuit placement and global routing as in Fig. 6(a). (Here, a dogleg is used for net d .) (c) The coloring graph of the interval packing instance of Fig. 6(b). Here, multi-pin nets are split into several same name 2-pin nets (vertices) with different subscripts.

The problem can be modeled again as a graph coloring problem. For a given selection of doglegs, all multi-pin nets are split appropriately into 2-pin subintervals. A graph G_d is constructed such that each vertex corresponds to a 2-D sub-interval. There is an edge between two vertices if and only if the two corresponding 2-D sub-intervals pass through a common C box and do not belong to the same net.

Fig. 6(a) shows an example of a simple detailed routing which requires 4 tracks ($W_d = 4$). Note that the corresponding global routing has density $W_g = 3$. Fig. 6(b) shows the same example detailed routed with doglegs. The edges of the graph G_d are shown in solid lines. The dotted edges denote the auxiliary edges connecting the vertices corresponding to 2-D sub-intervals of common nets. The vertices of common nets have the same *ids* with different subscripts. All sub intervals obtained by splitting a 2-D interval can be assigned to different or to the same track domains. Therefore, it is not necessary to include a solid edge in G_d between the vertices representing them.

We can observe that the chromatic number $X(G_d)$ (excluding the auxiliary edges) indicates a sufficient number of tracks required to pack the 2-D intervals. Thus, we have $W_d = X(G_d)$, where W_d is the minimum number of tracks for given nets to be routable with doglegs. In our example, allowing doglegs saves one track. Note that the track 4 is not used in dogleg routing.

Corollary 2.1: For a given choice of possible doglegs, [2-D IPP with doglegs] problem is polynomial time reducible to [Graph Coloring] problem, and $W_d = X(G_d)$.

If, additionally, penalties are introduced for using doglegs and the goal is to find detailed routes with as few doglegs as possible, one can first seek all colorings with the least number of colors $X(G_d)$, and then pick such a coloring among them which has the least distinct color vertex pairs incident to the dotted edges of G_d since each such a pair introduces a dogleg.

Note that there is a subtle distinction between the disjoint and overlapped architectures, and the routing problem for an overlapped architecture can not be directly reduced to the graph coloring problem.

V. COMPUTATIONAL COMPLEXITY ANALYSIS

In the previous section we have reduced the considered routing problem to a graph coloring problem. We are interested in what the properties of the graphs G_c and G_d are. For example, do these graphs possess any properties helpful in determining their chromatic numbers? Disjoint routing architectures are special instances of the exponentially large number of different S box topologies with the basic flexibility. We may ask if among this large domain, there exists a specific structure with routability better than others. In this section we will show that unfortunately, the routing problem is *NP*-complete for any fixed S box topology of the basic flexibility, even if all the nets are 2-pin nets, and there is no constant bound of the mapping ratio W_d/W_g .

A. Complexity of 2-D IPP Without Doglegs

We will restate our routability decision problem.

2-D IPP without Doglegs:

Input: A 2-D FPGA, an S box topology with W tracks on each side, and global routes of nets (2-D intervals).

Query: For each net, can we assign wire segments in the channels specified by the global route of each net, such that:

- 1) the wire segments can be connected by S boxes in the global route,
- 2) no wire segment is assigned to two different nets, and
- 3) a net may connect to at most wire segment track in a C box?

To prove that this problem is *NP*-complete for any fixed S box topology, we extend the definition of a track domain.

If a permutation P_k maps wire segment t_1 in a C box to wire segment t_2 in the adjacent C box (i.e., $t_2 = P_k(t_1)$), then wire segment t_1 and wire segment t_2 are said to be *connected through* P_k . For example, if permutation P_1 maps horizontal segment 1 on the left side of an S box to segment 4 on the bottom side of the S box, then track 1 on the left and track 4 on the bottom are connected through P_1 . Given a global route of

a net, a permutation P_i of an S box is said to be *contained in the global route*, if P_i denotes the connection relations of wire segments among two adjacent C boxes which are contained in the global route. A maximal set of the wire segments connected through the permutations contained in the global route is called a *subdomain of the global route*. The detailed route of a net must be contained in a single subdomain of the global route of the net. (Note that the subdomain is different from the track domain defined earlier.)

A global route of a net is said to have *disjoint subdomains* if all wire segments in the global route can be partitioned into W subdomains such that each subdomain contains exactly one wire segment in each C box of the global route.

Theorem 3: For an arbitrary fixed S box with basic flexibility, the problem [2-D IPP without Doglegs] is *NP*-complete, if $W \geq 3$.

Proof: Since we can easily see that [2-D IPP without Doglegs] is in *NP*, the theorem can be proved by showing that [Graph Coloring] problem which is known to be *NP*-complete for any fixed $W(\geq 3)$, is polynomially reducible to it.

We build a 2-D FPGA routing instance corresponding to a given graph $G = (V, E)$. For each vertex $i (1 \leq i \leq |V|)$ we create a net i and its global route in such a way that two global routes pass through a C box if their corresponding vertices are adjacent in the graph.

It is known that any permutation P can be decomposed into a product of several disjoint cyclic permutations. Let T be the least common multiple of the lengths of these cyclic permutations, then $(P)^T$ is an identity permutation. For example, if $P_x = \begin{pmatrix} 12345 \\ 35412 \end{pmatrix}$, then $P_x = (134)(25)$, and $(P_x)^6 = I$, where I is the identity permutation. We denote the T values of P_5 and P_6 as s and r respectively, then $(P_5)^s = (P_5^{-1})^s = I$, and $(P_6)^r = (P_6^{-1})^r = I$. (If $s = 1$, we will set it to 2 in this proof.) Since W is a fixed number, both s and r are also fixed numbers.

Let coordinates (x, y) indicate the box (L , C , or S box) located on the x th column and the y th row, as shown in Fig. 7(c). To decide the coordinates we count not only the columns and rows of logic cells but also the channels. The global route of each net i which we create will have a stair case shape. It originates with the unit segment in the C box at coordinates $(2 + 2(i-1)s, 1)$, and has a base horizontal run, starting from the C box at coordinates $(2 + 2(i-1)s + 2i, 1 + 2i(r+1))$ and terminating at the right most C box in the same horizontal channel. Between the starting unit segment and the base horizontal run, the global route has a unit segment for each $j (1 \leq j \leq i)$, such that if vertices i and j are adjacent, then the unit horizontal segment is in the C box at coordinates $(2 + 2(i-1)s + 2j, 1 + 2j(r+1))$, otherwise in the C box at coordinates $(2 + 2(i-1)s + 2j, 1 + 2(j-1)(r+1) + 2)$. All these segments of net i are connected vertically so that the route forms a meandering run like stairs. Note here that all the nets whose global routes are defined above can be 2-pin nets having pins at the starting and ending C boxes.

The size of the above FPGA instance is $O(|V|^2)$, and the reduction is done in $O(|V|^2)$ time. Fig. 7(c) illustrates a reduction example for a 4-clique (Fig. 7(a)) and a graph shown

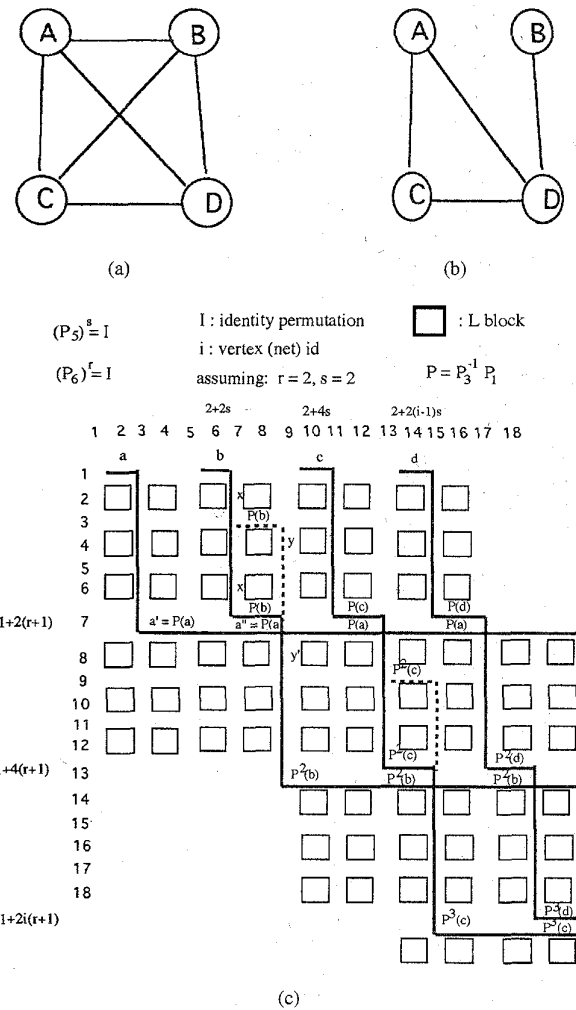


Fig. 7. (a) A 4-clique graph. (b) An arbitrary graph. (c) 2-D FPGA routing instance for (a) and (b).

in Fig. 7(b). The global route shown in solid lines represents the 4-clique and the dotted lines indicate the part of global routes changed to represent the case of Fig. 7(b) where some vertices are not adjacent.

In the above construction each global route of a 2-pin net has W disjoint subdomains, since it contains only one permutation in each S box and a permutation is a one-to-one mapping. We can represent each unique subdomain in such a global route by the track id of the starting C box of the global route and call this id the color of the subdomain.

Lemma 1: Consider the FPGA instance constructed above and an arbitrary C -box through which two global routes, R_1 and R_2 pass. For each track in such a C -box the color domain ids induced by R_1 and R_2 are the same.

Proof: See Appendix.

Using this fact we can color consistently all the tracks contained in the global routes constructed above by the colors of the subdomains in the global routes. Then we can partition all the tracks in the global routes into W sets, in such a way that each set contains the tracks of the same color. Moreover,

from the construction of the global routes, we can see that two nets can be assigned to the tracks with the same color, if and only if the vertices corresponding to the nets are not adjacent in the original graph G .

If a given graph is W colorable, then we number these colors from 1 to W , and according to the colors of the vertices we can assign a net to the subdomain in its global route with the same color as the color of the vertex corresponding to the net. Therefore, the nets created above are routable without doglegs in a given 2-D FPGA with W tracks in each channel. If these nets are routable in a given 2-D array FPGA without doglegs, then according to the colors of subdomains we can color the vertices of a given graph, and hence the graph is W colorable. \square

We have shown the NP-completeness in the case where the number W of tracks in a channel is greater than two, since 2-colorable problem is solvable in polynomial time. This proof covers all S box topologies including disjoint and nondisjoint architectures. Some simpler proofs for just the diagonal S box architecture can be found in [23], [24].

In the following, we illustrate the reduction concept in a less formal but simpler way using the example shown in Fig. 7.

Example: Let a, b, c , and d be the track id 's of the starting segments located in row one, assigned to the corresponding nets A, B, C , and D of the 4-clique. Denote $P = P_3^{-1}P_1$. We know that a valid detailed route should satisfy the following conditions: wire segment on track a in the C box (2, 1) is connected to the wire segment on track a' in C box (4, 7) and $a' = P(a)$. This is because $a' = P_3^{-1}(P_6)^*P_1(a) = P_3^{-1}IP_1(a) = P_3^{-1}P_1(a) = P(a)$. Additionally, $a'' = (P_5)^*(a') = I(a') = a' = P(a)$. Similarly, we can determine colors of the other base runs.

In a valid detailed route, $P(a)$, which represents the track id of the segment connected to the net A at C box (8, 7), must be different from $P(b)$, therefore, we have

$$\begin{aligned} a \neq b, \text{ since } P(a) \neq P(b) \\ \text{iff } P^{-1}P(a) \neq P^{-1}P(b) \text{ iff } a \neq b. \end{aligned} \quad (1)$$

In other words, the relation of passing through the same C box enforces nets A and B to be painted with different colors.

Similarly, we have

$$a \neq c \quad (2)$$

and

$$a \neq d \quad (3)$$

and

$$P^2(b) \neq P^2(c) \Rightarrow b \neq c \quad (4)$$

$$P^2(b) \neq P^2(d) \Rightarrow b \neq d \quad (5)$$

$$P^3(c) \neq P^3(d) \Rightarrow c \neq d. \quad (6)$$

The minimum number of colors required to paint nets A, B, C , and D , such that all the coloring constraints of (1) to (6) are satisfied is the chromatic number of the related graph, since their coloring constraints are exactly the same. To see how a missing edge is implemented, we show the reduction

of the graph in Fig. 7(b) which is the same as the graph in Fig. 7(a) without the edges (B, A) and (C, B) . The segment of the net B is now moved from the C box (8, 7) to the C box (8, 3). When the id b is decided, then the track id of y' is also uniquely decided and so are all the wire segments connected after y' regardless of whether the $x - x' - y'$ or $x - y - y'$ is chosen. Similarly, another segment is moved to (14, 9). The new FPGA instance fulfills all the above listed coloring constraints except (1) and (4). (End of the example).

B. Complexity of 2-D IPP with Doglegs

Let us consider the case when doglegs at pins are allowed. The problem can be formulated as follows.

2-D IPP with Doglegs:

Input: A 2-D FPGA, an S box topology with W tracks on each side, and global route of nets.

Query: Can we assign wire segments in the channels specified by the global routes of the nets, in such a way that

- 1) the segments can be connected by S boxes as specified by the global route,
- 2) no wire segment is assigned to two different nets, and
- 3) a net can connect to only one wire segment in a C box assigned to it if it has no pins there?

From the definition it is not difficult to see that there is a 2-pin net instance of [2-D IPP with Doglegs] which is equivalent to an instance of [2-D IPP without Doglegs] such that the instance is routable with doglegs if and only if the other instance is routable without doglegs. Therefore, from the fact that [2-D IPP without Doglegs] is NP-complete even if all nets are 2-pin nets, we conclude that [2-D IPP with Doglegs] is also NP-complete. Hence we have the following theorem.

Theorem 4: For an arbitrary fixed S box with basic flexibility, problem [2-D IPP with Doglegs] is NP-complete, if $W \geq 3$.

From Theorems 3 and 4, it follows that the difference between W_d and W_g can be arbitrarily large. Namely, to minimize the global channel density, W_g may not help to minimize the number of tracks in a channel needed in the detailed routing. Note that the global routing instance constructed in the proof of Theorem 3 has channel density $W_g = 2$, but the number W_d of tracks required for the instance to be (detailed) routed is equal to the chromatic number $X(G)$ of the corresponding graph G . Hence, if the graph G is a complete graph with n vertices, then $W_d = n$. Thus, we have the following theorem.

Theorem 5: For an arbitrary fixed S box with basic flexibility, there does not exist a constant bound c of the mapping ratio such that $W_d/W_g \leq c$ for routing with or without doglegs.

We conclude therefore that for any fixed S box topology, it is probably hard (unless $P = NP$) to find an efficiently computable necessary and sufficient condition for given global routes (and hence given nets) to be realizable in a given FPGA, even if all the nets are 2-pin nets. Moreover, we have shown that mapping ratio W_d/W_g cannot be bounded by a constant. As a side result, from the viewpoint of constructing a router for FPGA's, we also conclude that the originally proposed diagonal S box topology [12], although being the simplest, is

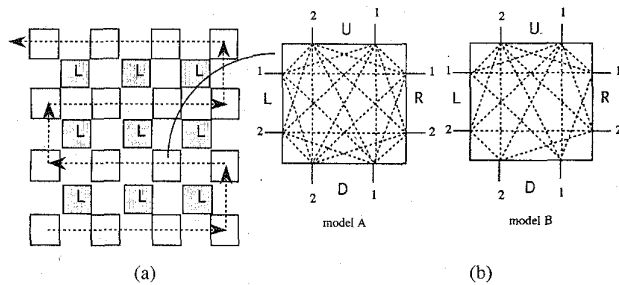


Fig. 8. (a) The switch box architecture and its line stretching sequence. (b) The super switch boxes.

not likely to be worse than any other S box topology with the same basic flexibility.

VI. 2-D ROUTING STRUCTURES WITH PREDICTABLE ROUTING

A. Adding More Flexibility to Switch Boxes

One approach to achieving a predictable global to detailed routing mapping is to increase the flexibility of S boxes without changing the topology of wire segments. We illustrate two ways of increasing S box flexibility (Fig. 8(b)). We call the switch box with increased flexibility the *super switch box*. In model A, a complete flexibility is allowed between all side pairs except between the left and right sides; while in model B, only the three side pairs (D, U), (L, U), and (R, U) are provided with complete flexibility.

Assuming that we are given a global routing instance, we imagine a "snake-shape" line passing through the rows of switch boxes as shown in the dashed line of Fig. 8(a). Note that the global routing is arbitrary and does not follow the snake line. If we stretch the line, our switch boxes will be placed on a line. We then transform the original 2-D interval packing problem into a classical channel routing problem without vertical constraints (1-D interval packing problem). Vertical 2-pin nets do not have to be considered in this transformed problem. In the linear packing phase we consider only the continuous horizontal segments and treat them as independent intervals in model A. In model B, down (D) box segments are also connected with the same net segments in either left or right C boxes. The transformed problem can be solved by a linear time algorithm [11] which will pack the intervals over this stretched row with minimized number of tracks. Then we fold back the linear arrangement of switch boxes into the original array. It is quite possible that some up or down C box segments of same nets are not assigned the same track id 's as their horizontal segments; however, all these connections can be completed by using the increased flexibility between the corresponding side pairs without adding additional tracks.

This architecture guarantees that any global routing can be mapped in linear time with $W_d = W_g$ tracks in super switch box model A, and within a constant bounded mapping ratio of $3/2$ for super switch box model B. (The proof is similar to the proof of Theorem 7).

This routing problem can be solved efficiently in $O(N + |LUT|)$ using the left edge algorithm [11], where N is the

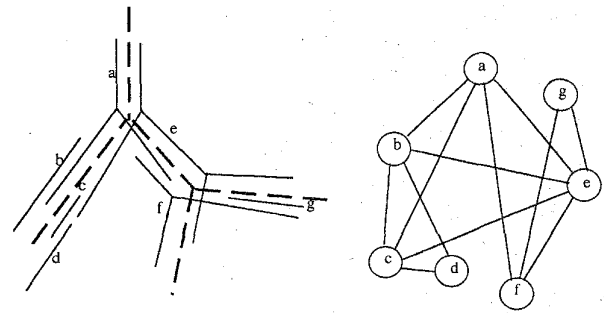


Fig. 9. A chordal graph and a subtree representation for it.

number of nets and $|LUT|$ is the total number of logic cells. With more subtle analysis, simpler super S boxes yielding predictable routing are still possible; due to the page limit, we do not elaborate on these models here.

B. Changing the Topology of Routing Resources

Another approach is to change a 2-D grid routing structure to a tree-type structure. This approach achieves a predictable routability and a decreased flexibility of an S box through eliminating certain topologies of global routes. To show good properties of this architecture, we make use of some properties of perfect graphs [10]. Here, we introduce some definitions and properties of perfect graphs.

A graph G is *perfect* if and only if the chromatic number $X(G)$ of the graph is the same as its maximum clique size $C(G)$ [10]. A graph is *chordal* if every simple circuit with more than three vertices has an edge connecting two non consecutive vertices [14]. A chordal graph is a perfect graph [10]. Let F be a family of nonempty sets. The intersection graph of F is obtained by representing each set in F by a vertex and connecting two vertices by an edge if and only if their corresponding sets intersect. The intersection graph of a family of subtrees in an undirected tree whose node degrees do not exceed 3 will be called a *subtree graph* G_i , which is also a chordal graph [9]. The chromatic number and all maximal cliques of a chordal graph $G = (V, E)$ can be calculated in $O(|V| + |E|)$ time [10].

For instance, Fig. 9 illustrates an example of a subtree graph, where the left half shows a set of subtrees of a tree and the right half shows a subtree graph (an intersection graph for these subtrees). In the left half, boldfaced dashed lines and solid lines indicate a tree and its subtrees, respectively.

Note here that an intersection graph of a family of 1-D intervals is called an *interval graph*, and it is also a perfect graph whose chromatic number and all maximal cliques can be calculated in linear time [10].

Our idea here is to use the properties of perfect graphs in such a way that each global route of a net would be a subtree of a certain tree. Then the intersection graph (subtree graph) G_i of global routes becomes a chordal graph. Therefore, if the routing problem can be reduced to a coloring problem of G_i as it is done in Section IV, an efficient coloring algorithm for a chordal graph could be applied to detailed routing. Hence, our routing problem can be solved in linear time of the size of G_i .

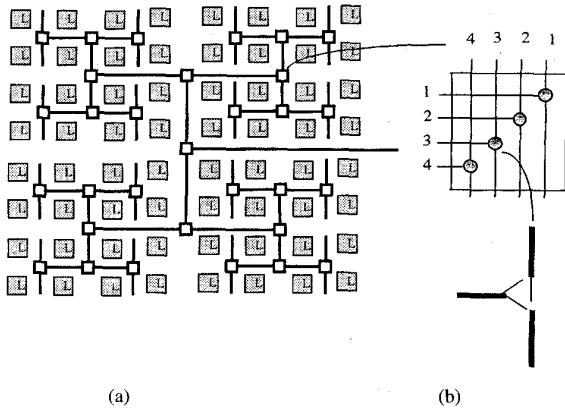


Fig. 10. (a) H -Tree perfect-graph architecture. (b) The 3-way connection point.

There are many ways of configuring the routing resources into a tree (with node degrees less or equal 3) structure. The model which we propose is an H -tree [15], as shown in Fig. 10. In this architecture, every logic cell can be connected to single-length wire segments, then a local cluster of 16 logic cells is connected to another same level cluster through the double-length wire segments, etc. Therefore, the number of S boxes used in connecting the longest possible path in the whole chip is bounded by $2 * l_g(|LUT|)$.

Another advantage of this approach is a simpler switch structure needed for the S boxes. Only 3-way switches ($F_s = 2$) are needed for all S box located in the H -tree, as shown in Fig. 10(b).

In the switch topology shown in Fig. 10(b), the wire segments in the H -tree are partitioned into W track domains, each of which consists of the segments on tracks with the same id . Hence, we can readily see that detailed routes of two nets cannot be assigned in a track domain if and only if the two global routes of the nets run in a common C box. Thus, the routing problem on the H -tree can be formulated as a graph coloring problem on the subtree graph G_i constructed from global routes, and as a result solved in linear time of the size of G_i .

Let N be the number of global routes, the size of intersection graph G_i becomes $O(N^2)$. However, if we take into account an H -tree structure which is not a general tree but a binary tree, we need not to construct the intersection graph G_i , and can solve the routing problem in $O(N + |LUT|)$ time.

In an H -tree as in Fig. 10(a), we define *root*, *parent*, *left-child*, and *right-child* similarly to those in a binary tree. Any S box (a vertex) v in the H -tree, has three incident edges. They are edge $e_P(v)$ between v and its parent, edge $e_L(v)$ between v and its left-child, and edge $e_R(v)$ between v and its right-child. In the following, we associate with an edge a set of consecutive C boxes and S boxes in the H tree routing structure, which are located on the edge. The relation between an edge and such a set is evident from Fig. 10(a).

By using edges $e_P(v)$, $e_L(v)$, and $e_R(v)$ incident with S box v , we divide all global routes passing through v into 4 types;

- Type I: global routes containing $e_P(v)$, $e_L(v)$, and $e_R(v)$,
- Type II: global routes containing $e_P(v)$ and $e_L(v)$,
- Type III: global routes containing $e_P(v)$ and $e_R(v)$,
- Type IV: global routes containing $e_L(v)$ and $e_R(v)$.

Let $n_T(v)$, $n_L(v)$, $n_R(v)$, and $n_C(v)$ be the numbers of global routes of these types, respectively.

Consider the following detailed routing process, and conduct it for each S box v on the H -tree in the depth-first or breadth-first manner from the root.

[Track Assignment at S box v]:

Suppose that the detailed routes in edge $e_P(v)$ have been determined already.

- 1) For each global route of Type I, II, and III, determine its detailed route in edges $e_L(v)$ and $e_R(v)$ consistently with track id in edge $e_P(v)$ and the S box topology.
- 2) For each global route of Type IV, assign track t in edges $e_L(v)$ and $e_R(v)$ such that t is the least track id and track t is not occupied yet by other detailed route in both $e_L(v)$ and $e_R(v)$.
- 3) For each global route containing a C box in edge $e_L(v)$, assign track t in edges $e_L(v)$ such that t is the least track id and track t is not occupied yet by other detailed route.
- 4) For each global route containing a C box in edge $e_R(v)$, assign track t in edge $e_R(v)$ such that t is the least track id and track t is not occupied yet by other detailed route.

Lemma 2: If the number W of tracks in a channel is not less than the chromatic number $X(G_i)$ of the subtree graph G_i of given global routes, then we can conduct this track assignment process successfully for all S boxes in the H -tree.

Proof: Since the number of tracks in edge $e_P(v)$ is equal to $X(G_i)$, the maximum track id in edge $e_L(v)$ or $e_R(v)$ assigned to a global route of Type I, II, or III is not greater than $X(G_i)$. From the definition of $X(G_i)$, we have $n_T(v) + n_L(v) + n_R(v) + n_C(v) \leq X(G_i)$, and hence we can find at least $n_C(v)$ tracks in both $e_L(v)$ and $e_R(v)$, which are not occupied by global routes of Type I, II, and III. Therefore, the nets of global routes of type IV are also assigned to tracks whose id is not greater than $X(G_i)$. From the definition of $X(G_i)$, we can see that steps (3) and (4) are also executed successfully without using more than $X(G_i)$ tracks. Thus, this process can be conducted from the root of the H -tree for all vertices. \square

If at an S box this process fails, then it means that $W < X(G_i)$ and given instance is not routable. It is not difficult to see that this process can be executed for all S boxes in time $O(N + |LUT|)$. Thus, we have the following theorem.

Theorem 6: Given global routes with N nets in an H -tree type routing architecture with W disjoint track domains, the routing decision problem and the problem of finding an optimum routing can be solved in $O(N + |LUT|)$ time.

Moreover, we can prove the following theorem.

Theorem 7: In an H -tree type routing architecture with W disjoint track domains, mapping ratio W_d/W_g is bounded by $3/2$.

Proof: The size of a maximal clique in G_i which is composed of vertices corresponding to global routes passing through a common edge is not greater than W_g . Hence, if

the maximum clique of G_i is composed of such vertices, then $X(G_i) \leq W_g$. Therefore, in this case we have

$$W_d/W_g = X(G_i)/W_g \leq 1.$$

Otherwise, the maximum clique is composed of vertices corresponding to global routes passing through an S box, say v . In this case, we can see from the definition of W_g that the following inequalities hold:

$$n_T(v) + n_L(v) + n_R(v) \leq W_g$$

$$n_T(v) + n_L(v) + n_C(v) \leq W_g$$

and

$$n_T(v) + n_R(v) + n_C(v) \leq W_g.$$

Therefore, we have

$$\begin{aligned} & 2\{n_T(v) + n_L(v) + n_R(v) + n_C(v)\} \\ & \leq n_T(v) + 2\{n_T(v) + n_T(v) + n_R(v) + n_C(v)\} \leq 3W_g. \end{aligned}$$

Moreover, $X(G_i)$ is bounded by

$$X(G_i) \leq n_T(v) + n_L(v) + n_R(v) + n_C(v).$$

Therefore, we have

$$\begin{aligned} 2W_d &= 2X(G_i) \\ &\leq 2\{n_T(v) + n_L(v) + n_R(v) + n_C(v)\} \leq 3W_g \end{aligned}$$

and

$$W_d/W_g \leq 3/2. \quad \square$$

The interesting property of this model is that due to the tree structure, all global routes are automatically decided by placement. Moreover, the routability can be decided efficiently in the placement phase.

VII. CONCLUSION

Due to high cost of hardware and loss of performance attributed to routing resources, practical FPGA technologies will most likely be limited to a relatively low flexibility architecture. We have analyzed the routing structures of the 2-D FPGA architecture with full C box flexibility and basic S box flexibility of 3. We observed that the Xilinx-like architecture which falls into this category, has a property of disjoint track domains. We have analyzed the general conditions for disjoint track domains of such architectures. We have shown that all disjoint architectures are exactly the same as the Xc4000 architecture which yields no predictable mapping between global and detail routing.

We further indicate that any arbitrarily arranged overlapped architecture of the same switch box flexibility can not ease this problem. We have proven that there does not exist such a switch box topology that can yield better routability than the one currently used. As a general result, we have proved that the track assignment problem encountered by a detailed router following net topologies determined by a global routers, for both disjoint and overlapped architectures, is NP-complete. There is no constant bound on the mapping ratio the number of tracks required to complete detailed routing over global

routing channel densities for this architecture. Finally, we show two directions of changing the routing architectures to yield polynomial time mapping solutions and constant bounded mapping ratios.

In this paper, we have formulated the mapping problem for a typical array type FPGA routing architecture as a 2-D interval packing problem, which seems to be the first 2-D interval packing formulation in CAD applications. We have explored the routing properties of this model. As a side result, we also conclude that the originally proposed diagonal switch box topology, although being the simplest, is not likely worse than any other switch box topology with the same flexibility. We hope that our theoretical results will contribute to insightful understanding of fundamental routing properties of this 2-D routing architecture.

APPENDIX

PROOF OF THEOREM 1 AND LEMMA 1

Given a permutation P_k and a track id t , $P_k(t)$ denotes a track id mapped from t by permutation P_k , and given two permutations P_k and P_h , $P_k P_h$ is a permutation mapping t into $P_k(P_h(t))$.

Theorem 1: Let I be the identity permutation, the routing structure is a disjoint routing architecture, if and only if the permutations defining the S box topology satisfy all the following conditions:

- 1) $P_2 P_3 P_4 P_1 = I$,
- 2) $P_4 P_3 P_2 P_1 = I$,
- 3) $P_3 P_2 = P_6$, $P_2 P_1 = P_5$.

Proof: In a disjoint routing structure, the wire segments are partitioned into W disjoint track domains. Hence, in each C box around any logic cell, there is exactly one member of a each track domain. Therefore, these members define permutations satisfying (1). Moreover, in each C box around any S box, this is also true, so that we have conditions (2) and (3). Thus, we can readily see the proof of "only if" part.

To prove "if" part we will show how to partition the wire segments. First we show the basis step of the proof by partitioning wire segments in the neighborhood of a logic cell, and then extend it by induction (see Fig. 11). Here, we prove the existence of the wire segments partition by using only P_1 , P_2 , P_3 , and P_4 , without using horizontal (P_5) and vertical (P_6) switches. The extension of this proof is similar and skipped.

There exists a partition into disjoint track domains around each logic cell as guaranteed by the condition (1) above ($P_2 P_3 P_4 P_1 = I$). We construct the complete disjoint segments partition as follows.

- a) Starting from an arbitrary logic cell, say L_1 , partition the segments around L_1 into W disjoint domains by linking every wire segment in a C box (say top C box) to a wire segment on its mapped track in the next consecutive C box according to the permutation relation (say P_1). Visit all the C boxes around L_1 in a clockwise direction linking wire segments as specified by appropriate permutations. Condition (1) guarantees that we will get disjoint track domains around L_1 .

- b) Similarly, construct W disjoint track domains surrounding the top neighbor of L_1 , say the L_2 block. Any two track domains around L_1 and L_2 which share a wire segment in their common adjacent connection box will be given the same domain id . We say that such two track domains have been merged.
- c) In a similar way we can extend the segments partition to the tracks surrounding the left or right neighbor of the block L_1 .
- d) Suppose that we are now considering an L block, say L_i , such that all the L blocks above and to the left of it have their surrounding wires assigned to appropriate disjoint domains as dictated by the permutations P_1, P_2, P_3, P_4 and that any two domains which shared a common segment were assigned the same track id . Now, we construct again the W disjoint track domains around L_i as specified by the permutations P_1, P_2, P_3 and P_4 . Take an arbitrary such a domain. Suppose its top wire has been assigned an id k in the previous construct and its left wire has been assigned an id m , see Fig. 11. Let us traverse the domain m starting at point B . We will follow a path $BAHG FED I J K L U T S R X O N C B$. If we start from the point B on a track in the domain m and follow this domain induced by the permutations around L_i , our path will be $BO'X'WVYZAB$. On the other hand, if we again start at the point B and this time follow the connections around the switch box S , we will traverse a loop $BO'N'CB$, what is quarantined by condition (2). But this leads to a contradiction, because now the mapping P_4 is not one-to-one since both N and N' which are on different tracks map to C . Therefore, we conclude that the points O and O' overlap and also that X and X' overlap. We can then merge the domains generated around L_i with the previously existing domains.
- e) By repeating this process, a wire segments partition can be constructed to cover the entire chip. \square

Lemma 1: Consider the FPGA instance, constructed in Theorem 3, and an arbitrary C -box through which two global routes, R_1 and R_2 pass. For each wire segment in such a C -box the color domain ids induced by R_1 and R_2 are the same (see Fig. 7(c)).

Proof: Let $P = P_3^{-1}P_1$, and consider the global route of a net i . For each j ($1 \leq j \leq i$), depending on if vertices i and j in the given graph G are adjacent or not, the global route passes through either C box $(2+2(i-1)s+2j, 1+2j(r+1))$ or C box $(2+2(i-1)s+2j, 1+2(j-1)(r+1)+2)$ (the dotted path in Fig. 7(c)). In both cases, we can show the following claims concerning subdomains in the global route.

Claim 1: At either C box $(2+2(i-1)s+2j, 1+2j(r+1))$ or C box $(2+2(i-1)s+2j, 1+2(j-1)(r+1)+2)$ ($1 \leq j \leq i$), wire segment $P_j(t)$ (and only this segment) is contained in subdomain with color t (i.e., the track id of net i at the starting C box is t).

Claim 2: At every C box $(2+2(i-1)s+2i+ks, 1+2i(r+1))$ ($k = 0, 1, 2, \dots$) through which the base horizontal run of the global route of a net i passes, wire segment $P_i(t)$ (and only this segment) is contained in subdomain of color t .

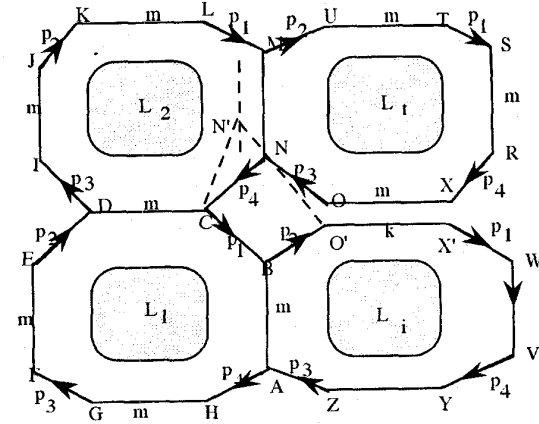


Fig. 11. Supporting example for proof of Theorem 1. (C and S boxes are omitted for clarity.)

Then, at C box $(2+2(i-1)s+2j, 1+2j(r+1))$ where two global routes pass, one is the base horizontal run of the net j and the other is a horizontal segment of the net i , subdomains with color t in both global routes of nets i and j have the same wire segment $P_j(t)$. Hence, the lemma. \square

Proof of Claim 1: In the above construction, if the global route of the net i is assigned the subdomain t then the track id 's of the net i segments in C box $(2+2(i-1)s+1, 2)$ and C box $(2+2(i-1)s+1, 2+2r)$ are all $P_1(t)$, since $(P_6^{-1})^r = I$. And the wire segment contained in the subdomain with the color t at C box $(2+2(i-1)s+2, 3)$ or at $(2+2(i-1)s+2, 1+2(r+1))$ is $P(t)$. Hence, we see that the claim holds for $j = 1$. Moreover, since $(P_6^{-1})^r = I$, we can see that a wire segment in C box $(2+2(i-1)s+3, 1+2(r+1)+1)$ contained in subdomain with the color t in the global route of the net i is $P_1P(t)$.

For example, consider subdomain with the color b in the global route of the net 2 in Fig. 8(b). The wire segment in C box $(7, 2)$ in the subdomain is $x = P_1(b)$, and hence the segments in the C box $(8, 3)$ is $P(b)$. The segment in the C box $(7, 6)$ in the subdomain is $x' = (P_6^{-1})^r(x) = x = P_1(b)$, and hence the segment in the C box $(8, 7)$ is also $P_1P_3^{-1}(b) = P(b)$. Moreover, the segment in the C box $(9, 8)$ in the subdomain is $y' = P_1P(b) = y$.

Thus if $j = 1$, then a segment in C box $(2+2(i-1)s+1+2j, 1+2j(r+1)+1)$ which is contained in subdomain with color t in the global route of net i is $P_1P^j(t)$. Therefore, through the similar argument, we can see that at C box $(2+2(i-1)s+2j, 1+2j(r+1))$ or C box $(2+2(i-1)s+2j, 1+2(j-1)(r+1)+2)$ ($j = 2$), the claim 1 holds. Thus, we observe that a segment in C box $(2+2(i-1)s+1+2j, 1+2j(r+1)+1)$ ($j = 2$) which is contained in subdomain with color t in the global route of net i is $P_1P^j(t)$. Repeating such a discussion, for $j = 2, 3, 4, \dots$, we have the claim 1. \square

Proof of Claim 2: From Claim 1 we see that at C box $(2+2(i-1)s+2i, 1+2i(r+1))$, subdomain with the color t in the global route of net i contains wire segment on a track whose id is $P^i(t)$. Therefore, at every C box

$(2 + 2(i - 1)s + 2i + ks, 1 + 2i(r + 1))(k = 0, 1, 2, \dots)$ through which the base horizontal run of the net i passes, the track id is $(P_5)^{ks}(P^i(t)) = IP^i(t) = P^i(t)$, if the net i is assigned subdomain color t .

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