On Computational Complexity of a Detailed Routing Problem in Two-Dimensional FPGAs

*Yu-Liang Wu +Shuji Tsukiyama *Malgorzata Marek-Sadowska

*Department of Electrical and Computer Engineering
University of California, Santa Barbara, CA 93106.

+Department of Information and System Engineering
Chuo University, Tokyo, Japan 112

Abstract

In this paper, we consider the problem of mapping a given global route to a detailed route for two dimensional homogeneous FPGAs. It has been shown that this problem is NP-complete on a popular Xilinx-4000-like routing architecture [1]. Here, we further prove that this problem remains NP-complete for an arbitrary fixed switch box topology of the same connection flexibility, with or without doglegs allowed in detailed routes.

Index Term: FPGA Routing, NP-Complete, Switch Box Topology.

1. Introduction

Because of the advantages of quick prototyping and low production cost on medium quantity productions, Field Programming Gate Arrays (FPGAs) have become an attractive circuit medium for ASIC implementations. Routability issues are of major the concern for current FPGA technologies, since the routing delay and routing resources are the dominating factors in the circuit performance and chip area.

In other mature design styles like macro cell, standard cell or gate array, routing, due to its complexity, is usually divided into global and detailed steps. Global routers are typically tuned to produce balance-distributed routing paths for all nets, to ease the work of the following detailed routing. Most of the existing FPGA routing approaches follow a similar strategy. Thus the success of routing is decided by the feasibility of finding detailed routes for the global routed nets. In this paper, we investigate the routability issue of FPGAs by looking at the problem of mapping a given global route to a detailed route for symmetrical-array (two-dimensional) homogeneous FPGAs.

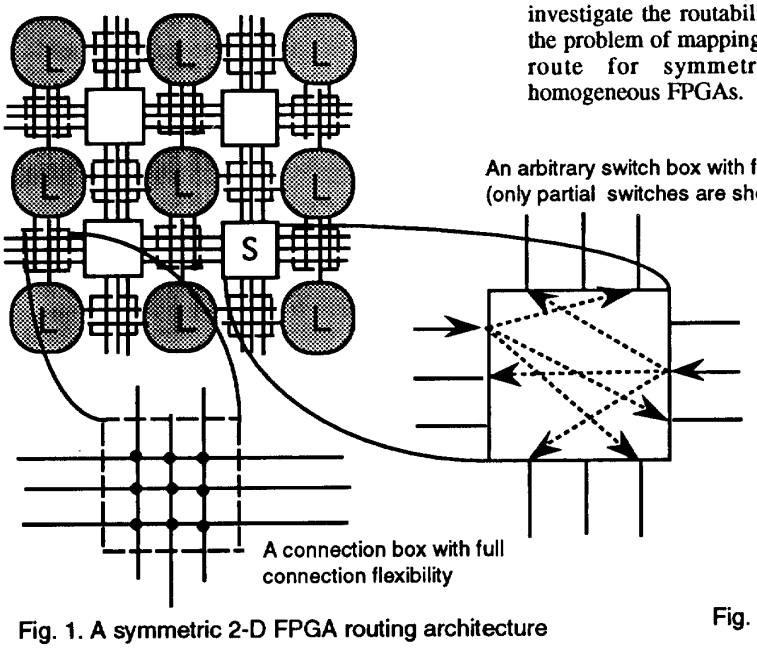


Fig. 1. A symmetric 2-D FPGA routing architecture

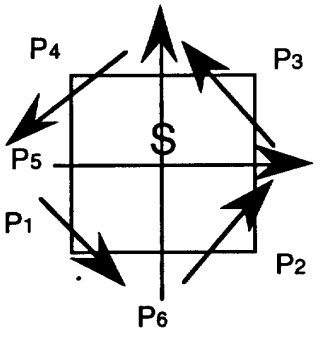


Fig. 2. Track permutation mappings.

The routability of FPGAs depends on the connectivity of routing resources, particularly on characteristics of connection boxes and switch boxes (see Fig. 1). Due to the particularly high hardware and performance cost attributed to routing resources, today's FPGA technologies will most likely be limited to a relatively low flexibility architecture. Past studies [3-4] based on a more general flexibility spectrum have suggested the connection flexibilities of 100% for connection boxes and flexibility of three for switch boxes considering both routability and reasonable hardware costs (for detailed definition, please see the next section). These are also connection flexibilities adopted by the current popular XC4000 [2] architectures. In this study, we will investigate properties of this typical routing architecture. Here, we assume that the routing architecture is homogeneous, i.e. all the routing boxes of the same type have the same switch connection topology.

Even in this kind of low flexibility routing architecture, however, there still exists exponentially large number of different switch connection arrangements inside a switch box. The search of a better routable switch connection patterns with the same hardware cost (the same number of connection switches per switch box) has been an attractive and practical objective for current FPGA manufacturers. The existence of such an architecture will be one of the major questions we want to answer in this paper.

In the following, we conduct our investigation by first showing that all the possible connection arrangements can be classified into two major types of routing architectures: disjoint and overlapped.

We show that the routing structure of the said Xilinx XC4000 FPGA architecture has a special property of disjoint track domains, thus classified as a special case of the disjoint routing architecture. We then show that all such disjoint routing architectures are equivalent from the routability point of view. Secondly, we show further that even any arbitrarily arranged overlapped architecture of the same switch box connection flexibility can not ease this problem. Therefore, we formally prove that there does not exist such a switch box topology that can rudimentally yield better routability than the currently used one [2].

In short, we have proved that the track assignment problem encountered by a detailed router following net topologies determined by a global router for both disjoint and overlapped architectures is NP-complete with or without allowing doglegs in detailed routes.

Additionally we study the bound on the ratio of track number required for 100% routing completion over the channel density determined by a global router for arbitrary switch box topologies .

2. Two-dimensional FPGA routing architectures

In this paper we are considering the Xilinx-like homogeneous array architecture [1-5]. This architecture is a Look-Up-Table (LUT) and SRAM technology based. As depicted in Fig. 1, it is a two-dimensional array of logic cells. Each logic cell is marked L and can be configured to be a Look-Up-Table, flip-flop,..etc [2]. Wire segments run between the cells in vertical and horizontal channels. Routing switches are grouped into the connection (C) boxes and switch (S) boxes. The C boxes contain routing switches that can be programmed to connect logic block pins to wire segments. The S boxes contain switches that allow one wire segment to be connected to another. The flexibility of a C block, F_C, is defined to be the number of tracks a logic pin can connect to, and the flexibility of S block, F_S, is defined to be the number of outgoing tracks that an incoming track can connect to. Similarly to [1,3-5], we consider only the unit-length wire segments, and assume W is the number of tracks of every horizontal and vertical routing channel.

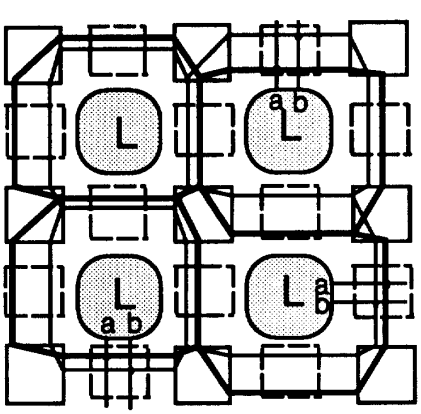
We will investigate routing problem for the array type architecture with connection boxes of full flexibility and switch boxes of flexibility 3. We consider 3 as the basic or minimum flexibility of a switch box, since a flexibility lower than this will render some nets unroutable even when there is no routing congestion. Such a structure of routing resources was experimentally concluded to be the most effective considering both routability and reasonable hardware cost [3-5]. This routing flexibility has been adopted in the Xilinx-4000 architecture [2]. The experimental results, in which a conventional global/detailed routing scheme was used, also have shown that there exists a difficulty in predicting the number of tracks needed to complete detailed routing (W_d) given the channel density determined by a global router (W_g).

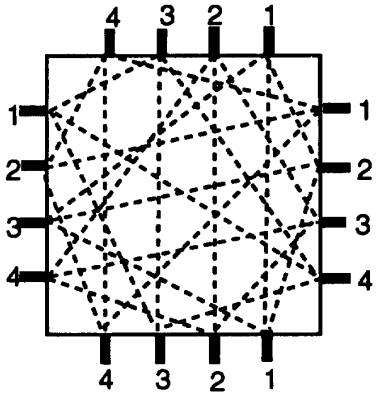
The tracks in each horizontal channel are numbered from top to bottom and in each vertical channel are numbered from right to left. A number assigned to each track is referred to as *track's id* . An internal topology of a switch box can be characterized by 6 track permutation [6] mappings (P_1~P_6) of the 4 sides (Fig. 2).

All two dimensional FPGAs can be classified into two categories: disjoint track domains and overlapped track domains architecture. A routing architecture has disjoint track domains if any two routes passing through a common C box on two different tracks remain on different tracks for any topology of these routes (Fig. 3a), otherwise the routing architecture has an overlapped track domains (Fig. 3b).

A detailed route of net A is a route without doglegs if every pin labeled A connects to exactly one track; otherwise, it is a dogleg route.

3. Complexity analysis of 2-D FPGA routing





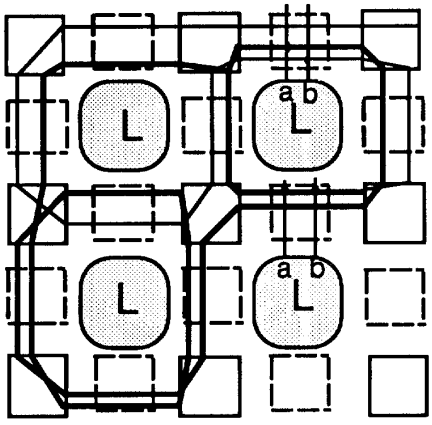
: S Box

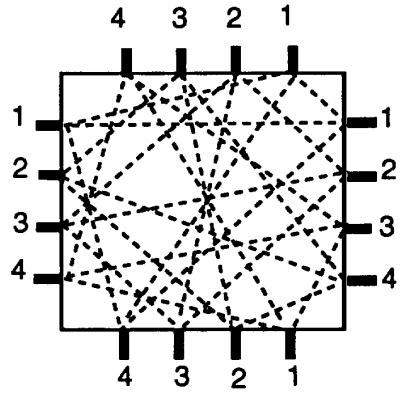
: C Box

$P_1 = \begin{pmatrix} 1 & 2 & 3 & 4 \\ 3 & 4 & 1 & 2 \end{pmatrix}$ $P_2 = \begin{pmatrix} 1 & 2 & 3 & 4 \\ 2 & 3 & 4 & 1 \end{pmatrix}$

$P_3 = \begin{pmatrix} 1 & 2 & 3 & 4 \\ 4 & 1 & 2 & 3 \end{pmatrix}$ $P_4 = \begin{pmatrix} 1 & 2 & 3 & 4 \\ 3 & 4 & 1 & 2 \end{pmatrix}$

Fig. 3a. A disjoint routing switch box structure
(Net a and net b will never overlap at any C box).





$P_1 = \begin{pmatrix} 1 & 2 & 3 & 4 \\ 4 & 2 & 3 & 1 \end{pmatrix}$ $P_2 = \begin{pmatrix} 1 & 2 & 3 & 4 \\ 3 & 4 & 2 & 1 \end{pmatrix}$

$P_3 = \begin{pmatrix} 1 & 2 & 3 & 4 \\ 1 & 2 & 4 & 3 \end{pmatrix}$ $P_4 = \begin{pmatrix} 1 & 2 & 3 & 4 \\ 1 & 3 & 2 & 4 \end{pmatrix}$

Fig. 3b. An overlapped routing architecture (
Net a and net b may overlap at some C boxes).

We address the questions raised in the previous section by studying the following problem.

[2-D FPGA Routing without doglegs]:
Instance: A global route of a circuit, 2-D array of logic cells, flexibility three S box of arbitrary topology of switches and channel capacity W.
Question: Does there exist a valid W track detailed routing without doglegs for the given global route?

Theorem 1. *Problem [2-D FPGA Routing without doglegs] is NP-complete for any fixed S box topology and flexibility three.*

Proof.

This theorem is proven by showing that the problem [W Coloring of a Graph] is polynomially reducible to our problem. It is known that if W is a constant greater than 2, this problem is NP-complete.

We will show that [W Coloring of a Graph] is polynomially reducible to our routing problem. In order to build a 2-D FPGA routing instance for a given graph G = (V, E), for each vertex i, $1 \le i \le |V|$, we create a net i and its global route in such a way that two routes pass through a connection box if and only if their corresponding vertices are adjacent in the graph.

It is known that any permutation P can be decomposed into a product of several disjoint cyclic permutations. Let T be the least common multiple of the lengths of these cyclic permutations, then $(P)^T$ is an identity permutation. For example, if $P_x = \begin{pmatrix} 1 & 2 & 3 & 4 & 5 \\ 3 & 5 & 4 & 1 & 2 \end{pmatrix}$, then $P_x = (134)(25)$, and $(P_x)^6 = I$. Let us denote the T values of P_5 and P_6 as s and r respectively, then $(P_5)^s = (P_5^{-1})^s = I$, and $(P_6)^r = (P_6^{-1})^r = I$. Since W is a constant, s and r are constants too. (If s = 1, we will set it to 2 in this proof.) This implies that a route using horizontal (vertical) segment with a track id of k will again use a segment of the same track id k after traversing horizontally (vertically) s (r) S boxes.

The global route of each net i which we create will have a stair case shape. It originates with the unit segment in the C box at coordinates (2+2(i-1)s, 1), and has a "base" horizontal run, starting from the C box at coordinates (2+2(i-1)s+2i, 2+2i(r+1)) and terminating at the rightmost C box on the same horizontal channel, where C box at coordinates (x, y) indicates the one located on the x-th column and the y-th row, as shown in Fig. 4.3.

Between the starting unit segment and the base horizontal run, the global route has a unit segment for each j, $1 \le j \le i$, in such a way that if vertices i and j are adjacent, then the unit horizontal segment is in the C box at coordinates (2+2(i-1)s+2j, 1+2j(r+1)), otherwise in the C box at coordinates (2+2(i-1)s+2j, 1+2(j-1)(r+1)+2). Then, all these segments of net i are connected by vertical routes so that the route forms a stair case like meandering run. The size of the FPGA instance built in this way is $O(|V|^2)$, and this reduction is done in $O(|V|^2)$ time. Fig. 4.3 illustrates a reduction example for a 4-clique, where the dotted lines indicate the case of Fig.4.2 where some vertices are not adjacent.

Now, let us try to color all tracks which belong to a net with the same color and this color is represented by the track id of the starting segment of this net. That is, any two nets starting from the same track id (at the first row) will be assigned the same color, otherwise two different colors. Let us assume that a net A starts from track a therefore all of its segments are painted with color a. Similarly net B is painted with certain color represented by the symbol b. It is obvious that a detailed routing is valid if and only if any two nets pass through the same C box are connected to different segments at that C box. Since any two adjacent segments of a 2-pin net are connected by a single switch which is uniquely determined by a side to side permutation mapping, all tracks to be painted of a certain net are uniquely decided when the starting segment is decided. Now, we will show that based on our former formulation, we will be able to claim that a detailed routing is valid if and only if two nets pass through the same C box are painted with different colors. And therefore deciding if the routing instance is W track routable is the same as deciding if all these nets are W colorable according to our coloring constraints.

In the following, we just illustrate the concept by an example shown in Fig.4, where an FPGA instance of a 4-clique graph is depicted. Let a, b, c, and d be the four unknown colors, i.e. track id's of their starting segments located at row one, assigned to the corresponding nets A, B, C, and D of the 4-clique. Then we know that a valid detailed route should satisfy the following conditions :

Let $P = P_3^{-1}P_1$,

then track a at the C box (2,1) is connected to track a' at C box (4,7) and a' = P(a), because $a' = P_3^{-1}(P_6)^r P_1(a) = P_3^{-1}IP_1(a) = P_3^{-1}P_1(a) = P(a)$.

$a'' = (P_5)^s(a') = I(a') = a' = P(a)$. Similar results can be shown on all base runs.

In a valid detailed route, P(a), which represents the track id of the segment connected to net A at C box (8,7), must be different to P(b), therefore,

we have: $a \neq b$, (1)

since $P(a) \neq P(b)$ iff $P^{-1}P(a) \neq P^{-1}P(b)$ iff $a \neq b$.

In other words, this relation of running through a same C box enforces nets A and B to be painted with different colors.

Similarly we have $a \neq c$, (2)

and $a \neq d$. (3)

and

$P^2(b) \neq P^2(c) \Rightarrow b \neq c$, (4)

$P^2(b) \neq P^2(d) \Rightarrow b \neq d$, (5)

$P^3(c) \neq P^3(d) \Rightarrow c \neq d$, (6)

The minimum number of colors required to paint nets A, B, C, and D, such that all the coloring constraints of (1) to (6) are satisfied will be the chromatic number of the related graph, since their coloring constraints are exactly the same.

To see how an "empty" edge is implemented, let us reduce a graph without edge (B,A) and (C,B) into a 2-D FPGA routing instance. The segment of net B is now moved to C box (8,3) instead of (8,7). Be aware that the track id of y' is uniquely decided and that all tracks connected after y' are uniquely decided also so long as track id b is decided, no matter which path, either x-x'-y' or x-y-y' is chosen. Similarly, another segment is moved to (14,9). It is clear that this new FPGA instance will have to fulfill all the above listed coloring constraints except (1) and (4). We have now shown that the W colorable decision problem of an arbitrary graph is reducible to a W track routable problem of the 2-D FPGA, thus we prove this theorem. **Q.E.D.**

$(P_5)^s = I$ I : identity permutation : L block

$(P_6)^r = I$ i : vertex (net) id $P = P_3^{-1} P_1$

assuming: r = 2, s = 2

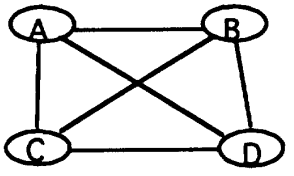


Fig. 4.1 a 4-clique graph

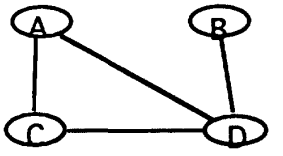


Fig. 4.2 an arbitrary graph

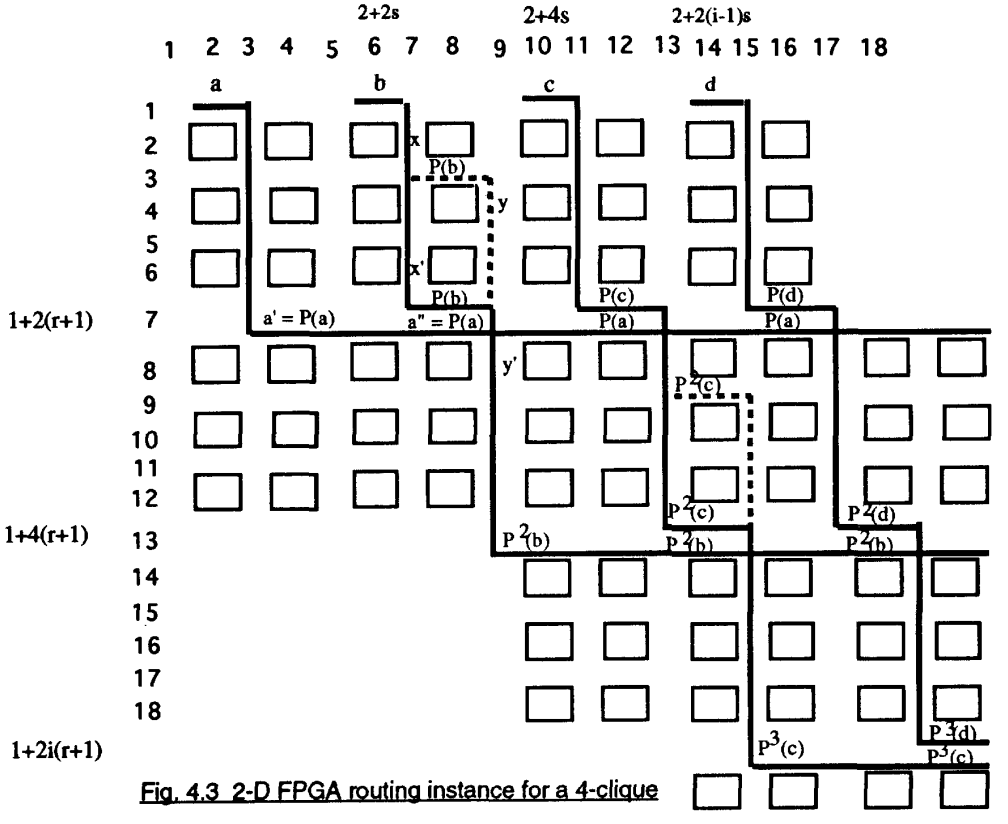


Fig. 4.3 2-D FPGA routing instance for a 4-clique

From this theorem we conclude that because the W track routability problem is NP-complete, it would be hard to construct an efficient algorithm for our mapping problem.

Since the problem of [2-D FPGA Routing without doglegs] reflects the process of mapping the global to detailed routing, we also conclude that any switch topology with Fs = 3 will not improve the routability of 2-D FPGAs.

Here we only consider the case where in each S box an incoming track must be connected directly to an outgoing track through a single switch specified by a permutation, i.e., an incoming track cannot be connected to an outgoing track through 2 or 3 switches. If we connected an incoming track to an outgoing track through 2 switches, then an additional wire segment not included in the global route would be used.

In this investigated mapping problem, the difference between Wd and Wg can be arbitrarily large,

where Wd is the number of tracks required in its optimal detailed routing and Wg is the channel density decided by a global router. In our proof we show that for an arbitrary graph in [W Coloring of a graph] we can create a global routing instance such that the nets correspond to the vertices of the graph, the global channel density Wg is 2, and the FPGA instance is Wd track routable if and only if the graph is Wd colorable. For example, if a given graph G is a complete graph with Wd vertices, then Wd tracks are necessary to complete the detailed routing.

Theorem 2. *Given a global routing of a 2-D FPGA chip with an arbitrary S box topology and flexibility three, there does not exist a constant c, s.t. Wd/Wg ≤ c for an instance of 2-pin nets. As before, W_d is the number of tracks required in the optimal detailed routing and Wg is the channel density decided by the global router.*

Now, let us consider the case of multi-terminal nets admitting doglegs for detailed routing. A dogleg may occur at a pin which belongs to a multi-pin net. Then we can readily derive the following theorem.

[2-D FPGA Routing with doglegs]:
Instance: A global route of a circuit, 2-D array of logic cells, and an arbitrary S box topology of flexibility three, channel capacity W.
Question: Does there exist a valid W track dogleg detailed routing for the given global route?

Theorem 3. *Problem [2-D FPGA Routing with doglegs] is NP-complete for any fixed S box topology and flexibility three.*

If a dogleg is allowed at a pin which belongs to a multi-pin net then the net is split at this pin into two nets. In particular, if doglegs are allowed on all pins, a net may be split into 2-pin nets. The subnets of a common net are assigned the same id with different subscript numbers. All nets with the common id's and different subscripts can be assigned to different tracks but also they may choose a common track what results in a route without doglegs.

The corresponding coloring graph G_d has nodes representing the subnets. If two subnets of a different net pass through a common C box, then there is an edge in G_d between the corresponding vertices. Two nodes representing subnets of the same net are connected by auxiliary edges. An auxiliary edge means that these two nodes can choose either the same or different colors when graph coloring is sought.

Using doglegs in routing does not decrease the computational complexity of the global to detail routing mapping problem. In general, the size of a graph for which chromatic number needs to be determined will be larger than for the corresponding case of simple routing. The optimal coloring for the dogleg style should be carried out in two stages. In the first step, all solutions with the least number of colors are sought for a graph without the auxiliary edges. In the second step we pick such a node coloring among those found earlier which have the least distinct color node pairs incident to the auxiliary edges, because each such a pair introduces a dogleg.

4. Conclusions

We have shown that for an arbitrary S box topology of flexibility three in the homogeneous two dimensional FPGA architectures, the final optimal detailed routing may require a number of tracks arbitrarily larger than the channel density found by the global router (even when the W_g is just 2).

We have shown that the difficulty of the 2-D FPGA routing problem can not be rudimentary improved by any permutation of the S box track connection patterns. As a side result, we also conclude that the originally proposed diagonal switch box topology [2], although the simplest, is not likely to be worse than any other switch box topology with the same flexibility.

5. References

[1]. Y. L. Wu and M. Marek-Sadowska, "Graph Based Analysis of FPGA Routing", *Proc. EURO-DAC with EURO-VHDL* pp. 104-109, 1993.

[2]. H. Hsieh, et. al. "Third-Generation Architecture Boosts Speed and Density of Field Programmable Gate Arrays", *Proc. CICC*, pp. 31.2.1-31.2.7. 1990.

[3]. J. Rose, and S. Brown, "The Effect of Switch Box Flexibility on Routability of Field Programmable Gate Arrays", *Proc. CICC*, pp. 27.5.1-27.5.4, 1990.

[4]. J. Rose, and S. Brown, "Flexibility of Interconnection Structures for Field Programmable Gate Arrays", *IEEE Journal of Solid-State Circuits* Vol. 26, No. 3. March 1991.

[5]. B. Tseng, J. Rose, and S. Brown, "Improving FPGA Routing Architecture Using Architecture and CAD Interactions", *Proc. ICCD*, pp. 99-104, 1992

[6]. C. L. Liu, "Introduction to Combinatorial Mathematics", *McGraw-Hill Book Company*, 1968.