### N92S100, N82S101 Bipolar Field Pro-CONNECTION DIAGRAM grammable Logic Array (16 x 48 x 8)

GENERAL DESCRIPTION

The 82S100 (tri-state outputs) and the 82S101 (open collector outputs) are Bipolar Programmable Logic Arrays, containing 48 product terms (AND terms), and 8 sum terms (OR terms). Each OR term controls an output function which can be programmed either true active-high (Fp), or true active-low (Fp). The true state of each output function is activated by any logical combination of 16-input variables, or their complements, up to 48 terms. Both devices are field programmable, which means that custom patterns are immediately available by following the fusing procedure outlined in this data

The 82S100 and 82S101 are fully TTL compatible, and include chip-enable control for expansion of input variables, and output inhibit. They feature either open collector or tri-state outputs for ease of expansion of product terms and application in bus-organized systems.

Both devices are available in commercial and military temperature ranges. For the commercial temperature range 0°C to +75°C) specify N82S100/101, I or N, and for the military temperature range (-55°C to +125°C) specify S82S100/101.I.

#### APPLICATIONS

- CRT display systems
- Random logic
- Code conversion
- Peripheral controllers
- Function generators Look-up and decision tables
- Microprogramming
- Address mapping
- Character generators
- Sequential controllers
- Data security encoders
- Fault detectors
- Frequency synthesizers

#### MAXIMUM BATINGS

PARAMETER	RATING		UNIT
	Min	Max	
VCC Supply voltage VIN Input voltage VOUTOutput voltage IIN Input currents IOUT Output currents Temperature range TA Operating	-30	+7 +5.5 +5.5 +30 +100	Vdc Vdc Vdc mA mA °C
N82S100/101 S82S100/101 TSTG Storage	0 -55 -65	+75 +125 +150	

#### LOGIC FUNCTION

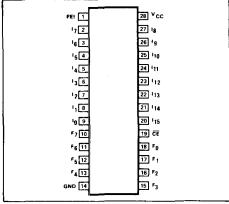
Typical Product Term:

 $P_0 = I_0 \bullet I_1 \bullet \overline{12} \bullet I_5 \bullet \overline{113}$ 

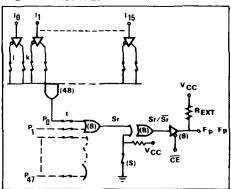
Typical Output Functions

 $F_0 = (\overline{CE}) + (P_0 + P_1 + P_2) @ S = Closed$   $F_0^* = (\overline{CE}) + (\overline{P_0} \bullet \overline{P_1} \bullet \overline{P_2}) @ S = Open$ 

For each of the 8 outputs, either the function  $F_p$  (active-high) or  $F_p^*$  (active low) is available, but not both. The required function polarity is programmed via link (S).



#### FPLA EQUIVALENT LOGIC PATH



TRUTH TABLE

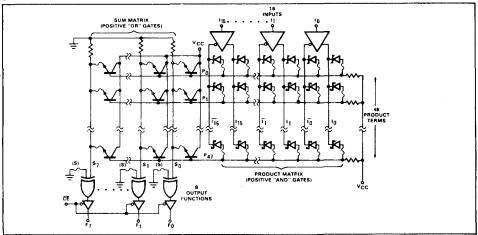
MODE	Pn	ΖĒ	Sr 2 f(Pn)	Fp	Fp*
Disabled (82S101)	×	1	×	1	T
Disabled (82\$100)				Hi-Z	Hi-Z
Read	1 0	0	Yes	1	0 1
Head	X	0	No	0	1

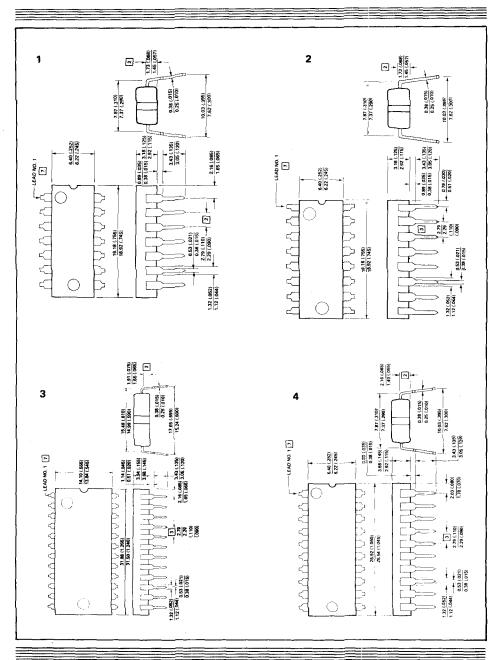
#### REFERENCE TABLE

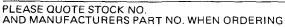


### N82S100, N82S101 Cont.

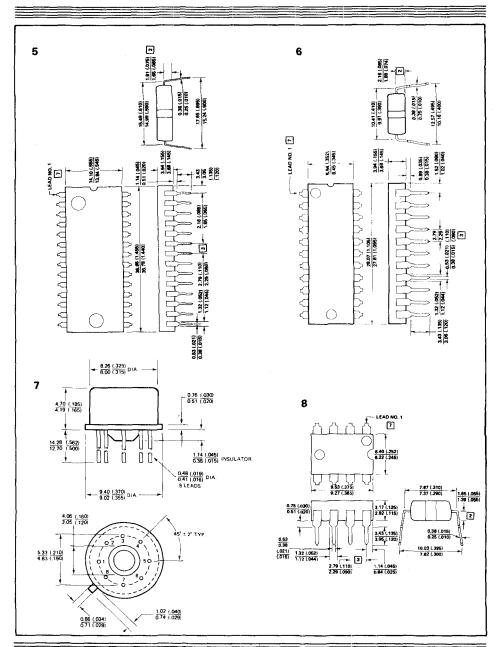
LOGIC DIAGRAM





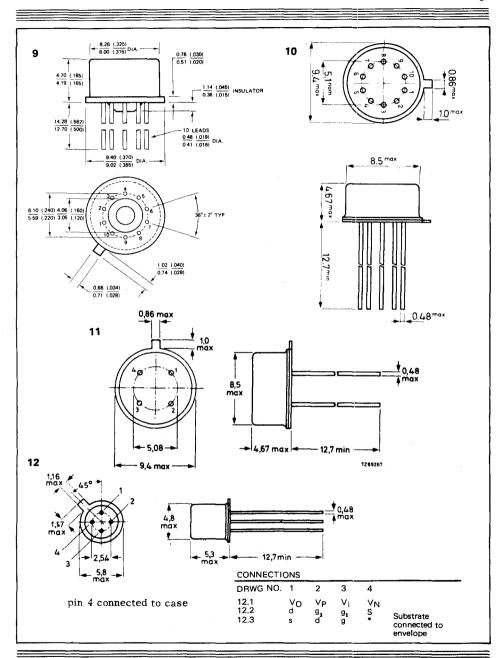








### **Outline Drawings**



PLEASE QUOTE STOCK NO.
AND MANUFACTURERS PART NO. WHEN ORDERING



