

DUE: Wednesday, October 1 at 11:59 PM.

Absolutely no late assignments accepted

Introduction:

You must work in pairs on this and the following assignments and submit only one electronic copy per team. Since team work will become increasingly important throughout the semester, you are expected to spend time reflecting on your team's strategies to deal with problems and work effectively. Eventually, you will have to assess in writing your own and your partner's performance. It is thus to your advantage, for this and every subsequent assignment, to take a deliberate approach to all aspects of your team's work and the skills that each one of you is bringing to the table, including responsibility and commitment, quality of work, timeliness of work, communication skills, helpfulness, and overall attitude.

For this assignment, you have to design and implement in our HDL a variety of combinational circuits. For full credit, each chip must work properly in all cases and the corresponding HDL file must be clearly organized.

Preparation:

1. Study the notes carefully
2. Download the a2.ZIP file from d2l and extract the files.
3. This folder contains 67 objects (65 files, 2 folders), including 3 files for each chip. The .HDL file is the only one you must modify to implement the chip. **DO THIS RIGHT AWAY:** write both partners' names in the comment block at the top of the Not.HDL file only. The .TST file contains the test script that you should load in the simulator. The .CMP file contains the expected output of the test script and will be automatically compared to your chip's output when you run the script from within the simulator. The other files and directories are needed by the HDL simulator but you need not worry about them.

Requirements:

The following is a list of the HDL files that you must complete in order to implement as many chips. The order of this list is crucial since it is the order in which you have to implement them: for each chip, you may only use gates and chips that have already been implemented. **You may assume that only the Nand gate is built in.** Furthermore, and for full credit, each chip implementation must use the smallest number of gates and chips needed to meet all of the requirements of the chip's API. For example, if one of the components in the implementation of a chip behaves like a 4-way 16-bit-wide multiplexer, you must use a single chip (namely, Mux4Way16) for this component, instead of re-implementing it with basic gates.

Make sure to test each new chip fully. At the bare minimum, each chip must pass the test cases including in the chip's test file. In addition, it is your responsibility to make sure that each chip works in all cases according to its API, even if the provided test file does not cover all possible cases.

1. Not
2. And
3. Or
4. Or16Way
5. Xor
6. Mux (2-to-1 multiplexer)
7. Mux4Way (4-to-1 multiplexer)
8. Mux8Way (8-to-1 multiplexer)
9. Mux16 (2-to-1 16-bit-wide multiplexer)

10. Mux4Way16 (4-to-1 16-bit-wide multiplexer)
11. Mux8Way16 (8-to-1 16-bit-wide multiplexer)
12. Mux16Way16 (16-to-1 16-bit-wide multiplexer)
13. DMux (1-to-2 demultiplexer)
14. DMux4Way (1-to-4 demultiplexer)
15. DMux8Way (1-to-8 demultiplexer)
16. DMux16Way (1-to-16 demultiplexer)
17. FullAdder (full 1-bit adder)
18. Add16 (16-bit adder)
19. Inc16 (16-bit add-1)
20. ALU1bit (1-bit Larc ALU)
21. ALU (16-bit Larc ALU)

Submission:

When you have implemented and fully tested all of the above chips, follow this submission procedure:

1. Make sure both of your names appear in the comments of every file you submit.
2. Create a new folder called a2.
3. Copy all of your .HDL files into this directory, which should now contain EXACTLY 21 files that load and run properly in the simulator. Zip up this directory and call the file a2.zip.
4. Submit a SINGLE copy of your work. Upload your .ZIP file to the a2 dropbox on d2l
5. For full credit, your submission directory must contain exactly 21 correctly named files. Make sure to delete ALL extraneous files before copying this directory.