Computer Architecture Report

Table:

Benchmark Programs	**Branch Stalls (Control Hazard) (Number of Cycles)**	**OF Stage (Number of Cycles) (Data Hazard)**	**Total Cycles (pipelined model)**	**Total Cycles (Without pipeline)**
Descending.out	217	245	615	1385
Evenodd.out	1	9	15	30
Fibonancci.out	33	85	158	390
Prime.out	25	15	59	145
Palindrome.out	15	101	122	245

Ratio Cycles(non-pipeline) / Cycles(pipeline)
2.25
2
2.468
2.457
2.008

Observations:

- The number of Clock cycles is directly proportional to the number of hazards
- Any program without any control or data hazards will be five times faster in a pipelines processor as compared to the non-pipelined processor approximately. The deviation might be due to implementation details and the latency initial instructions.
- The implemented solution for pipeline is stalled three cycles for data hazards to seem closer to the actual hardware implementation where all stages are processed parallelly
- Similarly for control hazards, Branch not taken has been implemented, where we allow the next instruction to be fetched and then check whether the branch is taken and if not the processor is allowed to continue normally.