Computer Architecture Report

Benchmark Programs	Pipelined Processor Total Cycles	Non-pipelined Processor Total Cycles	Total Cycles with IF and MA stalls
Descending.out	615	1385	11807
EvenorOdd.out	15	30	256
Palindrome.out	158	390	2024
Prime.out	59	145	1199
Fibonacci.out	122	245	3258

Observations:

- As in the pipelines and non-pipelined processors, even though the stalls are introduced in the IF and MA changes, a program having more instructions take more number of cycles to produce the output.
- The implementation of IF and MA stalling are 40 cycles each time an instruction or particular data is accessed from memory.
- The solution implemented also takes care of cases of control or data hazards which may arise due to MA stalling.