



## Datasheet

VL805  
4-Port USB 3.0 Host Controller

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## Revision History

Rev #	Status*	Date	Author	Reason for change/description
085		2012/11/13	John	<ol style="list-style-type: none"> <li>1. Add china charging</li> <li>2. Add In house UAS/Turbo driver</li> <li>3. Add Compatible with Windows 8 inbox driver</li> </ol>
086		2012/11/30	John	<ol style="list-style-type: none"> <li>1. Add Linux driver support</li> <li>2. Add Host Controller Capability Registers &amp; Host Controller Runtime Registers</li> <li>3. Add work temperature</li> </ol>
087		2012/12/13	John	<ol style="list-style-type: none"> <li>1. Refine the drawing of mechanical specification.</li> </ol>
088		2013/03/18	John	<ol style="list-style-type: none"> <li>1. Fix some typing errors</li> </ol>
090		2013/05/27	John	<ol style="list-style-type: none"> <li>1. Add triangle mark on VL806 pinout diagram.</li> </ol>
091		2013/09/05	John.	<ol style="list-style-type: none"> <li>1. Add the pin description for VCCA33SSM</li> </ol>
092		2013/11/29	John	<ol style="list-style-type: none"> <li>1. Modify the driver support</li> </ol>
093		2014/9/4	John	<ol style="list-style-type: none"> <li>1. Add Part Number for order information</li> </ol>

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# 1. Product Features

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## VL805

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### 4-Port USB 3.0 Host Controller

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- **Compliant to Universal Serial Bus 3.0 Specification Revision 1.0**
  - Supports all transfer types: Control, Bulk, Stream, Interrupt, Isochronous
- **Compliant to Universal Serial Bus 2.0 Specification**
- **Compliant to eXtensible Host Controller Interface (xHCI) Specification Revision 1.0**
  - **Support USB debugging capability on all super-speed ports**
- **Support Legacy USB Function**
  - Four down-stream ports support SuperSpeed(SS), High-Speed (HS), Full-Speed (FS), and Low-Speed (LS)
- **Support Battery Charging Specification**
  - Compliant to Battery Charging Specification Revision 1.2
  - Apple Charging
  - China Charging
- **Firmware Upgrade**
  - Support firmware upgrade with software tool under Microsoft DOS and Windows XP, Vista, Windows 7, Windows 8.
  - Option to integrate firmware in system BIOS (for on-board design.)
- **Compliant with PCI Express Base Specification 2.0**
  - Supports Express Card Standard
- **In-house USB and PCIe PHY employs advanced CMOS process to reduce power consumption**
  - 3.3 V and 1.05 V power supply
  - USB 3.0 low power states support
- **System Clock**
  - 25 MHz Crystal
- **Software**
  - Initial xHCI Host Controller Driver Support for Windows 8/8.1, Windows 7
    - Bulk Only Transfer (BOT)
    - USB Attached SCSI Protocol (UASP) mode
  - Provide In-House UAS/Turbo driver on Windows 7.
  - Compatible with Windows 8/8.1 in box driver.
  - Compatible with Linux xHCI driver since Linux kernel 3.2.53 and after.
- **Physical**
  - QFN 68 green package (8x8)
- **Applications**
  - Motherboard
  - Notebook/Netbook
  - Express Card
  - Add-in Card
  - Embedded System
  - Docking Station

## 2. VL805 System Overview

VLI VL805 is a single chip USB 3.0 Host controller which enables a PCI Express equipped platform to interface with USB Super-Speed (5 Gbps), High-Speed (480 Mbps), Full-Speed (12 Mbps), and Low-Speed (1.5 Mbps) devices. The root hub consists of two downstream facing ports, allowing simultaneous operation of up to 31 peripheral devices. The VL805 has an x1 PCI Express 2.0 bus interface that is backwards compatible with PCI Express 1.0.

The VL805 complies with the Universal Serial Bus 3.0 Specification and Intel's eXtensible Host Controller Interface (xHCI), and is fully backward compatible with USB 2.0 and 1.1 specifications, ensuring seamless connectivity of legacy USB devices.

With well-planned pinout and advanced process, VL805 based devices enjoy easy layout and low working temperature in a compact footprint. Sideband signal pins are available for showing power enable, over current, and LED status. VL805 is available in QFN 68 green package (8x8 mm) to fit small form-factor designs.

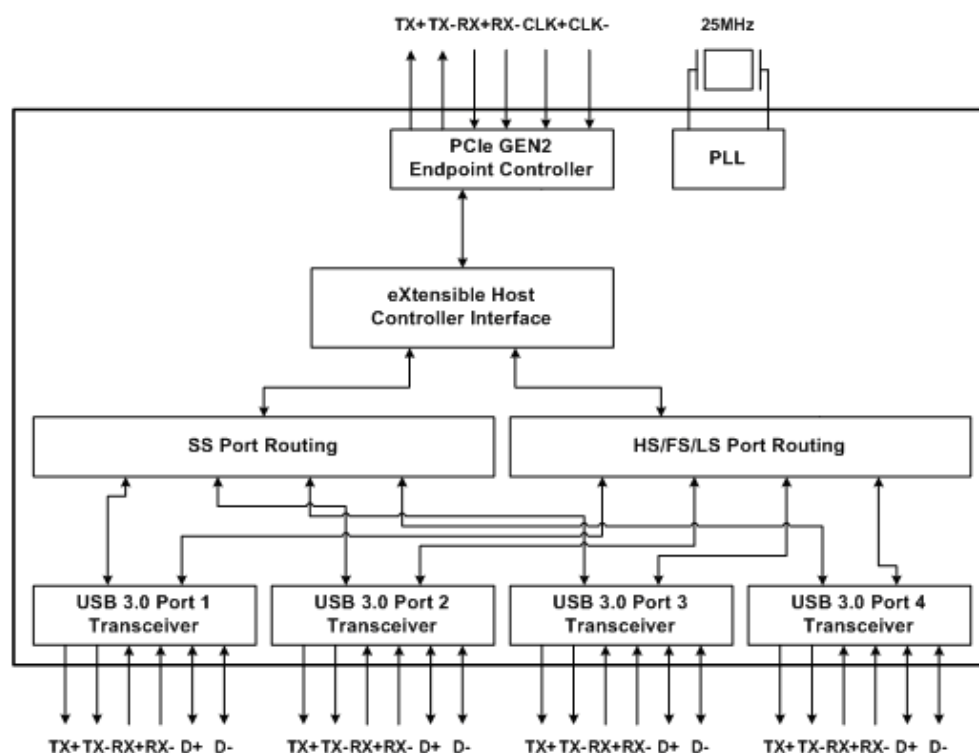


Figure 1 – VL805 Block Diagram

### 3. VL805 Pin Diagram

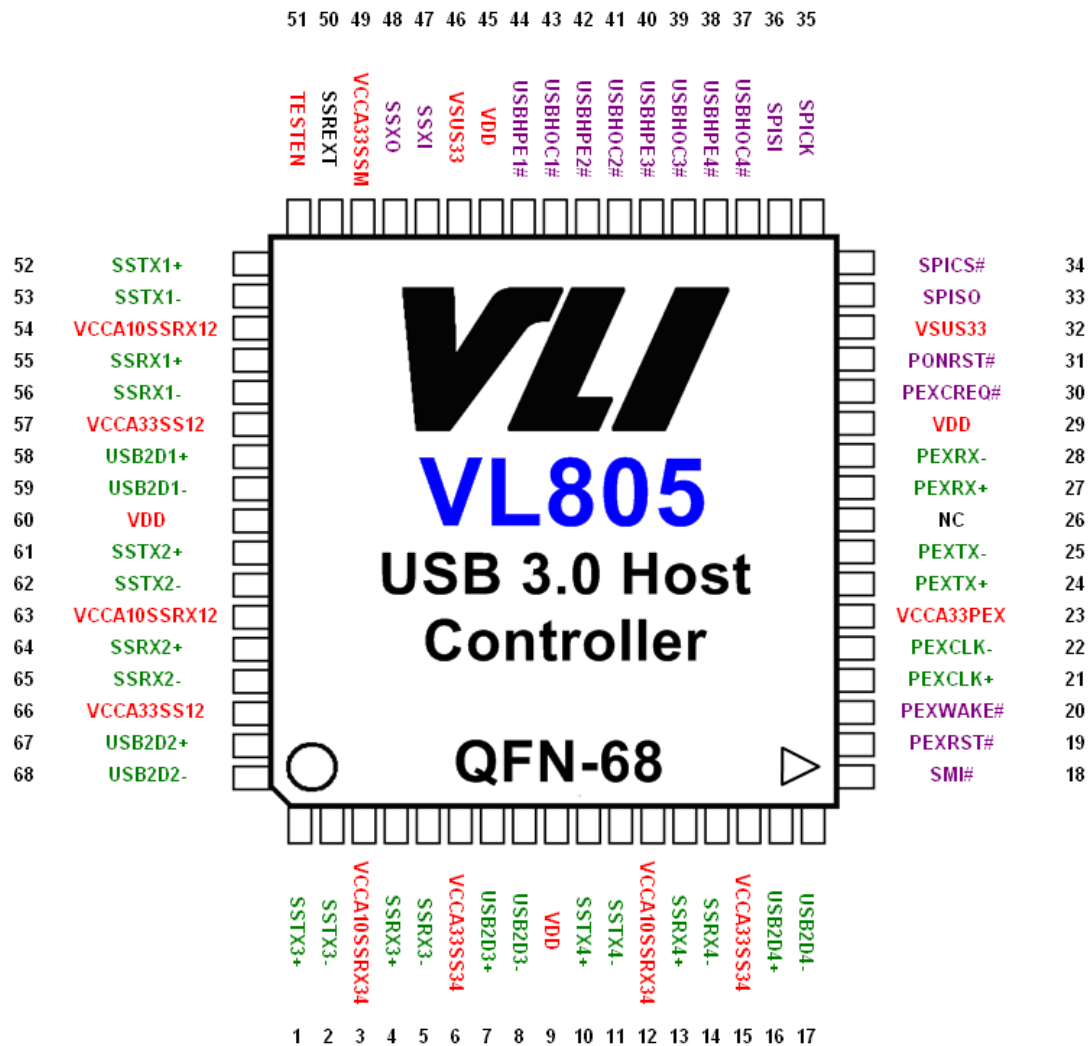


Figure 2 – VL805 Pin Diagram

## 4. PIN Function

### Signal Type Definition

Name	Type	Signal Description
Input	I	A standard input-only signal
Output	O	A standard active driver
Input/Output	I/O	A bi-directional signal
Open drain	OD	Allows multiple devices to share as a wire-OR.
Analog differential	A <sub>DIFF</sub>	Signal pair for the twisted-pair interface
Analog bias or reference signal	A <sub>BIAS</sub>	Must be tie to external resistor, as shown in the system schematic.
Power	PWR	A power pin
Ground	GND	A ground pin

### Power and Ground

Pin Name	Pin #	I/O	Signal Description
VDD	9,29,45,60	PWR	1.05V Core power
VSUS33	32,46	PWR	3.3V suspend power

### PCI Express x1 Interface

Pin Name	Pin #	I/O	Signal Description
VCCA33PEX	23	PWR	PCIE PHY 3.3V
PEXTX0+	24	A <sub>DIFF</sub>	PCIE Differential Transmit Data +
PEXTX0-	25	A <sub>DIFF</sub>	PCIE Differential Transmit Data -
PERX0+	27	A <sub>DIFF</sub>	PCIE Differential Receive Data +
PERX0-	28	A <sub>DIFF</sub>	PCIE Differential Receive Data -
PEXCLK+	21	A <sub>DIFF</sub>	PCIE Differential Reference Clock +/- . The PCIE externally provided differential clock with 100MHz. The SSC (Spread Spectrum Clock) is allowed and recommended within +300ppm and - 2300ppm.
PEXCLK-	22	A <sub>DIFF</sub>	

### Analog Command Block

Pin Name	Pin #	I/O	Signal Description
SSXI	47	I	25M crystal input, it can alternately be driven by external clock source ( <b>1.05V voltage swing main power source</b> ) with SSXO unconnected.
SSXO	48	O	25M crystal output
SSREXT	50	A <sub>BIAS</sub>	Connect to Band Gap reference resistor to add an external 6.04K(1%)resistor between this pin and ground for SuperSpeed USB

### SPI Flash Interface

Pin Name	Pin #	I/O	Signal Description
SPICS#	34	O	SPI Chip Select
SPISCLK	35	O	SPI Serial Clock Input
SPISI	36	O	SPI Serial Data Input
SPISO	33	I	SPI Serial Data Output

USB 3.0 Root Hub Interface

Pin Name	Pin #	I/O	Signal Description
SSTX1+	52	A <sub>DIFF</sub>	USB 3.0 DP1 Port Differential Transmit Data +
SSTX1-	53	A <sub>DIFF</sub>	USB 3.0 DP1 Port Differential Transmit Data -
SSRX1+	55	A <sub>DIFF</sub>	USB 3.0 DP1 Port Differential Receive Data +
SSRX1-	56	A <sub>DIFF</sub>	USB 3.0 DP1 Port Differential Receive Data -
VCCA10SSRX12	54,63	PWR	USB PHY 1.05V
VCCA33SS12	57,66	PWR	USB PHY 3.3V suspend power
SSTX2+	61	A <sub>DIFF</sub>	USB 3.0 DP2 Port Differential Transmit Data +
SSTX2-	62	A <sub>DIFF</sub>	USB 3.0 DP2 Port Differential Transmit Data -
SSRX2+	64	A <sub>DIFF</sub>	USB 3.0 DP2 Port Differential Receive Data +
SSRX2-	65	A <sub>DIFF</sub>	USB 3.0 DP2 Port Differential Receive Data -
SSTX3+	1	A <sub>DIFF</sub>	USB 3.0 DP3 Port Differential Transmit Data +
SSTX3-	2	A <sub>DIFF</sub>	USB 3.0 DP3 Port Differential Transmit Data -
SSRX3+	4	A <sub>DIFF</sub>	USB 3.0 DP3 Port Differential Receive Data +
SSRX3-	5	A <sub>DIFF</sub>	USB 3.0 DP3 Port Differential Receive Data -
VCCA10SSRX34	3,12	PWR	USB PHY 1.05V
VCCA33SS34	6,15	PWR	USB PHY 3.3V suspend power
SSTX4+	10	A <sub>DIFF</sub>	USB 3.0 DP4 Port Differential Transmit Data +
SSTX4-	11	A <sub>DIFF</sub>	USB 3.0 DP4 Port Differential Transmit Data -
SSRX4+	13	A <sub>DIFF</sub>	USB 3.0 DP4 Port Differential Receive Data +
SSRX4-	14	A <sub>DIFF</sub>	USB 3.0 DP4 Port Differential Receive Data -
VCCA33SSM	49	PWR	USB 3.3V suspend power for PLL

USB 2.0 Root Hub Interface

Pin Name	Pin #	I/O	Signal Description
USB2D1+	58	A <sub>DIFF</sub>	USB 2.0 DP1 Bus Data Plus (D+)
USB2D1-	59	A <sub>DIFF</sub>	USB 2.0 DP1 Bus Data Minus (D-)
USB2D2+	67	A <sub>DIFF</sub>	USB 2.0 DP2 Bus Data Plus (D+)
USB2D2-	68	A <sub>DIFF</sub>	USB 2.0 DP2 Bus Data Minus (D-)
USB2D3+	7	A <sub>DIFF</sub>	USB 2.0 DP3 Bus Data Plus (D+)
USB2D3-	8	A <sub>DIFF</sub>	USB 2.0 DP3 Bus Data Minus (D-)
USB2D4+	16	A <sub>DIFF</sub>	USB 2.0 DP4 Bus Data Plus (D+)
USB2D4-	17	A <sub>DIFF</sub>	USB 2.0 DP4 Bus Data Minus (D-)

Test Pin

Pin Name	Pin #	I/O	Signal Description
TESTEN	51	I	Test Mode Enable Do not connect for normal operation. Internal pull down.
Reserved	26		

Side Band signal and Miscellaneous

Pin Name	Pin #	I/O	Signal Description
USBHPE1#	44	OD	DP1 Power Enable
USBHPE2#	42	OD	DP2 Power Enable
USBHPE3#	40	OD	DP3 Power Enable
USBHPE4#	38	OD	DP4 Power Enable
USBHOC1#	43	I	DP1 Over Current Indicator
USBHOC2#	41	I	DP2 Over Current Indicator
USBHOC3#	39	I	DP3 Over Current Indicator
USBHOC4#	37	I	DP4 Over Current Indicator
PONRST#	31	I	Power on reset signal.
PEXCREQ#	30	O	PCI Express "CLKREQ#"Signal. Request to run/stop reference clock.
PEXRST#	19	I	System reset. <b>PCI Express Reset.</b> When PEXRST# is asserted low, the chip performs an internal system Hardware reset.
SMI#	18	OD	System Management Interrupt. To support USB function with BIOS, need to connect this pin to the platform chipset. If not to support USB function with BIOS, just pull up to 3.3V with 10K resistor.
PEXWAKE#	20	OD	Link Reactivation. <b>System Wake up.</b> The Signal is asserted low to reactivate the PCI Express slot's main power rails and reference clocks.



## 5. Electrical Characteristics

### 5.1 Operating Conditions

Symbol	Parameters	Min.	Typ.	Max.	Unit
VCCA10	Analog 1.05V power supply	1.0	1.05	1.1	V
VCCA33	Analog 3.3V power supply	3.0	3.3	3.6	V
VDD	Digital core power supply	1.0	1.05	1.1	V
VSUS33	Aux Power 3.3 power supply	3.0	3.3	3.6	V
PEXRST# V <sub>IH</sub>	PCIE Reset Input High Voltage	2.0	3.3	3.6	V
PEXRST# V <sub>IL</sub>	PCIE Reset Input Low Voltage	-0.5	0	0.8	V
T <sub>A</sub>	Operating ambient temperature	0		70	°C

### 5.2 Absolute Maximum Rating

Symbol	Parameters	Rating	Units
VCCA10	Analog 1.05V power supply	-0.5 to +1.4	V
VCCA33	Analog 3.3V power supply	-0.5 to +4.6	V
VDD	Digital core power supply	-0.5 to +1.4	V
VSUS33	Aux Power 3.3 power supply	-0.5 to +4.6	V

### 5.3 PCI Express Reference Clock

Symbol	Parameters	Min.	Max.	Units
T <sub>RISE</sub>	Rising Edge Rate	0.6	4.0	V/ns
T <sub>FALL</sub>	Falling Edge Rate	0.6	4.0	V/ns
V <sub>IH</sub>	Differential Input High Voltage	+150		mV
V <sub>IL</sub>	Differential Input Low Voltage		-150	mV
V <sub>CROSS</sub>	Absolute crossing point voltage	+250	+550	mV
V <sub>CROSS DELTA</sub>	Variation of VCROSS over all rising clock edgw		+140	mV
V <sub>RB</sub>	Ring-back Voltage Margin	-100	+100	mV
T <sub>STABLE</sub>	Time before V <sub>RB</sub> is allowed	500		ps
T <sub>PERIOD AVG</sub>	Average Clock Period Accuracy	-300	+2800	ppm
T <sub>PERIOD ABS</sub>	Absolute Period(including jitter and Spread Spectrum)	9.847	10.203	ns
V <sub>CCJITTER</sub>	Cycle to Cycle Jitter		150	ps

$V_{MAX}$	Absoulte Max input voltage		+1.15	V
$V_{MIN}$	Absoulte Min input voltage		-0.3	V
$Z_{C-DC}$	Clock source DC impedance	40	60	$\Omega$
	Duty Cycle	40	60	%
	Rising edge rate to falling dege rate matcing		20	%

## 5.4 USB Interface

Symbol	Parameters	Min.	Max.	Units
	Output pin impedance	40.5	49.5	$\Omega$
Input Levels for Low/Full Speed				
$V_{IH}$	High-level input voltage(drive)	2.0		V
$V_{IHZ}$	High-level input voltage(floating)	2.7	3.6	V
$V_{IL}$	Low-level input voltage		0.8	V
$V_{DI}$	Differential input sensitivity	0.2		V
$V_{CM}$	Differential input common mode range	0.8	2.5	V
Output Levels for Low/Full Speed				
$V_{OH}$	High-level output voltage	2.8	3.6	V
$V_{OL}$	Low-level output voltage	0.0	0.3	V
$V_{OSE1}$	SE1	0.8		V
$V_{CRS}$	Output signal crossover point voltage	1.3	2.0	V
Input Levels for High-Speed				
$V_{HSSQ}$	High-speed squelch detection threshold (differential signal)	100	150	mV
$V_{HSDSC}$	High-speed disconnect detection threshold (differential signal)	525	625	mV
$V_{HSCM}$	High-speed data signaling common mode voltage range	-50	+500	mV
Output Levels for High Speed				
$V_{HSOI}$	High-speed idle state	-10	+10	mV
$V_{HSOH}$	High-speed data signaling High	360	440	mV

V <sub>HSOL</sub>	High-speed data signaling Low	-10	+10	mV
V <sub>CHIRPJ</sub>	Chrip J level(differential signal)	700	1100	mV
V <sub>CHIRPK</sub>	Chrip K level(differential signal)	-900	-500	mV

## 6. PCI Configuration Registers

Header Registers (00-3Fh)

**Offset Address: 01-00h**

**Vendor ID Default Value: 1106h**

Bit	Attribute	Default	Description	Mnemonic
15:0	RO	1106h	VIA Technology ID Code	<b>VID</b>

**Offset Address: 03-02h**

**Device ID Default Value: 3483h**

Bit	Attribute	Default	Description	Mnemonic
15:0	RO	3483h	Device ID Code	<b>DEVID</b>

**Offset Address: 05-04h (D18F0)**

**PCI Command Default Value: 0000h**

Bit	Attribute	Default	Description	Mnemonic
15:11	RO	0	Reserved	<b>RESERVED</b>
10	RW	0	Interrupt Disable	<b>INTRDIS</b>
9	RO	0	Reserved	<b>RESERVED</b>
8	RW	0	SERR Enable	<b>SERREN</b>
7	RO	0	Reserved	<b>RESERVED</b>
6	RW	0	Parity Error Response	<b>RPTYERR</b>
5	RO	0	Reserved	<b>RESERVED</b>
4	RO	0	Memory Write and Invalidate	<b>MWRMEN</b>
3	RO	0	Reserved <b>Special cycle monitoring. Fixed at 0b (Not supported).</b>	<b>RESERVED</b>
2	RW	0	Bus Master	<b>BMASTREN</b>
1	RW	0	Memory Space	<b>MMSPACE</b>
0	RW	0	I/O Space	<b>IOSPACE</b>



**PCI Status**      **Default Value: 0010h**

**Offset Address: 08h**

<b>Revision ID</b>	<b>Default Value: 01h</b>
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**Offset Address: 0B-09h (D18F0)**

<b>Class Code</b>	<b>Default Value: 0C0330h</b>
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### Offset Address: 0Ch

**Cache Line Size**      **Default Value: 00h**

**Offset Address: 0Dh**

**Latency Timer**      **Default Value: 00h**

**Offset Address: 0Eh**

**Header Type**      **Default Value: 00h**

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**Offset Address: 0Fh**

**Built In Self Test (BIST) Default Value: 00h**

Bit	Attribute	Default	Description	Mnemonic
7:0	RO	0	BIST Fixed at 00h	BIST

**Offset Address: 13-10h**

**XHCI Memory Mapped I/O Low Base Address Default Value: 00000004h**

Bit	Attribute	Default	Description	Mnemonic
31:1 2	RW	0	XHCI Memory Mapped I/O Registers Low Base Address Memory Address for the base of the USB 3.0 XHCI MMIO Register..	BASEADDR0_LO
11:3	RO	0	Reserved	RESERVED
2:1	RO	10b	Base Address Type Reads 10b for 64-bit addressing.	BARTYPE0
0	RO	0	Reserved	RESERVED

**Offset Address: 17-14h (D18F0)**

**XHCI Memory Mapped I/O High Base Address Default Value: 00000000h**

Bit	Attribute	Default	Description	Mnemonic
31:0	RW	0	XHCI Memory Mapped I/O Registers High Base Address Memory Address for the base of the USB 3.0 XHCI MMIO Register..	BASEADDR0_HI

**Offset Address: 18-2Bh (D18F0) – Reserved**

**Offset Address: 2D-2Ch (D18F0)**

**Subsystem Vendor ID Default Value: 1106h**

Bit	Attribute	Default	Description	Mnemonic
15:0	RW	1106h	Subsystem Vendor ID	SYSVID

**Offset Address: 2F-2Eh**

**Subsystem ID Default Value: 3483h**

Bit	Attribute	Default	Description	Mnemonic
15:0	RW	3483h	Subsystem ID	SUBSID

**Offset Address: 30-33h Reserved**

**Offset Address: 34h**

**Capability Pointer Default Value: 80h**

Bit	Attribute	Default	Description	Mnemonic
7:0	RO	80h	Capability Pointer This register contains the offset address from the start of the configuration space. Fixed at 80h.	CAPPTR

**Offset Address: 35-3Bh Reserved**

**Offset Address: 3Ch**

**Interrupt Line Default Value: 00h**

Bit	Attribute	Default	Description	Mnemonic
7:0	RW	0	USB Interrupt Routing 'h00: Disable                      'h01: IRQ1 'h02: Reserved                   'h03: IRQ3 'h04: IRQ4                        'h05: IRQ5 'h06: IRQ6                        'h07: IRQ7 'h08: IRQ8                        'h09: IRQ9 'h0a: IRQ10                       'h0b: IRQ11 'h0c: IRQ12                       'h0d: IRQ13 'h0e: IRQ14                       Other: Disable	<b>INTLN</b>

**Offset Address: 3Dh**

**Interrupt Pin Default Value: 01h**

Bit	Attribute	Default	Description	Mnemonic
7:0	RO	01h	Interrupt Pin Fixed at 01h (INTA#).	<b>INTPIN</b>

**Offset Address: 3E-3Fh Reserved**

## XHCI-Specific Configuration Registers (40-FFh)

**Offset Address: 40-43h Reserved**

**Offset Address: 48-4Bh**

**XHCI CRCR Mirror Low Register Default Value: 00000000h**

Bit	Attribute	Default	Description	Mnemonic
31:0	RO	0	XHCI CRCR Mirror Low Register	<b>CRCR_MIRROR_LO</b>

**Offset Address: 4C-4Fh Reserved**

**Offset Address: 50-53h**

**XHCI MCU Firmware Version Default Value: 00000000h**

Bit	Attribute	Default	Description	Mnemonic
31:0	RO	0	XHCI MCU Firmware Version	<b>FW_VERSION</b>

**Offset Address: 5C-5Dh**

**Subsystem Vendor ID For SW Default Value: 1106h**

Bit	Attribute	Default	Description	Mnemonic
15:0	RW	1106h	Subsystem Vendor ID (SW can update)	<b>SYSVID_SW</b>

**Offset Address: 5E-5Fh**

**Subsystem ID For SW Default Value: 3483h**

Bit	Attribute	Default	Description	Mnemonic
15:0	RW	3483h	Subsystem ID (SW can update)	<b>SUBSID_SW</b>

**Offset Address: 60h**

**Serial Bus Release Number (SBRN) Default Value: 30h**

Bit	Attribute	Default	Description	Mnemonic
7:0	RO	30h	Serial Bus Specification Release Number. <b>All other combinations are reserved.</b> <b>Bits[7:0] Release Number</b> <b>30h Release 3.0</b>	<b>SBRN</b>

**Offset Address: 61h**

**Frame Length Adjustment (FLADJ) Default Value: 20h**

Bit	Attribute	Default	Description	Mnemonic
7:6	ROS	0	Reserved	<b>RESERVED</b>
5:0	RWS	20h	Frame Length Timing Value. <b>Each decimal value change to this register corresponds to 16 high-speed bit times. The SOF cycle time (number of SOF counter clock periods to generate a SOF microframe length) is equal to 59488 + value in this field. The default value is decimal 32 (20h), which gives a SOF cycle time of 60000.</b> <b>Frame Length</b> <b>(# HS bit times) FLADJ Value</b> <b>(decimal) (decimal)</b> <b>59488 0 (00h)</b> <b>59504 1 (01h)</b> <b>59520 2 (02h)</b> <b>...</b> <b>59984 31 (1Fh)</b> <b>600032 (20h)</b> <b>...</b> <b>60480 62 (3Eh)</b> <b>60496 63 (3Fh)</b>	<b>FLADJ</b>

**Offset Address: 78-7Bh**

**XHCI Optional Bits Configuration Address Default Value: 00000000h**

Bit	Attribute	Default	Description	Mnemonic
31:2 0	RO	0	Reserved	<b>RESERVED</b>
19:0	RW	0	XHCI Option Bits Configuration Address.	<b>OPTCFGADDR</b>

**Offset Address: 7C-7Fh**

**XHCI Optional Bits Configuration Data Default Value: 00000000h**

Bit	Attribute	Default	Description	Mnemonic
31:0	RW	0	XHCI Option Bits Configuration Data.	<b>OPTCFGDATA</b>

**Offset Address: 80h**

**Power Management Capability ID Default Value: 01h**

Bit	Attribute	Default	Description	Mnemonic
7:0	ROS	01h	Power Management Capability ID	<b>PMCAPID</b>

**Offset Address: 81h**

**Next Item Pointer 1 Default Value:90h**

Bit	Attribute	Default	Description	Mnemonic
7:0	ROS	90h	Next Item Pointer 1	<b>PMNXTPTR</b>

**Offset Address: 82-83h**

**Power Management Capability Default Value:4803h**

Bit	Attribute	Default	Description	Mnemonic
15:0	ROS	4803h	Power Management Capability	<b>PMCAP</b>

**Offset Address: 84-85h**

**Power Management Capability Control / Status Default Value:0000h**

Bit	Attribute	Default	Description	Mnemonic
15	RWS	0	PME Status <b>0: Not active 1: Active</b>	<b>PMESTATUS</b>
14:9	ROS	0	Reserved	<b>RESERVED</b>
8	RWS	0	PME Enable <b>0: Disable 1: Enable</b>	<b>PMEEN</b>
7:2	ROS	0	Reserved	<b>RESERVED</b>
1:0	RWS	00b	Power State <b>00: D0 01: D1 10: D2 11: D3 Hot</b>	<b>PMSTATE</b>

**Offset Address: 86-8Fh**

**Offset Address: 90h**

**MSI Capability ID Default Value:05h**

Bit	Attribute	Default	Description	Mnemonic
7:0	RO	05h	MSI Capability ID	<b>MSIID</b>

**Offset Address: 91h**

**Next Item Pointer 2 Default Value:C4h**

Bit	Attribute	Default	Description	Mnemonic
7:0	RO	C4h	Next Item Pointer 2	<b>MSINXTPTR</b>



**Offset Address: 92-93h**

**MSI Message Control Default Value: 0084h**

Bit	Attribute	Default	Description	Mnemonic
15:9	RO	0	Reserved	<b>RESERVED</b>
8	RO	0	Per-vector Masking Capable <b>1: Function supports MSI per-vector masking</b> <b>0: Function does NOT support MSI per-vector masking</b>	<b>MSIMSKCAP</b>
7	RO	1b	64 Bit Address Capable <b>1: Function is capable of sending a 64-bit message address.</b> <b>0: Function is NOT capable of sending a 64-bit message address.</b>	<b>MSIADDR64CAP</b>
6:4	RW	0	Multiple Message Enable <b>Software writes to this field to indicate the number of allocated vectors. The number of allocated vectors is aligned to a power of two.</b> <b>000: 1 vector allocated</b> <b>001: 2 vectors allocated</b> <b>010: 4 vectors allocated</b> <b>011: 8 vectors allocated</b> <b>100: 16 vectors allocated</b> <b>101: 32 vectors allocated</b> <b>110: Reserved</b> <b>110: Reserved</b>	<b>MSIMLTEN</b>
3:1	RO	010b	Multiple Message Capable <b>System software reads this field to determine the number of requested vectors.</b> <b>000: 1 vector allocated</b> <b>001: 2 vectors allocated</b> <b>010: 4 vectors allocated</b> <b>011: 8 vectors allocated</b> <b>100: 16 vectors allocated</b> <b>101: 32 vectors allocated</b> <b>110: Reserved</b> <b>110: Reserved</b>	<b>MSIMULCAP</b>
0	RW	0	MSI Enable <b>If 1 and the MSI-X Enable in MSI-X Message Control register is 0, the function is permitted to use MSI to request service and is prohibited from using its INTx pin.</b> <b>If 0, the function is prohibited from using MSI to request service.</b>	<b>MSIEN</b>

**Offset Address: 94-97h**

**MSI Message Address Low Default Value: 00000000h**

Bit	Attribute	Default	Description	Mnemonic
31:2	RW	0	Message Address (Low 32 Bits). <b>System specified message address.</b>	<b>MSIADDRLO</b>
1:0	RO	0	Reserved	<b>RESERVED</b>

**Offset Address: 98-9Bh**

**MSI Message Address High Default Value: 00000000h**

Bit	Attribute	Default	Description	Mnemonic
31:0	RW	0	Message Address (High 32 Bits). <b>System specified message address.</b>	<b>MSIADDRHI</b>

**Offset Address: 9C-9Dh**

**MSI Data Default Value: 0000h**

Bit	Attribute	Default	Description	Mnemonic
15:0	RW	0	Message Data. <b>System specified message data.</b>	<b>MSIDATA</b>

Offset Address: 9E-FFh Reserved

## 7. Host Controller Capability Registers

### Host Controller Capability Registers(Base+00h-Base+1Bh)

Note: The beginning of the host controller's MMIO address space is referred to as Base Address Register at Rx10h of PCI Configuration Space throughout this document.

**Offset Address: 00h (USB3.0-MMIO)**

**Capability Registers Length (CAPLENGTH) Default Value: 20h**

Bit	Attribute	Default	Description	Mnemonic
7:0	RO	20h	Capability Registers Length This register is used as an offset to add to register base to find the beginning of the Operational Register Space.	CAPLENGTH

**Offset Address: 01h (USB3.0-MMIO) – Reserved**

**Offset Address: 03-02h (USB3.0—MMIO)**

**Host Controller Interface Version Number (HCIVERSION) Default Value: 0100h**

Bit	Attribute	Default	Description	Mnemonic
15:0	RO	0100h	Host Controller Interface Version Number This is a two-byte register containing a BCD encoding of the xHCI specification revision number supported by this host controller. The most significant byte of this register represents a major revision and the least significant byte is the minor revision. e.g. 0100h corresponds to xHCI version 1.0.	HCIVERSION

**Offset Address: 07-04h (USB3.0—MMIO)**

**Structural Parameters 1 (HCSPARAMS1) Default Value: 05000420h**

Bit	Attribute	Default	Description	Mnemonic
31:24	RO	05h	Number of Ports (MaxPorts). This field specifies the number of physical downstream ports implemented on this host controller. The value of this field determines how many port registers are addressable in the Operational Register Space (see Table 26). Valid values are in the range of 1h to FFh.	MAXPORTS
23:19	RO	0	Reserved	RESERVED
18:8	RO	04h	Number of Interrupters (MaxIntrs). This field specifies the number of Interrupters implemented on this host controller. Each Interrupter is allocated to a vector of MSI-X and controls its generation and moderation. The value of this field determines how many Interrupter Register Sets are addressable in the Runtime Register Space (see section 5.5). Valid values are in the range of 1h to 400h. A '0' in this field is undefined.	MAXINTRS
7:0	RO	20h	Number of Device Slots (MaxSlots). This field specifies the maximum number of Device Context Structures and Doorbell Array entries this host controller can support. Valid values are in the range of 1 to 255. The value of '0' is reserved.	MAXSLOTS

Offset Address: 0B-08h (USB3.0—MMIO)

Structural Parameters 2 (HCSPARAMS2)

Default Value: FC000031h

Bit	Attribute	Default	Description	Mnemonic
31:27	RO	1Fh	Max Scratchpad Buffers (Max Scratchpad Bufs). Valid values are 0-31. This field indicates the number of Scratchpad Buffers system software shall reserve for the xHC. See section 4.20 for more information.	MAXSCRBUF
26	RO	1b	Scratchpad Restore (SPR). If <i>Max Scratchpad Buffers</i> is > '0' then this flag indicates whether the xHC uses the Scratchpad Buffers for saving state when executing Save and Restore State operations. If <i>Max Scratchpad Buffers</i> is = '0' then this flag shall be '0'. See section 4.23.2 for more information. A value of '1' indicates that the xHC requires the integrity of the Scratchpad Buffer space to be maintained across power events. A value of '0' indicates that the Scratchpad Buffer space may be freed and reallocated between power events.	SPR
25:21	RO	0	Max Scratchpad Buffers (Max Scratchpad Bufs Hi)	MAXSCRBUF_HI
20:8	RO	0	Reserved	RESERVED
7:4	RO	3h	Event Ring Segment Table Max (ERST Max). Valid values are 0 – 15. This field determines the maximum value supported the <i>Event Ring Segment Table Base Size</i> registers (5.5.2.3.1), where: The maximum number of Event Ring Segment Table entries = 2 ERST Max. e.g. if the ERST Max = 7, then the xHC <i>Event Ring Segment Table(s)</i> supports up to 128 entries, 15 then 32K entries, etc.	MAXERST
3:0	RO	1h	Isochronous Scheduling Threshold (IST). The value in this field indicates to system software the minimum distance (in time) that it must stay ahead of the host controller while adding TRBs, in order to have the host controller process them at the correct time. The value shall be specified in terms of number of frames/microframes. If bit [3] of IST is set to '0', software can add a TRB no later than IST[2:0] Microframes before that TRB is scheduled to be executed. If bit [3] of IST is set to '1', software can add a TRB no later than IST[2:0] Frames before that TRB is scheduled to be executed. Refer to Section 4.14.2 for details on how software uses this information for scheduling isochronous transfers.	IST

**Offset Address: 0F-0Ch (USB3.0—MMIO)**

**Structural Parameters 3 (HCSPARAMS3)**

**Default Value: 00E70004h**

Bit	Attribute	Default	Description	Mnemonic
31:16	RO	00E7h	U2 Device Exit Latency. Worst case latency to transition from U2 to U0. Applies to all root hub ports. The following are permissible values: Value Description 0000h zero 0001h less than 1 $\mu$ s. 0002h less than 2 $\mu$ s. ... 07FFh less than 2047 $\mu$ s. 0800-FFFFh reserved	U2DEVEXTLT
15:8	RO	0	Reserved	RESERVED
7:0	RO	04h	U1 Device Exit Latency. Worst case latency to transition a root hub port link state from U1 to U0. Applies to all root hub ports. The following are permissible values: Value Description 00h zero 01h less than 1 $\mu$ s 02h less than 2 $\mu$ s. ... 0Ah less than 10 $\mu$ s. 0B-FFh reserved	U1DEVEXTLT

**Offset Address: 13-10h (USB3.0—MMIO)**

**Capability Parameters (HCCPARAMS)**

**Default Value: 002841EBh**

Bit	Attribute	Default	Description	Mnemonic
31:16	RO	0028h	xHCI Extended Capabilities Pointer (xECP). This field indicates the existence of a capabilities list. The value of this field indicates a relative offset, in 32-bit words, from Base to the beginning of the first extended capability. For example, using the offset of Base is 1000h and the xECP value of 0068h, we can calculate the following effective address of the first extended capability: $1000h + (0068h \ll 2) \rightarrow 1000h + 01A0h \rightarrow 11A0h$	XECP
15:12	RO	4h	Maximum Primary Stream Array Size (MaxPSASize). This field identifies the maximum size Primary Stream Array that the Xhc supports. The Primary Stream Array size = $2MaxPSASize + 1$ . Valid MaxPSASize values are 1 to 15.	MAXPSASIZE
11:9	RO	0	Reserved	RESERVED
8	RO	1b	Parse All Event Data (PAE)	PAE
7	RO	1b	No Secondary SID Support (NSS). This flag indicates whether the host controller implementation supports Secondary Stream IDs. A '1' in this bit indicates that Secondary Stream ID decoding is not supported. A '0' in this bit indicates that Secondary Stream ID decoding is supported. (refer to Sections 4.12.2 and 6.2.3).	NSS

6	RO	1b	<p>Latency Tolerance Messaging Capability (LTC).</p> <p>This field indicates whether the host controller implementation supports Latency Tolerance Messaging (LTM). A '1' in this bit indicates that LTM is supported. A zero in this bit indicates that LTM is not supported. See section 4.13.1 for more information on LTM.</p>	LTC
5	RO	1b	<p>Light HC Reset Capability (LHRC).</p> <p>This field indicates whether the host controller implementation supports a Light Host Controller Reset. A '1' in this bit indicates that Light Host Controller Reset is supported. A '0' in this bit indicates that Light Host Controller Reset is not supported. The value of this field affects the functionality of the Light Host Controller Reset field in the USBCMD register (see Section 5.4.1).</p>	LHRC
4	RO	0	<p>Port Indicators (PIND).</p> <p>This bit indicates whether the xHC root hub ports support port indicator control. When this bit is a '1', the port status and control registers include a read/writeable field for controlling the state of the port indicator. See Section 5.4.8 for definition of the <i>Port Indicator Control</i> field.</p>	PIND
3	RO	1b	<p>Port Power Control (PPC).</p> <p>This field indicates whether the host controller implementation includes port power control. A '1' in this bit indicates the ports have port power switches. A '0' in this bit indicates the port do not have port power switches. The value of this field affects the functionality of the <i>Port Power</i> field in each port status and control register (see Section 5.4.8).</p>	PPC
2	RO	0	<p>Context Size (CSZ).</p> <p>If this bit is set to '1', then the xHC uses 64 byte Context data structures.</p> <p>If this bit is set to '0', then the xHC uses 32 byte Context data structures.</p> <p>Note: This flag does <i>not</i> apply to Stream Contexts.</p>	CSZ
1	RO	1b	<p>BW Negotiation Capability (BNC).</p> <p>This field identifies whether the xHC has implemented the Bandwidth Negotiation. Values for this field have the following interpretation:</p> <p>0b BW Negotiation not implemented</p> <p>1b BW Negotiation implemented</p> <p>See section 4.16 for more information on Bandwidth Negotiation.</p>	BNC
0	RO	1b	<p>64-bit Addressing Capability (AC64).</p> <p>This field documents the addressing range capability of this implementation. The value of this field determines whether the xHC has implemented the high order 32 bits of 64 bit register and data structure pointer fields. Values for this field have the following interpretation:</p> <p>0b 32-bit address memory pointers implemented</p> <p>1b 64-bit address memory pointers implemented</p> <p>If 32-bit address memory pointers are implemented, the xHC shall ignore the high order 32 bits of 64 bit data structure pointer fields, and system software shall ignore the high order 32 bits of 64 bit xHC registers.</p>	AC64

**Offset Address: 17-14h (USB3.0—MMIO)**

**Doorbell Offset (DBOFF)      Default Value:00000100h**

Bit	Attribute	Default	Description	Mnemonic
-----	-----------	---------	-------------	----------

31:2	RO	40h	Doorbell Array Offset. This field defines the Dword offset of the Doorbell Array base address from the Base (i.e. the base address of the xHCI Capability register address space).	<b>DBOFF</b>
1:0	RO	0	Reserved	<b>RESERVED</b>

**Offset Address: 1B-18h (USB3.0—MMIO)**

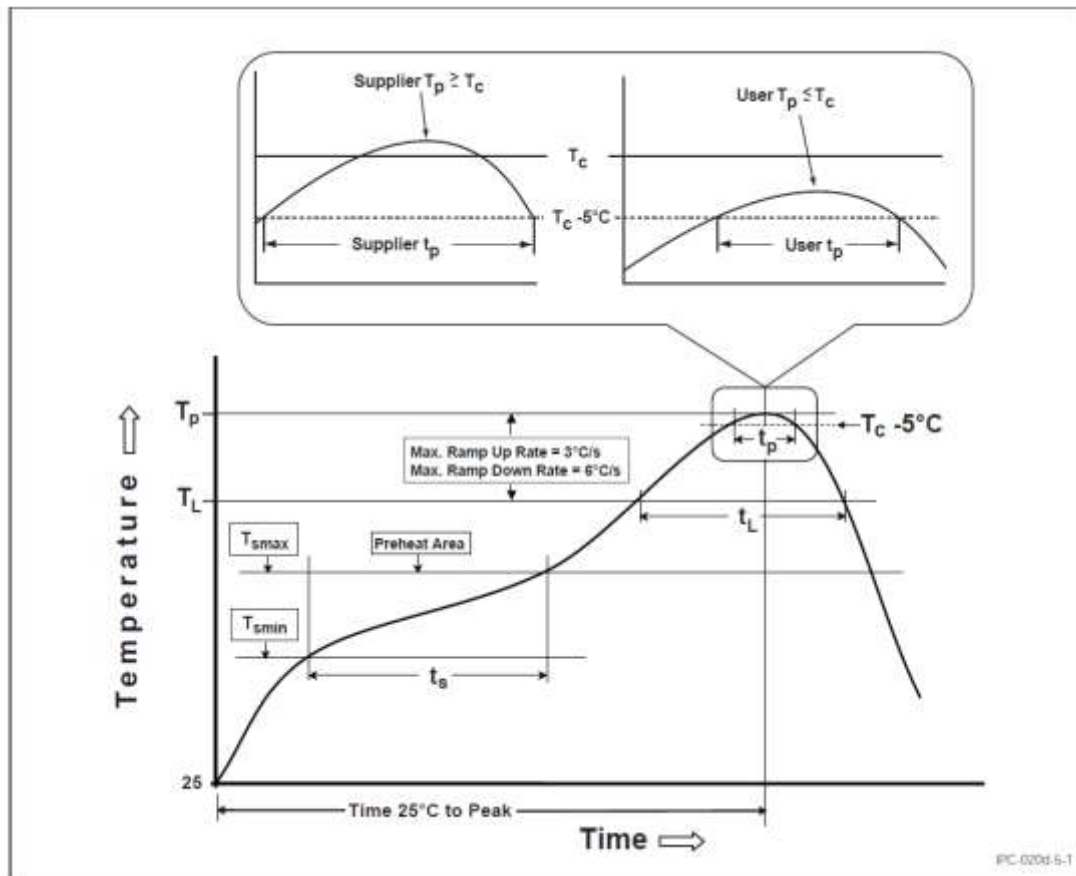
**Runtime Register Space Offset (RTSOFF)**

**Default Value: 00000200h**

Bit	Attribute	Default	Description	Mnemonic
31:5	RO	10h	Runtime Register Space Offset. This field defines the 32-byte offset of the xHCI Runtime Registers from the Base. i.e. Runtime Register Base Address = Base + Runtime Register Set Offset.	<b>RTSOFF</b>
4:0	RO	0	Reserved	<b>RESERVED</b>

**Offset Address: 1C-1Fh (USB3.0-MMIO) – Reserved**

## 8. General Reflow Profile Guidelines



Profile Feature	Sn-Pb Eutectic Assembly	Pb-Free Assembly
<b>Preheat/Soak</b>		
Temperature Min ( $T_{smin}$ )	100 °C	150 °C
Temperature Max ( $T_{smax}$ )	150 °C	200 °C
Time ( $t_s$ ) from ( $T_{smin}$ to $T_{smax}$ )	60-120 seconds	60-120 seconds
Ramp-up rate ( $T_L$ to $T_p$ )	3 °C/second max.	3 °C/second max.
Liquidous temperature ( $T_L$ )	183 °C	217 °C
Time ( $t_L$ ) maintained above $T_L$	60-150 seconds	60-150 seconds
Peak package body temperature ( $T_p$ )	For users $T_p$ must not exceed the Classification temp in Table 4-1. For suppliers $T_p$ must equal or exceed the Classification temp in Table 4-1.	For users $T_p$ must not exceed the Classification temp in Table 4-2. For suppliers $T_p$ must equal or exceed the Classification temp in Table 4-2.
Time ( $t_p$ )* within 5 °C of the specified classification temperature ( $T_c$ ), see Figure 5-1.	20* seconds	30* seconds
Ramp-down rate ( $T_p$ to $T_L$ )	6 °C/second max.	6 °C/second max.
Time 25 °C to peak temperature	6 minutes max.	8 minutes max.

\* Tolerance for peak profile temperature ( $T_p$ ) is defined as a supplier minimum and a user maximum.

**Note 1:** All temperatures refer to the center of the package, measured on the package body surface that is facing up during assembly reflow (e.g., live-bug). If parts are reflowed in other than the normal live-bug assembly reflow orientation (i.e., dead-bug),  $T_p$  shall be within  $\pm 2$  °C of the live-bug  $T_p$  and still meet the  $T_c$  requirements, otherwise, the profile shall be adjusted to achieve the latter. To accurately measure actual peak package body temperatures refer to JEP140 for recommended thermocouple use.

**Note 2:** Reflow profiles in this document are for classification/preconditioning and are not meant to specify board assembly profiles. Actual board assembly profiles should be developed based on specific process needs and board designs and should not exceed the parameters in Table 5-2.

For example, if  $T_c$  is 260 °C and time  $t_p$  is 30 seconds, this means the following for the supplier and the user:

For a supplier: The peak temperature must be at least 260 °C. The time above 255 °C must be at least 30 seconds.

For a user: The peak temperature must not exceed 260 °C. The time above 255 °C must not exceed 30 seconds.

**Note 3:** All components in the test load shall meet the classification profile requirements.

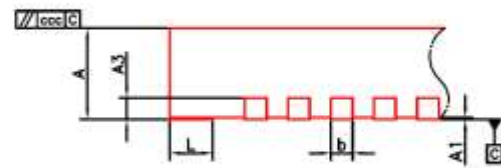
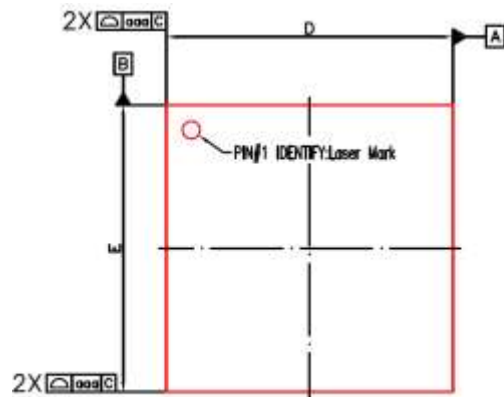
**Note 4:** SMD packages classified to a given moisture sensitivity level by using Procedures or Criteria defined within any previous version of J-STD-020, JEDEC22-A112 (rescinded), IPC-8M-786 (rescinded) do not need to be reclassified to the current revision unless a change in classification level or a higher peak classification temperature is desired.



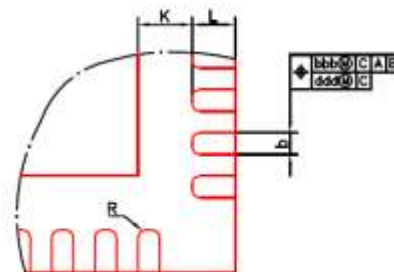
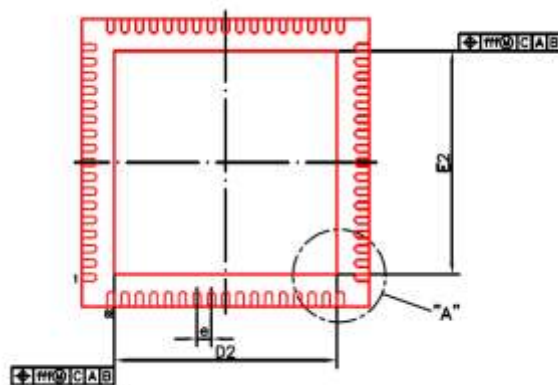
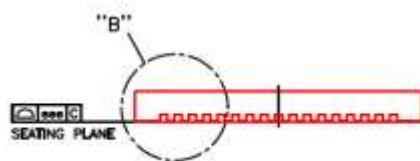
## 9. Package Mechanical Specifications

### Pb-free Maximum Temperature for IR Reflow

Parameter	Value	Unit
Maximum Temperature $T_p$	250	°C
Max Time within 5°C of $T_p$	30	seconds



DETAIL : "B"



DETAIL : "A"



Symbol	Dimension in mm			Dimension in inch		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.80	0.85	0.90	0.031	0.033	0.035
A1	0.00	0.02	0.05	0.000	0.001	0.002
A3	0.20 REF			0.008 REF		
b	0.15	0.20	0.25	0.006	0.008	0.010
D/E	7.90	8.00	8.10	0.311	0.315	0.319
D2	6.05	6.20	6.35	0.238	0.244	0.250
E2	6.05	6.20	6.35	0.238	0.244	0.250
e	0.40 BSC			0.016 BSC		
L	0.30	0.40	0.50	0.012	0.016	0.020
R	0.075	----	----	0.003	----	----
K	0.20	----	----	0.008	----	----
aaa	0.10			0.004		
bbb	0.07			0.003		
ccc	0.10			0.004		
ddd	0.05			0.002		
eee	0.08			0.003		
fff	0.10			0.004		

NOTE:

1. CONTROLLING DIMENSION : MILLIMETER
2. REFERENCE DOCUMENT: JEDEC MO-220.

VIA

Figure 3 – Mechanical Specification – QFN68 8x8 mm Package

## 10. Package Top Side Marking

VX: First character stand for Company brand name and second character stand for product attribute

NNN: Product Name Series

PC: Package Code

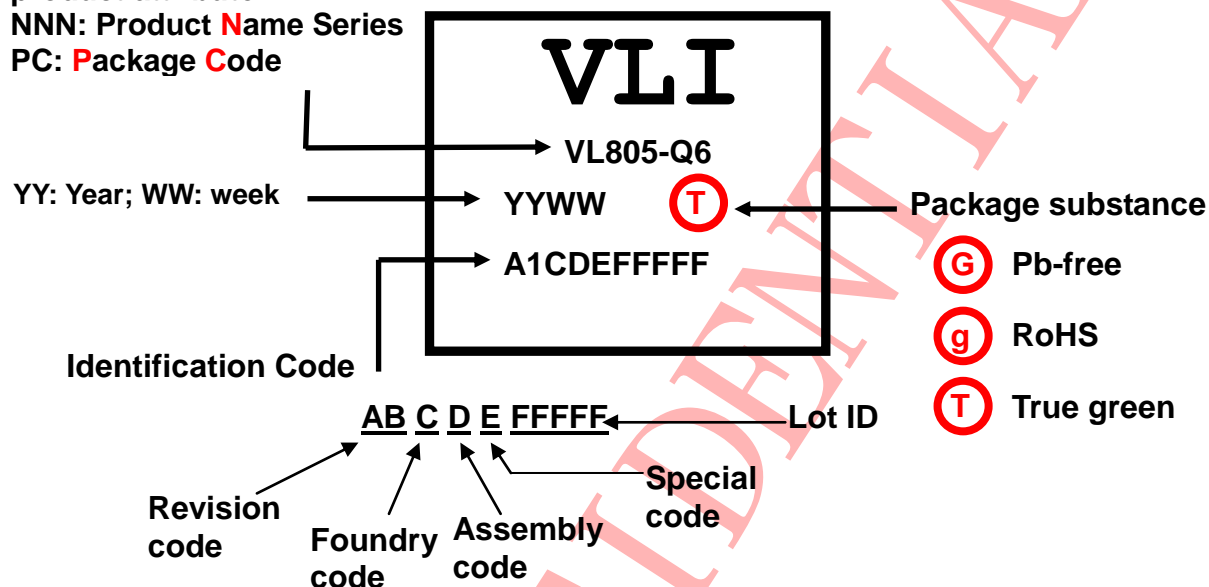


Figure 4 – Package Top Side Marking

## 11. Order Information

Part Number	Package Type
VL805 – Q6 T	QFN68 8x8 mm

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