Durham University

AOM Driver User Guide: AD9910 DDS Version 1

L. A. McArd

October 1, 2020

1 Introduction

This document provides a user guide for the AD9910 direct digital synthesizer (DDS) based AOM driver. The AD9910 DDS is designed to produce sinusoidal waveform at frequencies up to 400 MHz. Moreover, this DDS allows the user control over frequency, phase, and amplitude. The DDS is clocked at 1 GHz and has a tuning resolution is 0.23 Hz. The DDS also enables fast phase and amplitude switching capability (switching times of 100 ns have been observed).

The AD9910 is programmed using internal control registers which are loaded using a serial I/O port (SPI). This is programmed by a PSoC micro-controller which provides the interface between the computer terminal and the DDS. When using the PSoC controller three modes of operation are available: single tone profile mode, RAM playback mode and linear ramp generation mode. Details of these can be found in section 2. For more advanced modulation functions, the DDS module can be upgraded to be programmed using a high speed parallel data port controlled by a FPGA. This mode is described in section 3.

A graphic user interface (GUI) has been designed to simplify the programming for the DDS. A description of this can be found in section 4. Finally, a series of user tests can be found in section 5. These are designed to guide the user through the setup process of the operating modes described above.

1.1 Summary of DDS features

- 1 GHz internal clock speed (up to 400 MHz analog output)
- 14-bit DAC
- 0.23 Hz frequency resolution
- Phase noise 125 dBc/Hz @ 1 kHz offset (400 MHz carrier)
- Arbitrary frequency, phase, and amplitude sweep capability
- 8 frequency and phase offset profiles. Profiles switching delay of 100 ns from a TTL trigger.
- Integrated 1024 word, 32-bit RAM
- Parallel datapath interface for more complex modulations
- Multichip synchronization
- Manual on/off amplitude switch

1.2 Specification of the AOM driver

This DDS unit is intended to be a substitute for the standard voltage-controlled oscillator (VCO) AOM driver.

- Maximum output frequency of 400 MHz
- Stability of below 1 kHz drift per day (AD9910 and internal clock are a suitable combination)
- Each rack should be able to drive at least 5 AOMs (same as the current package)
- Output of the unit should be able to drive up to 1 W
  - Typically we use a minicircuits ZHL-3A amplifier. With this gain (24 dB), the output of the DDS would need to be 6 dBm
  - Some AOMs require inputs of up to 2 W, however, a 33 dB amplifier would be used instead
- Frequency control
  - Single-tone, fixed frequency
  - Programmable steps in frequency
  - Ramps- 5 to 50 MHz from the AOM centre frequency in something like 1 to 100ms.
- Amplitude control
  - Step control (on/off on the order of 10 us)
  - Simple ramps
- 8 pre-sets for amplitude and frequency.
- Interface
  - DEXTER triggers (3.3 V TTLs) - response must be repeatable
  - The programmable over USB,

Additional amplitude correction to account for the output filter is intended to be a later update.

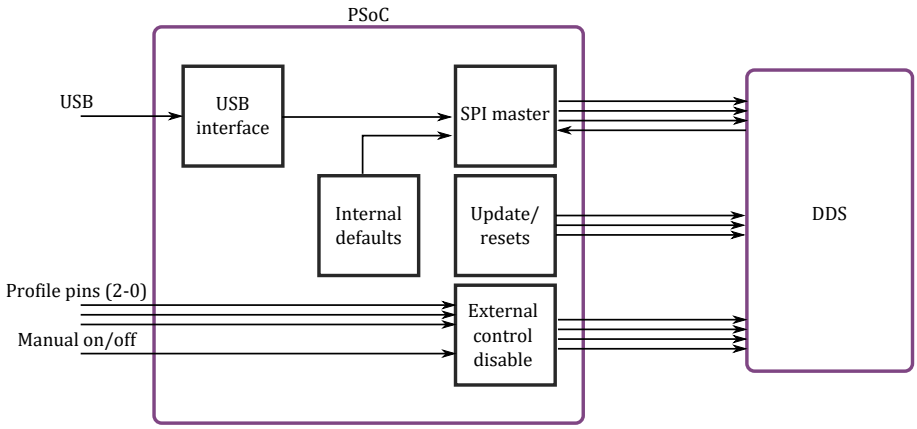

Figure 1: The block diagram of the PSoC controlled DDS. USB connection is hideously simplified.

2 Basic DDS control: PSoC micro-controller

This section contains information on the basic AOM driver which uses a PSoC to interface with the DDS. Section 2.1 provides a pictorial summary of the circuitry involved, however, further details can be found in the PSoC "main.c" file and the DDS Development lab book. The final three sections detail the operating mode available using the PSoC controller. A description of the single tone profiles can be found in section 2.2, the RAM playback can be found in section 2.3 and the linear ramp mode is detailed in section 2.4.

2.1 Block diagram

Figure 1 shows the functional block diagram for the PSoC controlled DDS. Note, the PSoC has the right to decline user input only during the loading of new RAM data. This is necessary to ensure the memory is written correctly.

2.2 Single tone profiles

In single tone mode, the DDS control parameters are supplied directly from eight internal registers. Each profile is an independent register which contains frequency, phase, and amplitude information. The user can select the active profile using the three profile BNCs on the front panel of the driver module. The profile pins are weakly pulled to ground, hence with no TTLs attached the default profile is 0 (a typical application would be for spectroscopy). Table 1 shows the address scheme used by the DDS.

It is possible to control the amplitude of the DSS output with the "amplitude scale factor" or the "Manual on/off" control (see Manual OSK in the AD9910 datasheet). Note, the DDS does not allow these features to be activated simultaneously. The amplitude scale factor allows the amplitude of each of the 8 profiles to be set

Profile-pins			Profile number
2	1	0	
0	0	0	0
0	0	1	1
0	1	0	2
0	1	1	3
1	0	0	4
1	0	1	5
1	1	0	6
1	1	1	7

Table 1: Profile select using the 3-bit address system.

using a 14-bit number between 0 and 1. If this mode is inactive then the DDS assumes an amplitude scale factor of 1 for all profiles. When in the Manual on/off mode, the user can use the "on/off" BNC on the front panel of the DDS to enable and disable the DDS output. This channel is active high and thus requires a TTL to enable the output.

2.3 RAM modulation mode

The PSoC can be used to initiate the DDS in RAM mode modulation mode.The DDS loads parameters directly from a 1024-word RAM. Note, care should be taken to make sure the desired waveform fits within the memory. This mode provides an incredibly flexible method for generating arbitrary, time dependent waveforms.

The user can load the RAM with one or multiple concatenated waveforms. For concatenated waveforms, each section of the waveform can be assigned to one of the 8 profiles. The user can specify the rate at which the DDS steps through the RAM and where in the RAM block to start and end for each of the 8 profiles. Since the RAM profiles are independent, it is also possible to define profiles with overlapping address ranges. Changes in the RAM state are enabled using the 3 profile pins. It is important to note that that each profile modulates the same parameter i.e. either amplitude or phase, or frequency. Polar modulation on the other hand does allow simultaneous amplitude and phase modulation but is of little use for an AOM driver. Additional ramp generation can be added as a future update (depending on feedback) to allow for a linear ramp of one parameter while the RAM modulates another parameter.

Each of the 8 profiles can be programmed with different modes of playback. This enables a fairly complicated modulation to be constructed despite the limited memory available. Additionally, a series of internal controls can be added to automatically switch between different profiles. This feature is useful to reduce the number of TTLs used by the DDS. The following sections describes how each of these modes operates.

2.3.1 Direct playback

In this mode the RAM is not used as a waveform generator, instead only the start address of the selected profile is passed to the DDS. This mode is therefore useful for a default or for jumps in waveform parameters. Note, the no-dwell switch is ignored in this mode.

2.3.2 Direct playback with zero-crossings

The zero-crossing feature only applies in direct mode and while the phase is being modulated. This was added solely for completeness. Enabling this feature causes the DDS to delay the update of a new phase value until such time at which a change in phase will have minimum impact on the amplitude of the waveform. As this feature is unlikely to be used when driving an AOM, it is recommended to refer to the data-sheet for more information.

2.3.3 RAM ramp-up mode

When a profile in the ramp-up mode is selected, the RAM begins operating as a waveform generator. The chosen parameter is modulated over the specified address range at the rate programmed for that profile. The RAM plays through the memory from the start address and continues until the end address is reached.

An important feature to note is the use of the no-dwell control. If the no-dwell feature is enabled, the RAM playback jumps back to the start address and maintains the tuning parameters stored at this address. This is shown in figure 2a). If the no-dwell feature is disabled, however, the parameter held in the end address used instead. This is shown in figure 2b). Note, the step rate is figure 2 is given in units of dt.

2.3.4 RAM ramp-up mode with additional internal profile controls

When any of the internal profile controls are selected the 3 profile pins are ignored as is the no-dwell feature. The dynamics of this variation of the ramp-up mode remains the same, however, the profile switching is done automatically. The profiles cycle according to table 2.

The table can be divided into burst and continuous waveforms. In both cases, profile 0 is selected first (therefore the RAM playback uses the start and end addresses and rate specified by profile 0). After reaching the end address of Profile 0, the next profile is automatically loaded and playback of profile 1 begins. This stepping through the profiles continues until the end profile (as outlined in table??) is reached. If burst mode is selected then waveform generated is defined by last parameter loaded to the DDS In continuous mode, the RAM loader automatically jumps to profile 0 and the cycle continues. Illustrations of the burst and continuous internal control methods can be found in figures 3 and 4 respectively.

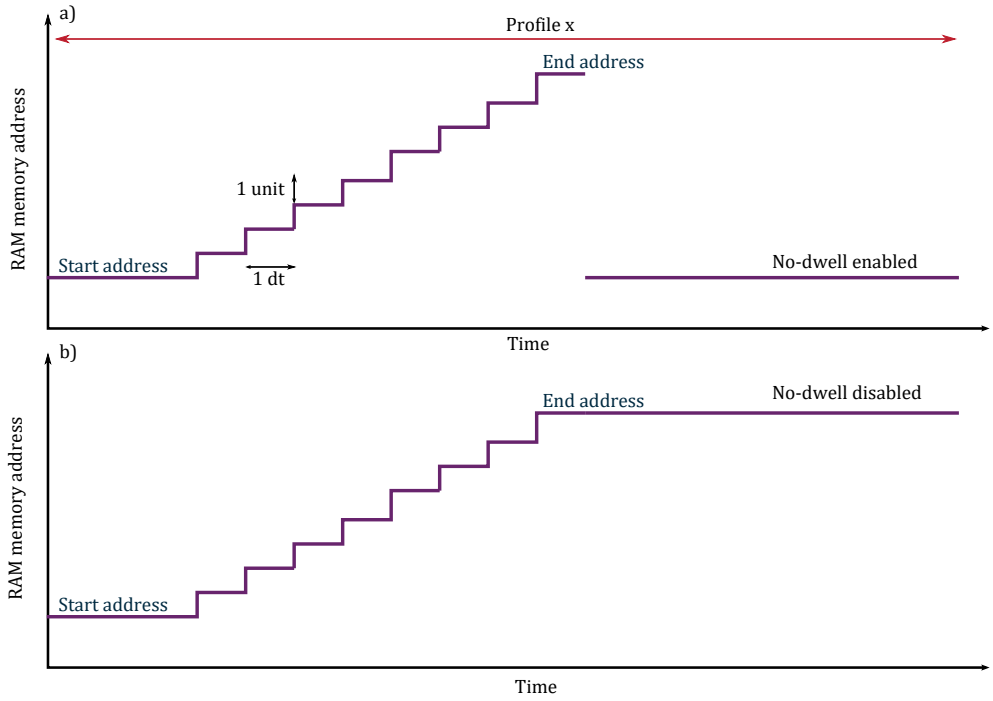

Figure 2: The timing diagram of the ramp-up RAM playback mode with a) with the no-dwell feature enabled and b) the no-dwell feature disabled.

2.3.5 RAM bidirectional ramp mode

In this mode, once the data is programmed the RAM begins operating as a waveform generator using the parameters programmed only into RAM Profile 0. In other words, the address range and rate used loaded into the profile 0 register. This mode of playback is different to those previously described as the profile-pins 1 and 2 are ignored, as is the no-dwell feature. To initialise, profile-pin 0 is held at logic 0 and the RAM data from the start address is loaded and held. When profile-pin 0 is set to logic 1, data extraction from the RAM begins. The memory address is incremented provided profile-pin 0 remains at logic 1. If the end address is reached, that parameter is held. When profile-pin 0 is set to logic 0, the memory address is decremented though the address range until the start address is reached. If profile-pin 0 changes state before the extrema of the the address range is reached, the direction of data extraction is reversed. Figure 5 shows an illustration of the bidirectional ramp mode.

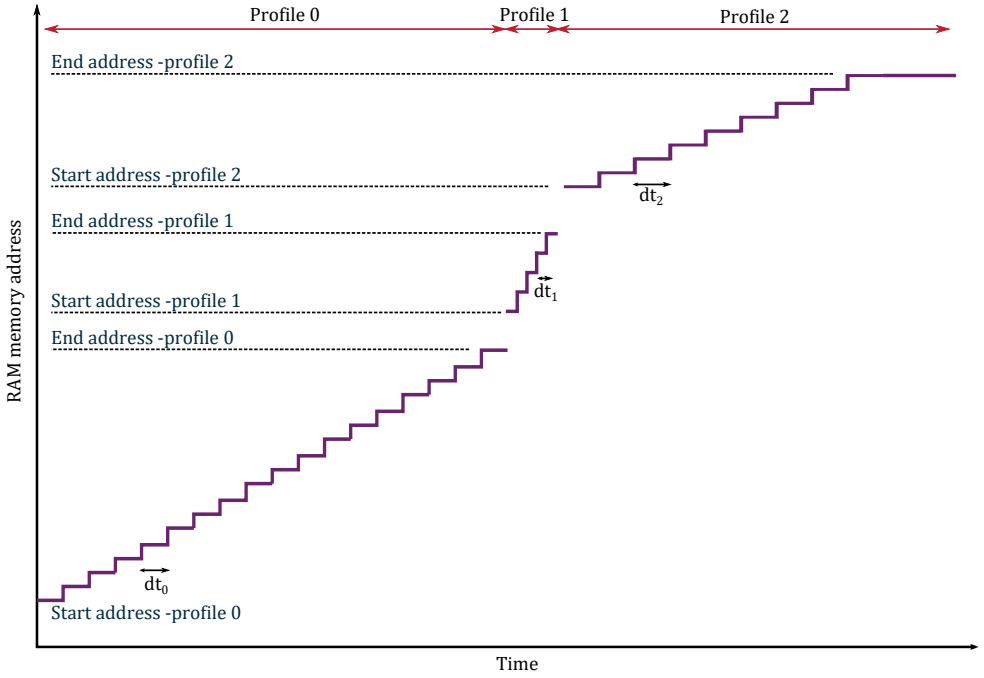

Figure 3: The timing diagram of the ramp-up RAM playback mode the burst internal control enabled.

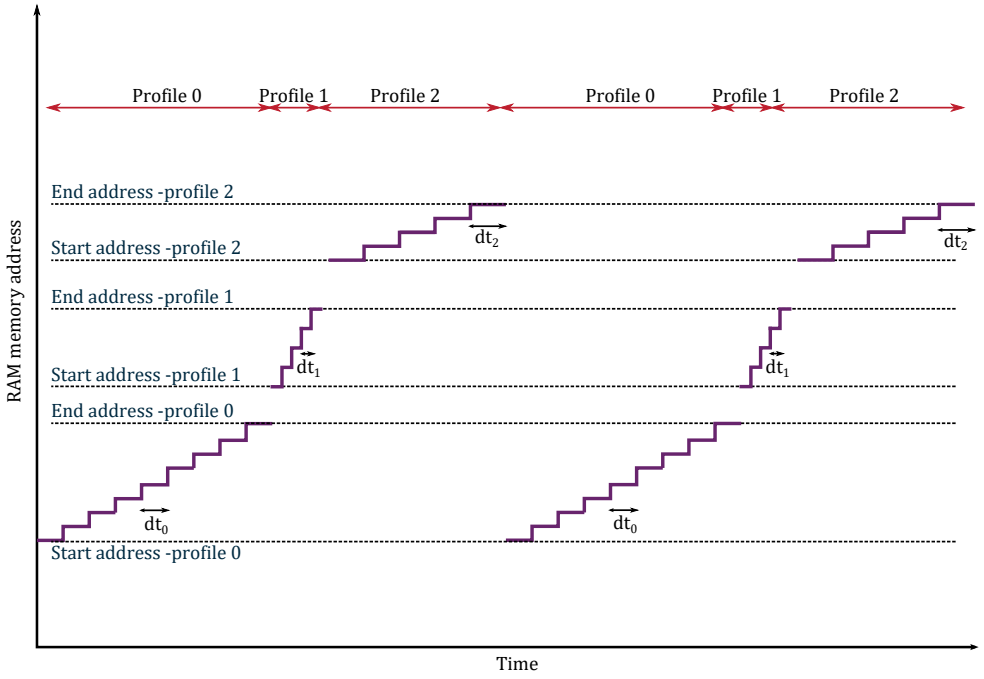

Figure 4: The timing diagram of the ramp-up RAM playback mode the continuous internal control enabled.

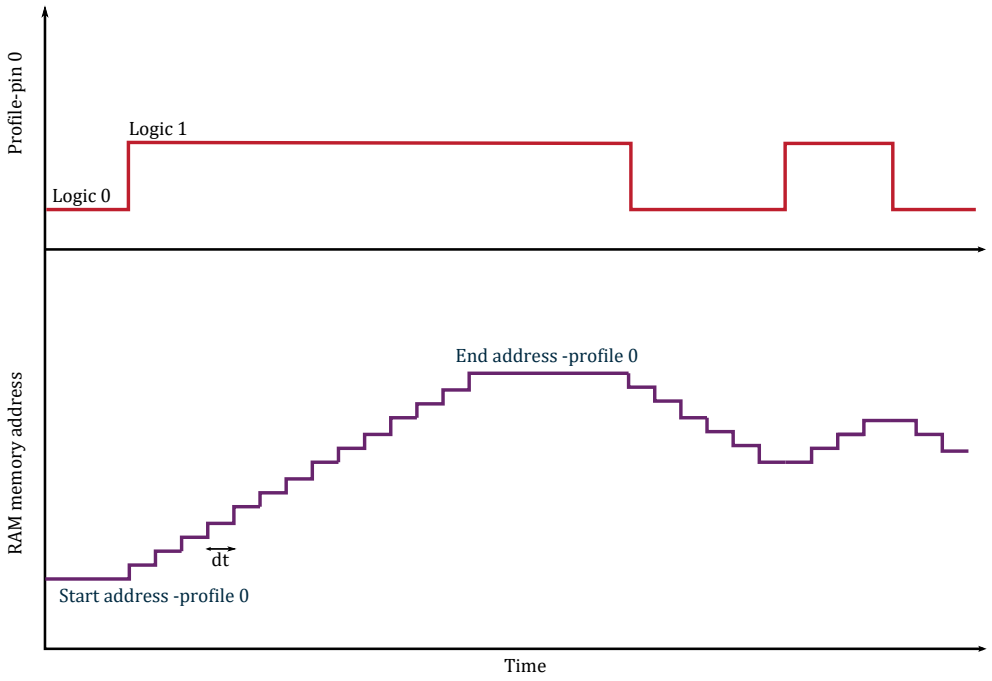

Figure 5: The timing diagram of the bidirectional ramp RAM playback mode. The state of profile-pin 0 is also shown.

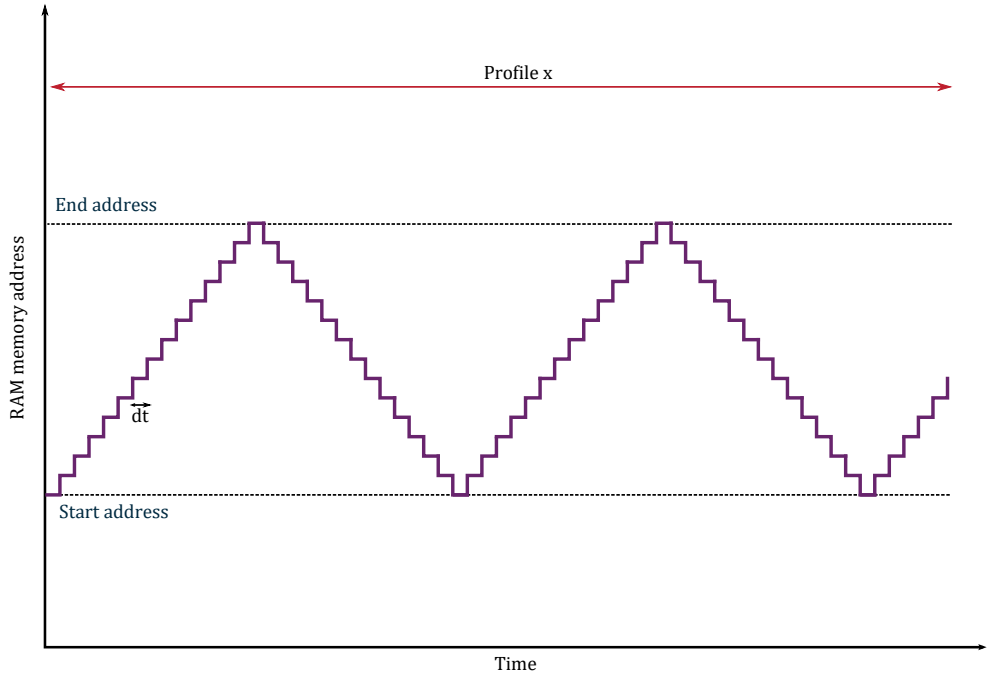

Figure 6: The timing diagram of the continuous bidirectional ramp RAM playback mode.

Mode number	Waveform type	Description
1	–	Internal profile control disabled
2	Burst	Execute profiles 0 - 1, then halt
3	Burst	Execute profiles 0 - 2, then halt
4	Burst	Execute profiles 0 - 3, then halt
5	Burst	Execute profiles 0 - 4, then halt
6	Burst	Execute profiles 0 - 5, then halt
7	Burst	Execute profiles 0 - 6, then halt
8	Burst	Execute profiles 0 - 7, then halt
9	Continuous	Execute profiles 0 - 1 continuously
10	Continuous	Execute profiles 0 - 2 continuously
11	Continuous	Execute profiles 0 - 3 continuously
12	Continuous	Execute profiles 0 - 4 continuously
13	Continuous	Execute profiles 0 - 5 continuously
14	Continuous	Execute profiles 0 - 6 continuously
15	Continuous	Execute profiles 0 - 7 continuously

Table 2: Summary of the internal profile control modes for the RAM.

2.3.6 RAM continuous bidirectional ramp mode

In continuous bidirectional ramp mode functions can be programmed for each profile (hence the start and end address and step rate are set with each profile). The no-dwell high feature is also ignored in this mode. Data is extracted from the memory according to the address range and rate of the current profile selected. The memory address is incremented until the end address is reached. At which point, the memory address is decremented until the start address is reached. Once again the memory address is incremented. This cycle continues indefinitely until a new profile is selected. Figure 6 depicts the continuous bidirectional ramp mode in action.

2.3.7 RAM continuous recirculate mode

This mode is similar to the ramp-up mode, except when the end address is reached, that value is held for the step time before the address jumps to the start address. The no-dwell feature is ignored in this mode. Also note, that when a new profile is selected the current waveform is aborted. Figure 7 shows an illustration of the continuous recirculate mode.

2.4 Linear ramp generation mode

An additional feature of the AD9910 DDS is the ability to linearly sweep frequency, phase or amplitude between a start and end point at arbitrary rates. This can be achieved using the digital ramp generator. Moreover, this unit is completely separate to the RAM and single tone profile modes so can be used in addition these previously described features.

The ramp characteristics are defined using upper and lower ramp limits. Furthermore, the gradients of the positive and negative slopes are independent (i.e. the step size and step rate can be defined for each type of sweep). The direction of the ramp is controlled by the ramp-control pin. While held at logic 0, the generator

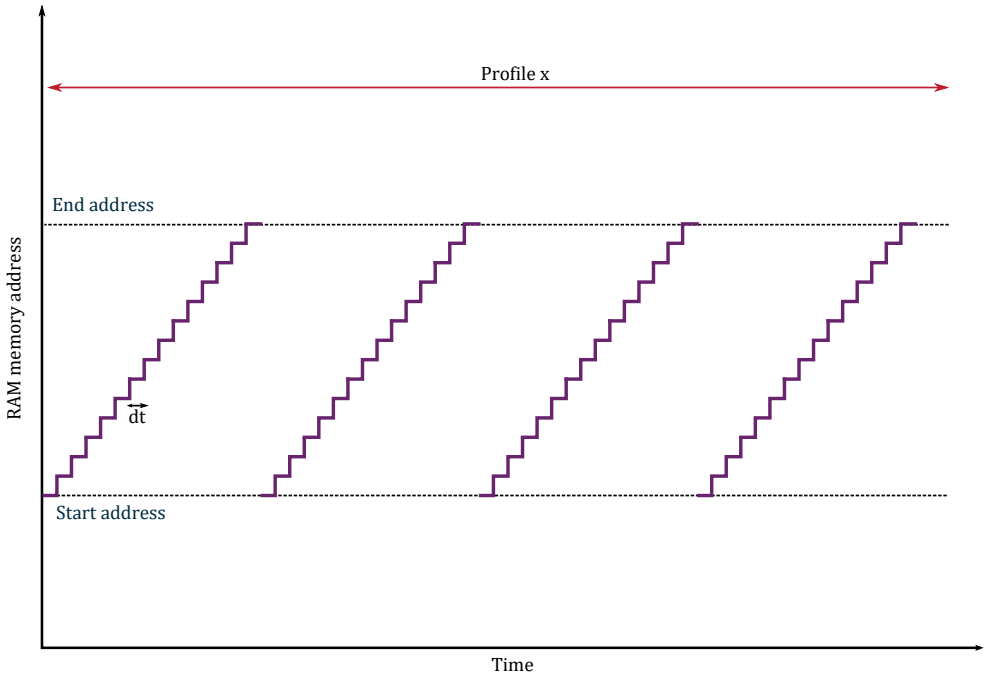

Figure 7: The timing diagram of the continuous recirculate ramp RAM playback mode.

produces a linear ramp with a negative slope. A logic 1 produces a ramp with a positive slope. Note, the ramp generator does not ramp beyond the defined limits.

The ramp-hold pin can also be used to pause the ramp. This is an active high (i.e. requires logic 1) control pin. Another important note is that the ramp generator works in conjunction with other DDS features. **The DDS signal control parameters that are not modulated by the ramp generator are taken from the active profile.**

2.4.1 Ramp control

The positive and negative slope step rates are clocked in a similar fashion as the RAM playback rate. The intervals are characterised by two 16-bit numbers giving a resolution of 4 ns and a maximum rate of every 262.14 μs.

The step size of the modulation in the positive and negative directions are stored as a 32-bit number, giving the full precision for frequency control. In should be stressed that although the ramp generator module is 32-bit precision the phase and amplitude controls are 16- and 14-bit respectively. Hence for these parameters the step size programmed is really an average value due to the data truncation.

Additional notes:

- There are two methods the typical user can use to reset the ramp generator. The first is a change of state of the ramp-control pin and the second is enabling the load LRR feature. The latter feature allows the reset of the ramp controller through a change of state of the profile pin.

- The output of the ramp generator will never exceed the programmed limits. Even is the step size is greater that the different in the upper and lower limits.

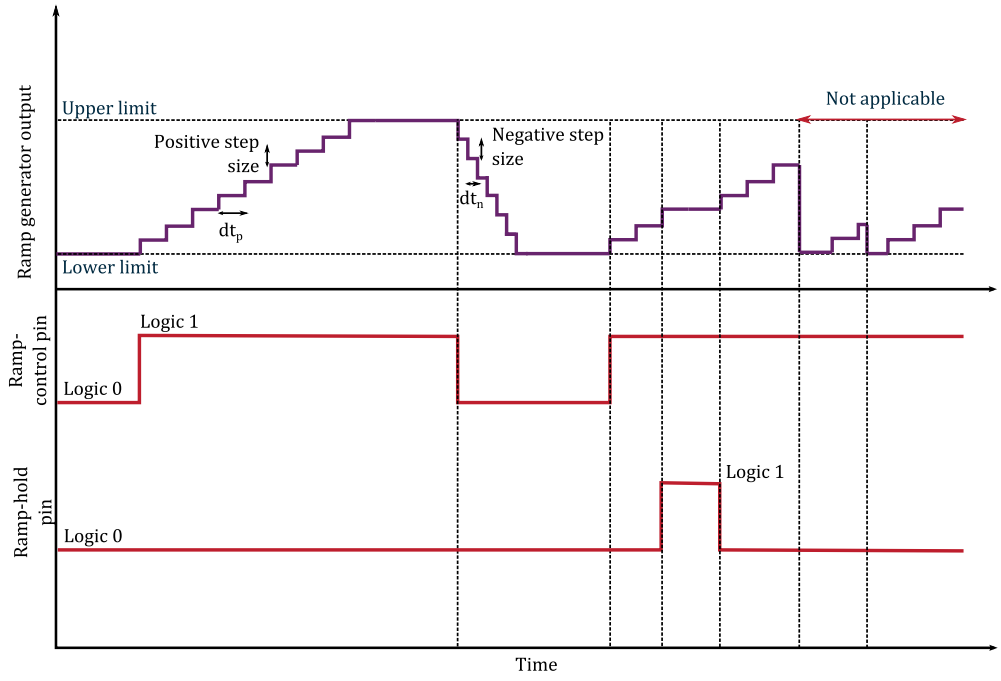

Figure 8: Timing diagram of the ramp generator in normal operation. Note the end section of the waveform is current not applicable.

- The upper limit value must be greater than the lower limit.
- The ramp generator can be reset to 0. When reset, the modulation is forced back to the programmed lower limit.

2.4.2 Normal ramp generation

This name has been chosen to be consistent with the data-sheet. This mode is achieved if both no-dwell high and low features are disabled. Figure 8 shows the timing diagram of a typical "normal" ramp. Included in the figure is signals used to control the ramp generator.

In normal ramp mode, once the ramp reaches either of the limits the modulated will be held at this value until the control pins dictate otherwise. Also note, if the state of the ramp-control pin changes before one of the limits has been reach, the output will continue to be modulated by the ramp generator until a limit is reached.

2.4.3 No-dwell ramp generation

The no-dwell high and low features add extra flexibility to the ramps that can be generated. In no-dwell operation, the output does not necessarily stay at the limit. For example, if the no-dwell high feature is enabled and the upper limit is reached, the ramp generator instantaneously jumps to the lower limit. When the no-dwell low feature is enabled, when the ramp reaches the lower limit the output jumps immediately to the upper limit.

The type of logic transition (either positive edge or negative edge) of the ramp-control pin is important when the no-dwell features are enabled. For instance, with

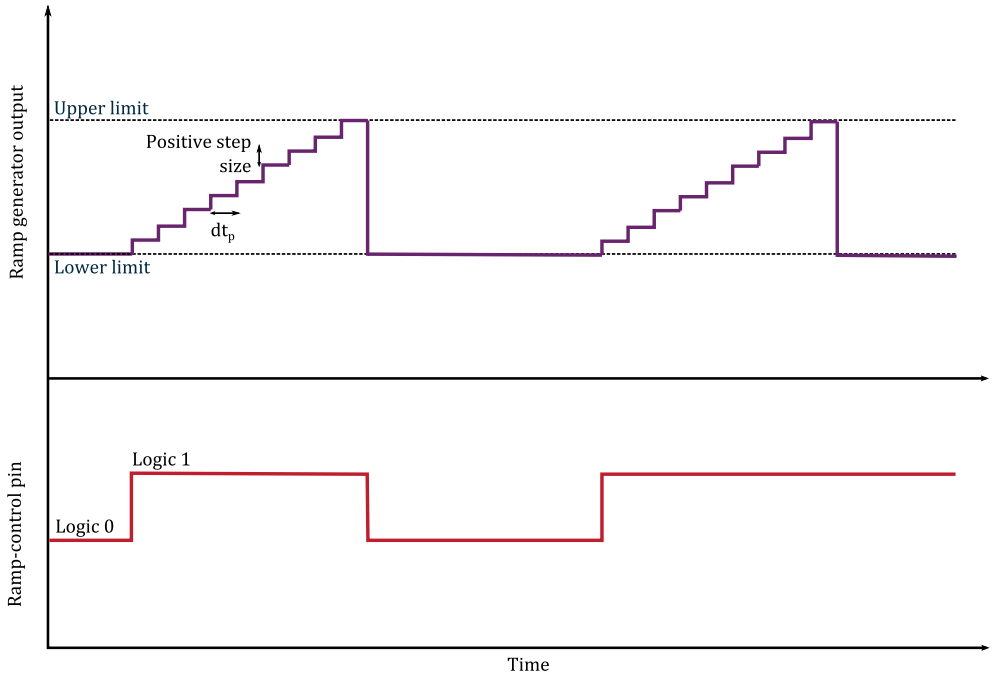

Figure 9: Timing diagram of the ramp generator with the no-dwell high feature enabled.

the no-dwell low feature enabled, a negative edge transition of the ramp-control pin begins a negative slope ramp. To reiterate, this ramp will continue uninterrupted despite of the ramp-control pin until the lower limit is reached. While with the no-dwell high feature enabled, a positive edge of the ramp-control pin initiates a positive slope ramp. Again, to labour the point, this ramp will continue uninterrupted until the upper limit is reached.

Both the no-dwell high and low features can be enabled together. This equates to continuous ramping mode of operation. In this case, the modulated output automatically oscillates between the two limits using the programmed slope parameters. The function of the ramp-control pin is again slightly different, now this pin changes the direction of the ramp sequence. Hence, if the ramp gradient is positive and a negative edge of the ramp-control pin is detected, then the negative gradient ramp begins. Again oscillating between the two limits. Alternatively, if during a negative gradient ramp a positive edge is detected on the ramp-control pin, a positive gradient ramp begins (oscillating between two limits).

Figure 9 shows a timing diagram of when the no-dwell high feature is active. With the no-dwell low feature enabled the operation is similar, however, the output now ramps in the negative direction on a Logic negative edge of the ramp-control pin. The ramp generator will jump to the upper limit upon reaching the lower limit.

3 FPGA Control

This section contains information on the FPGA upgrade of the AOM driver. This upgrade is necessary for more complex modulations and for modulation which cannot be stored in the 1024 RAM of the DDS. Section 3.1 provides a pictorial summary of the circuitry involved, however, further details can be found in the FPGA "main.hdl" file and the DDS Development lab book.

Additional sections will be added once I have picked a suitable FPGA and determined the best way to load the trajectories.

3.1 Block diagram

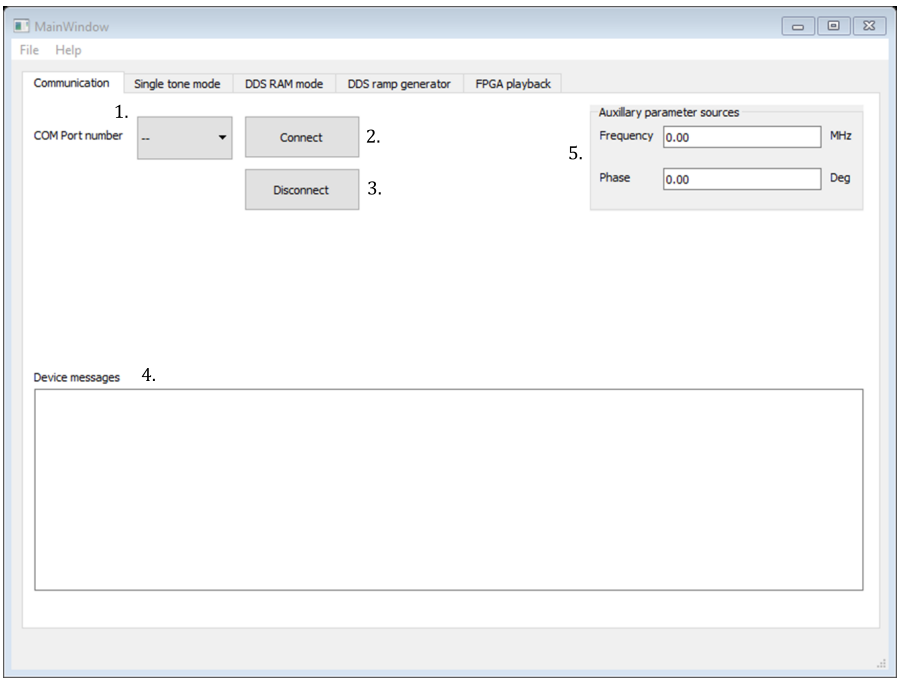

Figure 10: Annotated capture of the communications tab.

4 User interface

The following describes the function available to the user when using the python GUI interface. The purpose of the GUI is to mask a lot of the conversions necessary to programme the DDS while allowing user to design and visualise RAM mode trajectories. This section is divided into four sections corresponding to the four tabs on the GUI. Section 4.1 describes how to initialise the communication with the DSS. Section 4.2 details how the user can set up the single tone profiles and section **??** describes setting up the DDS RAM playback. Section 4.5 describes the load data features the AOM driver GUI is capable of. Finally, section 4.6 explains the FPGA programmer.

4.1 Communication

Figure 10 shows the annotated communication tab of the AOM driver control GUI.

1. Communication port select. Once the AOM driver is recognised by the computer it will be assigned a serial COM port. You may need to open the device manager to locate the correct number.

2. Connect to device. Once a COM port has been selected, this button is used to establish the serial communication.

3. Disconnect from device. This allows safe closing of the COM port.

4. Device message display. Displays information and errors from the AOM driver.

5. Loads additional parameters (needed for FPGA control).

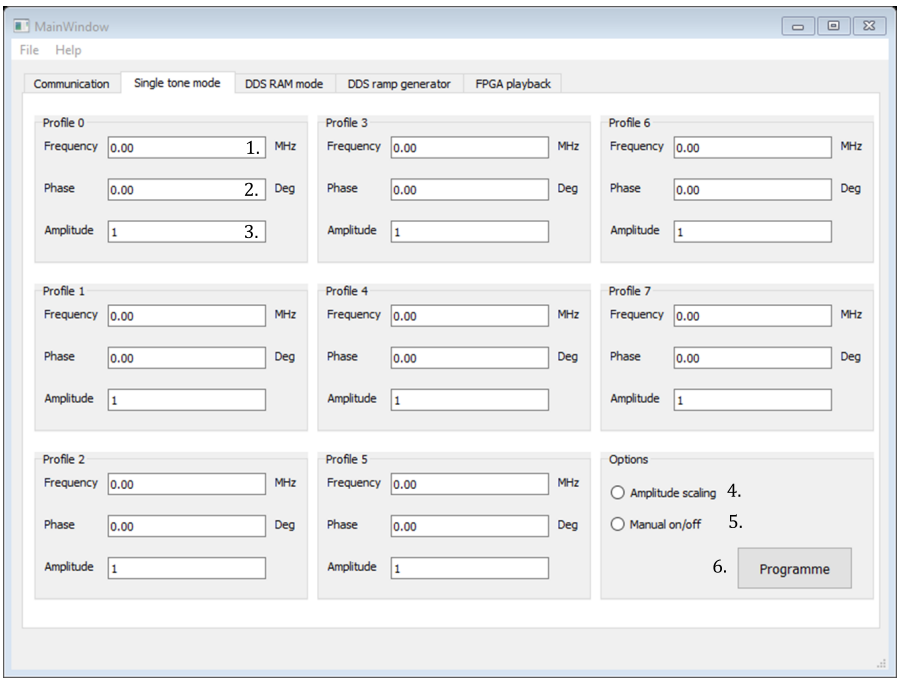

Figure 11: Annotated capture of the single profile tab.

4.1.1 Installing the PSoC drivers

If the device is not recognised (i.e. the operating cannot find the drivers). Follow these steps (windows only):

1. Communication port select.

4.1.2 Example of initialisation

The following describes the method how to establish communication with the AOM driver (windows only).

1. Communication port select.

4.2 Single tone profile

Figure 11 shows the annotated single tone profile tab of the AOM driver control GUI.

1. Frequency control. Floating number in MHz. If the value entered is zero this profile is skipped. 32-bit resolution.

2. Phase of the waveform. Floating number in degrees. 16-bit resolution.

3. Amplitude scale factor. This only works if amplitude scaling enabled, otherwise defaults to 1. Floating number from 0 to 1. 14-bit resolution.

4. Amplitude scaling enable. When selected, the profiles each can be assigned with a different amplitude. Does not work simultaneously with the manual on/off.

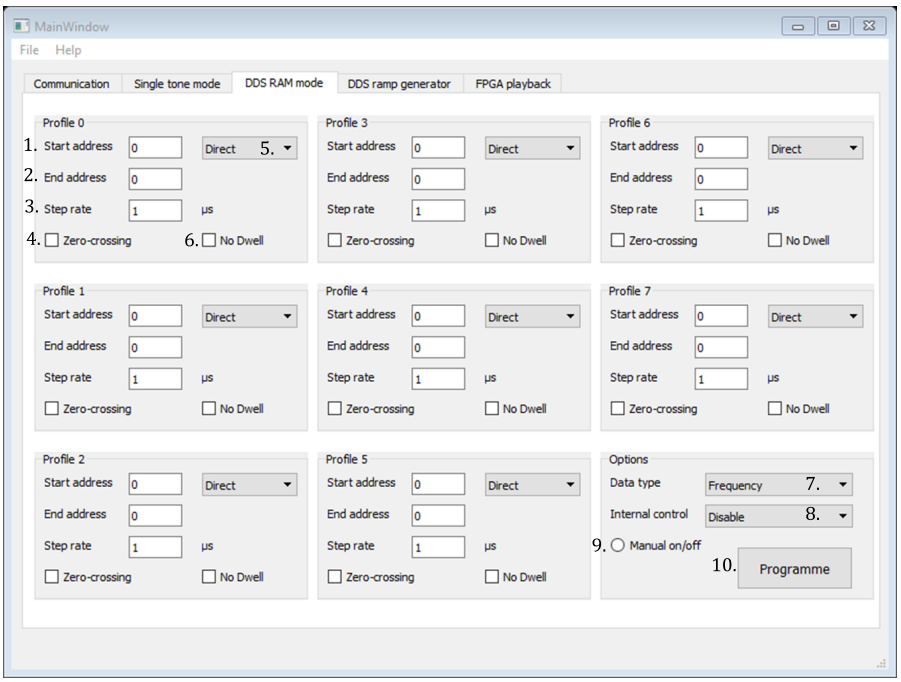

Figure 12: Annotated capture of the DDS RAM playback tab.

5. Manual on/off enable. When selected the user can switch the amplitude of the profiles to zero. Does not work simultaneously with the amplitude scaling factor.

6. Programme. Transfers the data to the selected AOM driver. This also saves a csv file containing the information of the values sent to the driver.

4.3 DDS RAM mode

Figure 12 shows the annotated DDS RAM mode tab of the AOM driver control GUI.

1. Start address. Tells the DDS where to begin loading the data stored in RAM. Positive integer between 0 - 1023. Must be less than the end address of a particular profile.

2. End address. Tells the DDS where to end extracting the data stored in RAM. Positive integer between 1 - 1023. Must be greater than the start address of a particular profile.

3. Step rate, μs. The time interval between the RAM loading new data. The resolution of this value is 4 ns. The range of time intervals this can take is 4 ns up to 262.14 μs.

4. Zero-crossing enabled. Only applicable when phase is the modulation target and direct mode is selected.

5. Playback mode. Selects the type of playback use for a particular profile. For more details see section 2.3. The modes include:

(a) Direct (with zero-crossing option)

(b) Ramp-up (with no-dwell and internal profile control options)

(c) Bidirectional ramp

(d) Continuous bidirectional ramp

(e) Continuous recirculate

6. No-dwell enable. Only applicable when ramp-up mode is selected.

7. Data type. This selects which parameter will be modulated the options include:

   (a) Frequency

   (b) Phase

   (c) Amplitude

   (d) Polar (phase and amplitude)

8. Internal profile control select, only applicable to the ramp-up mode. See table 2 for details.

9. Manual on/off enable. Enable the ability to switch the amplitude of waveform on and off. Note, the internal priority of the DSS data loader may cause issues if the user is modulating amplitude and switching the profile-pins and the manual on/off simultaneously.

10. Counter. Shows the number of RAM addresses left to fill. Note 1024 is maximum.

11. Programme. Transfers the data to the selected AOM driver. This also saves a csv file containing the information of the values sent to the driver. Only possible if the total RAM addresses is less than 1024 and a modulation trajectory has been designed/loaded.

4.3.1 RAM mode trajectory designer

1. Functional form of the time dependent modulation. Not applicable in direct playback mode. Selections opens the waveform editor. The functions include:

   (a) Linear

   (b) Gaussian

   (c) Minimum jerk

   (d) Exponential

   (e) Exponential saturate

   (f) Logarithmic

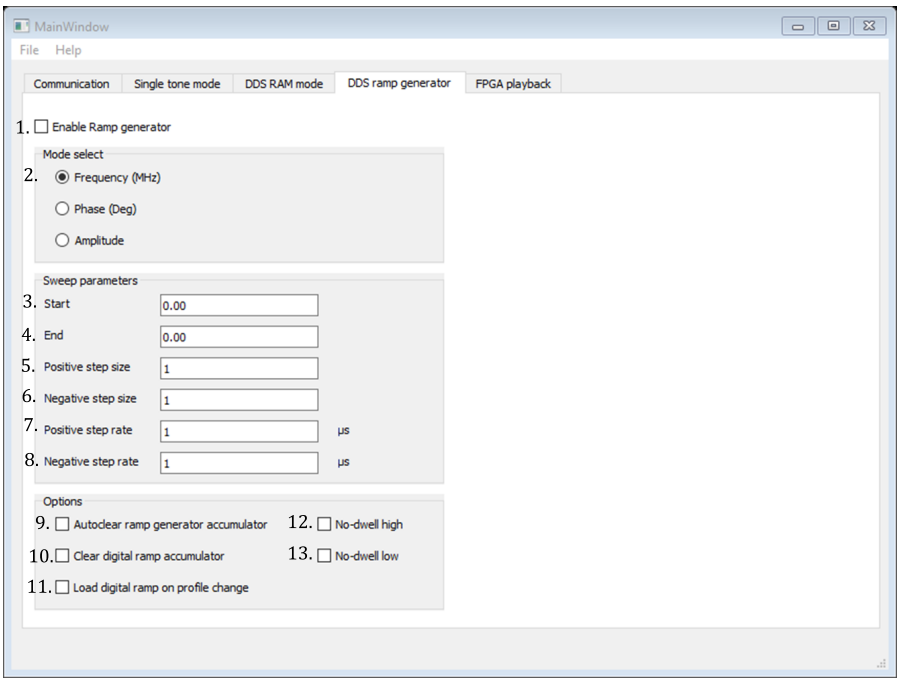

Figure 13: Annotated capture of the DDS ramp generator tab.

4.4 Ramp generator

Figure 13 shows the annotated ramp generator tab of the AOM driver control GUI.

1. Ramp generator enable. Must be clicked to load the generator module with data.

2. Parameter to be modulated by the ramp. Is in RAM mode, the user must ensure that the same parameter is not modulated by the ramp generator and the RAM.

3. Start value of the ramp also referred to as the lower limit of the ramp. Note the units are provided by the parameter being modulated.

4. End value of the ramp also referred to as the upper limit of the ramp. Note the units are provided by the parameter being modulated.

5. Positive step size. This defines how larger step in taken by the parameter being modulated when the linear ramp has a positive gradient. Note the units are provided by the parameter being modulated.

6. Negative step size. This defines how larger step in taken by the parameter being modulated when the linear ramp has a negative gradient. Note the units are provided by the parameter being modulated.

7. Positive step rate. The time interval before the another step size unit is added to the current output while the ramp gradient is positive. The resolution of this value is 4 ns. The range of time intervals this can take is 4 ns up to 262.14 μs.

8. Negative step rate. The time interval before the another step size unit is subtracted to the current output while the ramp gradient is negative. The resolution of this value is 4 ns. The range of time intervals this can take is 4 ns up to 262.14 μs.

9. Auto-clear the ramp generator enable. Added for completeness since the typical user does not have access to this. This will only reset the ramp generator if the reset on profile change feature is enabled.

10. Clear the ramp generator enable. Added for completeness since the typical user does not have access to this. This will only reset the ramp generator if the reset on profile change feature is enabled.

11. Reset on profile change enable. Allow the above two featured to be used. Changing the state of the profile pins will clear the ramp generator and reset it to the lower limit.

12. No-dwell high enable.

13. No-dwell low enable.

Note, that there is no dedicated programme button for the ramp generator. This is because the user must programme either the single tone profiles or the RAM mode for this feature to work.

4.5 Loading data to the GUI

This will be added later.

4.6 FPGA playback

Soon... but not now.

5 Test cases

This section provides new users with a guide to set up the AOM driver. By default, the AOM driver is set into the single tone profile mode with the amplitude scaling and manual on/off disabled. The first example will explain the switch-on procedure and provide example measurements that the user will be able use to ensure that the driver is working correctly. The two additional examples provides a step-by-step guide to programming the AOM driver in the single tone profile mode with the manual on/off switch enabled and how to construct a frequency ramp using the DDS RAM playback.

For these tests, it is assumed that any amplification has been removed and you are looking at the DDS output only. You will also require:

- An oscilloscope with a frequency maths function. A Picoscope from the prep room is suitable for this.
- A TTL source (3.3 V)

5.1 Getting started

As previously mentioned, by default the AOM driver is configured in the single tone profile mode. The first test will confirm this.

1. Connect the TTL triggers to the AOM driver. If only one TTL is available connect it to profile pin 0.
2. Connect the output BNC of the AOM driver to oscilloscope.
3. Power the assembly using the 5 V adapter provided.
4. Connect the USB (wait for drivers to install, see section ??). This order is important!
5. With profile pin 0 held at logic 0, you should read a frequency of 80 MHz.
6. With profile pin 0 held at logic 1, you should read a frequency of 100 MHz. You should be able to recreate figure ?? if the oscilloscope is triggered off profile pin 0.

FIGURE

5.2 Setting up a single tone profile with the amplitude switch

1. Connect the output BNC of the AOM driver to oscilloscope.
2. Power the assembly using the 5 V adapter provided
3. Connect the USB (wait for drivers to install, see section ??). This order is important!
4. Open the AD9910 AOM driver GUI.

5. Use the process described in section ?? to establish communication with the driver.

6. Open the single tone profile tab.

7. Set profiles 0 and 1 with the values listed in table ??.

8. Click the manual on/off enable button.

9. Programme the driver.

10. With the oscilloscope set so that it is triggered off a rising-edge on profile pin 0. This should recreate figure ?? a).

11. If you have access to a single TTL connect it to the manual on/off BNC and set the oscilloscope to trigger from the manual on/off.

12. Pulse the manual on/off. You should see the amplitude mimic the TTL. A multi-plot waveform can be used to measure the ensure a delay on the order of 100 ns. See figure ??b).

TABLE
FIGURE

5.3 Loading a frequency sweep using the RAM mode

This test requires two TTL sources.

1. Connect the output BNC of the AOM driver to oscilloscope.

2. Power the assembly using the 5 V adapter provided

3. Connect the USB (wait for drivers to install, see section ??). This order is important!

4. Open the AD9910 AOM driver GUI.

5. Use the process described in section ?? to establish communication with the driver.

6. Open the DDS playback tab.

7. Set profiles 0, 1, 2 and 3 with the values listed in table ??.

8. Ensure that the manual on/off button is disabled.

9. Click file and then click the load RAM playback. WHAT NEXT?

10. Programme the driver.

11. Trigger the oscilloscope with the profile pins 0 and 1 one after the other. Concatenating the three This should recreate figure ?? a).

12. If you have access to a single TTL connect it to the manual on/off BNC and set the oscilloscope to trigger from the manual on/off.

13. Pulse the manual on/off. You should see the amplitude mimic the TTL. A multi-plot waveform can be used to measure the ensure a delay on the order of 100 ns. See figure ??b).