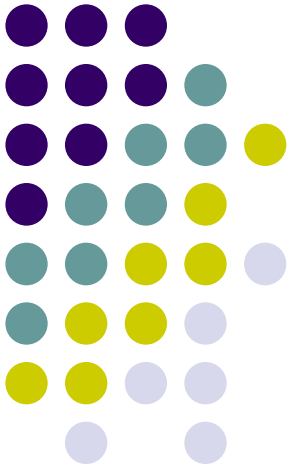
超大规模集成电路基础

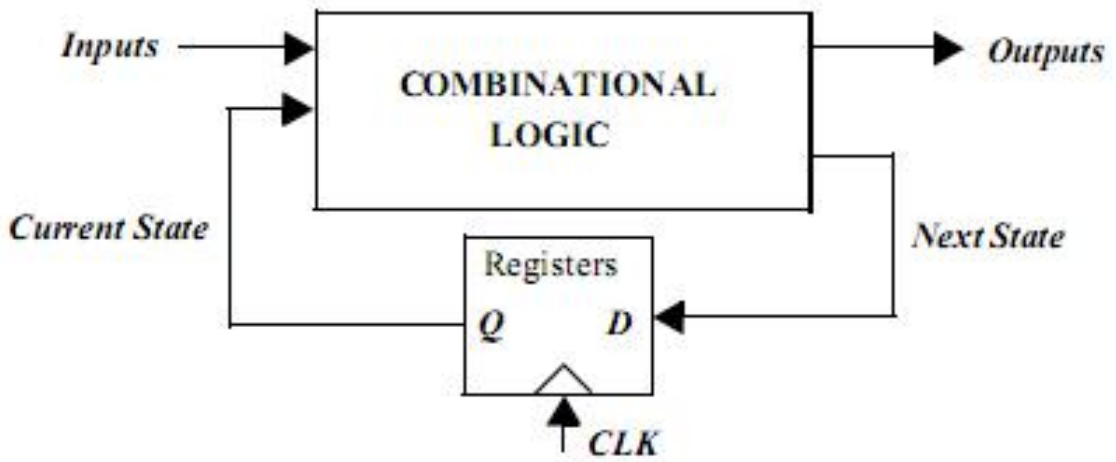
Fundamental of VLSI

第七章 时序逻辑



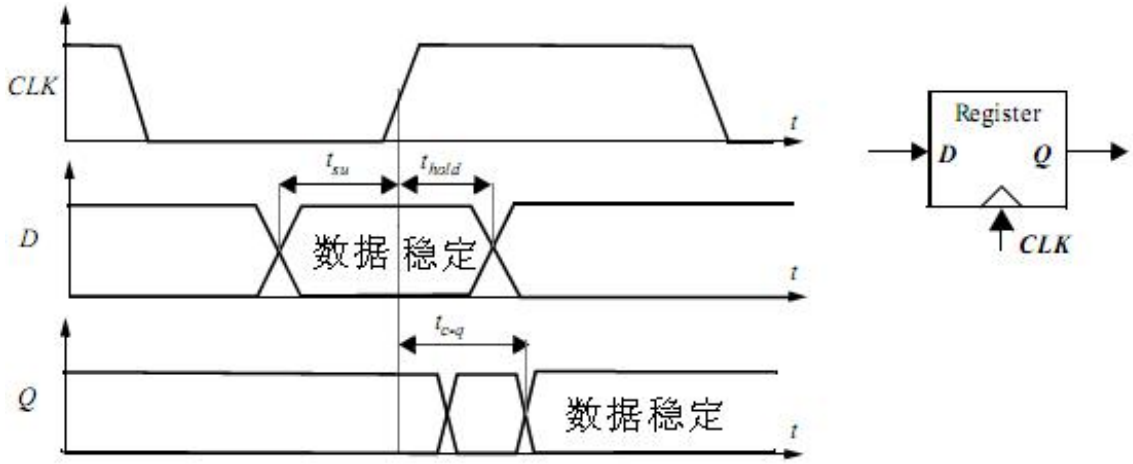
时序逻辑电路

- 电路的输出不仅取决于当前的输入值，也取决于原先的输入值



时序逻辑电路

- 时序电路的时间参数
  - 建立时间：t_{su}
  - 维持时间：t_{hold}
  - 寄存器最大传播延时：t_{c-q}
  - 污染延时：t_{cd}



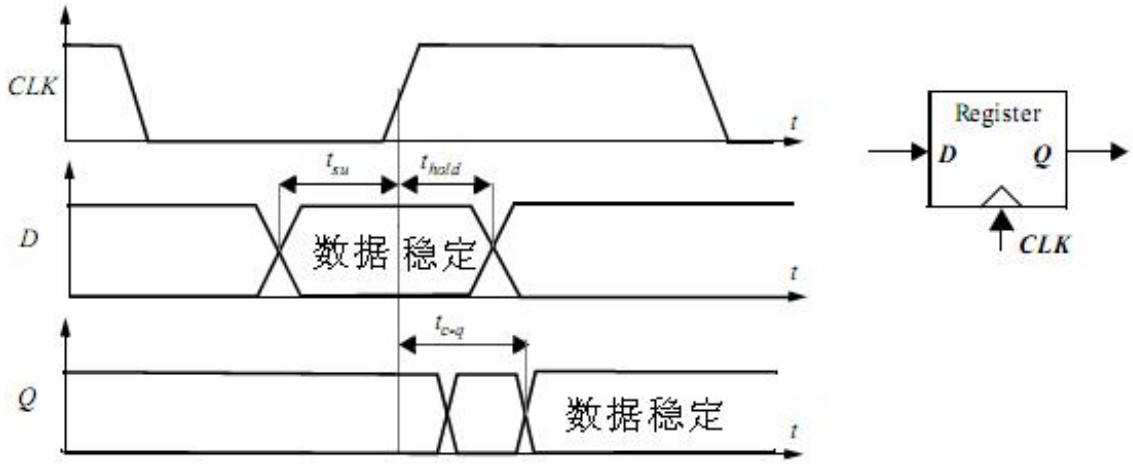
时序逻辑电路

- 时序电路的时间参数
  - 时序电路正确工作所需要的最小延时T

$$T \geqslant t_{c-q} + t_{plogic} + t_{su}$$

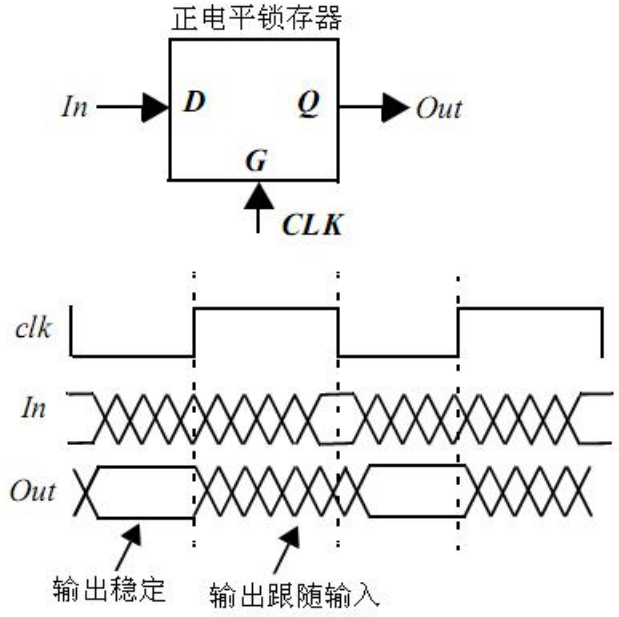
  - 寄存器维持时间约束

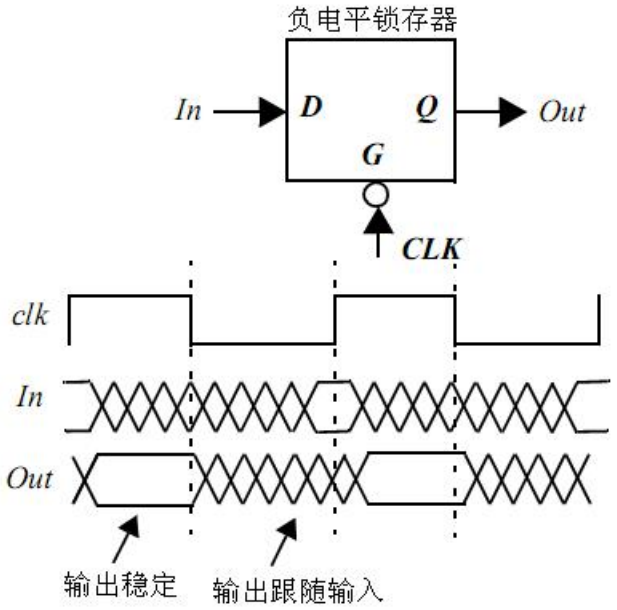
$$t_{cdregister} + t_{cdlogic} \geqslant t_{hold}$$



时序逻辑电路

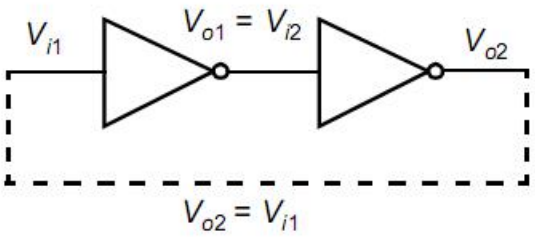
- 存储单元分类
  - 前台存储器与后台存储器
  - 静态存储器与动态存储器
  - 锁存器与寄存器

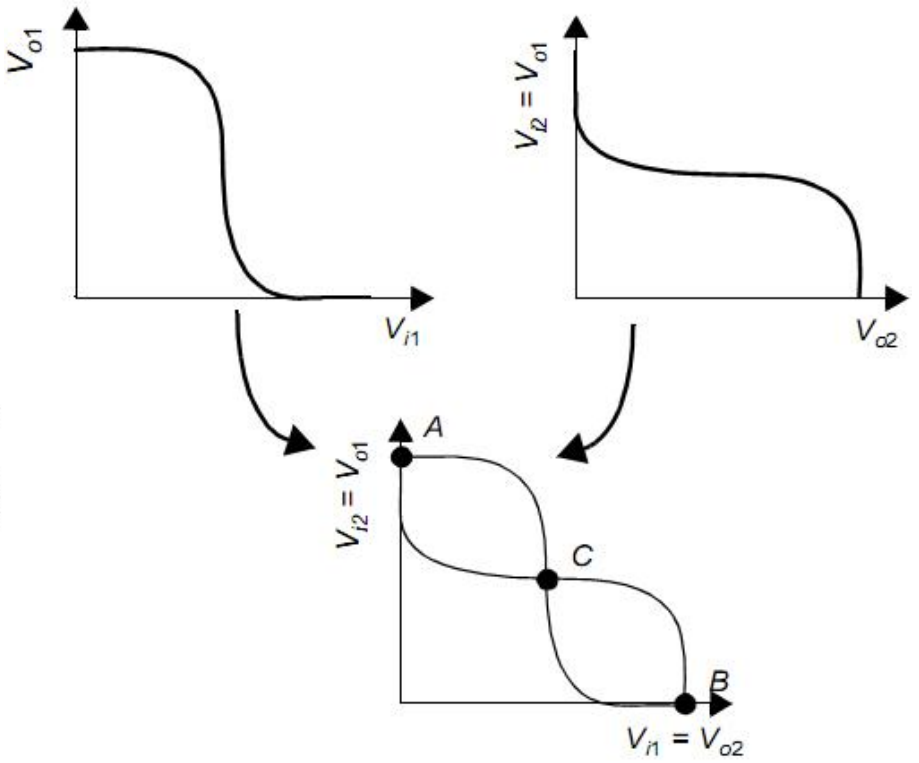




静态锁存器和寄存器

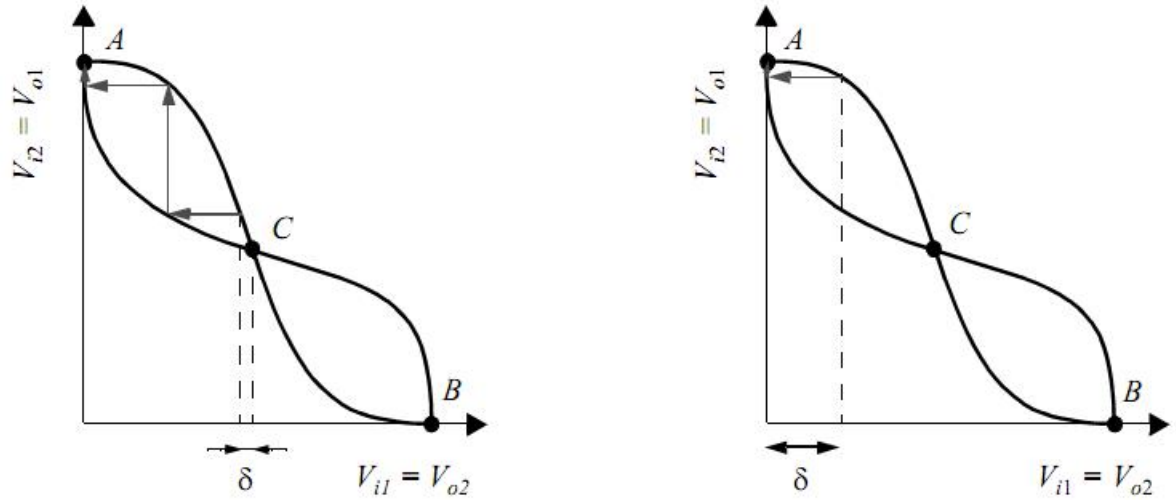
- 双稳态原理
  - 利用再生性
  - 信号可以“无限”保持
  - 对扰动不敏感





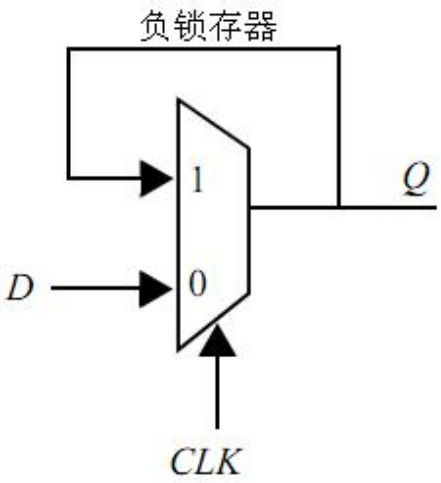
静态锁存器和寄存器

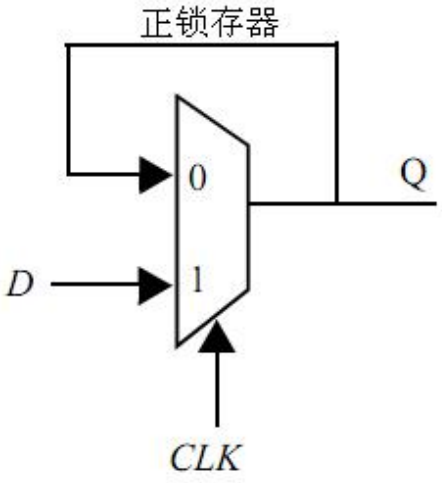
- 状态切换
  - 切断反馈环路
    - 多路开关型锁存器
  - 触发强度超过反馈环
    - 在输入端加上一个更强的触发信号，使稳态电路进行状态切换

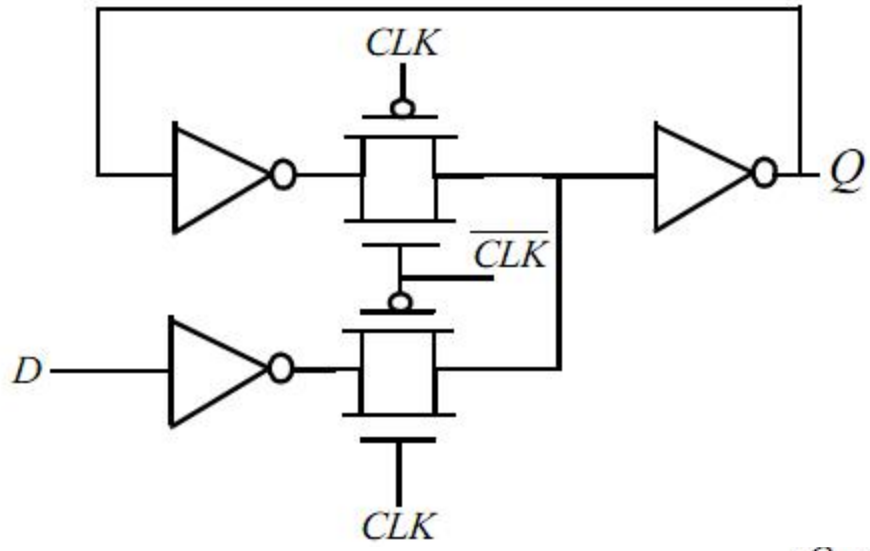


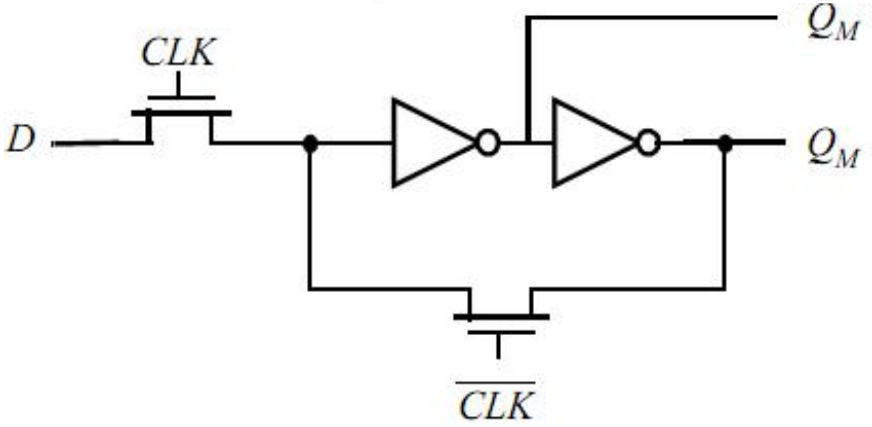
静态锁存器和寄存器

- 多路开关型锁存器



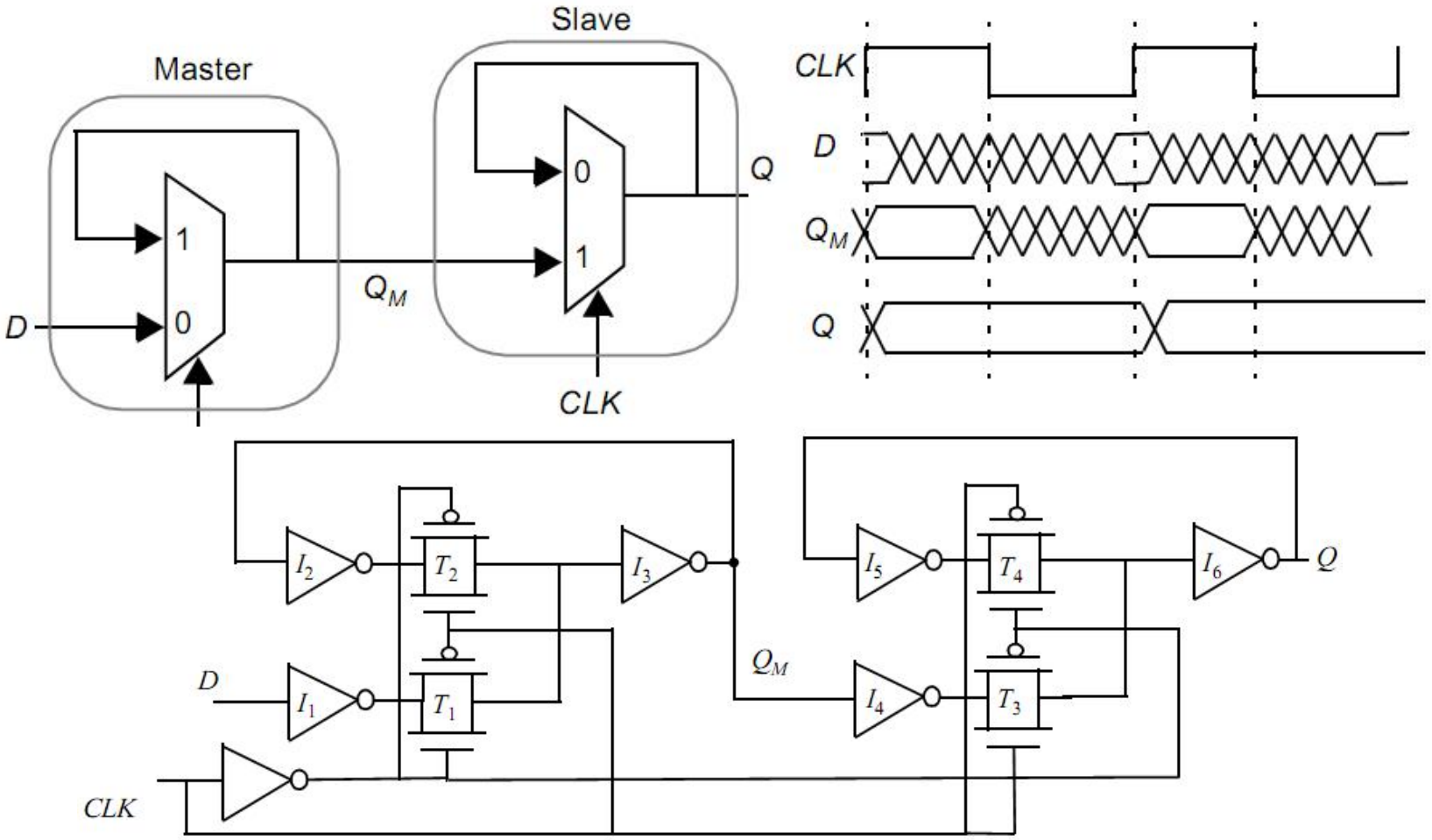






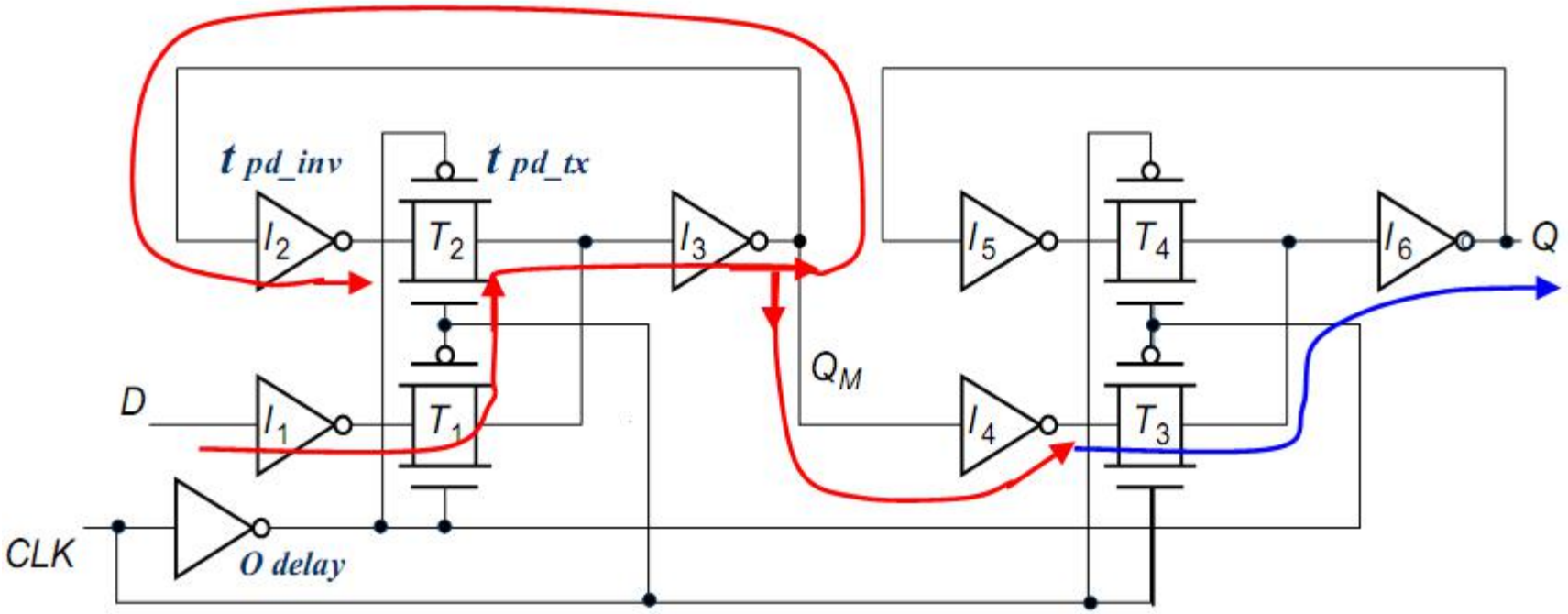
静态锁存器和寄存器

- 主从边沿触发寄存器



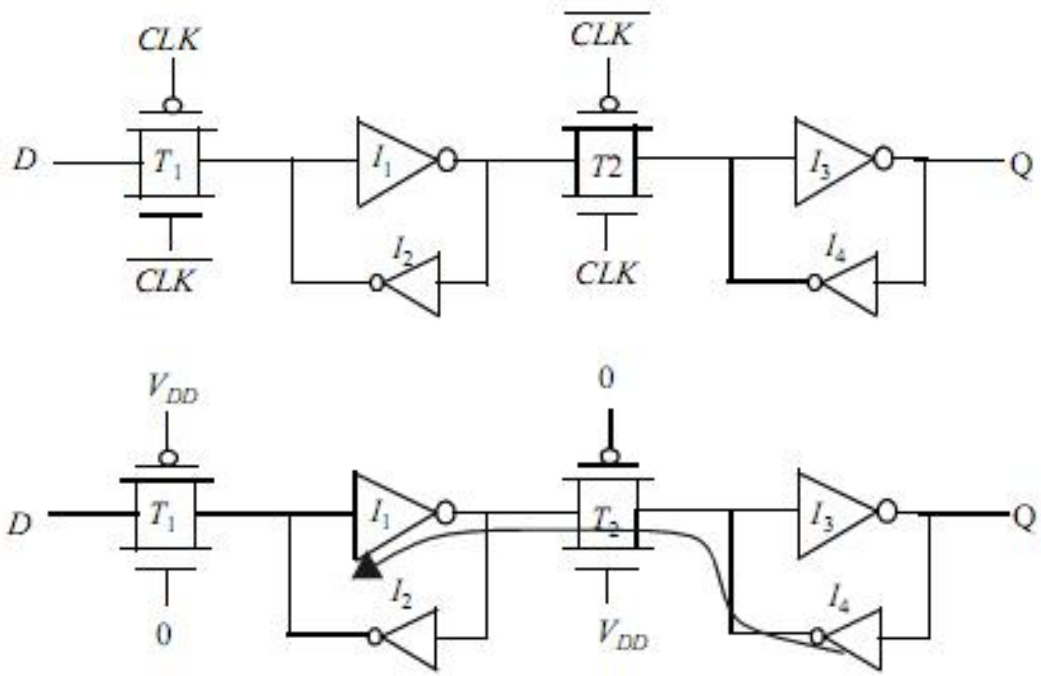
静态锁存器和寄存器

- 多路开关型主从寄存器的时序特性



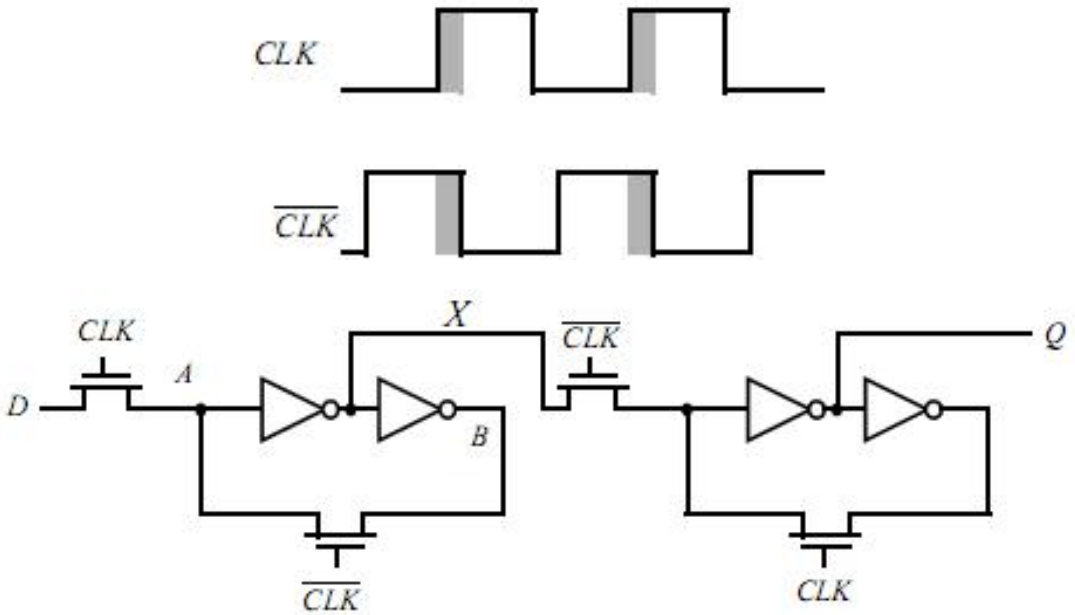
静态锁存器和寄存器

- 减少时钟负载的静态主从寄存器
  - 减少时钟驱动门的数目
  - 导致有比电路
  - 反向传导影响



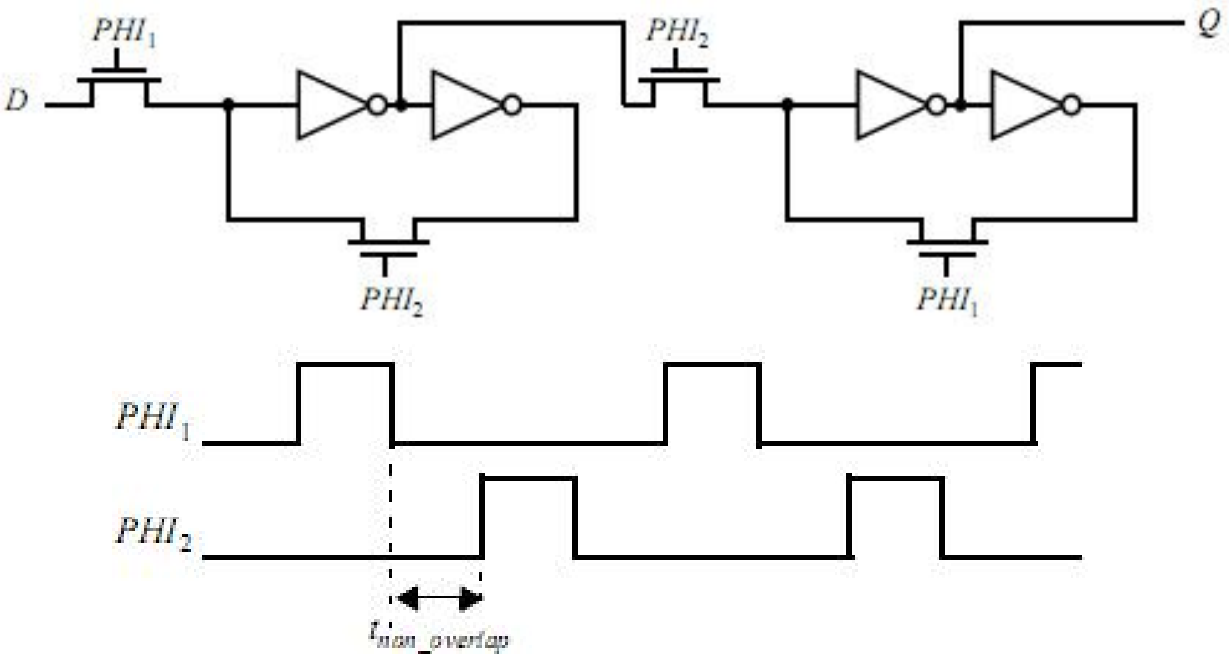
静态锁存器和寄存器

- 非理想时钟信号
- *CLK* 和 $\overline{CLK}$ 存在同时为高电平和低电平的时间
  - 时钟重叠期主从锁存器同时导通
  - 寄存器内部节点A处于不稳定状态



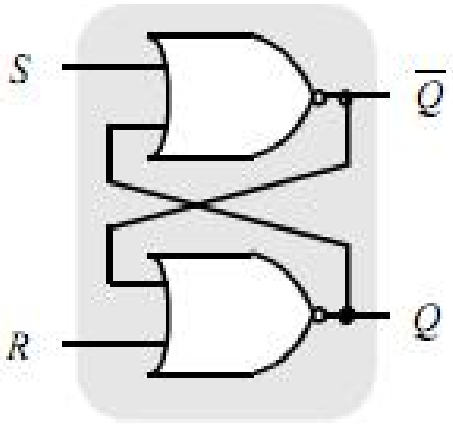
静态锁存器和寄存器

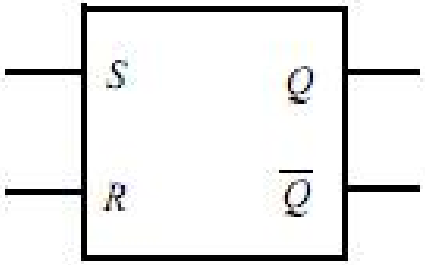
- 两相不重叠时钟
- CLK 和 $\overline{CLK}$ 不存在同时为高电平的时间



静态锁存器和寄存器

- 静态SR触发器
  - NOR代替双稳态电路中的反相器



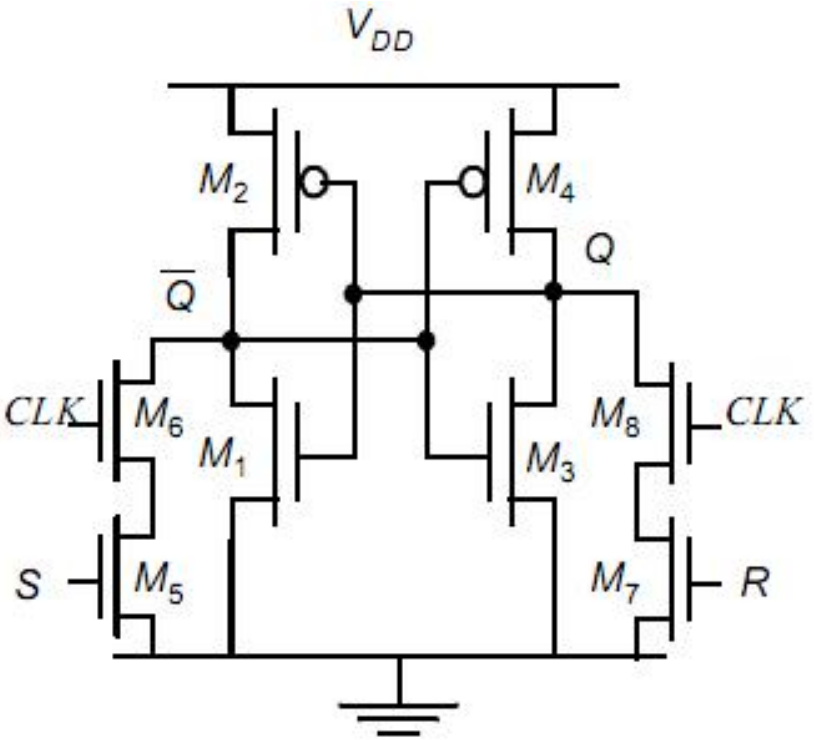


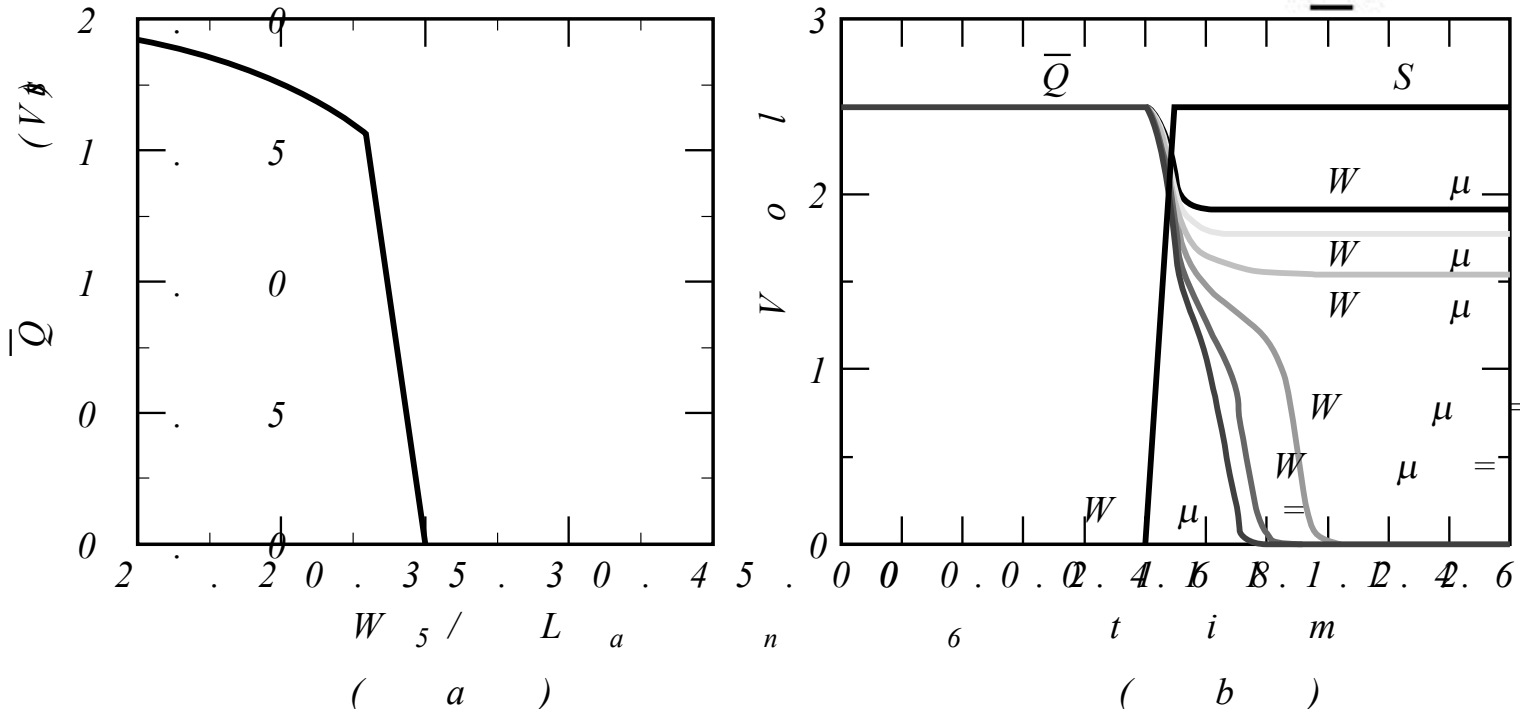
S	R	Q	$\overline{Q}$
0	0	Q	$\overline{Q}$
1	0	1	0
0	1	0	1
1	1	0	0

禁止状态

静态锁存器和寄存器

- CMOS时钟SR触发器
  - 用时钟同步SR触发器



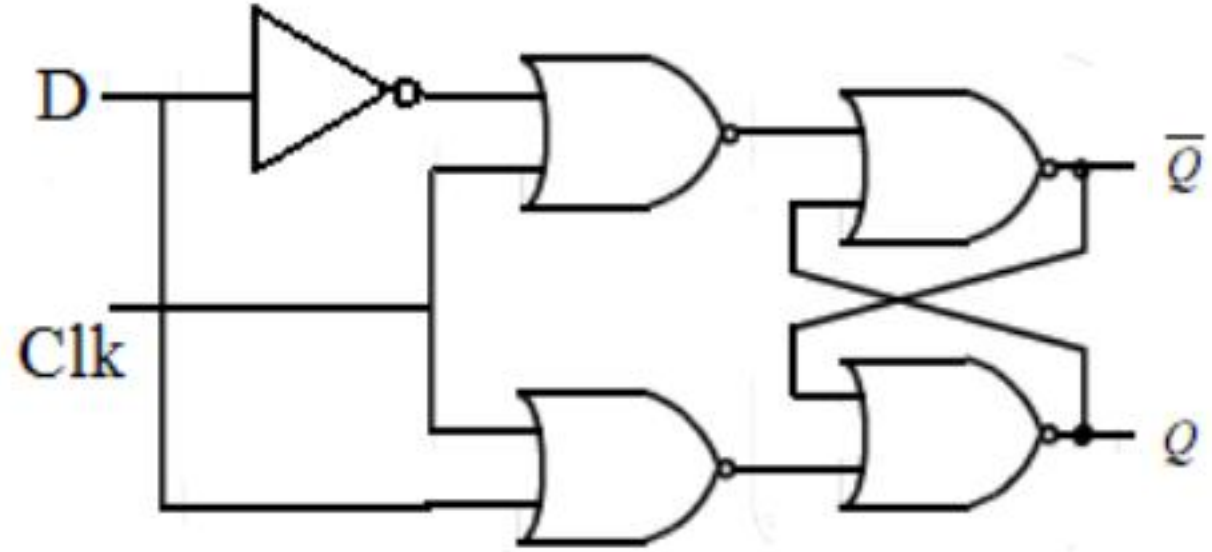


静态锁存器和寄存器

- D触发器

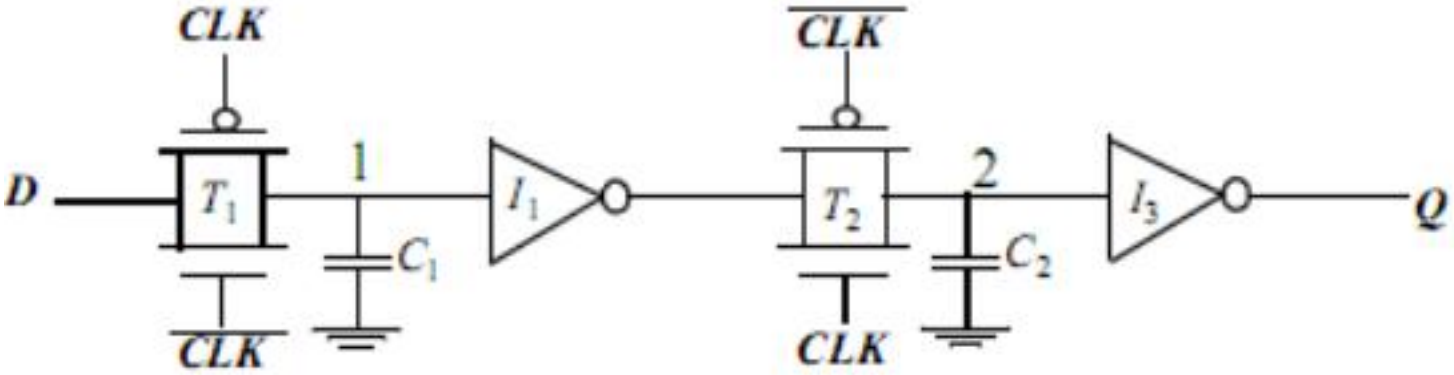
S	R	Q	$\overline{Q}$
0	0	Q	$\overline{Q}$
1	0	1	0
0	1	0	1
1	1	0	0

禁止状态



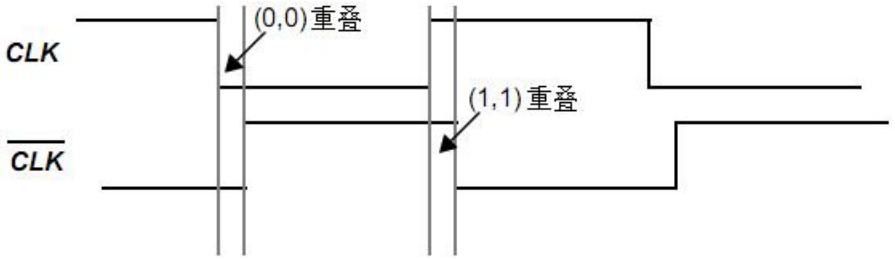
动态锁存器和寄存器

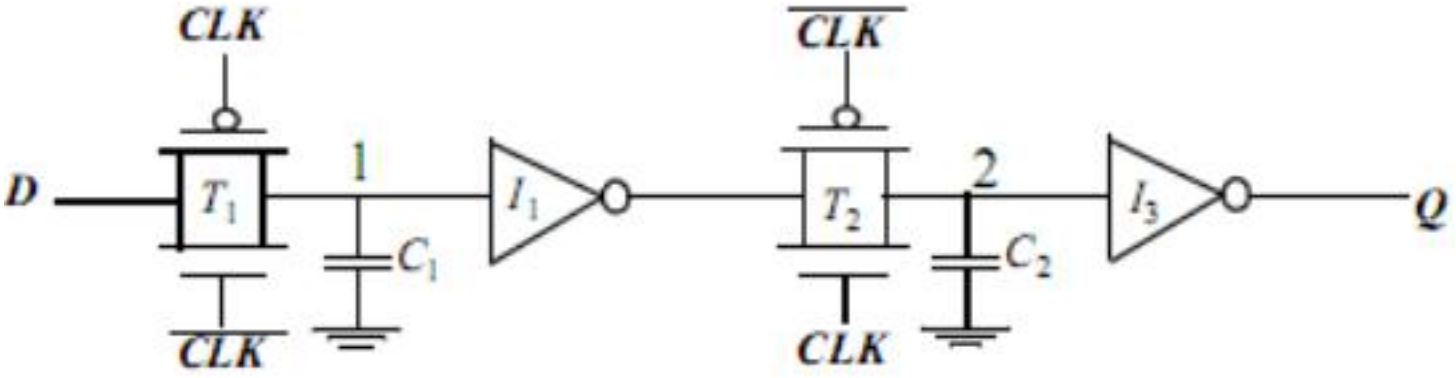
- 动态边沿触发寄存器
  - 中间节点状态需要周期刷新
  - 8个晶体管
  - 寄存器传播延时：$t_{c-q} = t_{I1} + t_{T2} + t_{I3}$
  - 受时钟重叠影响



动态锁存器和寄存器

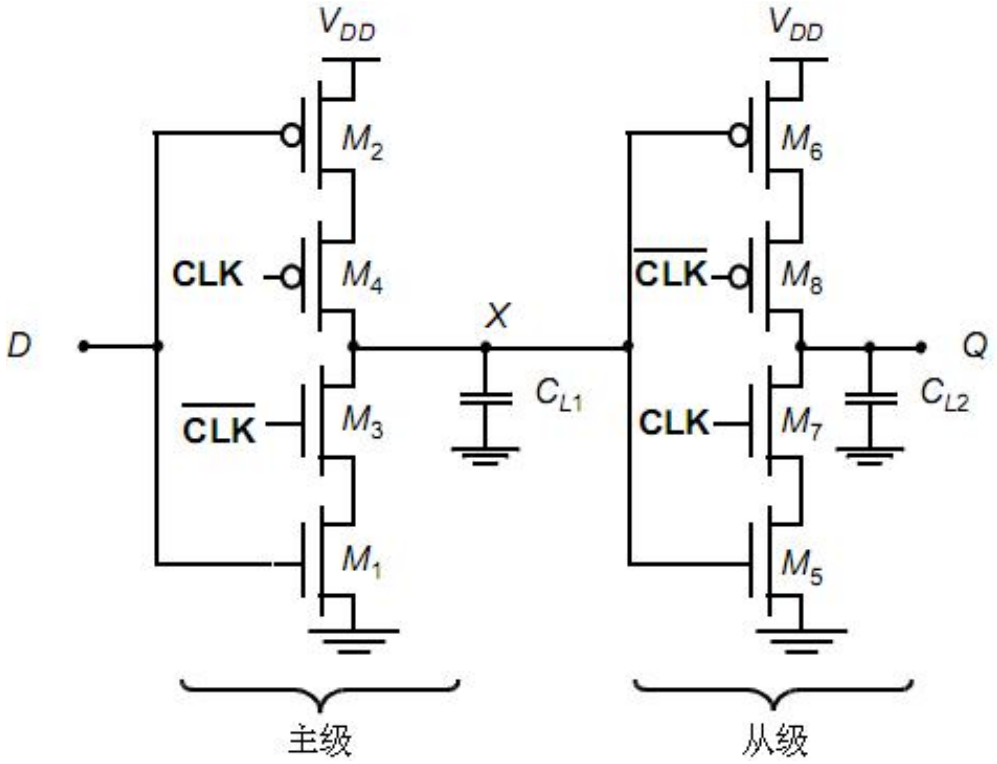
- 动态边沿触发寄存器的时钟重叠影响考虑
  - 1-1重叠
    - 确保充分的输入维持时间 $t_{hold} > t_{overlap1-1}$
  - 0-0重叠
    - $t_{overlap0-0} = t_{T1} + t_{I1} + t_{T2}$





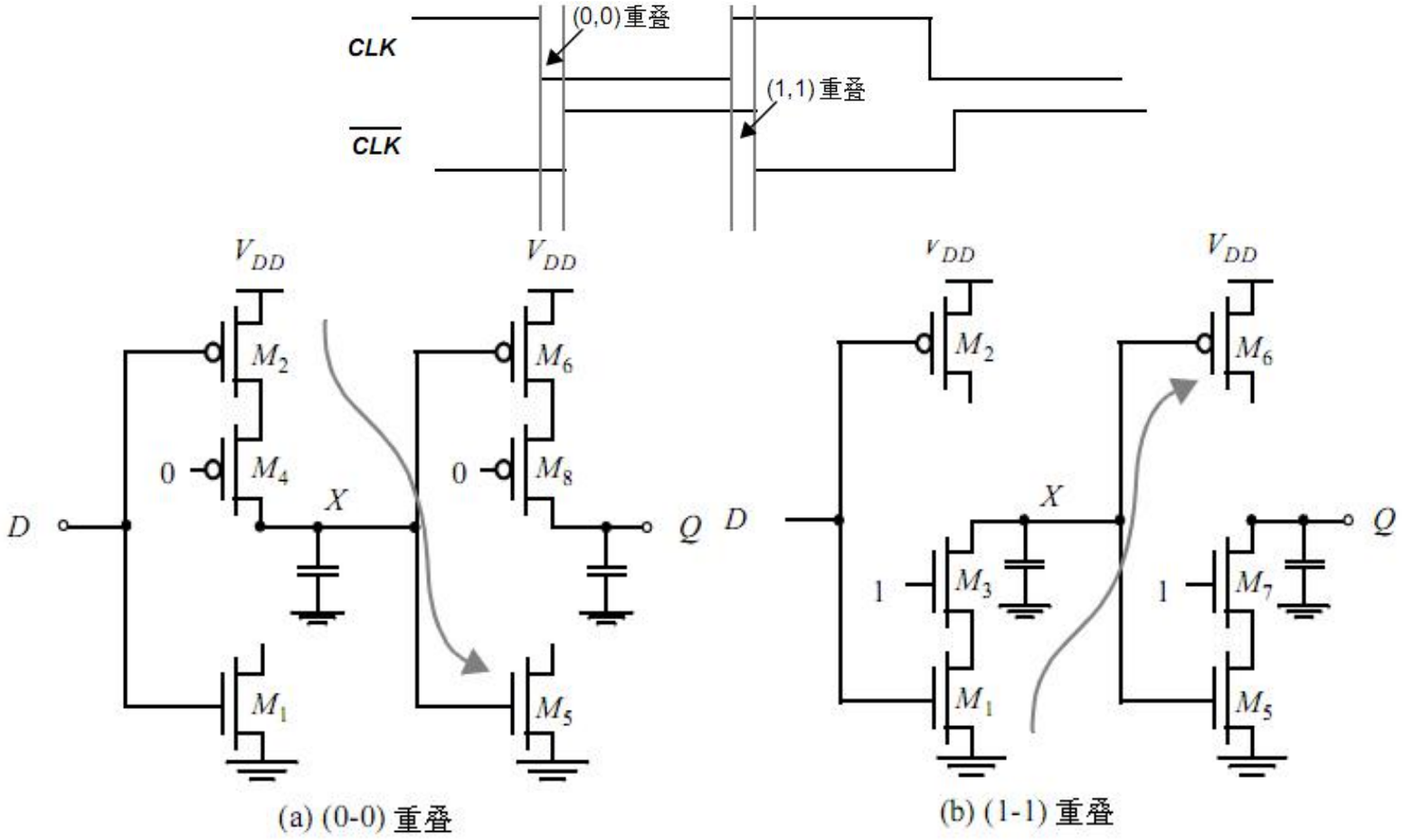
动态锁存器和寄存器

- 时钟控制CMOS寄存器（C²MOS）
  - 对时钟重叠不敏感的正沿触发器



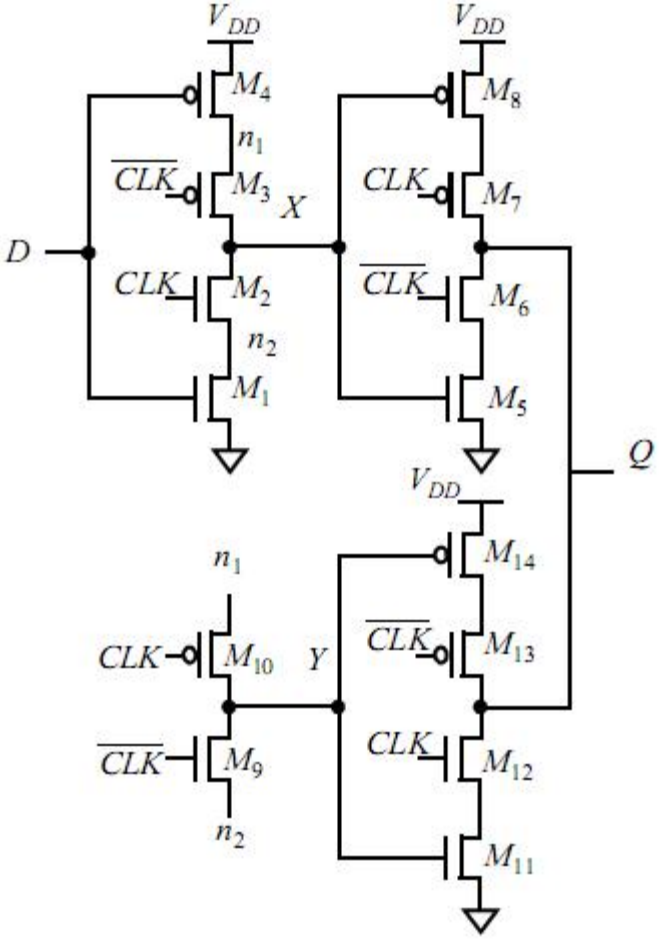
动态锁存器和寄存器

- 时钟控制CMOS寄存器（C²MOS）



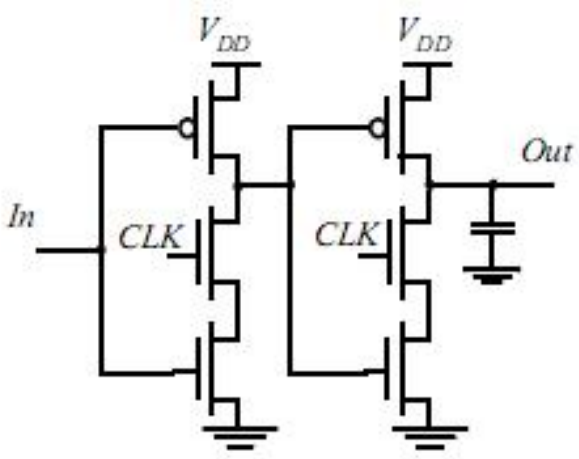
动态锁存器和寄存器

- 基于C²MOS的双边沿寄存器
  - 处理同样的数据

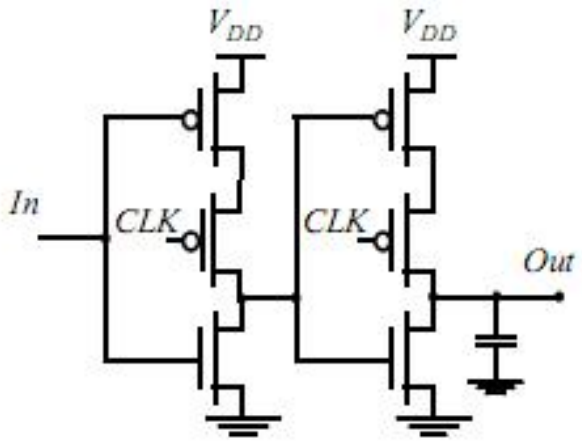


动态锁存器和寄存器

- 真单向钟控寄存器（TSPCR）
  - 优点：只用单相位时钟
  - 缺点：晶体管数目增加



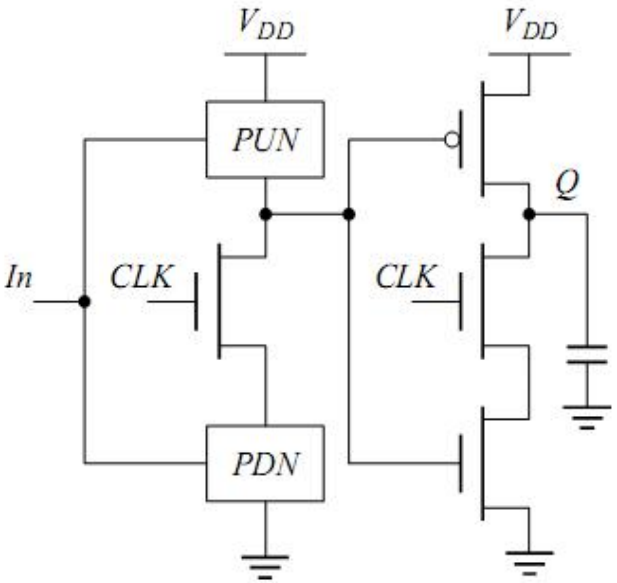
正锁存器



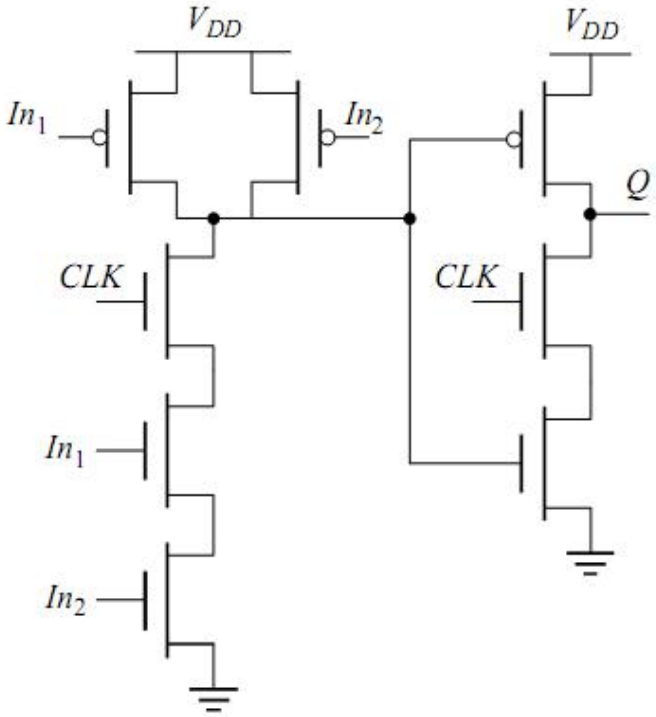
负锁存器

动态锁存器和寄存器

- 真单向钟控寄存器（TSPCR）
  - 锁存器中可嵌入逻辑单元



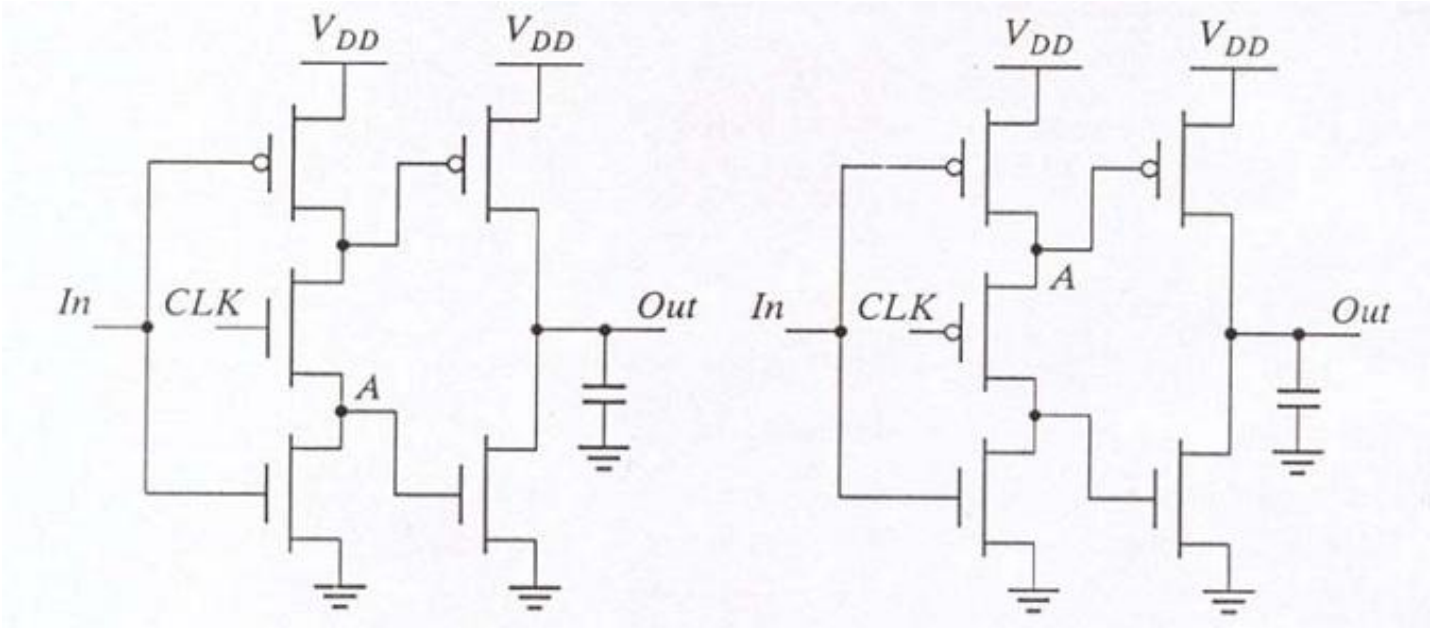
嵌入逻辑的锁存器



AND锁存器

动态锁存器和寄存器

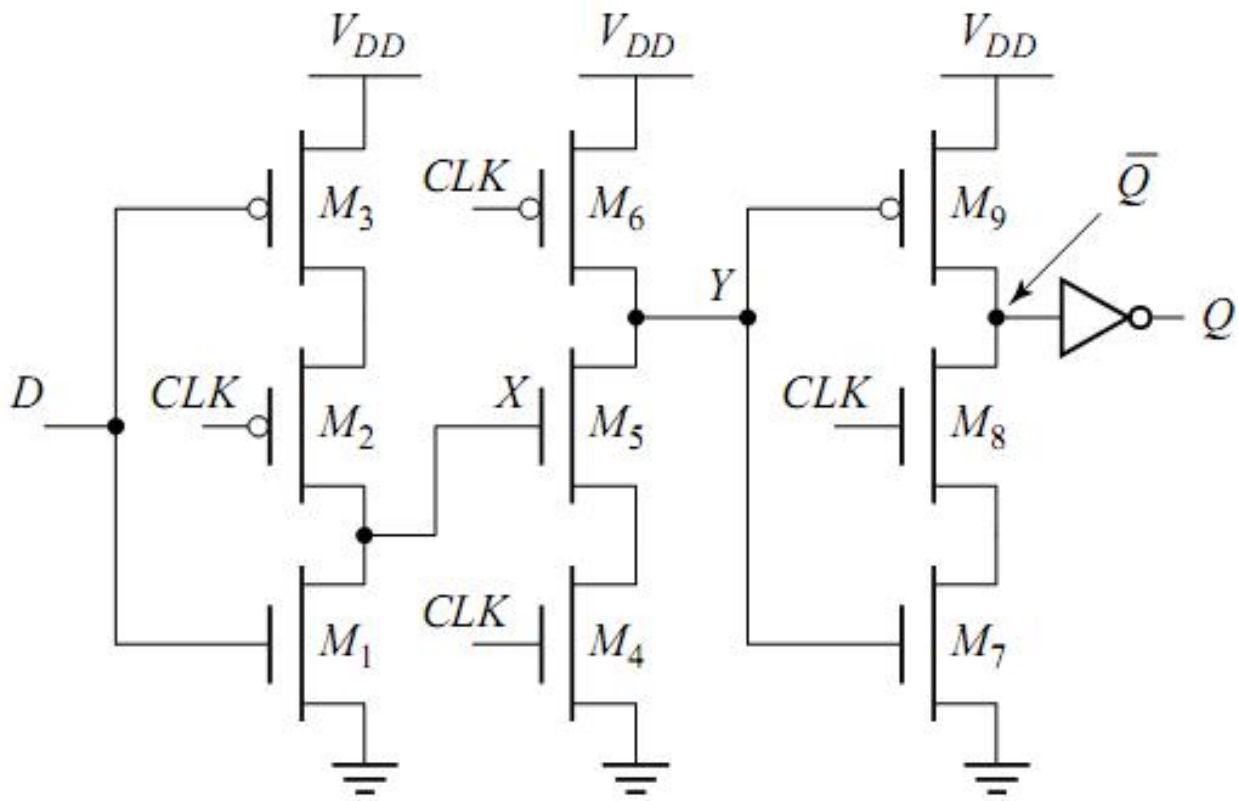
- 简化的真单向钟控寄存器（TSPCR）
  - 优点：晶体管数目减少，时钟数目也减少了
  - 缺点：内部节点不是全摆幅



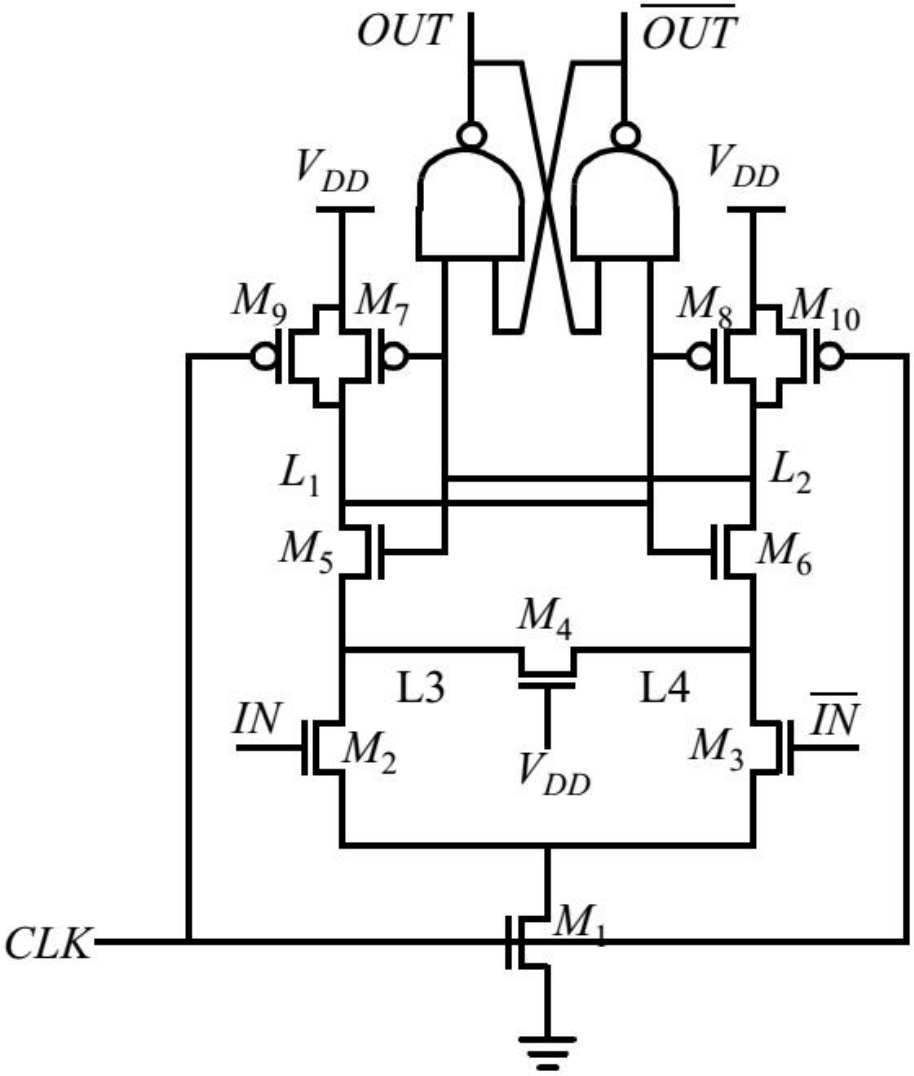
正锁存器　　负锁存器

动态锁存器和寄存器

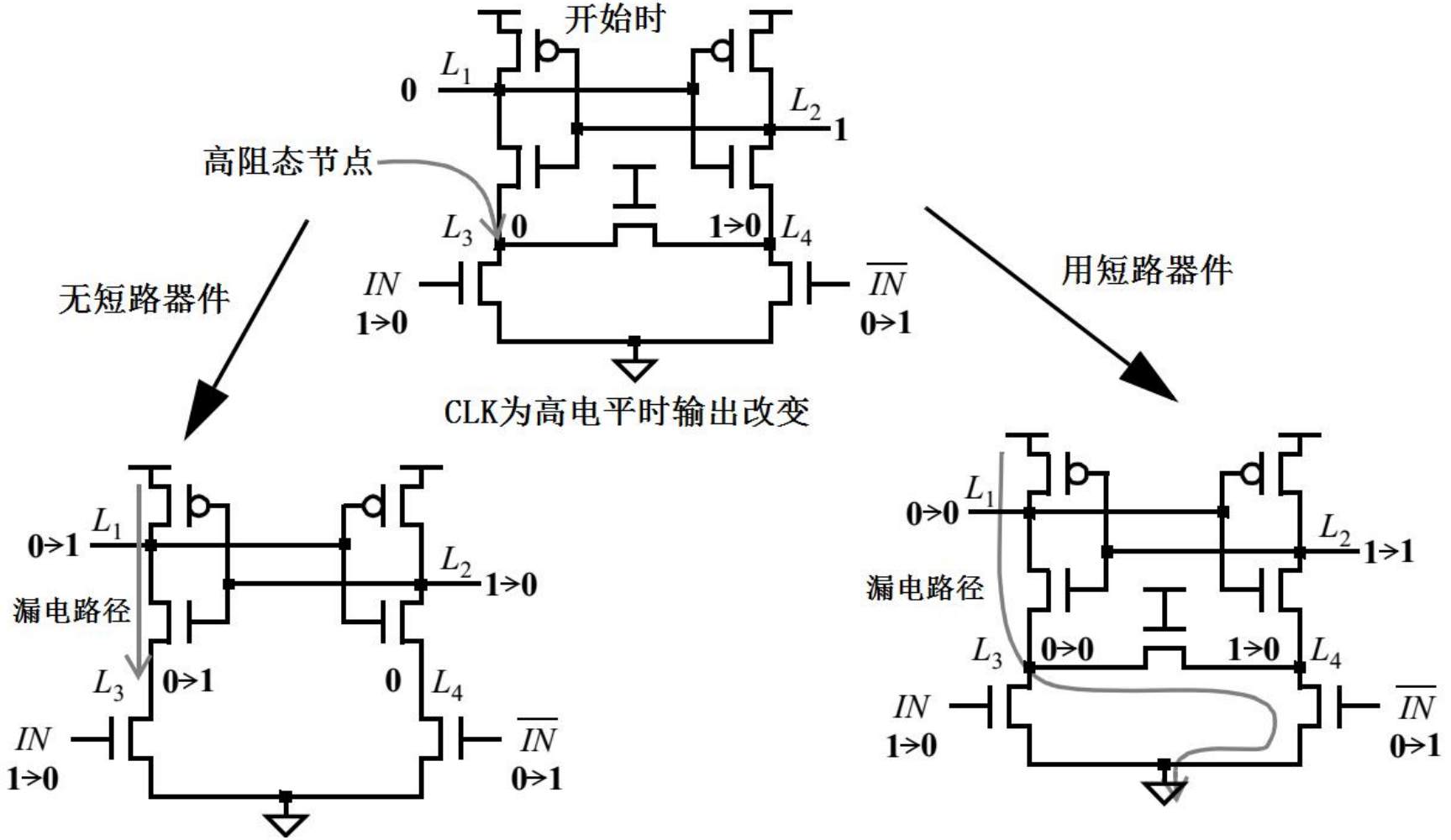
- 动态电路构成的真单向钟控寄存器（TSPCR）



灵敏放大器型寄存器

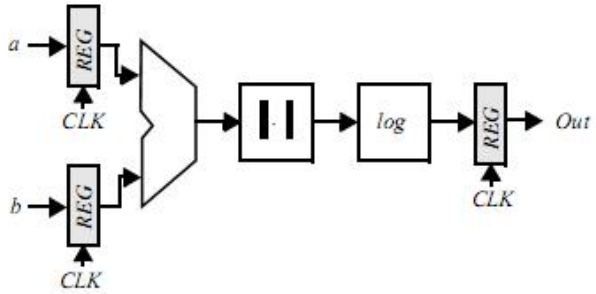

OUT
$\overline{OUT}$
V_{DD}
V_{DD}
M_9
M_7
M_8
M_{10}
L_1
L_2
M_5
M_6
M_4
L3
L4
IN
M_2
V_{DD}
M_3
$\overline{IN}$
CLK
M_1

灵敏放大器型寄存器

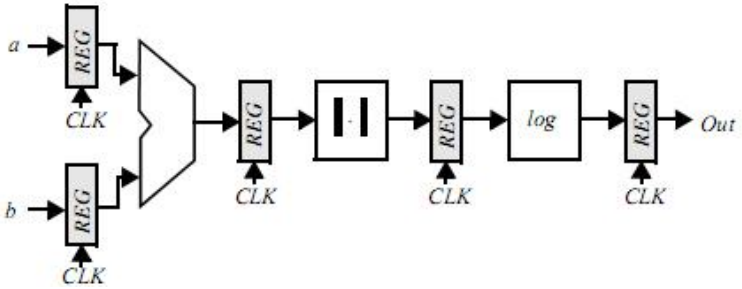

开始时
0
L_1
L_2
1
高阻态节点
L_3
0
1→0
L_4
IN
1→0
$\overline{IN}$
0→1
CLK为高电平时输出改变
无短路器件
用短路器件
0→1
L_1
L_2
1→0
漏电路径
L_3
0→1
0
L_4
IN
1→0
$\overline{IN}$
0→1
0→0
L_1
L_2
1→1
漏电路径
L_3
0→0
1→0
L_4
IN
1→0
$\overline{IN}$
0→1

流水线

- 时钟周期：$T_{min}=t_{c-q}+t_{plogic}+t_{su}$
- 流水线例子：log(|a+b|)
  - $T_{min}=t_{c-q}+max(t_{padd}, t_{pabs}, t_{plog})+t_{su}$

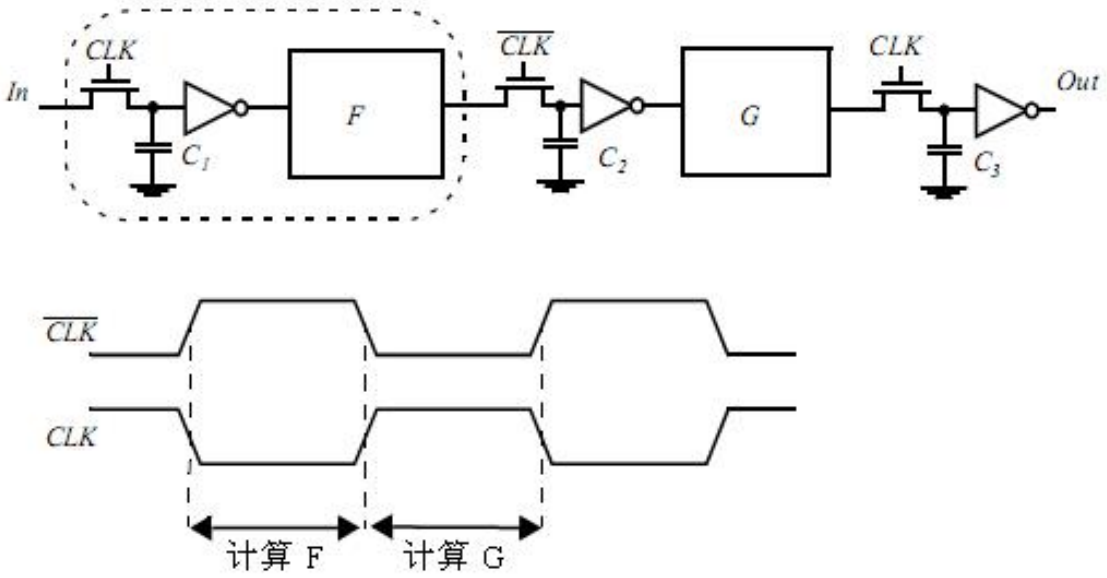


Clock Period	Adder	Absolute Value	Logarithm
1	a_1+b_1		
2	a_2+b_2	$\|a_1+b_1\|$	
3	a_3+b_3	$\|a_2+b_2\|$	$\log(\|a_1+b_1\|)$
4	a_4+b_4	$\|a_3+b_3\|$	$\log(\|a_2+b_2\|)$
5	a_5+b_5	$\|a_4+b_4\|$	$\log(\|a_3+b_3\|)$



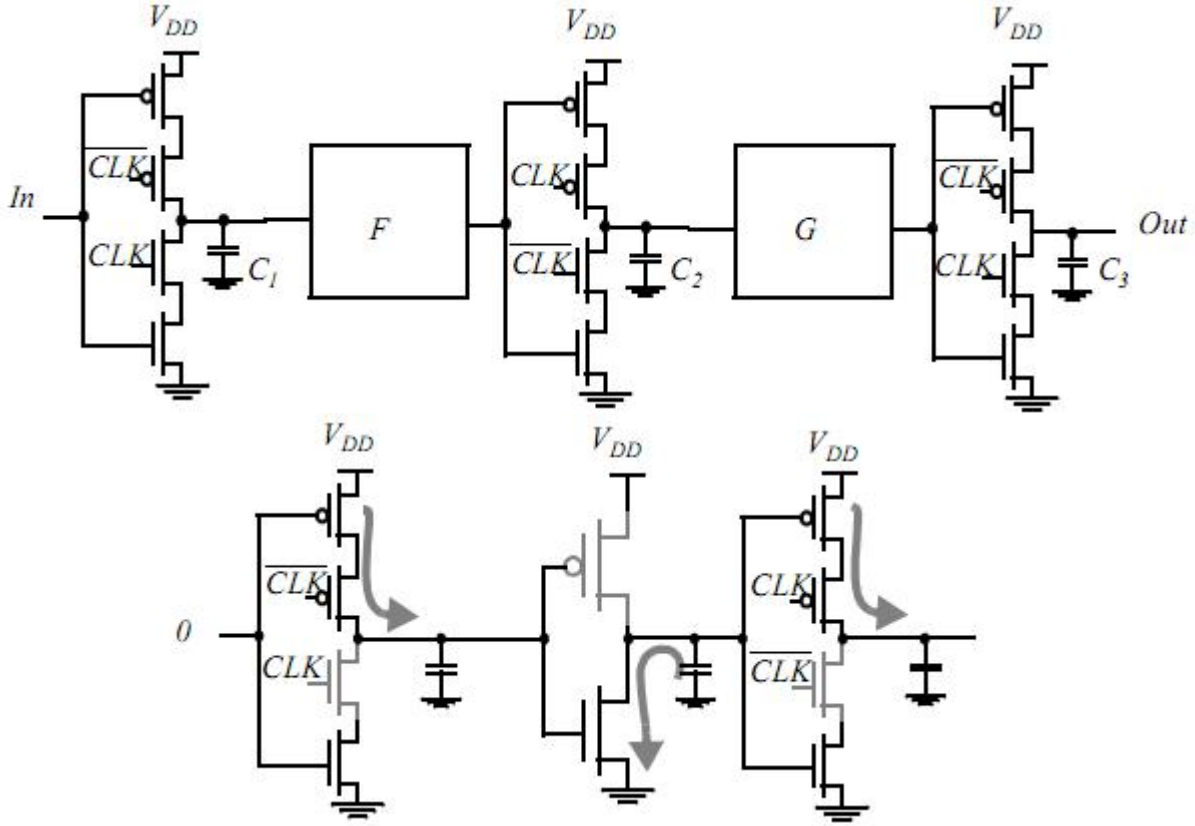
流水线

- 锁存器型流水线和寄存器型流水线



流水线

- 无竞争CMOS（NORA-CMOS）流水线结构
  - 只要锁存器之间的所有逻辑功能块输出非反向，CMOS的流水线电路即是无竞争的。

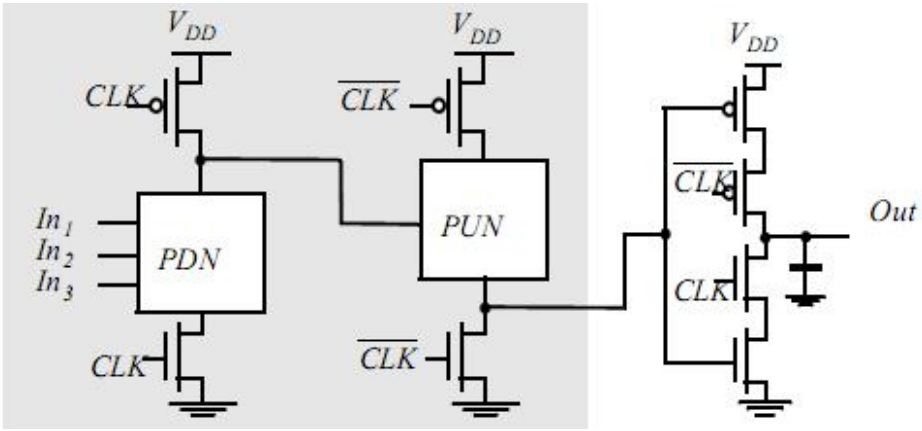


流水线

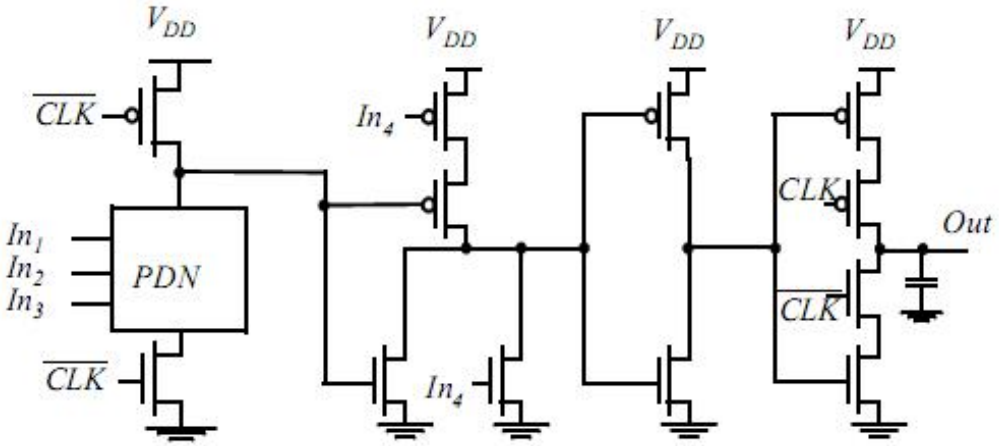
	CLK 模块		$\overline{CLK}$ 模块	
	逻辑	锁存器	逻辑	锁存器
$CLK = 0$	预充电	维持	求值	求值
$CLK = 1$	求值	求值	预充电	维持

- 无竞争CMOS（NORA-CMOS）流水线结构

CLK 模块

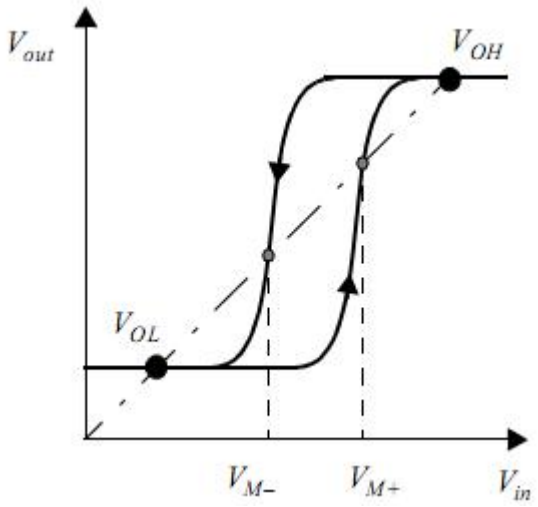


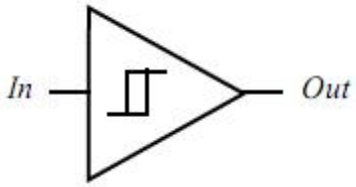
$\overline{CLK}$模块



非双稳态时序电路

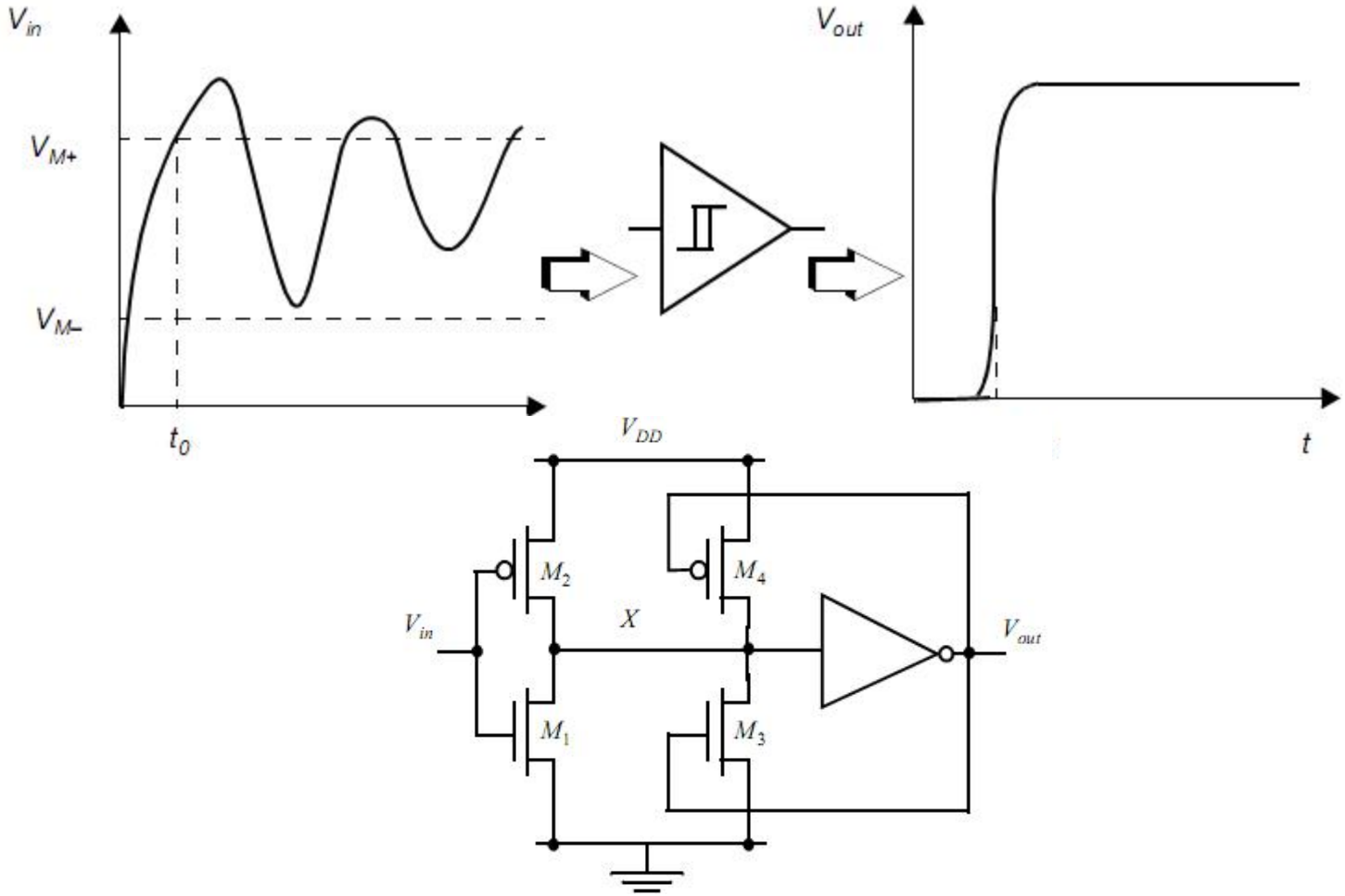
- 施密特触发器
  - 对于一个变换很慢的输入波形，在输出端有一个快速翻转的响应
  - 正向和负向变换的输入信号有不同的开关阈值





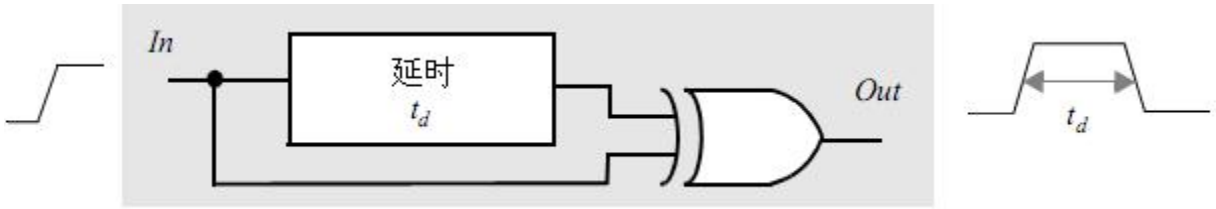
非双稳态时序电路

- 施密特触发器



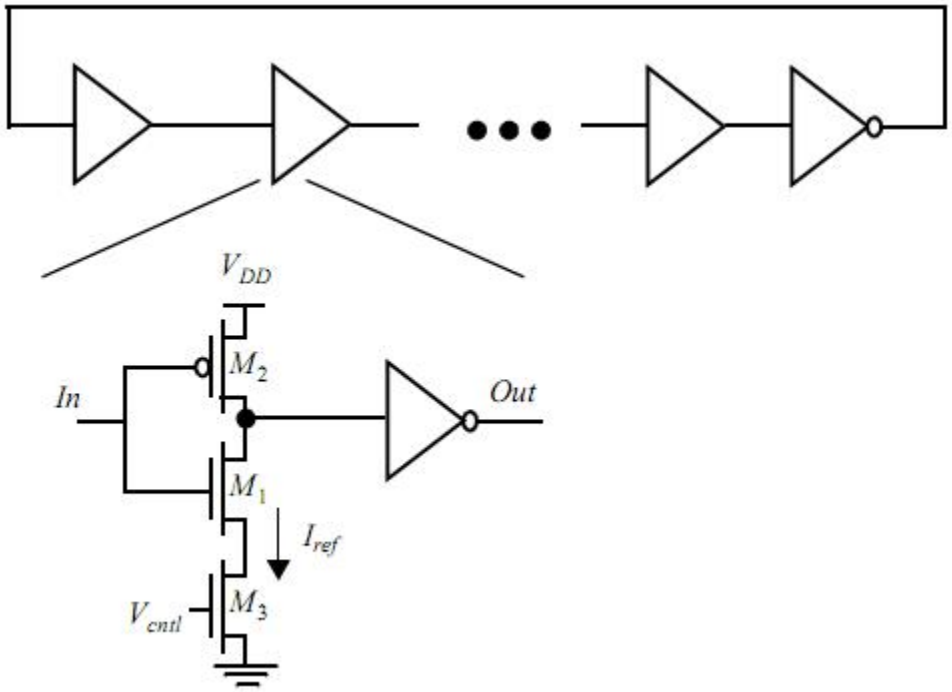
非双稳态时序电路

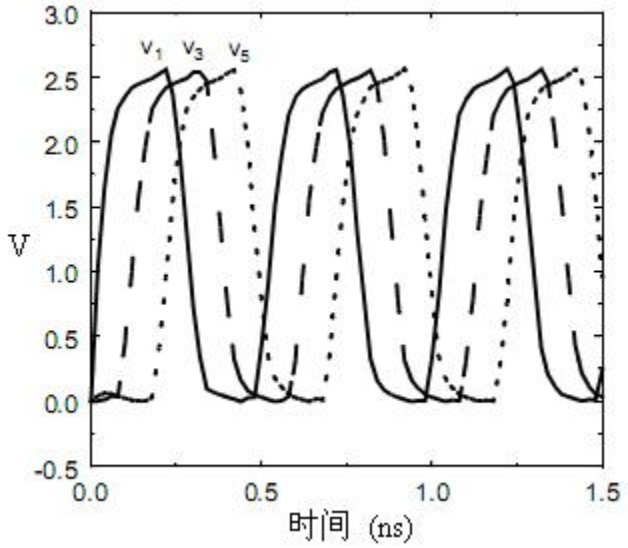
- 单稳时序电路
  - 只有一个稳定状态
  - 可产生脉冲电路



非双稳态时序电路

- 不稳时序电路
  - 不具有稳定状态
  - 输出在两个准稳态之间振荡



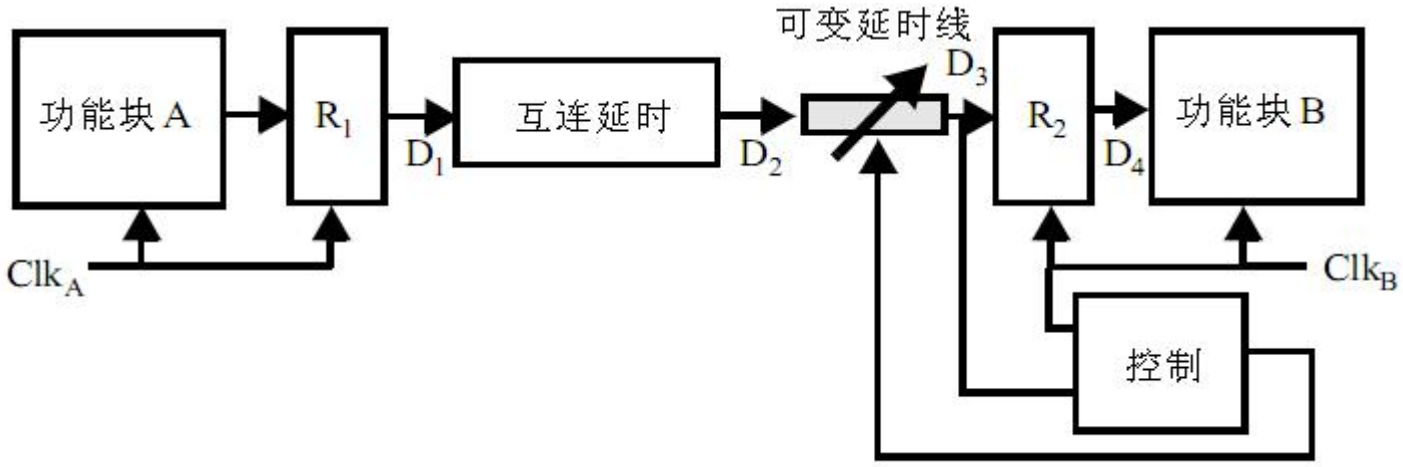


数字系统的时序分类

- 同步互连
  - 时钟信号频率相同
  - 相位差固定

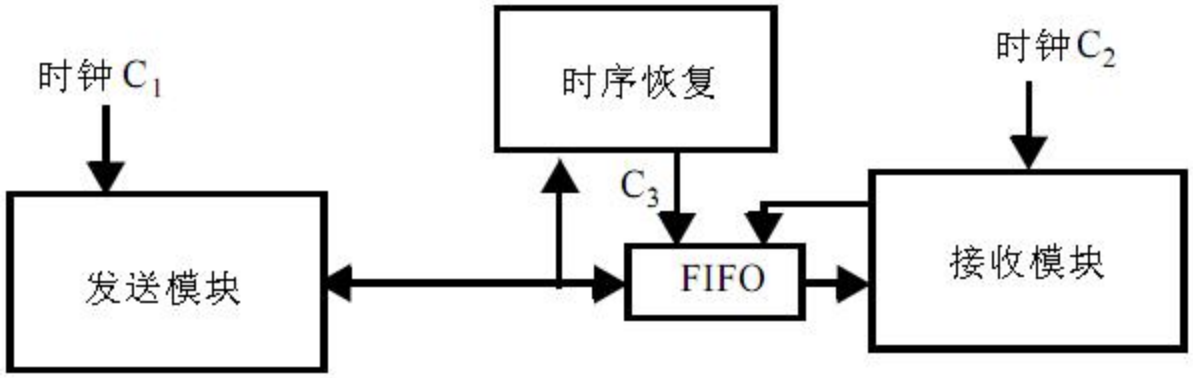
数字系统的时序分类

- 中等同步互连
  - 时钟信号频率相同
  - 相位差未知



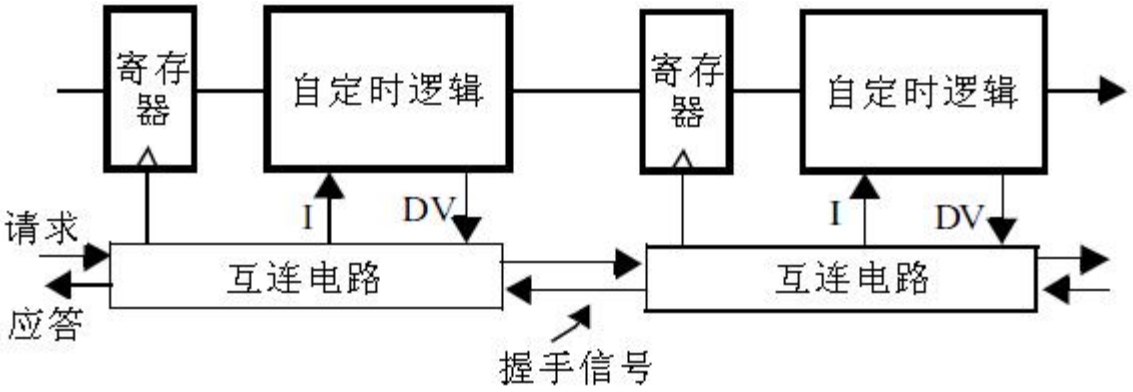
数字系统的时序分类

- 近似同步互连
  - 时钟信号频率稍有不同
  - 相位差未知



数字系统的时序分类

- 异步互连
  - 异步信号可以在任何时刻变化

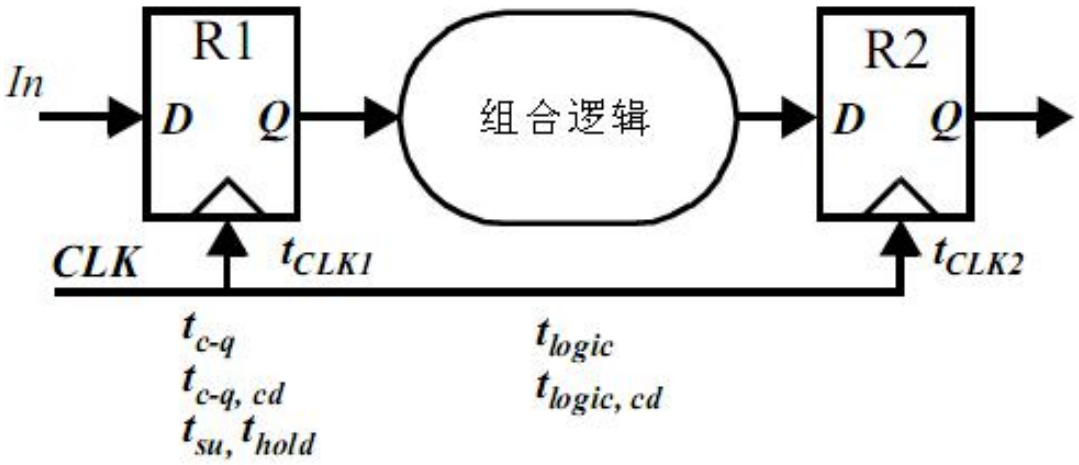


同步设计

- 同步时序原理
  - 理想时钟约束

$T > t_{c\text{-}q} + t_{plogic} + t_{su}$

$t_{hold} < t_{cdregister} + t_{cdlogic}$



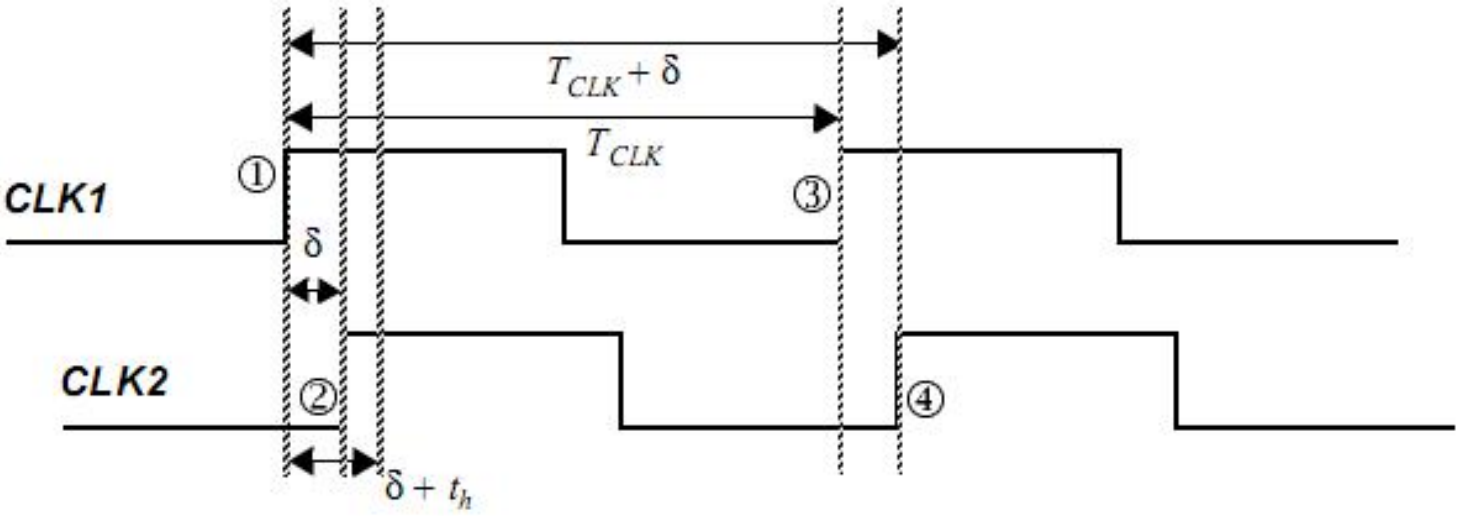
同步设计

- 时钟偏差
  - 一个时钟翻转的到达时间在空间相位上的差别

$\delta(R1, R2)= t_{R2}-t_{R1}$

$T+\delta > t_{c\text{-}q}+t_{plogic}+t_{su}$ 或 $T > t_{c\text{-}q}+t_{plogic}+t_{su}-\delta$

$t_{hold}+\delta < t_{cdregister}+t_{cdlogic}$ 或 $t_{hold} < t_{cdregister}+t_{cdlogic}-\delta$

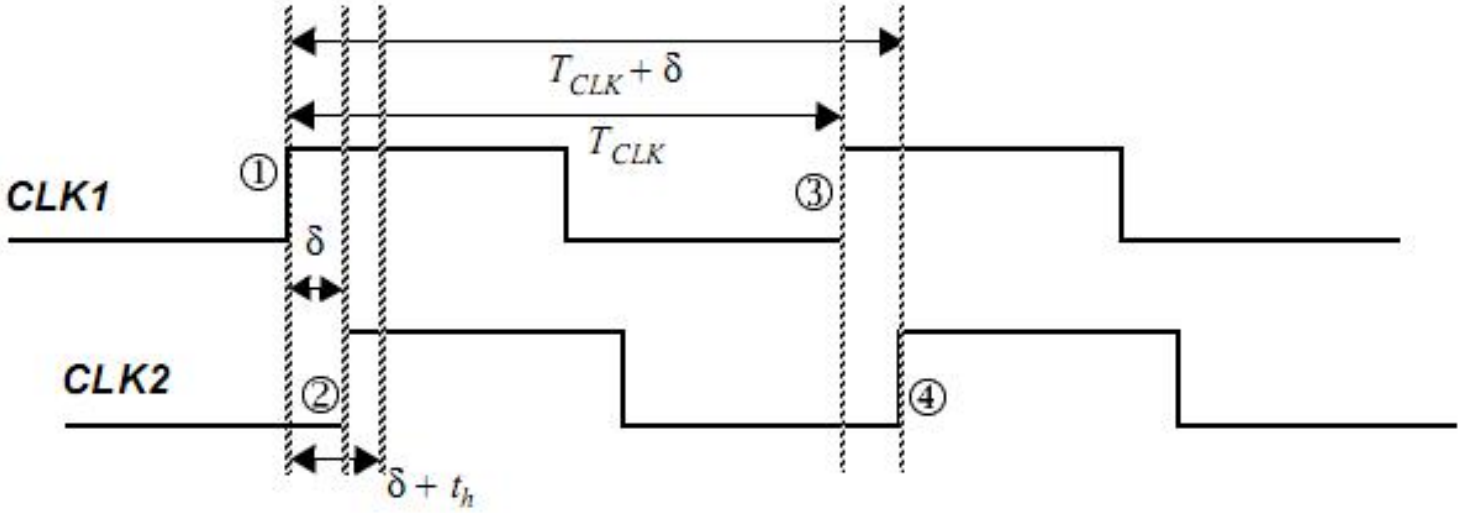


同步设计

- 时钟偏差
  - 时钟正偏差 $\delta>0$

$$T+\delta > t_{c\text{-}q}+t_{plogic}+t_{su} \text{ 或 } T>t_{c\text{-}q}+t_{plogic}+t_{su}-\delta$$

$$t_{hold}+\delta < t_{cdregister}+t_{cdlogic} \text{ 或 } t_{hold} < t_{cdregister}+t_{cdlogic}-\delta$$



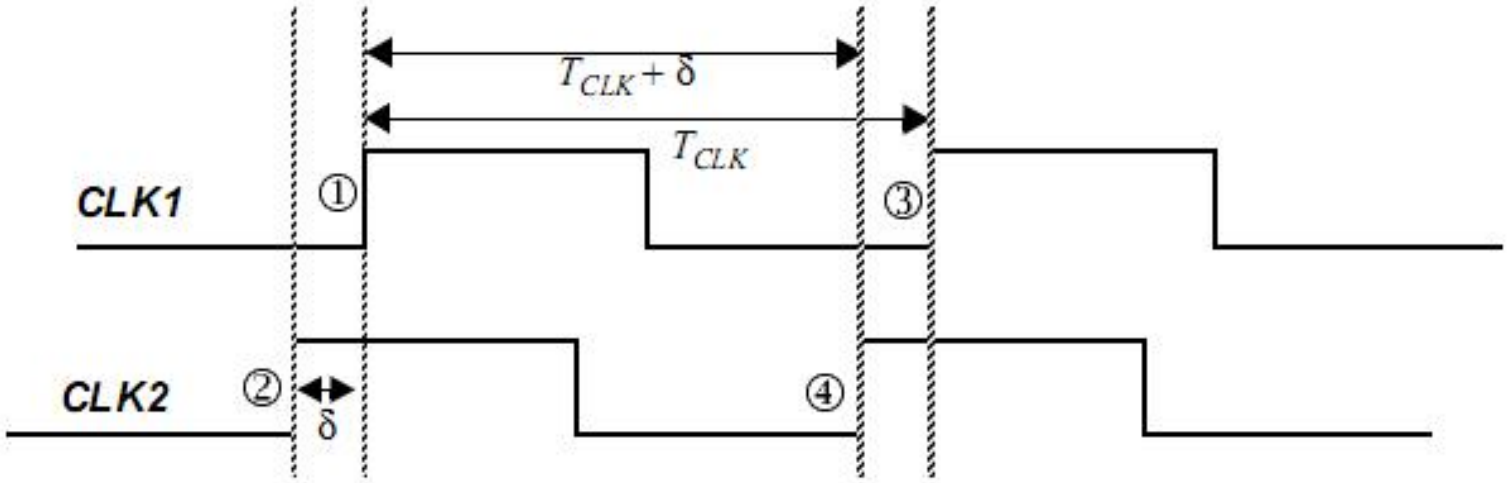
同步设计

- 时钟偏差
  - 时钟负偏差 $\delta<0$

    $\delta(R1, R2)= t_{R2}-t_{R1}$

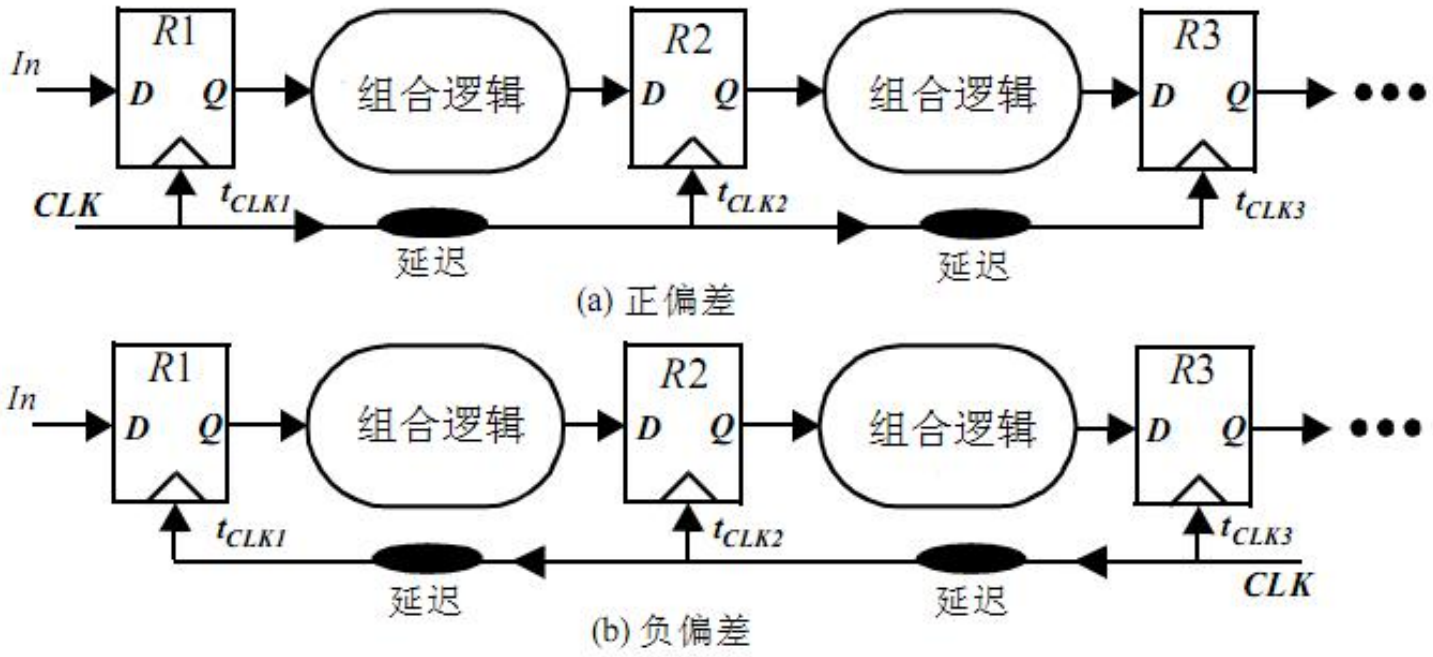
    $T+\delta > t_{c\text{-}q}+t_{plogic}+t_{su}$ 或 $T>t_{c\text{-}q}+t_{plogic}+t_{su}-\delta$

    $t_{hold}+\delta < t_{cdregister}+t_{cdlogic}$ 或 $t_{hold} < t_{cdregister}+t_{cdlogic}-\delta$



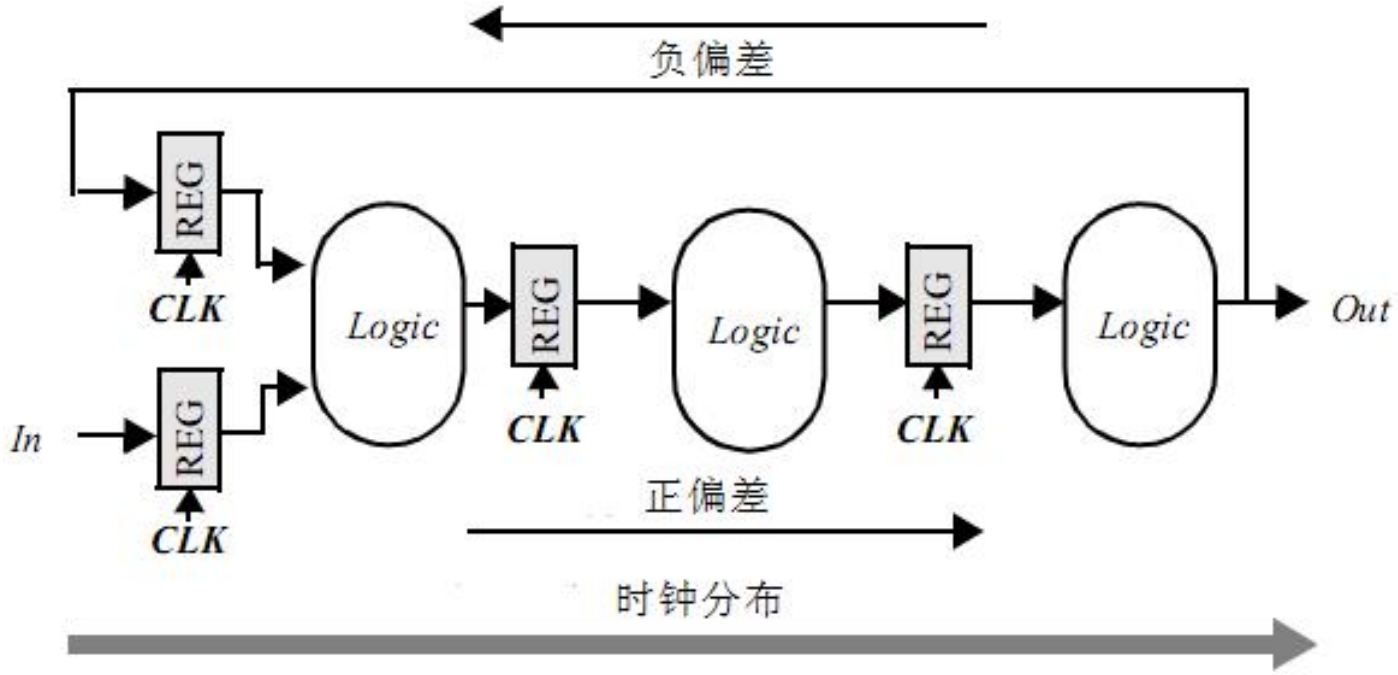
同步设计

- 时钟偏差
  - 时钟正负偏差共同存在



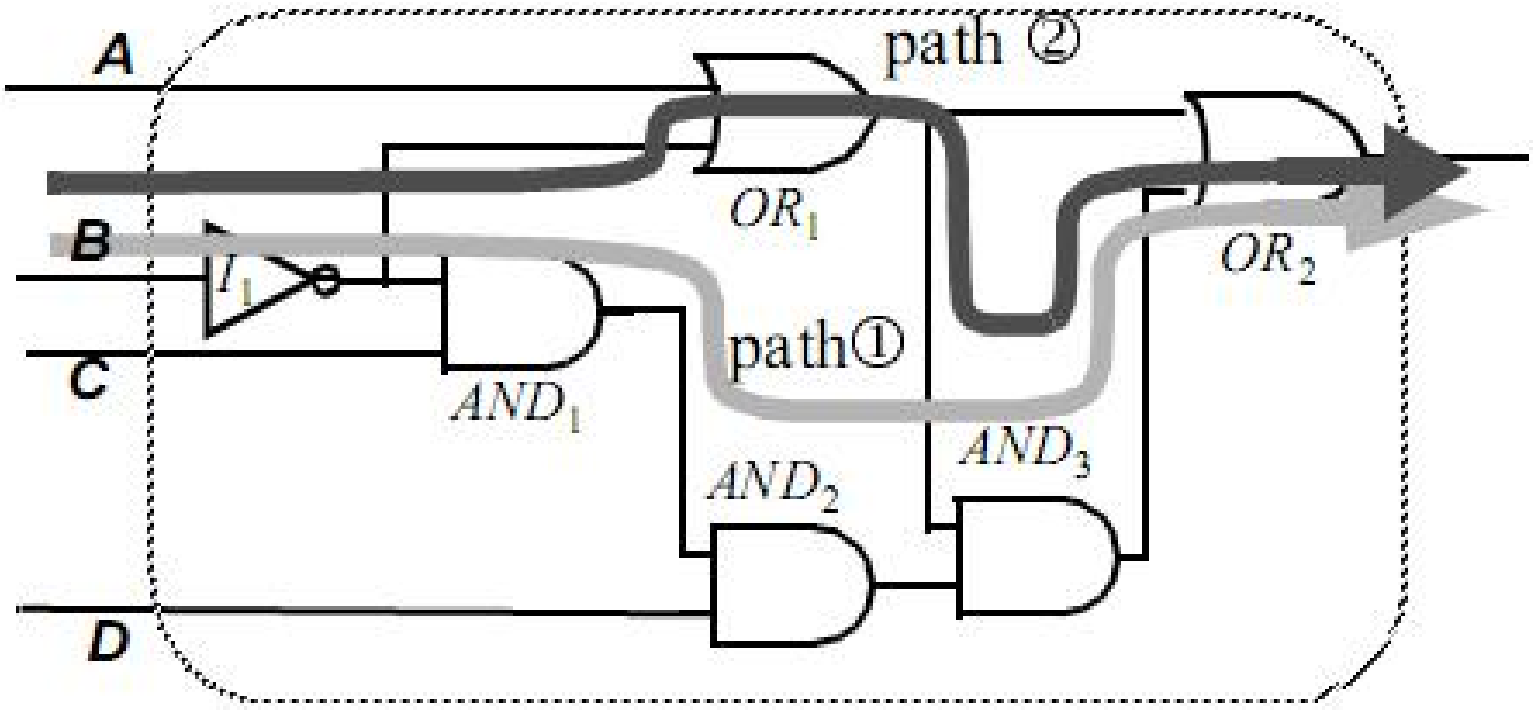
同步设计

- 时钟偏差
  - 时钟正负偏差共同存在

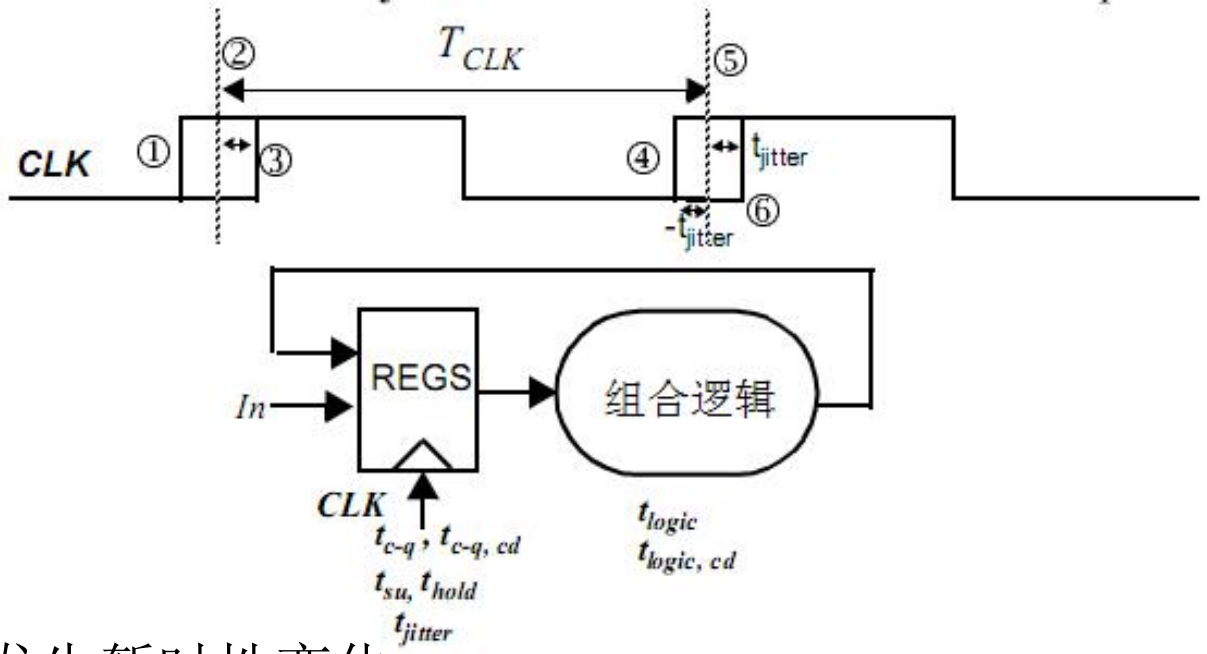


同步设计

- 电路的传播延时和污染延时



同步设计



- 时钟抖动
  - 某点上时钟周期发生暂时性变化
    - 绝对抖动
      - 给定位置处的时钟边沿相对于理想时钟边沿最坏情形下的偏差
    - 周期抖动
      - 单个时钟周期相对于理想参照时钟的时变偏差
      - 空间位置i的周期抖动 $T^{i}_{jitter}(n)=t^{i}_{clk,n+1}-t^{i}_{clk,n}-T_{CLK}$

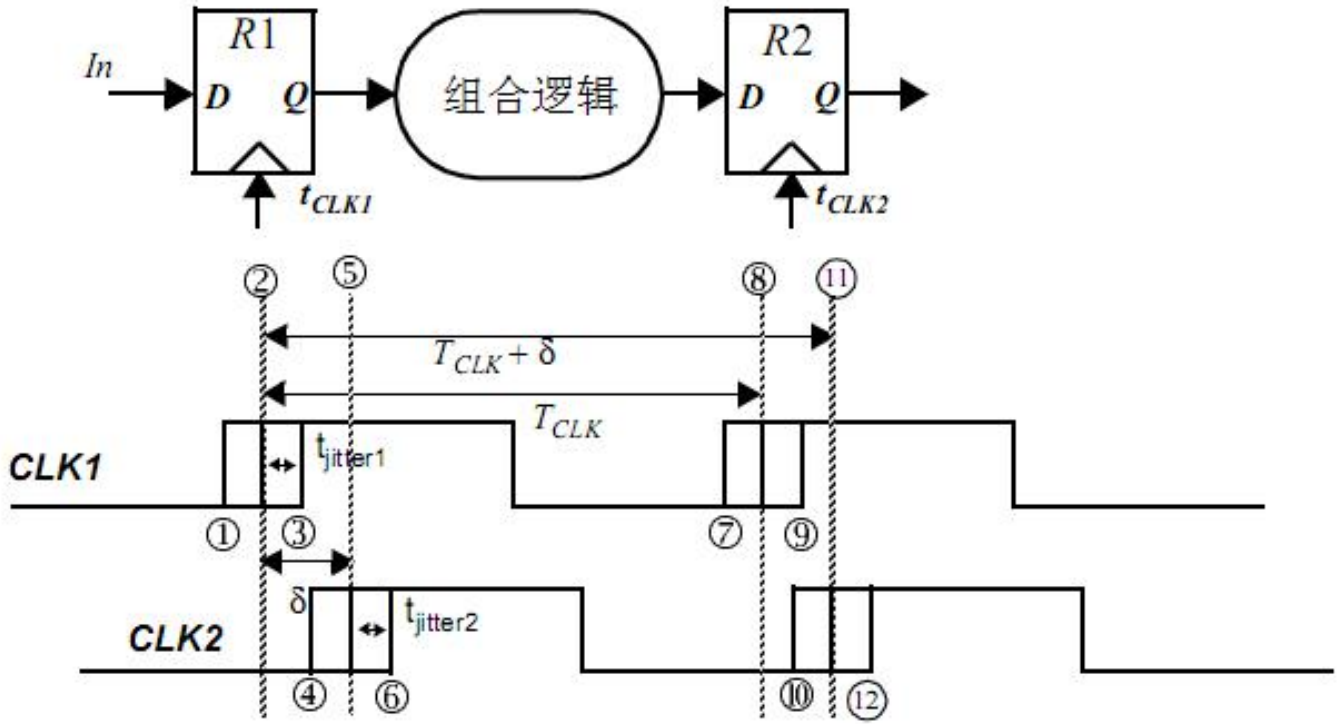
$T_{CLK}-2t_{jitter} > t_{c\text{-}q}+t_{plogic}+t_{su}$ 或 $T_{CLK} > t_{c\text{-}q}+t_{plogic}+t_{su}+2t_{jitter}$

同步设计

- 时钟偏差和抖动的共同影响

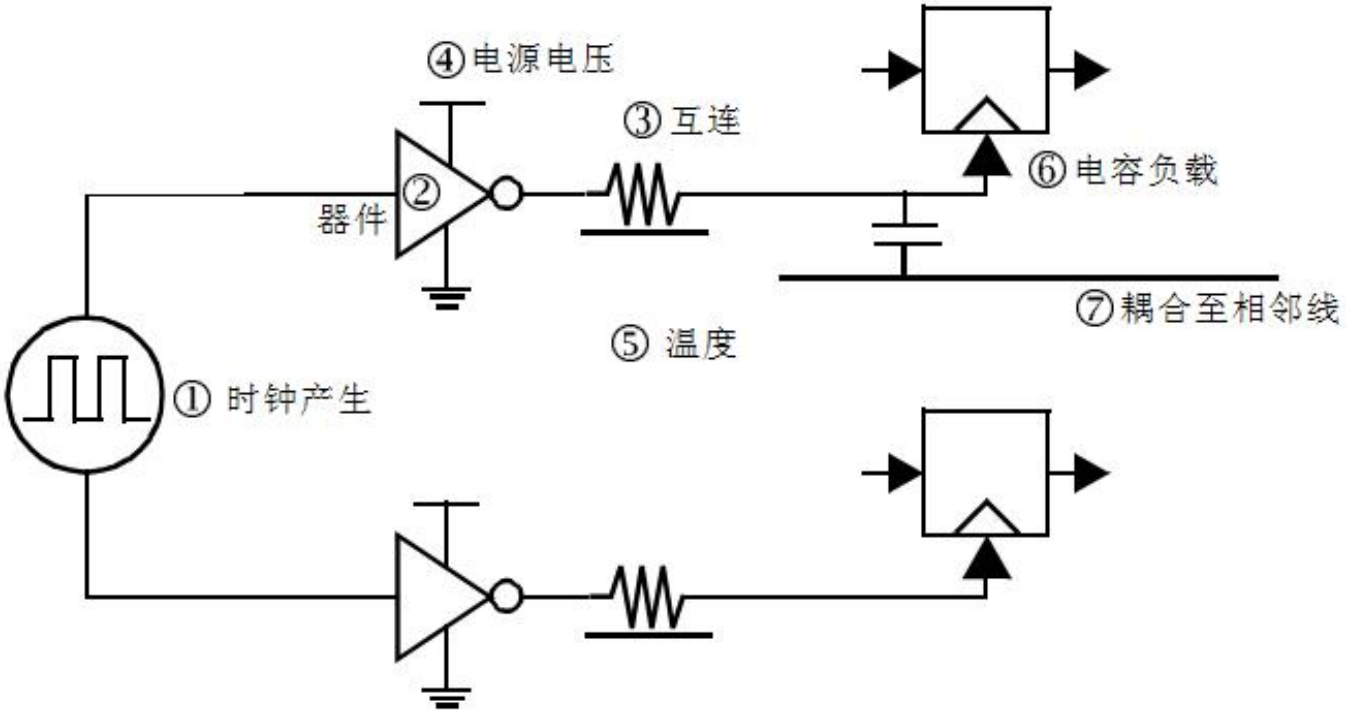
$T_{CLK}+\delta-2t_{jitter} > t_{c-q}+t_{plogic}+t_{su}$ 或 $T_{CLK} > t_{c-q}+t_{plogic}+t_{su}-\delta+2t_{jitter}$

$t_{hold}+\delta+2t_{jitter} < t_{cdregister}+t_{cdlogic}$ 或 $t_{hold} < t_{cdregister}+t_{cdlogic}-\delta-2t_{jitter}$



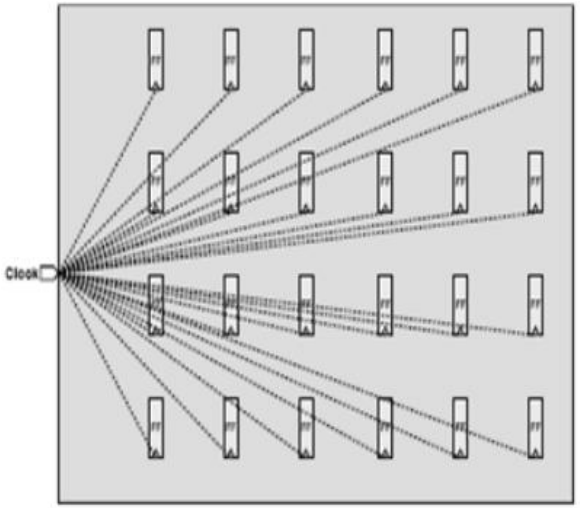
同步设计

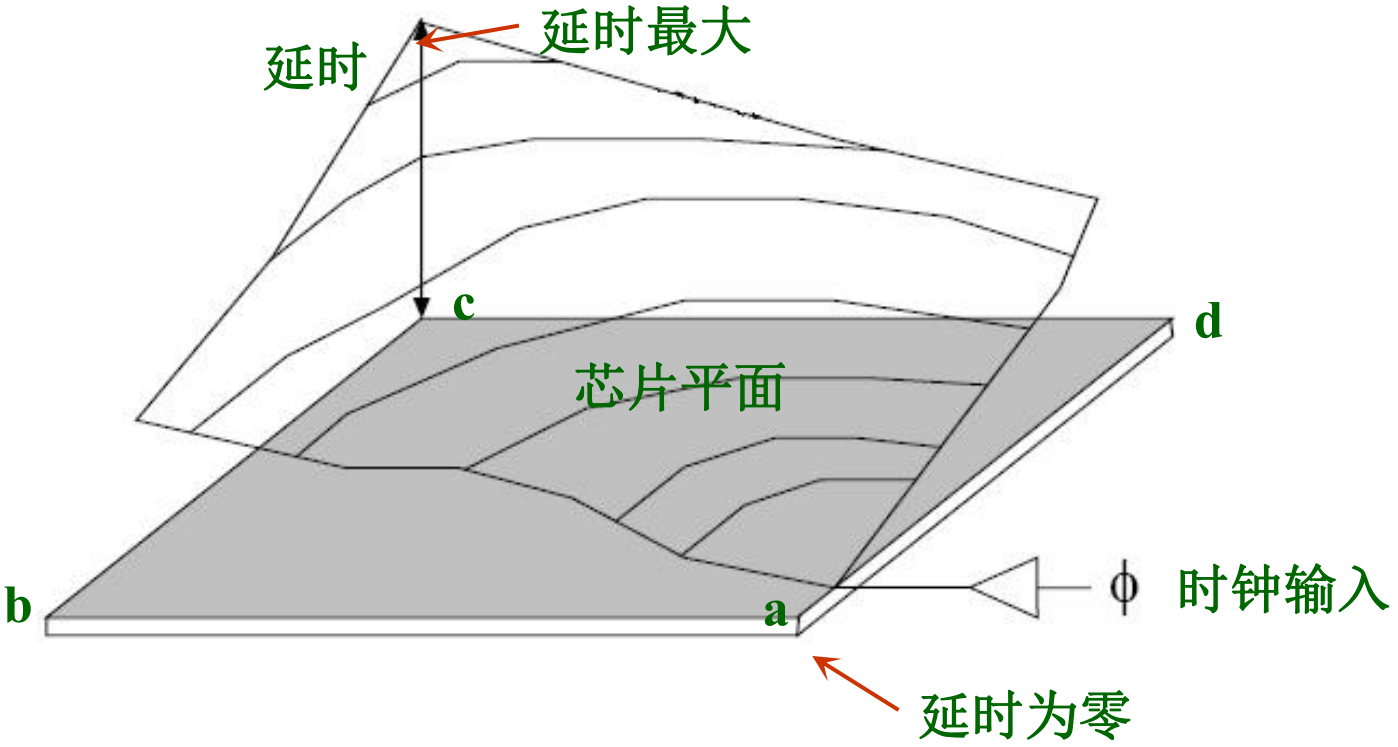
- 时钟偏差和抖动的来源
  - 时钟信号产生
  - 器件制造偏差
  - 互连偏差
  - 环境变化
  - 电容耦合



时钟分布

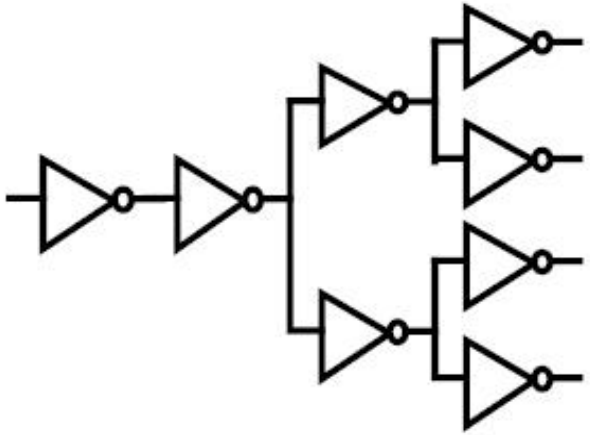
- 时钟延时分布



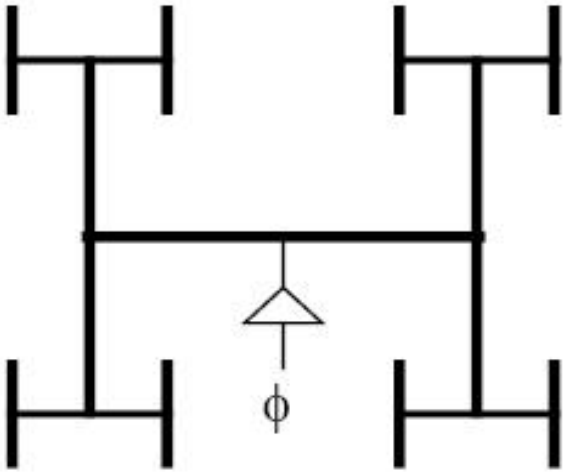


时钟分布

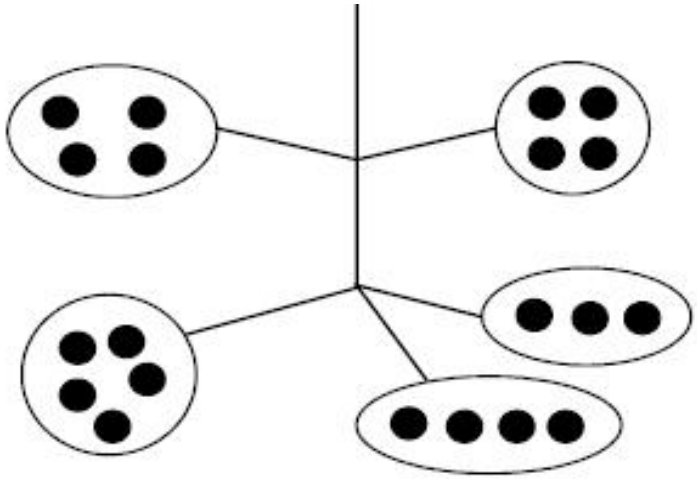
- 时钟分布技术
  - 相位相同（相对延时相同）
  - 常用时钟网络



（C）二叉树



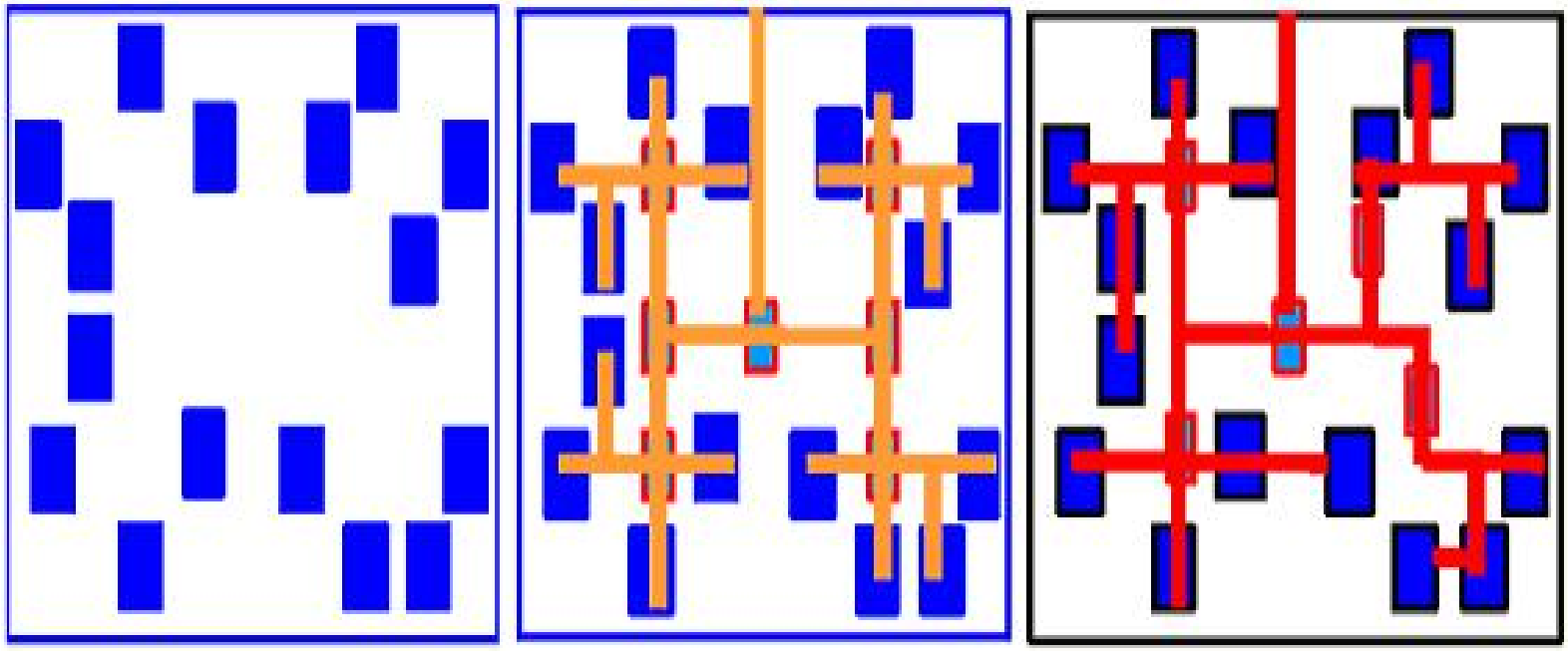
(a)H-树



(b)平衡树

时钟分布

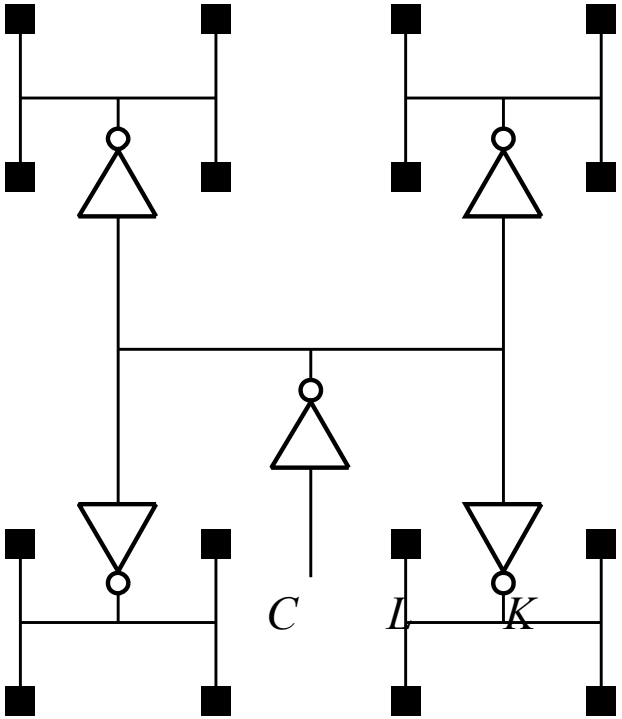
- 时钟树

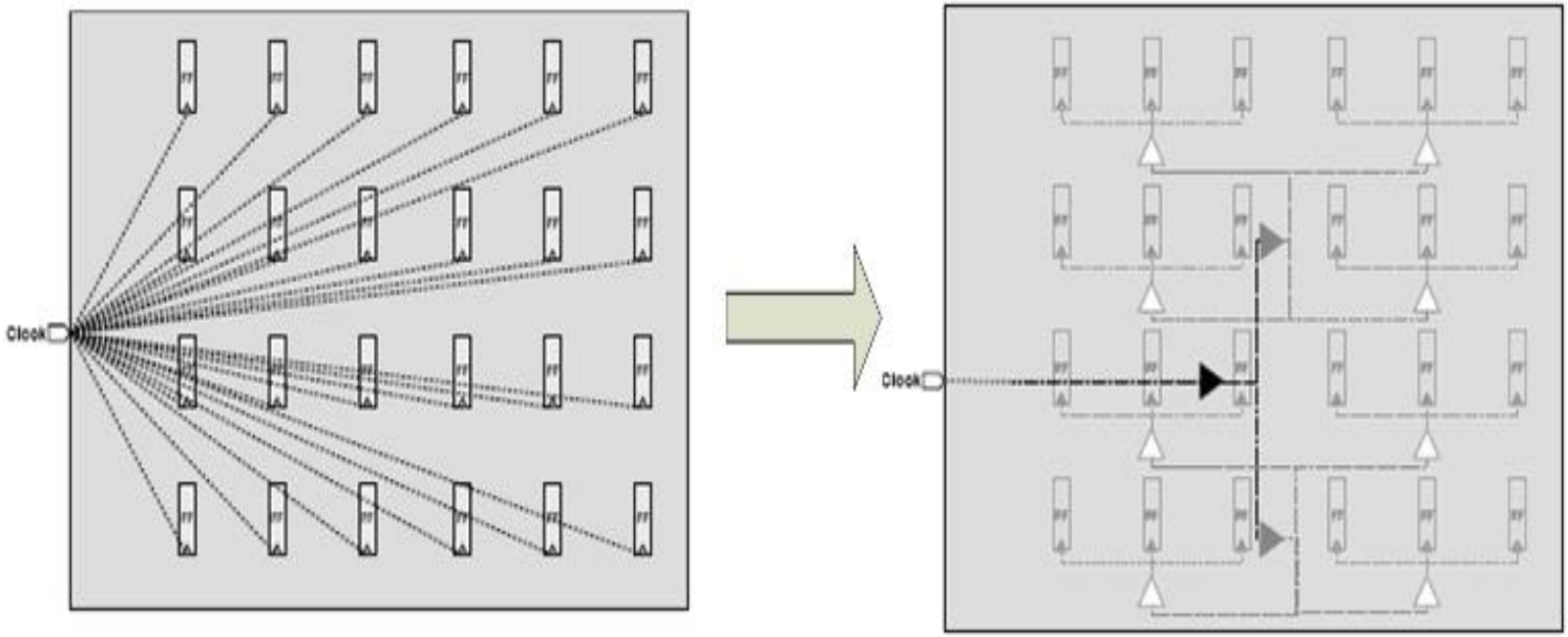


不含时钟树　　零偏斜时钟树　　可变时间时钟树

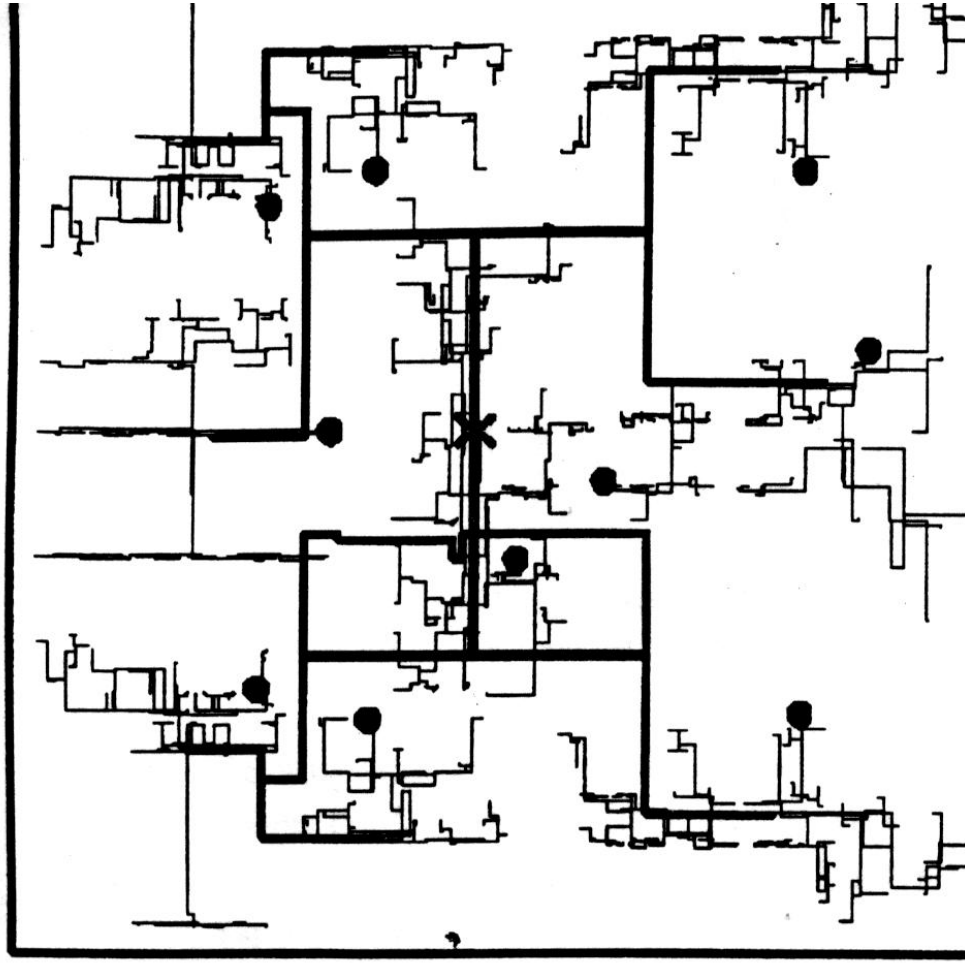
时钟分布

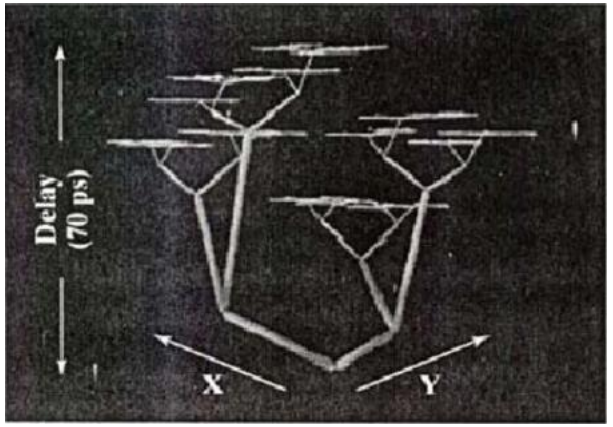
- H树

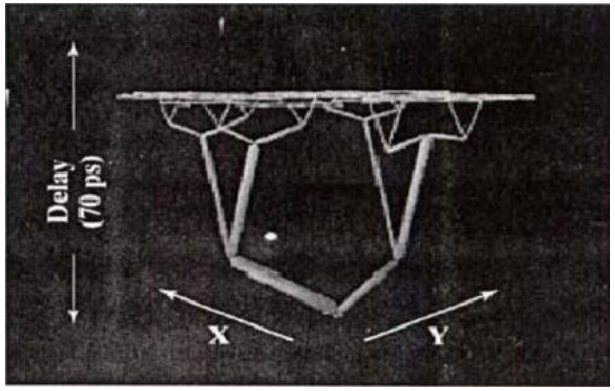




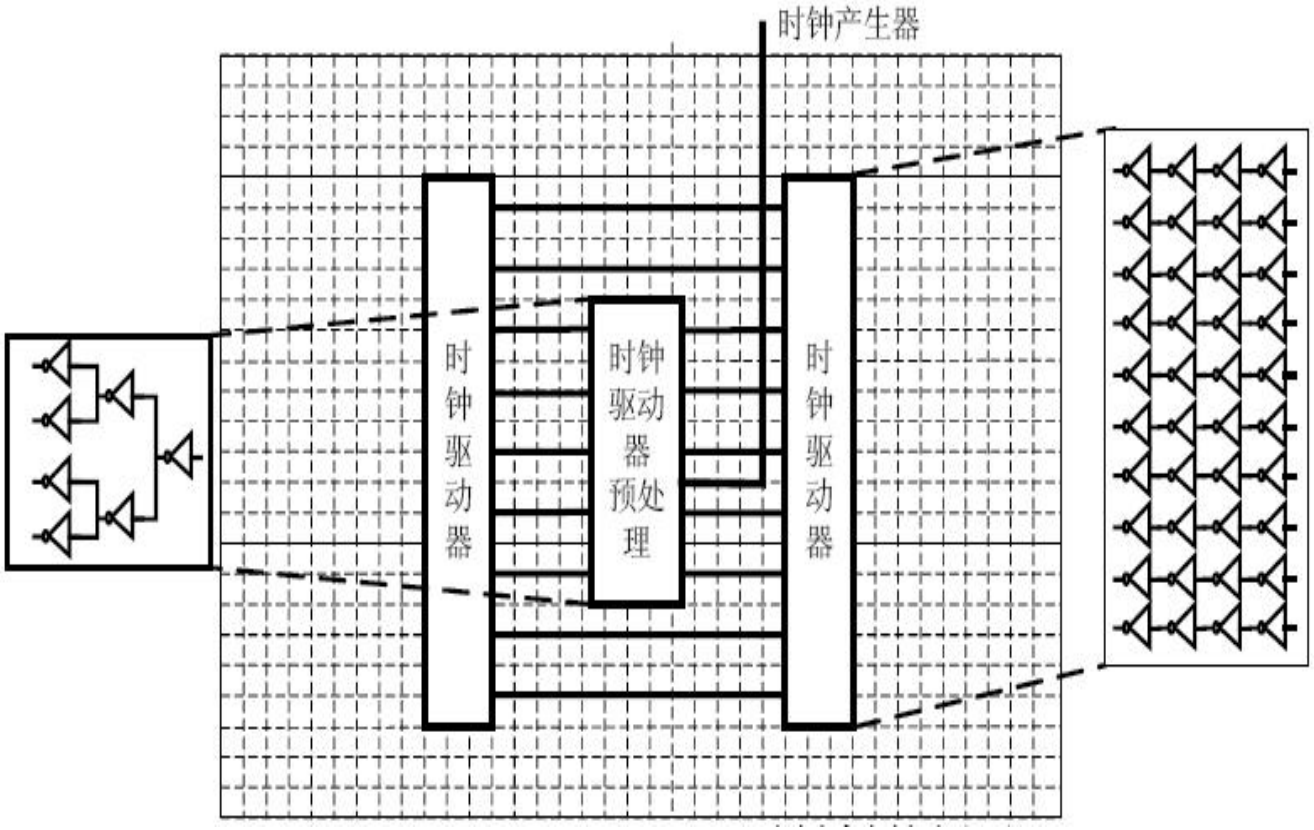
时钟分布







时钟分布



DEC Alpha 21164 CPU时钟树的例子