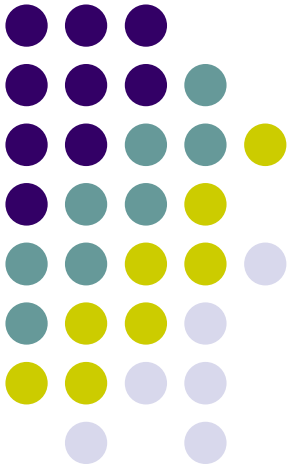
超大规模集成电路基础

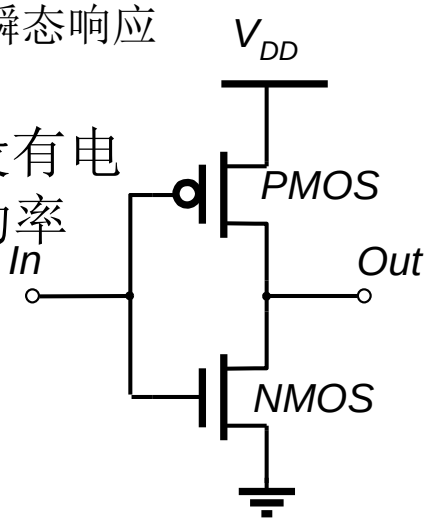
Fundamental of VLSI

第五章 CMOS 反相器

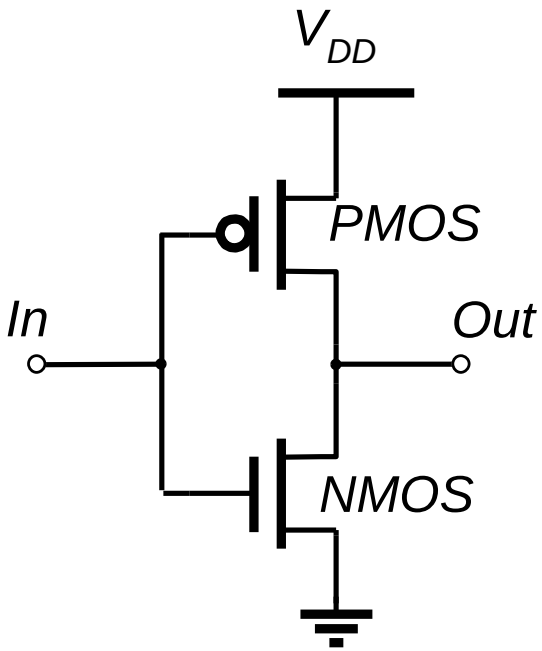


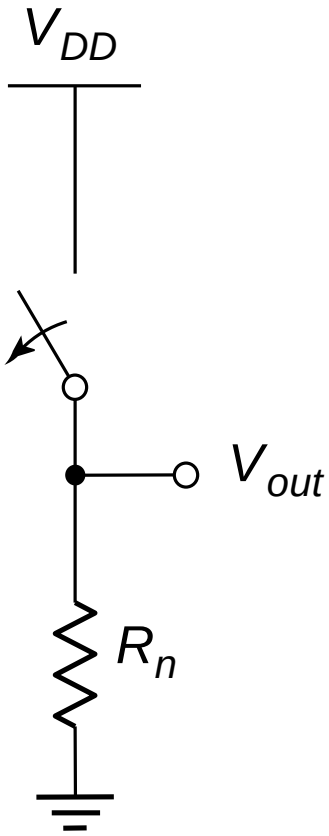
CMOS反相器

- 输出高电平和低电平分别为V_{DD}和GND
- 逻辑电平与器件的相对尺寸无关（无比逻辑），所以晶体管可采用最小尺寸
- 稳态时输出和V_{DD}或GND之间总存在一条具有有限电阻的通路，好的CMOS反相器设计应该具有低输出阻抗
- CMOS反相器输入电阻极高，稳态输入电流几乎为零
  - 理论上，单个反相器可以驱动无穷多个门（或者说扇出无穷大）而仍能够正常工作，尽管大的扇出对稳态特性没有影响，但会使瞬态响应变差
- CMOS在稳态情况下电源线和地线没有直接通路，没有电流存在（忽略漏电流），因此该门不消耗任何静态功率

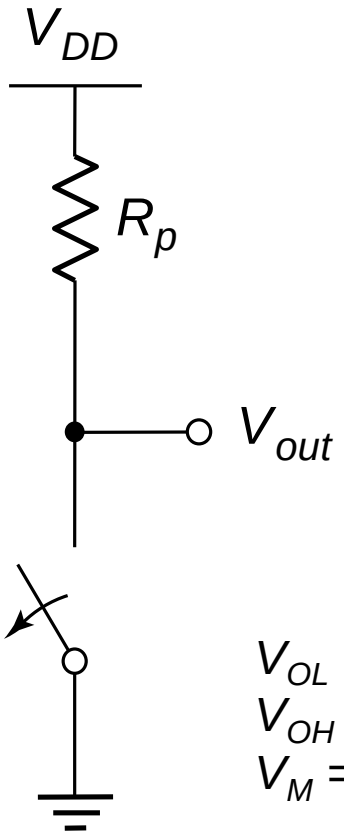


CMOS反相器





$V_{in} = V_{DD}$



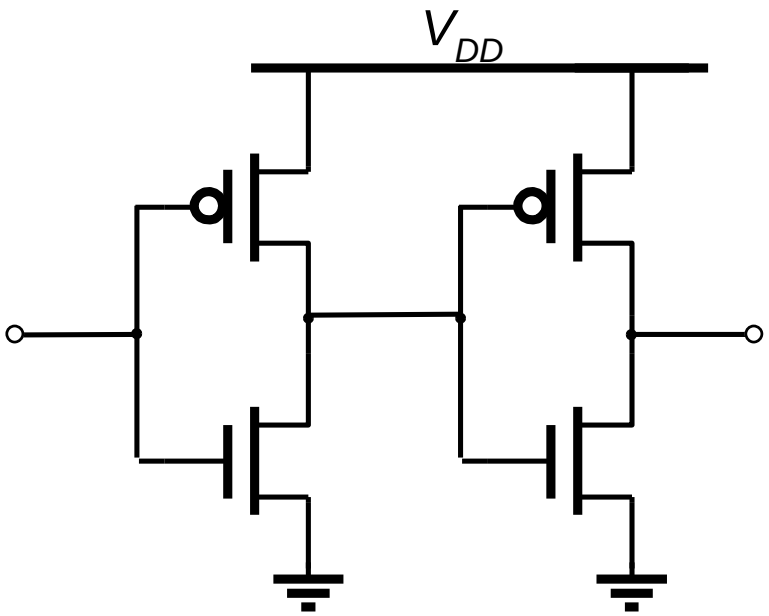
$V_{in} = 0$

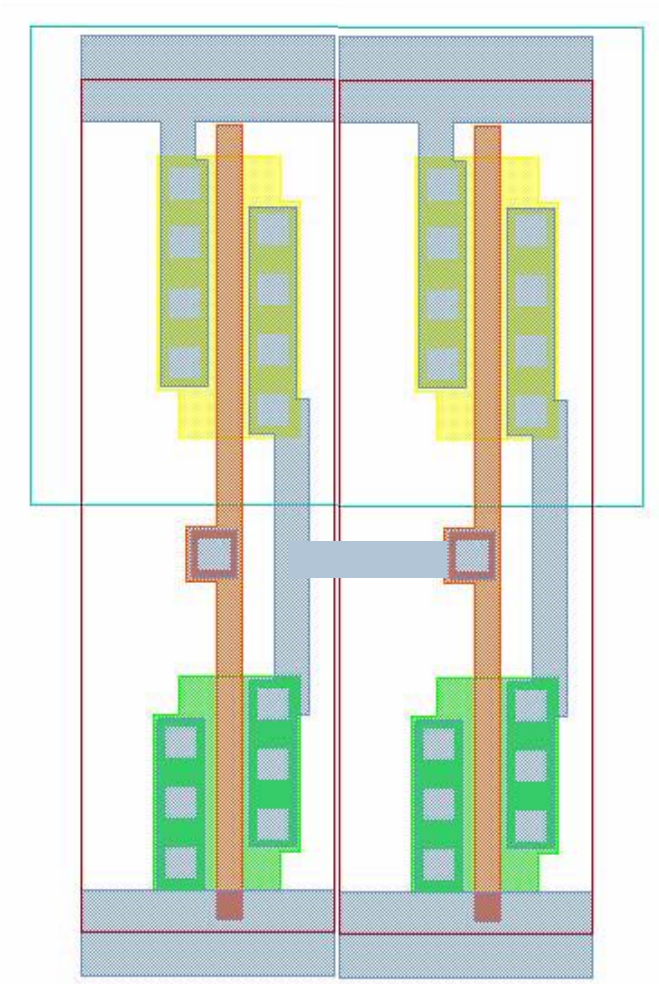
$V_{OL} = 0$

$V_{OH} = V_{DD}$

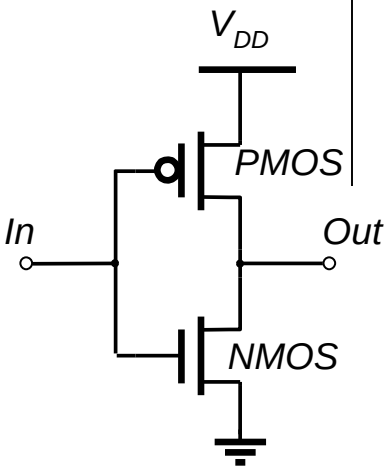
$V_M = f(Rn, Rp)$

CMOS反相器

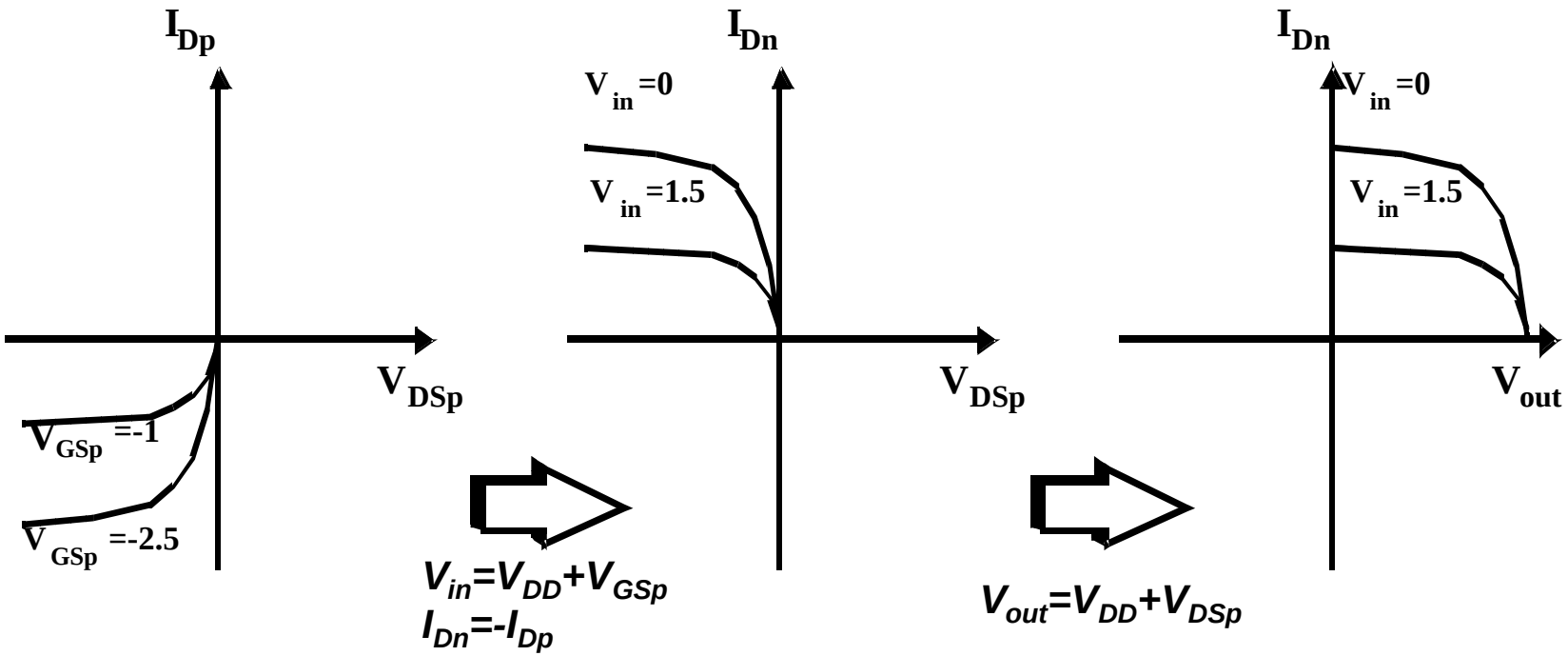




PMOS负载曲线



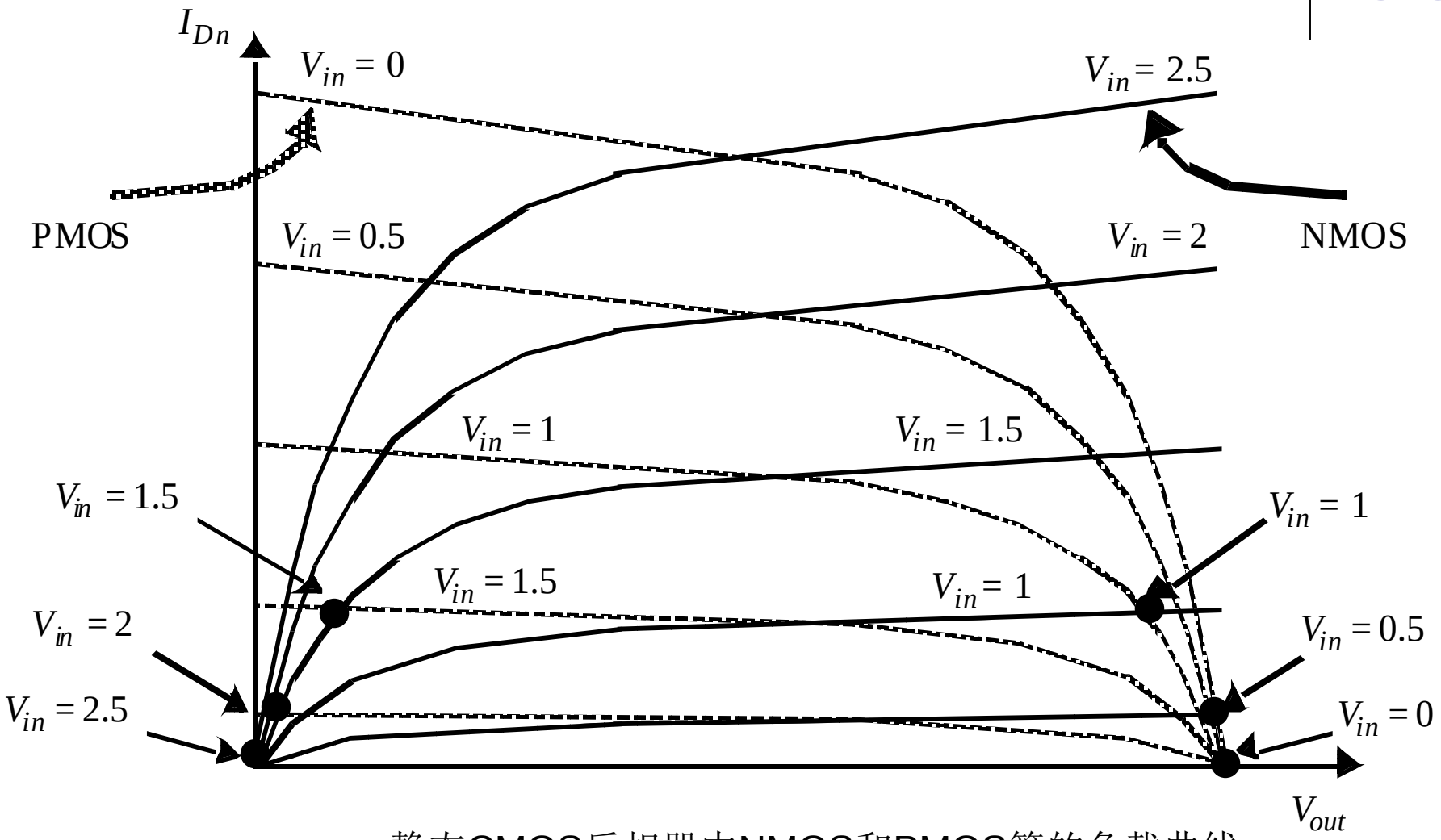
$$I_{DSp}=-I_{DSn}$$
$$V_{GSn}=V_{in};\quad V_{GSp}=V_{in}-V_{DD}$$
$$V_{DSn}=V_{out};\quad V_{DSp}=V_{out}-V_{DD}$$



$V_{in}=V_{DD}+V_{GSp}$
$I_{Dn}=-I_{Dp}$

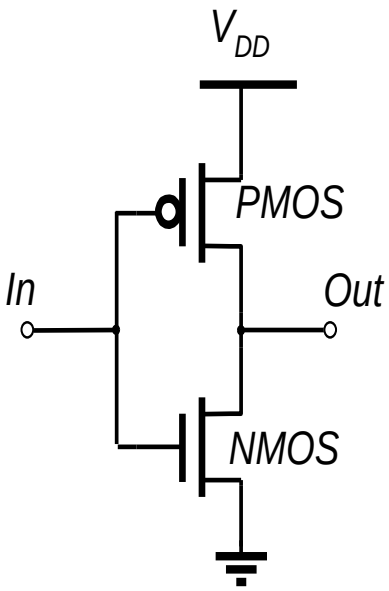
$V_{out}=V_{DD}+V_{DSp}$

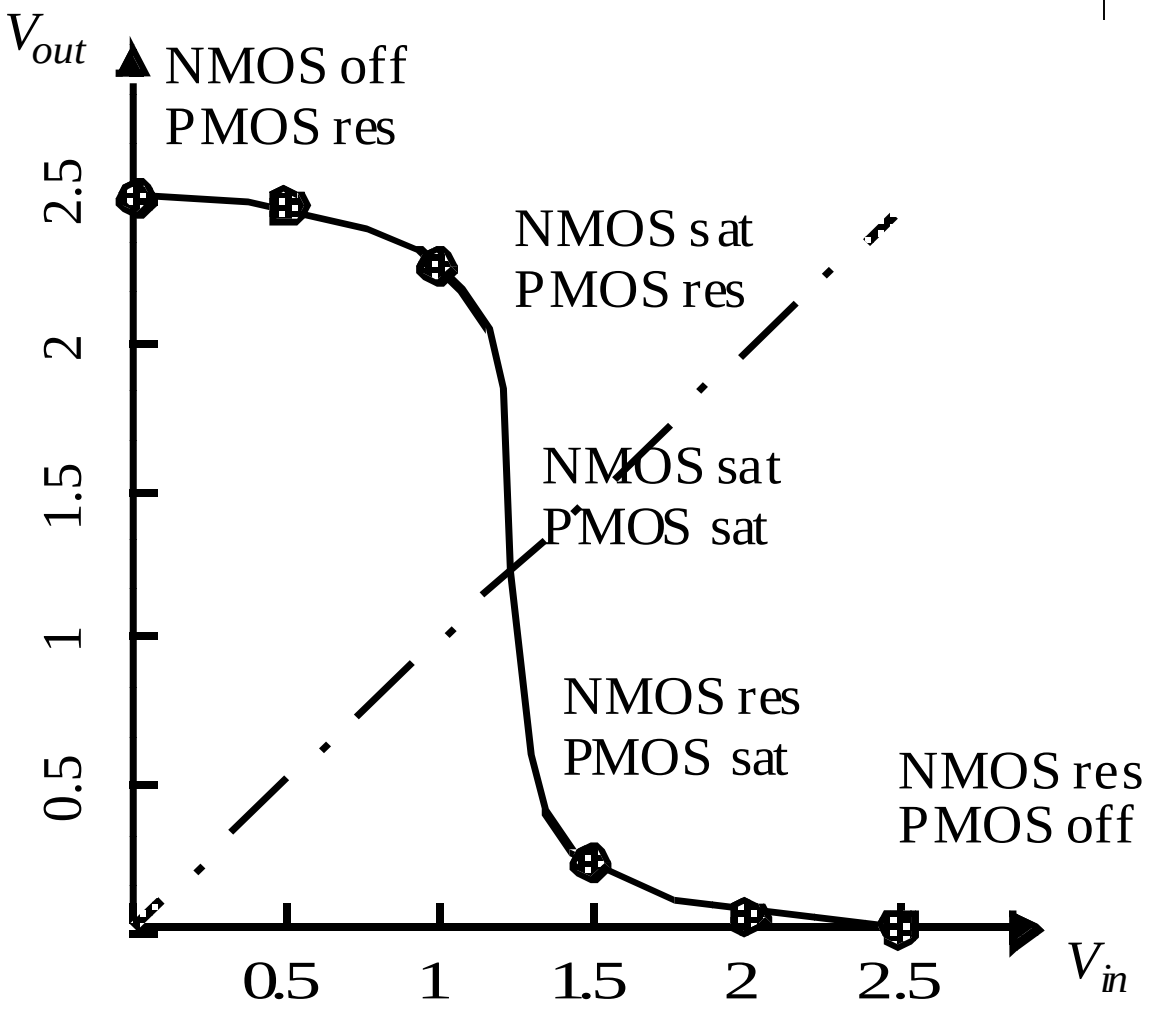
CMOS反相器负载曲线



静态CMOS反相器中NMOS和PMOS管的负载曲线

CMOS反相器VTC


V_{DD}
PMOS
In
Out
NMOS


V_{out}
NMOS off
PMOS res
NMOS sat
PMOS res
NMOS sat
PMOS sat
NMOS res
PMOS sat
NMOS res
PMOS off
2.5
2
1.5
1
0.5
0.5
1
1.5
2
2.5
V_{in}

CMOS反相器的静态特性

- 开关阈值$V_M=f(V_M)$
- 假设电源电压足够高，器件处于速度饱和（即$V_{DSAT}<V_M-V_T$）

$$k_n V_{DSATn}\left(V_M - V_{Tn} - \frac{V_{DSATn}}{2}\right) + k_p V_{DSATp}\left(V_M - V_{DD} - V_{Tp} - \frac{V_{DSATp}}{2}\right) = 0$$

求解V_M得到：

$$V_M = \frac{\left(V_{Tn} + \frac{V_{DSATn}}{2}\right) + r\left(V_{DD} + V_{Tp} + \frac{V_{DSATp}}{2}\right)}{1+r} \qquad r = \frac{k_p V_{DSATp}}{k_n V_{DSATn}} = \frac{\upsilon_{satp} W_p}{\upsilon_{satn} W_n}$$

如果V_{DD}很大，V_M计算可进一步简化为 $V_M = \frac{rV_{DD}}{1+r}$

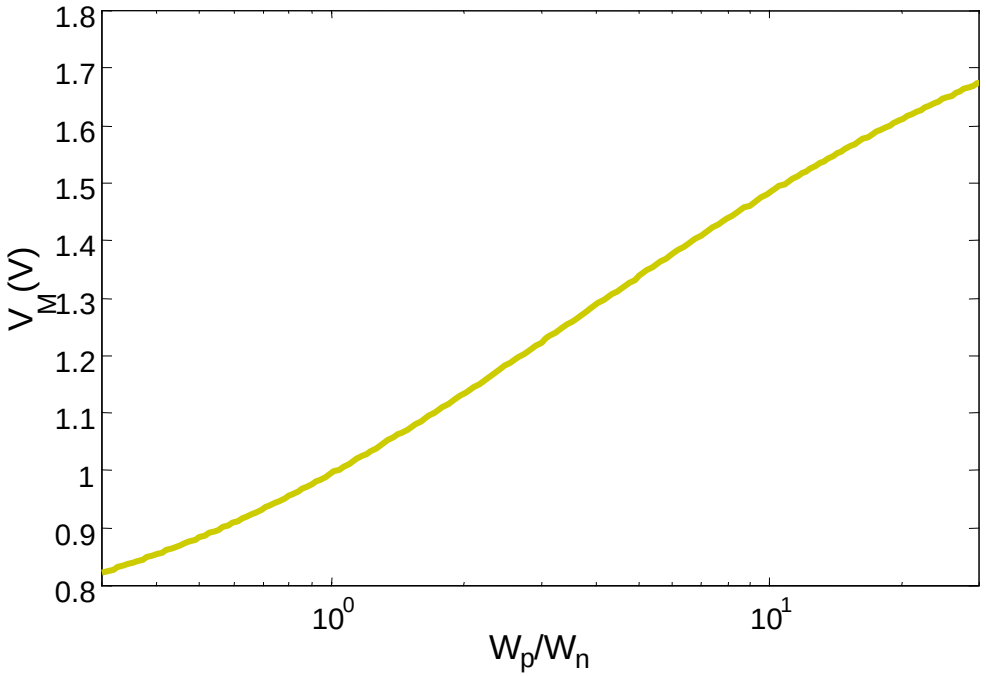
CMOS反相器的静态特性

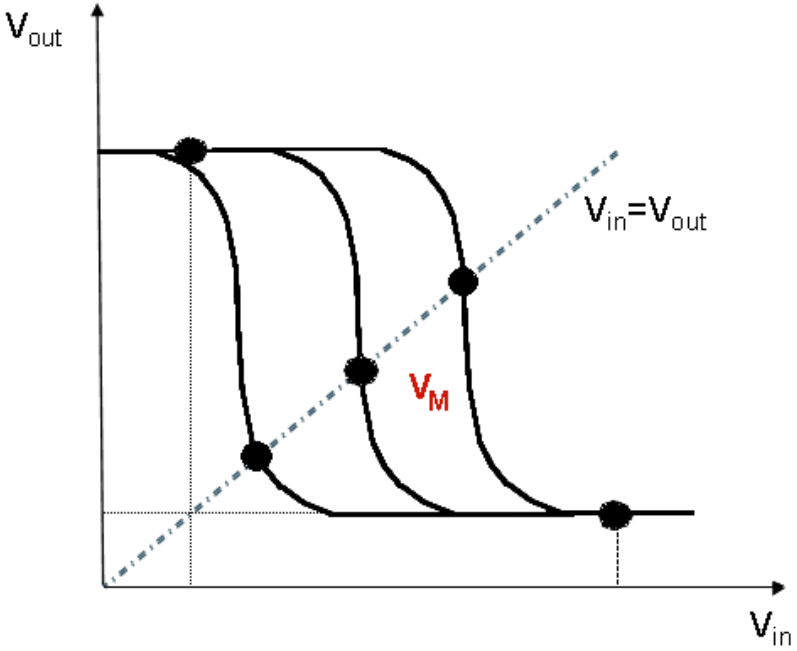
- 给定开关阈值确定PMOS和NMOS器件的尺寸

$$\frac{(W/L)_p}{(W/L)_n} = \frac{k_n' V_{DSATn}\left(V_M - V_{Tn} - \frac{V_{DSATn}}{2}\right)}{-k_p' V_{DSATp}\left(V_M - V_{DD} - V_{Tp} - \frac{V_{DSATp}}{2}\right)}$$

CMOS反相器的静态特性

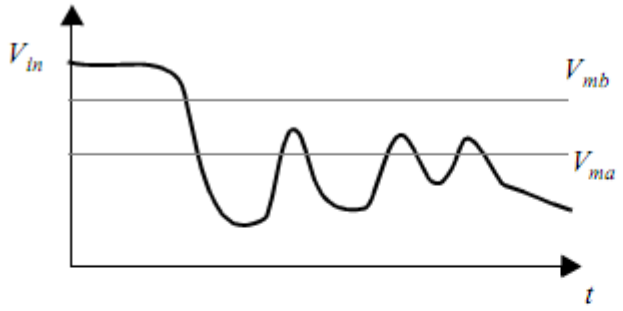
- 反相器阈值V_M具有特点
  - V_M对于器件比值的变化不敏感
  - 改变W_p/W_n的影响是使反相器的VTC过渡区平移

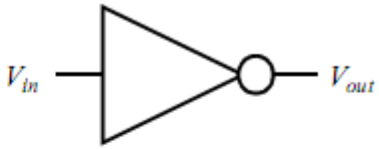


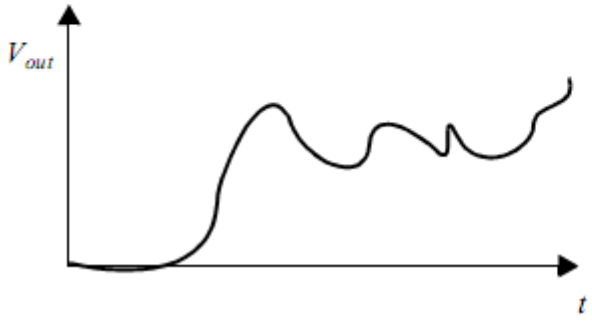


CMOS反相器的静态特性

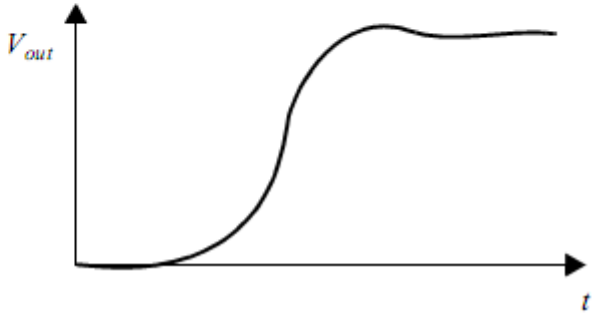
- 反相器阈值V_M调整







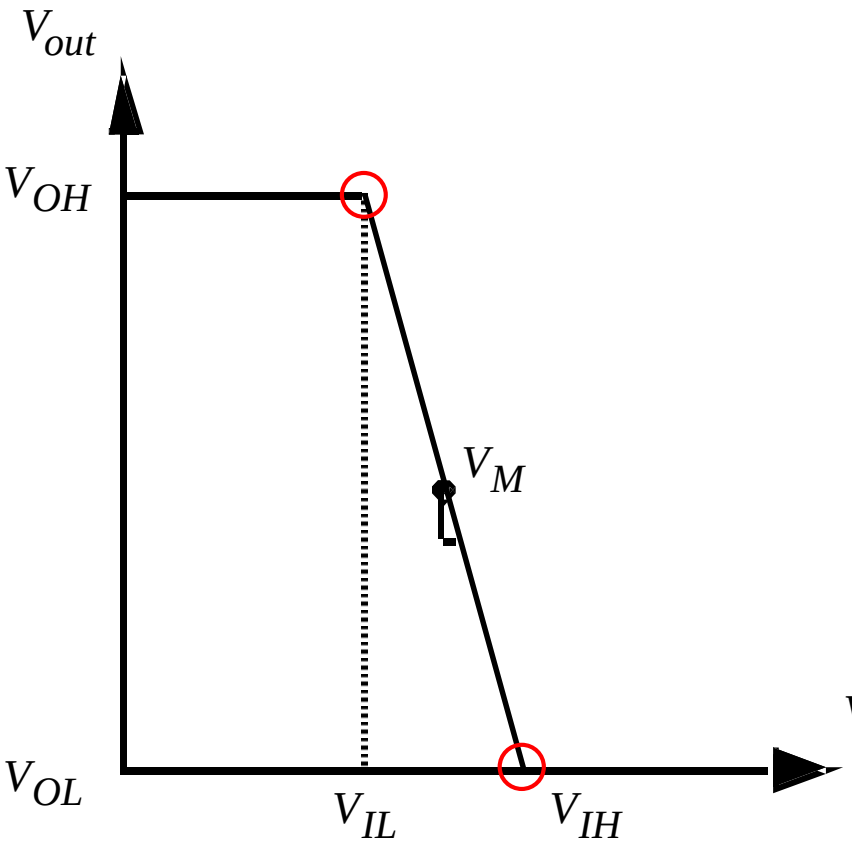
标准反相器的响应

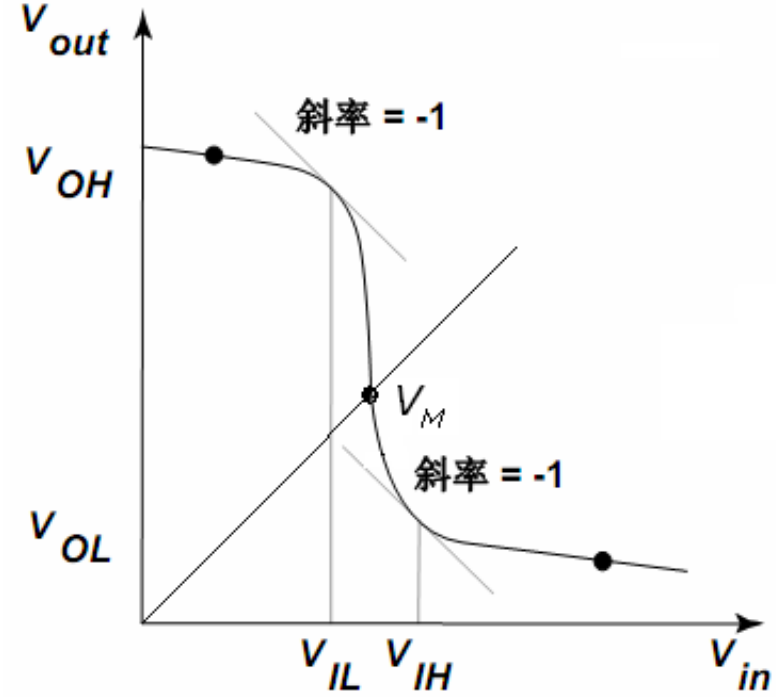


改变阈值后的反相器的响应

CMOS反相器的静态特性

- 噪声容限
  - 反相器VTC线性近似





$$V_{IH} - V_{IL} = -\frac{(V_{OH} - V_{OL})}{g} = \frac{-V_{DD}}{g}$$

$$V_{IH} = V_M - \frac{V_M}{g} \qquad V_{IL} = V_M + \frac{V_{DD} - V_M}{g}$$

$$NM_H = V_{DD} - V_{IH} \qquad NM_L = V_{IL}$$

CMOS反相器的静态特性

- 噪声容限
  - 反相器增益g计算

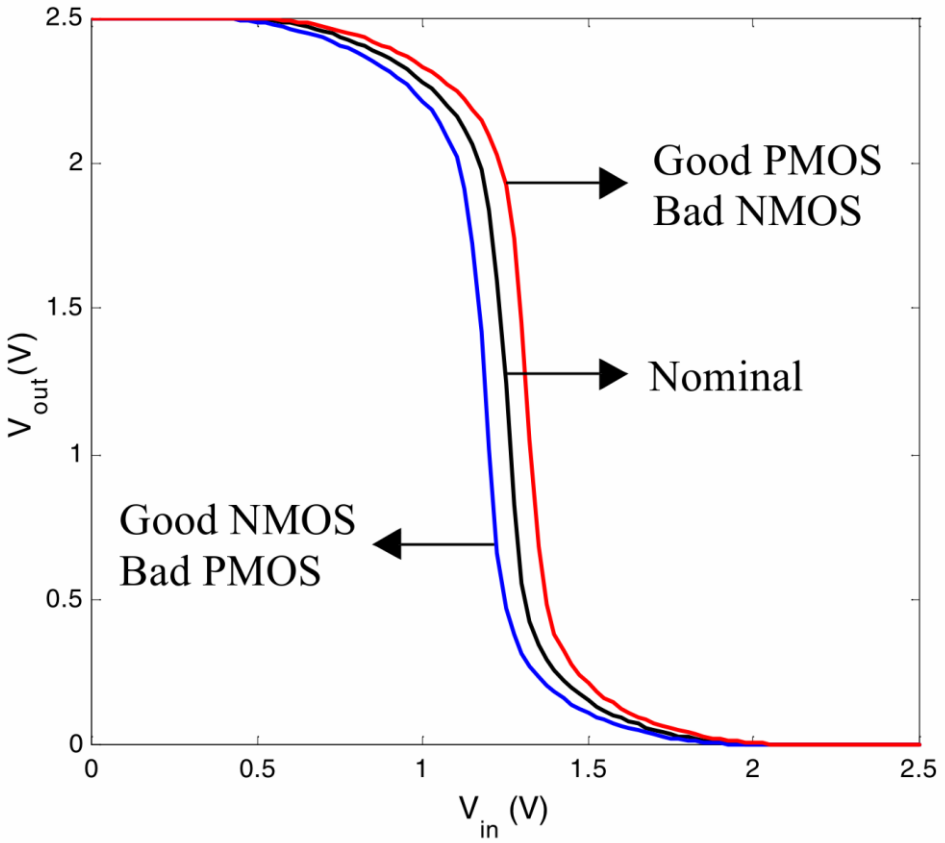
$$k_n V_{DSATn}\left(V_{in}-V_{Tn}-\frac{V_{DSATn}}{2}\right)(1+\lambda_n V_{out})+k_p V_{DSATp}\left(V_{in}-V_{DD}-V_{Tp}-\frac{V_{DSATp}}{2}\right)(1+\lambda_p V_{out}-\lambda_p V_{DD})=0$$

$$g=\frac{dV_{out}}{dV_{in}}=-\frac{k_n V_{DSATn}(1+\lambda_n V_{out})+k_p V_{DSATp}(1+\lambda_p V_{out}-\lambda_p V_{DD})}{\lambda_n k_n V_{DSATn}\left(V_{in}-V_{Tn}-\frac{V_{DSATn}}{2}\right)+\lambda_p k_p V_{DSATp}\left(V_{in}-V_{DD}-V_{Tp}-\frac{V_{DSATp}}{2}\right)}$$

$$g\approx-\frac{k_n V_{DSATn}+k_p V_{DSATp}}{I_D(V_M)(\lambda_n-\lambda_p)}=\frac{1+r}{(V_M-V_{Tn}-\frac{V_{DSATn}}{2})(\lambda_n-\lambda_p)}$$

CMOS反相器的静态特性

- 稳定性
  - 器件参数变化对CMOS反相器静态特性的影响
    - 温度
    - 器件工艺参数
      - 栅氧厚度
      - 沟道长L
      - 栅极宽W
      - 阈值电压VT
  - 只对阈值有较小影响

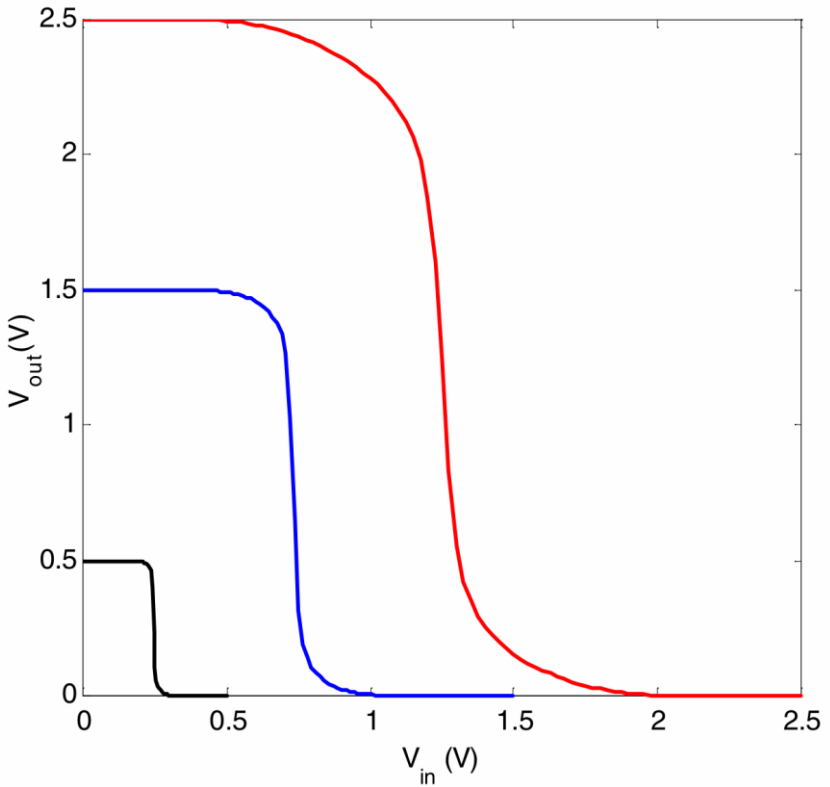


CMOS反相器的静态特性

- 稳定性
  - 工作电压对CMOS反相器静态特性的影响
    - 增益g随VDD的降低而增大
    - 然而VDD不能任意降低，会有负面作用
      - 延时增加
      - 对器件参数敏感
      - 对外部噪声敏感

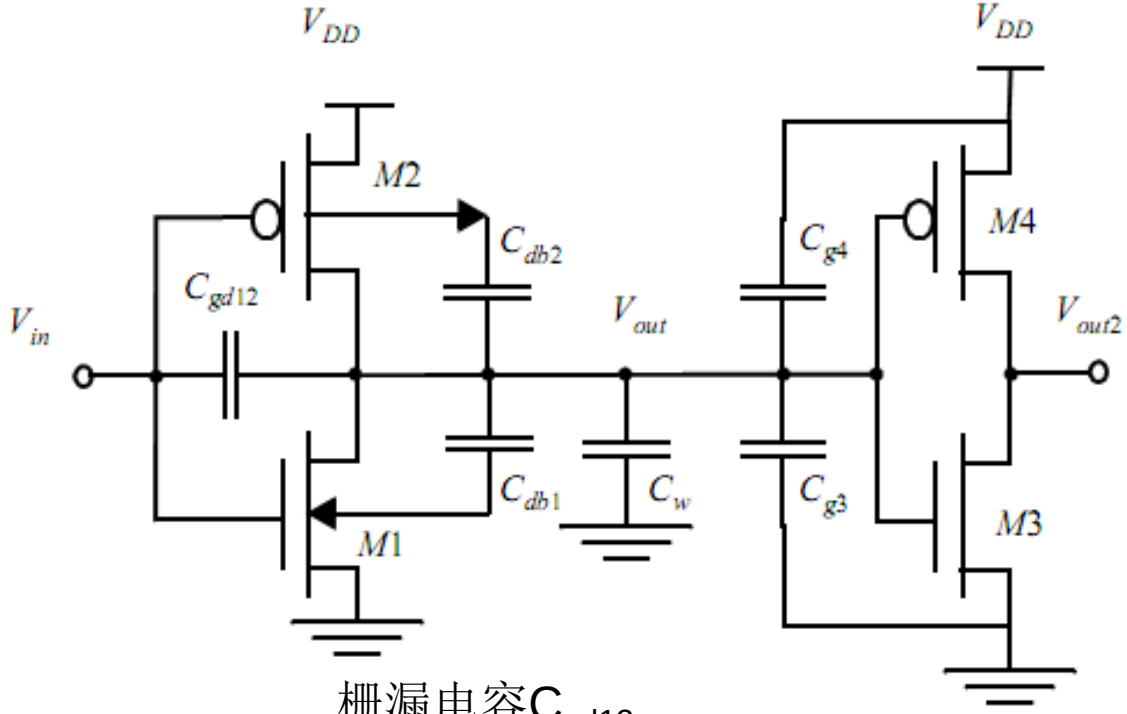
$$g \approx -\frac{k_n V_{DSATn} + k_p V_{DSATp}}{I_D(V_M)(\lambda_n - \lambda_p)}$$

$$= \frac{1+r}{(V_M - V_{Tn} - \frac{V_{DSATn}}{2})(\lambda_n - \lambda_p)}$$



CMOS反相器的动态特性

- CMOS反相器寄生电容



栅漏电容C_{gd12}

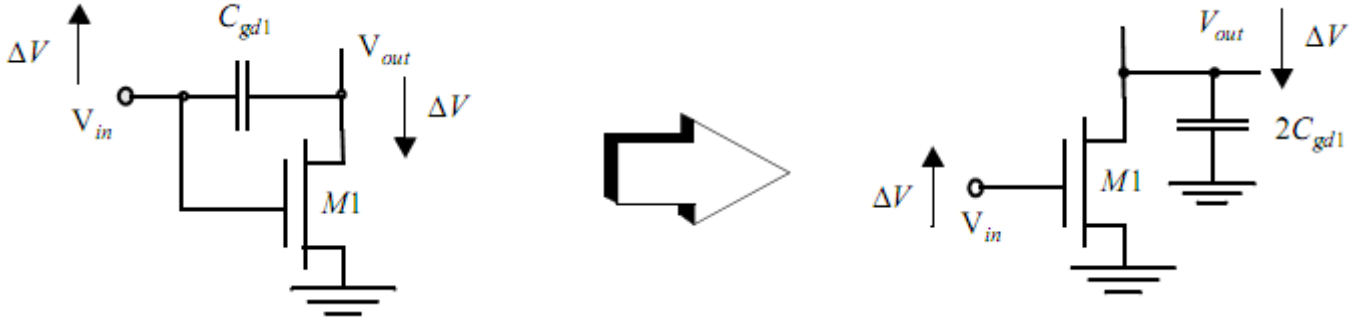
扩散电容C_{db1}和C_{db2}

连线电容C_W

扇出的栅电容C_{g3}和C_{g4}

CMOS反相器的动态特性

- CMOS反相器寄生电容
  - 栅漏电容C_{gd12}
  - $C_{gd12}=C_{gd1}+C_{gd2}$
  - $C_{gd1}=C_{ox}x_{dM1}W_{M1}$
  - 米勒效应



工作区域	C_{GCB}	C_{GCS}	C_{GCD}	C_{GC}	C_G
截止区	$C_{ox}WL$	0	0	$C_{ox}WL$	$C_{ox}WL+2C_oW$
电阻区	0	$C_{ox}WL/2$	$C_{ox}WL/2$	$C_{ox}WL$	$C_{ox}WL+2C_oW$
饱和区	0	$(2/3)C_{ox}WL$	0	$(2/3)C_{ox}WL$	$(2/3)C_{ox}WL+2C_oW$

CMOS反相器的动态特性

- CMOS反相器寄生电容
  - 扩散电容C_{db1}和C_{db2}
    - 扩散电容是高度非线性的，通常对其线性化处理

$$C_{eq} = K_{eq} C_{j0}$$

$$K_{eq} = \frac{-\phi_0^m}{(V_{high} - V_{low})(1-m)} \left[(\phi_0 - V_{high})^{1-m} - (\phi_0 - V_{low})^{1-m} \right]$$

	C_{ox} (fF/μm^2)	C_O (fF/μm)	C_{j0} (fF/μm^2)	m_j	ϕ_b (V)	C_{jsw} (fF/μm)	m_{jsw}	ϕ_{bsw} (V)
NMOS	6	0.31	2	0.5	0.9	0.28	0.44	0.9
PMOS	6	0.27	1.9	0.48	0.9	0.22	0.32	0.9

CMOS反相器的动态特性

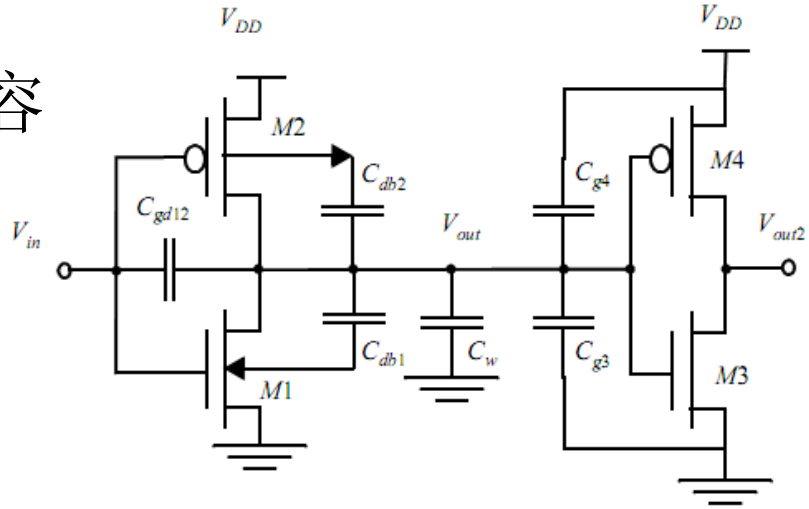
- CMOS反相器寄生电容
  - 连线电容C_w
    - 与连线的长度和宽度及扇出的数目有关
  - 扇出的栅电容C_{g3}和C_{g4}
    - 由负载门M_3和M_4的栅电容构成

$$C_{fan-out} = C_{gate}(NMOS) + C_{gate}(PMOS)$$
$$= (C_{GSOn} + C_{GDOn} + W_n L_n C_{ox}) + (C_{GSOp} + C_{GDOp} + W_p L_p C_{ox})$$

  - 表达式简化
    - 假设栅电容的所有部分都连在V_{out}和GND（或V_{DD}）之间，并且忽略了栅漏电容上的米勒效应
    - 近似认为所连接的门的沟道电容在关注时间内保持不变为WLC_{ox}

CMOS反相器的动态特性

- CMOS反相器寄生电容



Capacitor	Expression	Value (fF) (H→L)	Value (fF) (L→H)
C_{gd1}	2 $CGD0_n$ W_n	0.23	0.23
C_{gd2}	2 $CGD0_p$ W_p	0.61	0.61
C_{db1}	K_{eqn} AD_n CJ + K_{eqswn} PD_n CJSW	0.66	0.90
C_{db2}	K_{eqp} AD_p CJ + K_{eqswp} PD_p CJSW)	1.5	1.15
C_{g3}	($CGD0_n$+$CGSO_n$) W_n + C_{ox} W_n L_n	0.76	0.76
C_{g4}	($CGD0_p$+$CGSO_p$) W_p + C_{ox} W_p L_p	2.28	2.28
C_w	From Extraction	0.12	0.12
C_L	Σ	6.1	6.0

CMOS反相器的动态特性

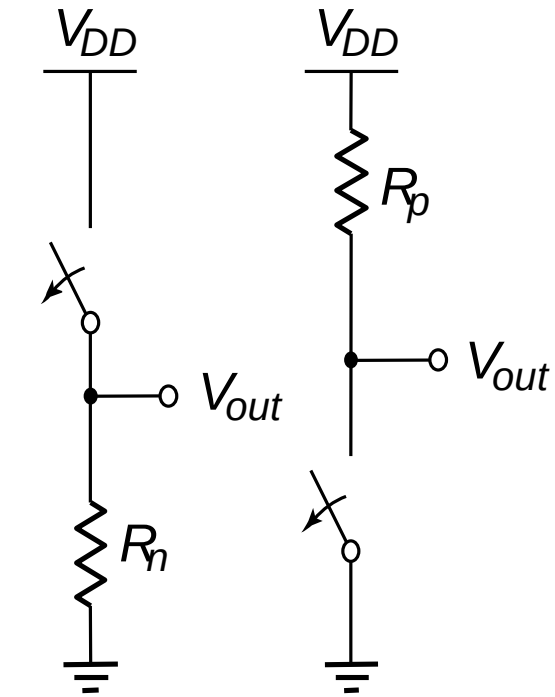
- 传播延时：一阶分析
  - 传播延时t_p=RC

$$t_p = \int_{v_1}^{v_2} \frac{C_L(v)}{i(v)} dv$$

$$R_{eq} = \frac{1}{-V_{DD}/2} \int_{V_{DD}}^{V_{DD}/2} \frac{V}{I_{DSAT}(1+\lambda V)} dV \approx \frac{3}{4} \frac{V_{DD}}{I_{DSAT}} \left(1 - \frac{7}{9}\lambda V_{DD}\right)$$

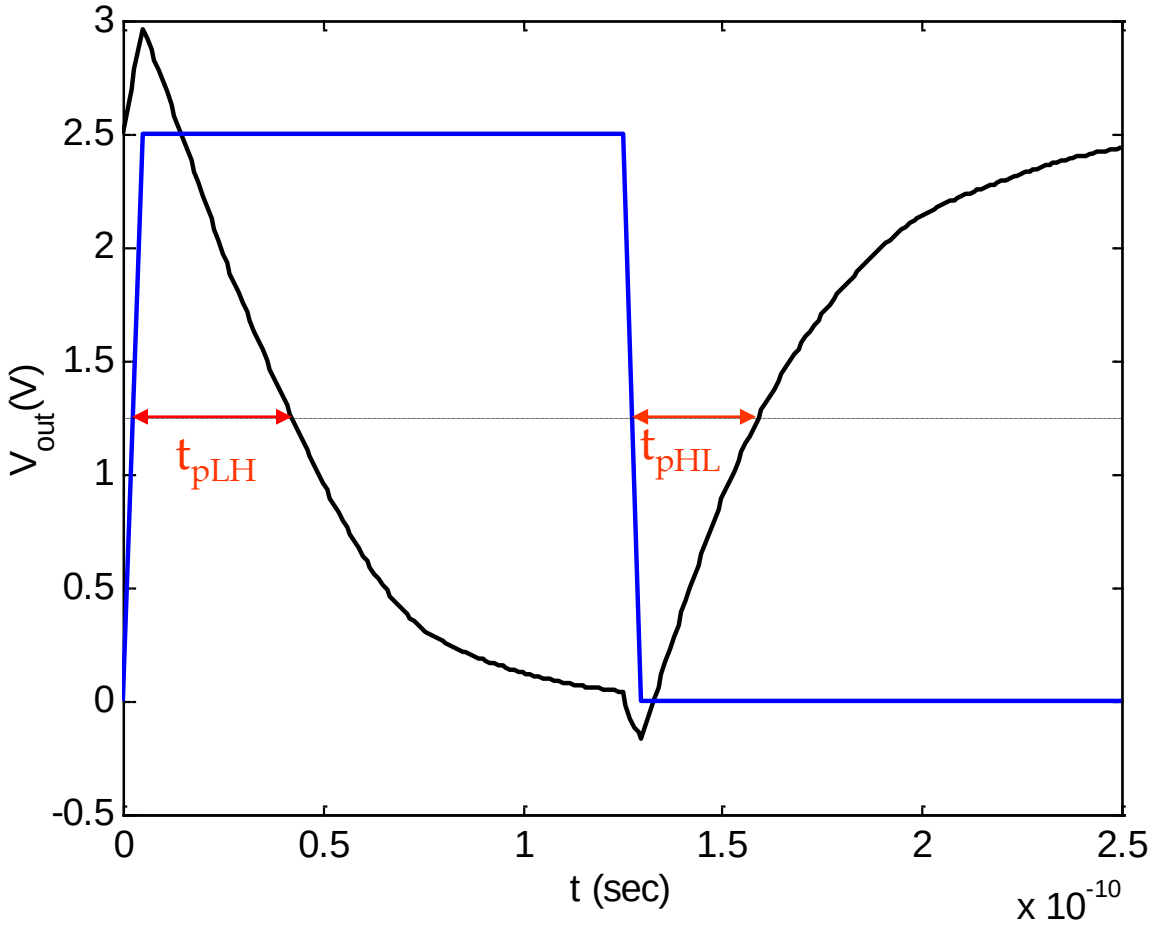
其中 $$I_{DSAT} = k' \frac{W}{L} \left((V_{DD} - V_T) V_{DSAT} - \frac{V_{DSAT}^2}{2} \right)$$

$$t_{pHL} = \ln(2) R_{eqn} C_L = 0.69 R_{eqn} C_L$$
$$t_{pLH} = \ln(2) R_{eqp} C_L = 0.69 R_{eqp} C_L$$
$$t_p = \frac{t_{pHL} + t_{pLH}}{2} = 0.69 C_L \left(\frac{R_{eqn} + R_{eqp}}{2} \right)$$



CMOS反相器的动态特性

- 传播延时：一阶分析



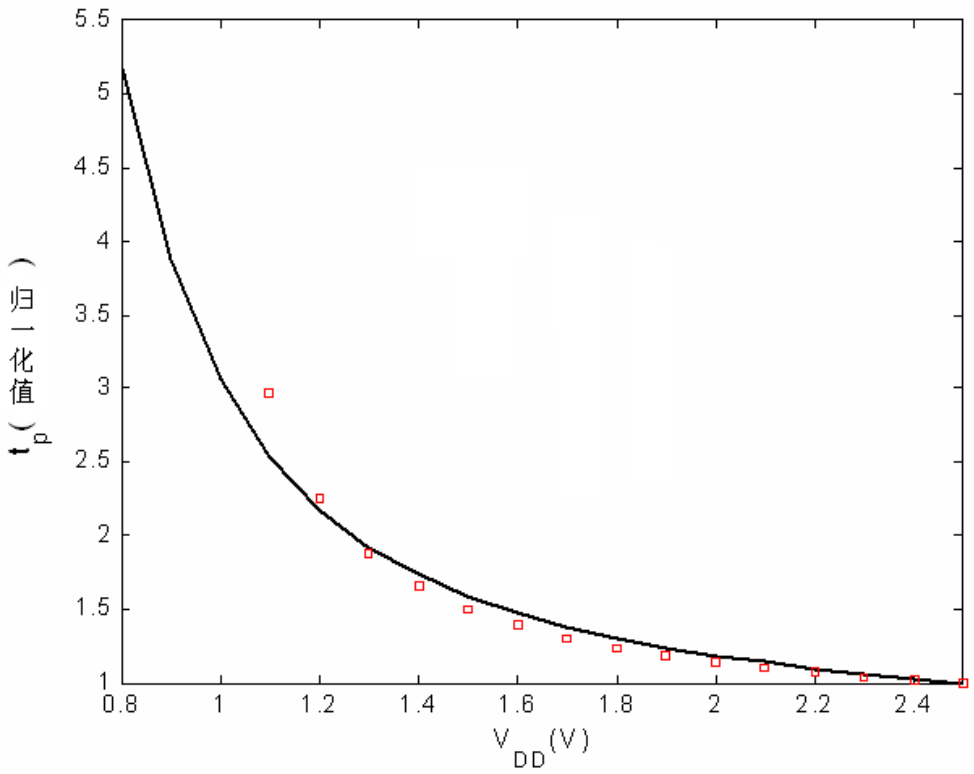
CMOS反相器的动态特性

- 减少CMOS门传播延时的设计技术
  - 减少C_L
    - 使门本身的内部扩散电容、互连线电容和扇出电容减少
  - 增加晶体管的W/L比
    - 减少电阻负载，但反过来会增加电容，称为自载效应
    - 较宽的晶体管具有较大的栅电容，增加了驱动门的扇出系数
  - 提高V_{DD}
    - 增加功耗
    - 降低可靠性

CMOS反相器的动态特性

- 减少CMOS门传播延时的设计技术
  - 电源电压V_{DD}对延时的影响

忽略沟道调制系数λ $t_{pHL} = 0.69\frac{3}{4}\frac{C_L V_{DD}}{I_{DSATn}} = 0.52\frac{C_L V_{DD}}{(W/L)_n k_n' V_{DSATn}(V_{DD} - V_{Tn} - V_{DSATn}/2)}$



如果$V_{DD} >> V_{Tn} - V_{DSATn}/2$

$$t_{pHL} = 0.52\frac{C_L}{(W/L)_n k_n' V_{DSATn}}$$

CMOS反相器的动态特性

- 从设计角度考虑延时
  - NMOS与PMOS比

$$C_L = (C_{dp1} + C_{dn1}) + (C_{gp2} + C_{gn2}) + C_W$$

$$\beta = (W/L)_p / (W/L)_n \qquad \begin{matrix} C_{dp1} \approx \beta C_{dn1} \\ C_{gp2} \approx \beta C_{gn2} \end{matrix} \qquad C_L = (1+\beta)(C_{dn1} + C_{gn2}) + C_W$$

$$t_p = \frac{0.69}{2}\left((1+\beta)(C_{dn1} + C_{gn2}) + C_W\right)\left(\mathrm{R}_{eqn} + \frac{\mathrm{R}_{eqp}}{\beta}\right) \qquad r = \frac{\mathrm{R}_{eqp}}{\mathrm{R}_{eqn}}$$

$$= 0.345\left((1+\beta)(C_{dn1} + C_{gn2}) + C_W\right)\mathrm{R}_{eqn}\left(1 + \frac{r}{\beta}\right)$$

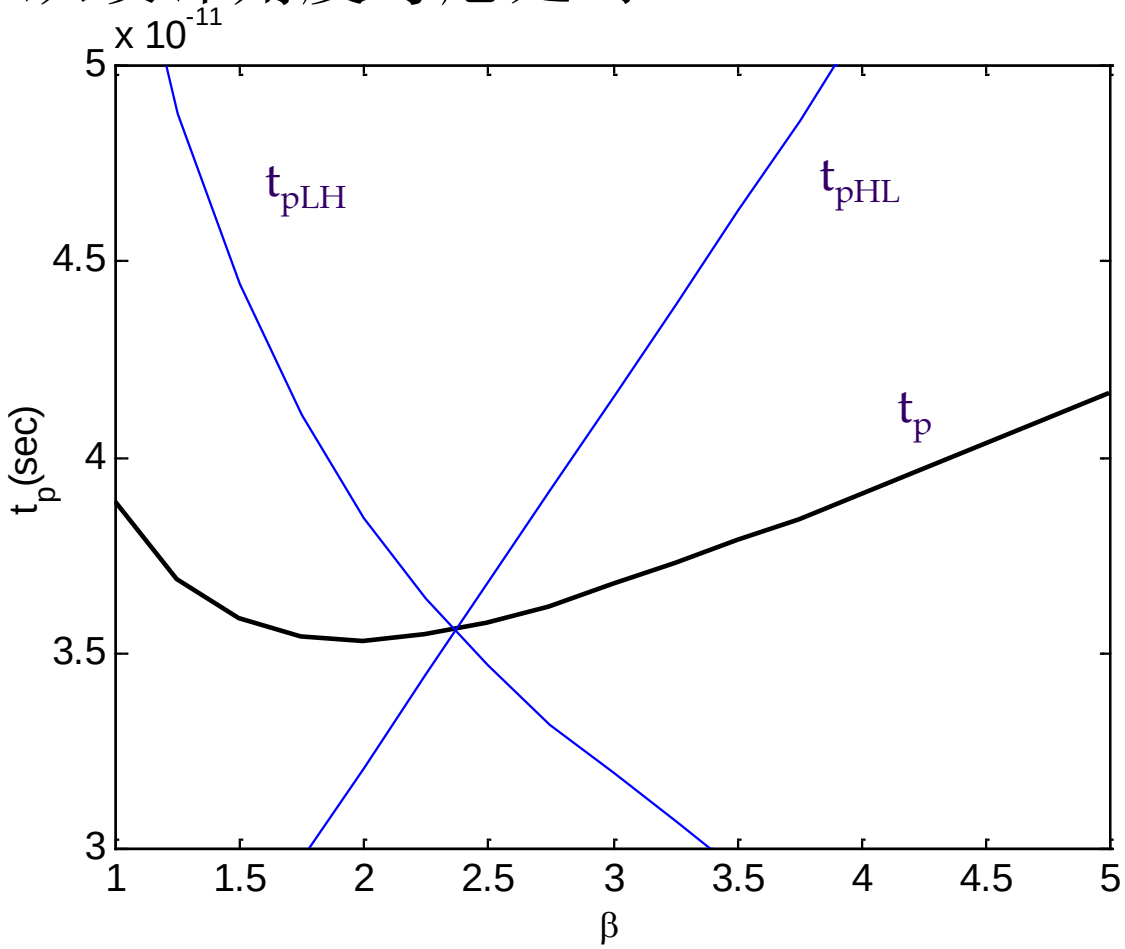
$$\frac{\partial t_p}{\partial \beta} = 0.345\,\mathrm{R}_{eqn}\left[\left(C_{dn1} + C_{gn2}\right)\left(1 + \frac{r}{\beta}\right) - \left((1+\beta)(C_{dn1} + C_{gn2}) + C_W\right)\frac{r}{\beta^2}\right] = 0$$

$$\left(\beta^2 + r\beta\right) = \left((1+\beta) + \frac{C_W}{(C_{dn1} + C_{gn2})}\right)r$$

$$\beta^2 = r\left(1 + \frac{C_W}{(C_{dn1} + C_{gn2})}\right) \qquad \beta_{opt} = \sqrt{r\left(1 + \frac{C_W}{(C_{dn1} + C_{gn2})}\right)}$$

CMOS反相器的动态特性

- 从设计角度考虑延时



$$\beta = W_p / W_n$$

$$\beta_{opt} = \sqrt{r\left(1+\frac{C_W}{(C_{dn1}+C_{gn2})}\right)}$$

CMOS反相器的动态特性

- 考虑性能时反向器尺寸的确定
  - 负载电容可以分为本征和外部电容两部分
    - 本征电容C_{int}：扩散电容和栅漏覆盖电容
    - 外部电容C_{ext}：扇出和导线电容

$$C_L = C_{\text{int}} + C_{ext}$$

$$\begin{aligned} t_p &= 0.69\,\mathrm{R}_{eq}(C_{\text{int}} + C_{ext}) \\ &= 0.69\,\mathrm{R}_{eq}\,C_{\text{int}}(1 + C_{ext}/C_{\text{int}}) = t_{p0}(1 + C_{ext}/C_{\text{int}}) \end{aligned}$$

引入尺寸系数S　$C_{\text{int}} = SC_{iref}$　$\mathrm{R}_{eq} = R_{ref}/S$

$$\begin{aligned} t_p &= 0.69(\mathrm{R}_{ref}/S)(SC_{iref})(1 + C_{ext}/SC_{iref}) \\ &= 0.69\,\mathrm{R}_{ref}\,C_{iref}(1 + C_{ext}/SC_{iref}) = t_{p0}(1 + C_{ext}/SC_{iref}) \end{aligned}$$

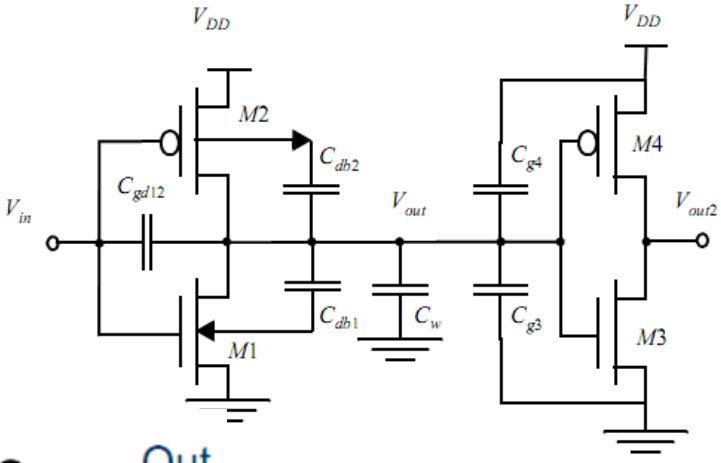
  - 从上式可以得出两个重要的结论
    - 反相器的本征延时t_{p0}与门的尺寸无关
    - 使S无穷大可使性能最大可能的得到改善

CMOS反相器的动态特性

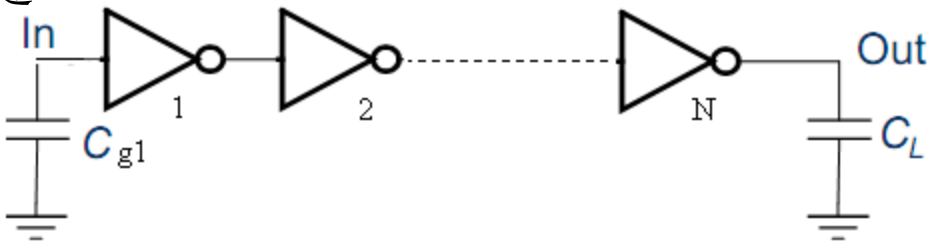
- 反相器链的尺寸优化
  - 反相器的输入电容C_g与本征输出电容之间的关系

$$C_{\text{int}} = \gamma C_g \qquad C_{ext} = fC_g$$

$$t_p = t_{p0}\left(1+\frac{C_{ext}}{\gamma C_g}\right) = t_{p0}\left(1+\frac{fC_g}{\gamma C_g}\right) = t_{p0}\left(1+\frac{f}{\gamma}\right)$$



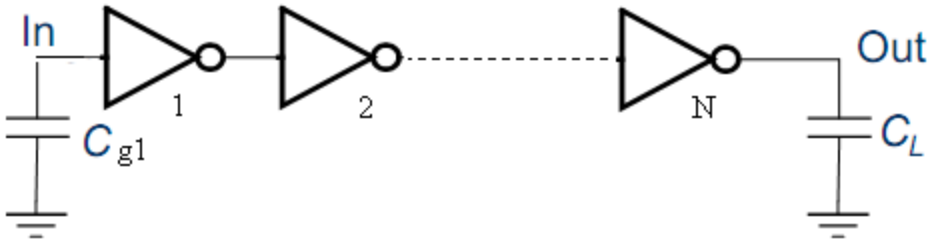
  - 反相器链



$$t_{p,j} = t_{p0}\left(1+\frac{C_{g,j+1}}{\gamma C_{g,j}}\right) = t_{p0}\left(1+\frac{f_j}{\gamma}\right)$$

CMOS反相器的动态特性

- 反相器链的尺寸优化



$$t_p = \sum_{j=1}^{N} t_{p,j} = t_{p0} \sum_{j=1}^{N} \left(1 + \frac{C_{g,j+1}}{\gamma C_{g,j}} \right) \qquad \text{其中} C_{g,N+1} = C_L$$

求t_p关于$C_{g,j}$的导数可得最小延时的约束条件

$$C_{g,j+1} / C_{g,j} = C_{g,j} / C_{g,j-1} \qquad \text{其中(j=2...N)}$$

$$C_{g,j} = \sqrt{C_{g,j-1} C_{g,j+1}}$$

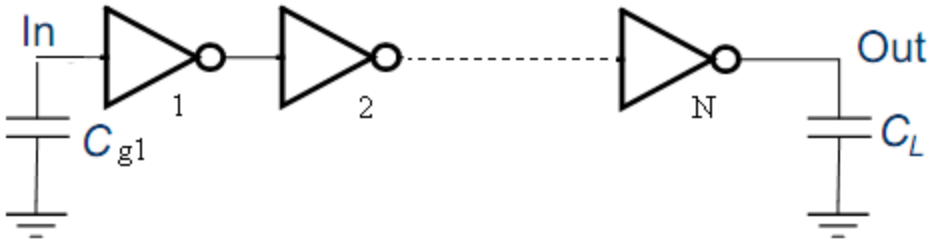
每个反相器有相同的等效扇出 $f = f_j = C_{g,j} / C_{g,j-1}$

给定$C_{g,1}$和C_L，可得尺寸系数 $f = \sqrt[N]{C_L / C_{g,1}}$

因此反相器链的最小延时：$t_p = N t_{p0} (1 + \sqrt[N]{F} / \gamma)$

CMOS反相器的动态特性

- 反相器链的正确级数



$$t_p = Nt_{p0}(1+\sqrt[N]{F}/\gamma)$$

求t_p关于级数N的导数可得最优解

$$\gamma + \sqrt[N]{F} - \frac{\sqrt[N]{F}\ln F}{N} = 0$$

$$f = e^{(1+\gamma/f)}$$

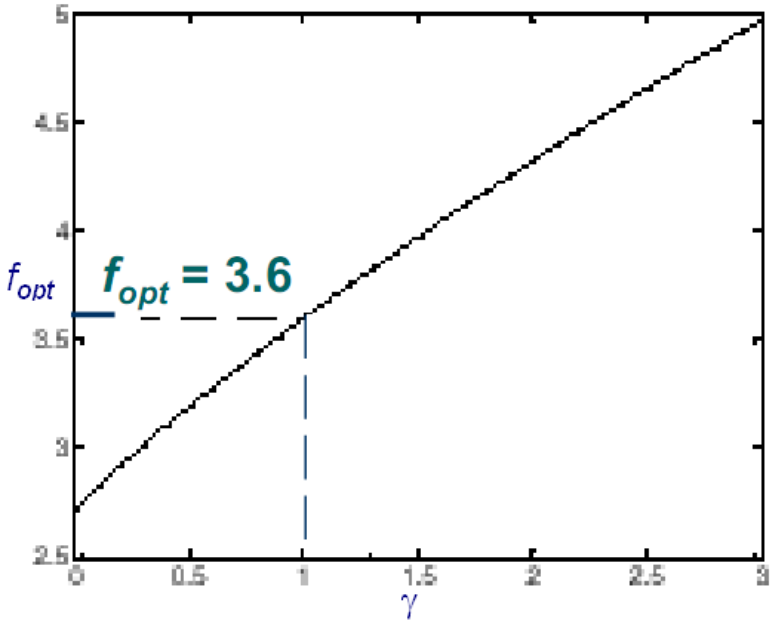
上式只有一个收敛解 $\gamma = 0$ 此时忽略自载

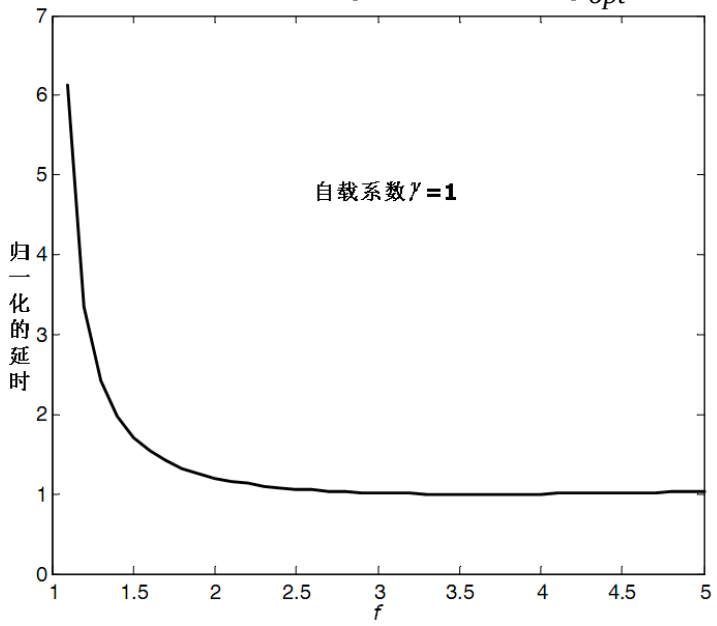
CMOS反相器的动态特性

- 反相器链的正确级数

$$f_{opt} = \sqrt[4]{F}$$

$$N > 4,\ f = \sqrt[N]{F} < f_{opt}$$





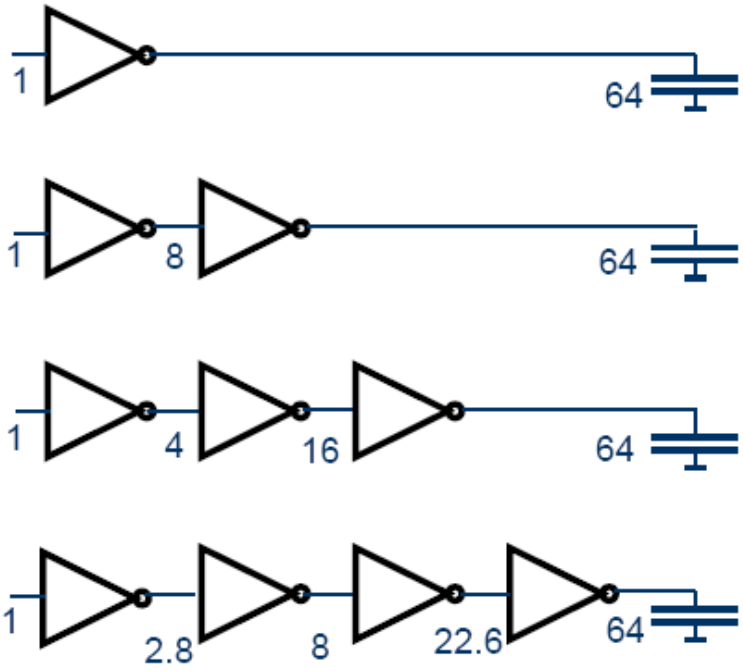
不同驱动器结构的t_{opt}/t_{p0}与F的关系

F	无缓冲器	两级反相器	反相器链
10	11	8.3	8.3
100	101	22	16.5
1000	1001	65	24.8
10,000	10,001	202	33.1

CMOS反相器的动态特性

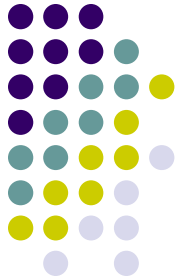
- 反相器链的正确级数

$$t_p = Nt_{p0}(1+\sqrt[N]{F}/\gamma)$$



N	f	t_p
1	64	65
2	8	18
3	4	15
4	2.8	15.3

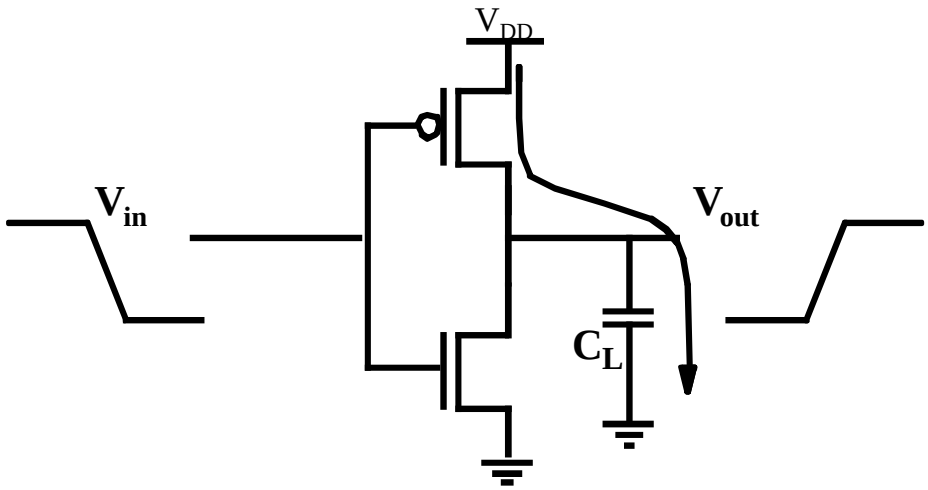
CMOS反相器的功耗能量和能量延时



- CMOS反相器的功耗包括
  - 动态功耗
    - 充放电电容
    - 短路电流
  - 静态功耗
    - 漏电电流

CMOS反相器的功耗能量和能量延时

- 动态功耗



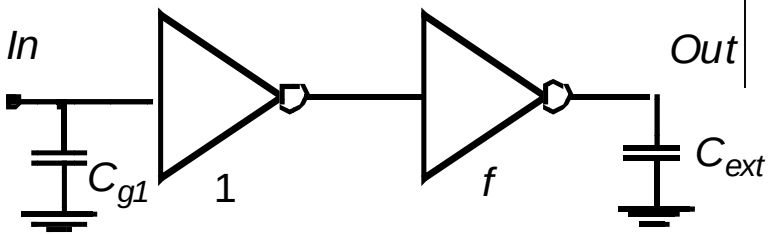
能量/翻转 $C_L V_{DD}^2$

功率=能量/翻转×频率= $C_L V_{DD}^2 f_{0\to1}$

- 从上式可以看出
  - 动态（翻转）的能量和功耗与驱动器件的电阻无关
  - 为减少功耗需要减少 C_L，V_{DD}，$f_{0\to1}$

CMOS反相器的功耗能量和能量延时

- 为减少能耗的尺寸优化



$$t_p = t_{p0}\left(\left(1+\frac{f}{\gamma}\right)+\left(1+\frac{F}{f\gamma}\right)\right)$$

$$t_{pHL} = 0.69\frac{3}{4}\frac{C_L V_{DD}}{I_{DSATn}} = 0.52\frac{C_L V_{DD}}{(W/L)_n k_n' V_{DSATn}(V_{DD}-V_{Tn}-V_{DSATn}/2)}$$

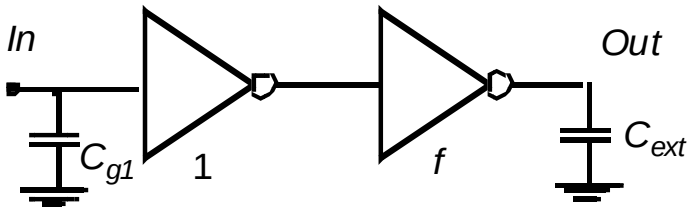
$$t_{p0} \sim \frac{V_{DD}}{V_{DD}-V_T-V_{DSAT}/2}$$

$$C_L = Cg1+(\gamma Cg1+fCg1)+(f\gamma Cg1+FCg1) = Cg1\left((1+\gamma)(1+f)+F\right)$$

$$E = V_{DD}^2 Cg1\left((1+\gamma)(1+f)+F\right)$$

CMOS反相器的功耗能量和能量延时

- 为减少能耗的尺寸优化



$$t_p = t_{p0}\left(\left(1+\frac{f}{\gamma}\right)+\left(1+\frac{F}{f\gamma}\right)\right)$$

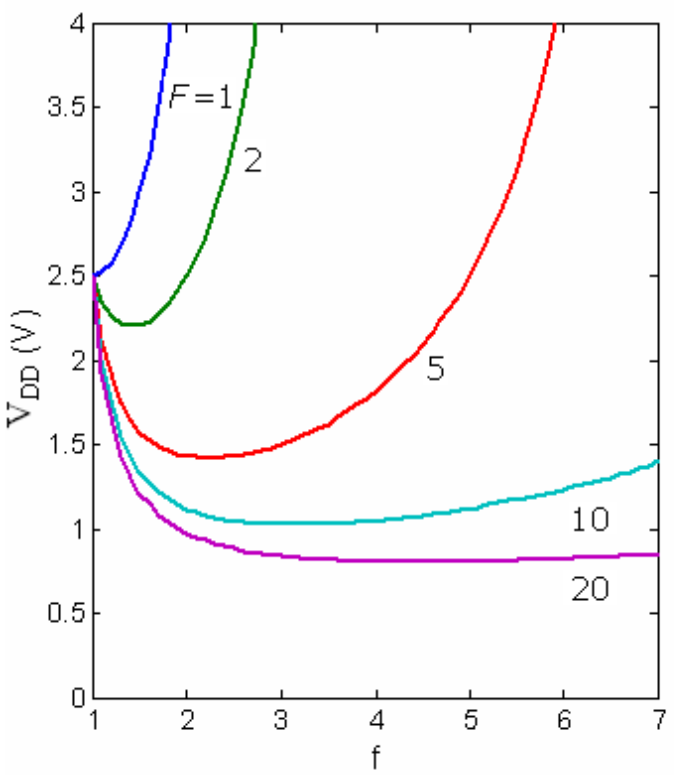
  - 性能约束就是指尺寸放大电路的传播延时应当等于或小于参考电路（f=1，$V_{dd}=V_{ref}$）的延时

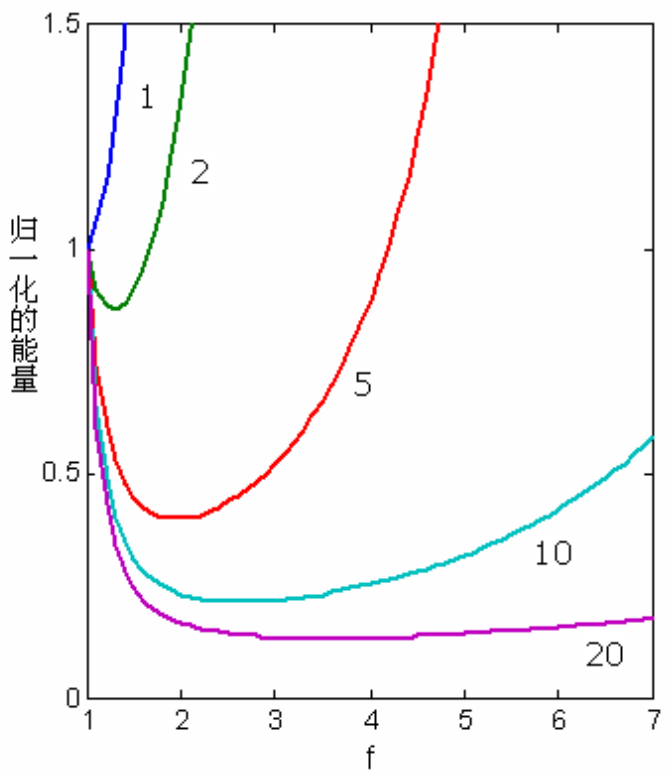
$$\frac{t_p}{t_{pref}} = \frac{t_{p0}\left(2+f+\frac{F}{f}\right)}{t_{p0ref}\left(3+F\right)} = \left(\frac{V_{DD}}{V_{ref}}\right)\left(\frac{V_{ref}-V_{TE}}{V_{DD}-V_{TE}}\right)\left(\frac{2+f+\frac{F}{f}}{3+F}\right) = 1$$

$$\frac{E}{E_{ref}} = \left(\frac{V_{DD}}{V_{ref}}\right)^2\left(\frac{2+2f+F}{4+F}\right)$$

CMOS反相器的功耗能量和能量延时

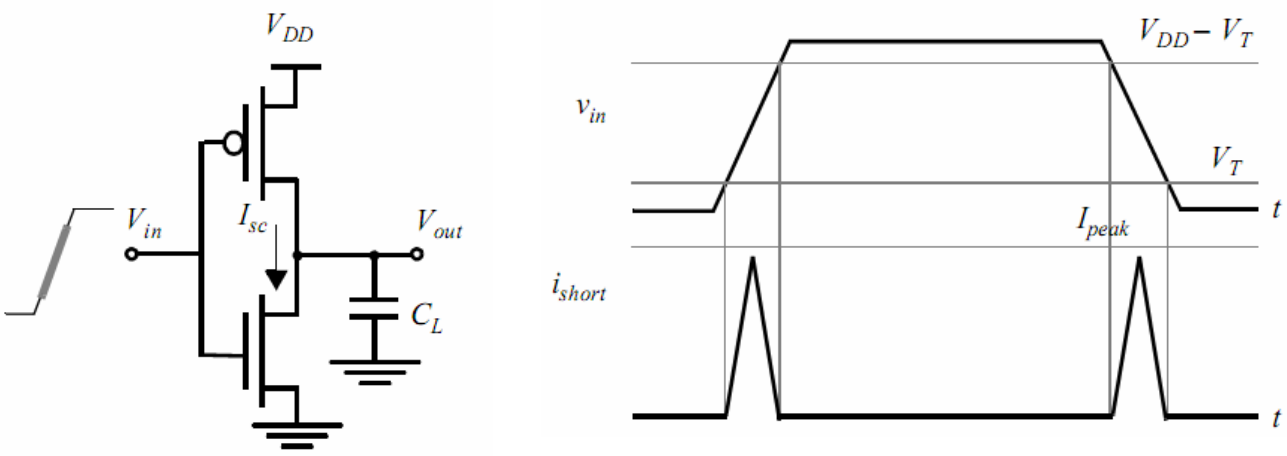
- 为减少能耗的尺寸优化
  - 改变器件尺寸并降低电源电压是减小逻辑电路能耗的有效办法
  - 在最优值之外过多加大晶体管尺寸会消耗更多能量





CMOS反相器的功耗能量和能量延时

- 直接通路电流引起的功耗
  - 输入信号的逐渐变化造成了开关过程中V_{DD}和GND之间在短期内出现一条直流通路，此时NMOS和PMOS管同时导通

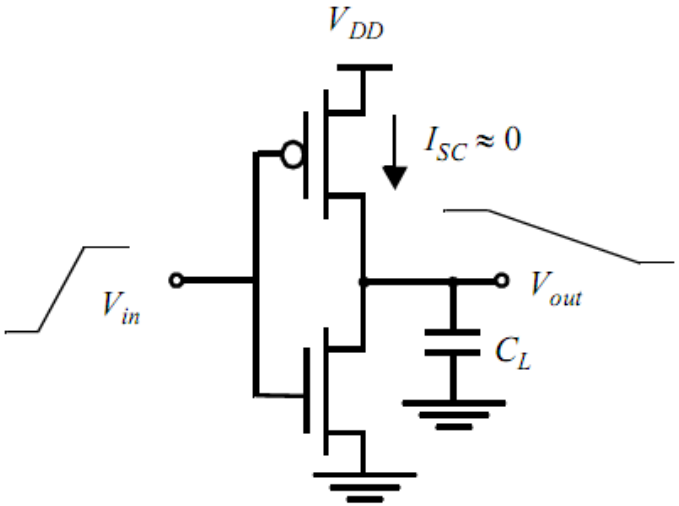


$$E_{dp} = V_{DD}\frac{I_{peak}t_{sc}}{2} + V_{DD}\frac{I_{peak}t_{sc}}{2} = V_{DD}I_{peak}t_{sc}$$

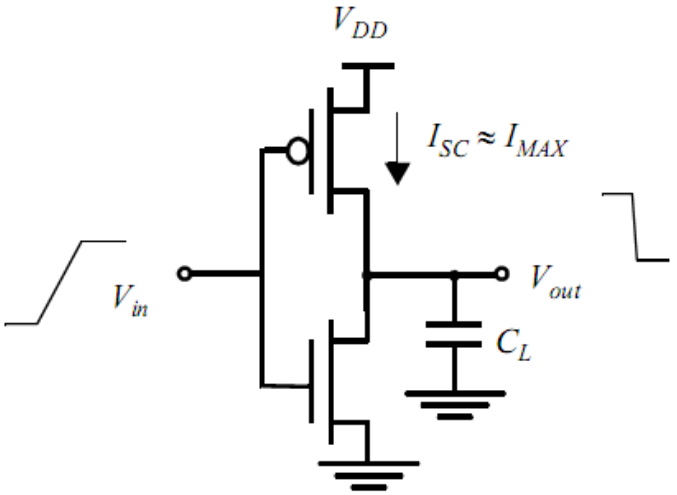
$$P_{dp} = V_{DD}I_{peak}t_{sc}f = C_{sc}V_{DD}^2 f$$

CMOS反相器的功耗能量和能量延时

- 直接通路电流引起的功耗
  - 峰值短路电流
    - 取决于器件的饱和电流，因此与器件的尺寸有关
    - 降低电源电压可以减少短路电流
    - 与输入输出的斜率比有关



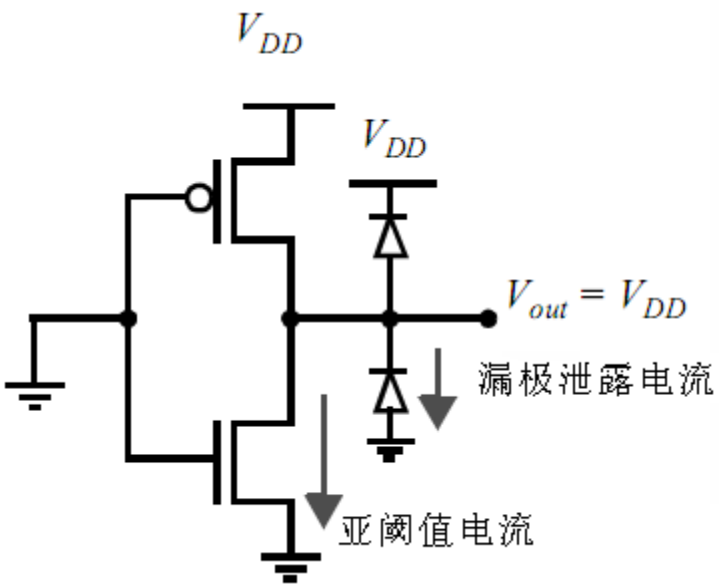
大电容负载



小电容负载

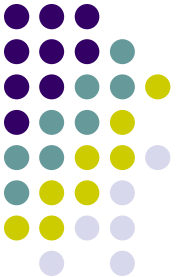
CMOS反相器的功耗能量和能量延时

- 静态功耗
  - 峰值短路电流（漏电流功耗）



$$P_{stat} = I_{stat} V_{DD}$$

CMOS反相器的功耗能量和能量延时



- 综合考虑
  - 总功耗

$$P_{tot} = P_{dyn} + P_{dp} + P_{stat} = \left(C_L V_{DD}^2 + V_{DD} I_{peak} t_s \right) f_{0\to 1} + V_{DD} I_{leak}$$

  - 功耗-延时积或每操作的能量损耗

$$PDP = P_{av} t_p$$

$$PDP = C_L V_{DD}^2 f_{\max} t_p = \frac{C_L V_{DD}^2}{2}$$

  - 能量-延时积

$$EDP = PDP \times t_p = P_{av} t_p^2 = \frac{C_L V_{DD}^2}{2} t_p$$