1. Description

1.1. Project

Project Name	sw_table_stm32
Board Name	custom
Generated with:	STM32CubeMX 6.14.1
Date	11/20/2025
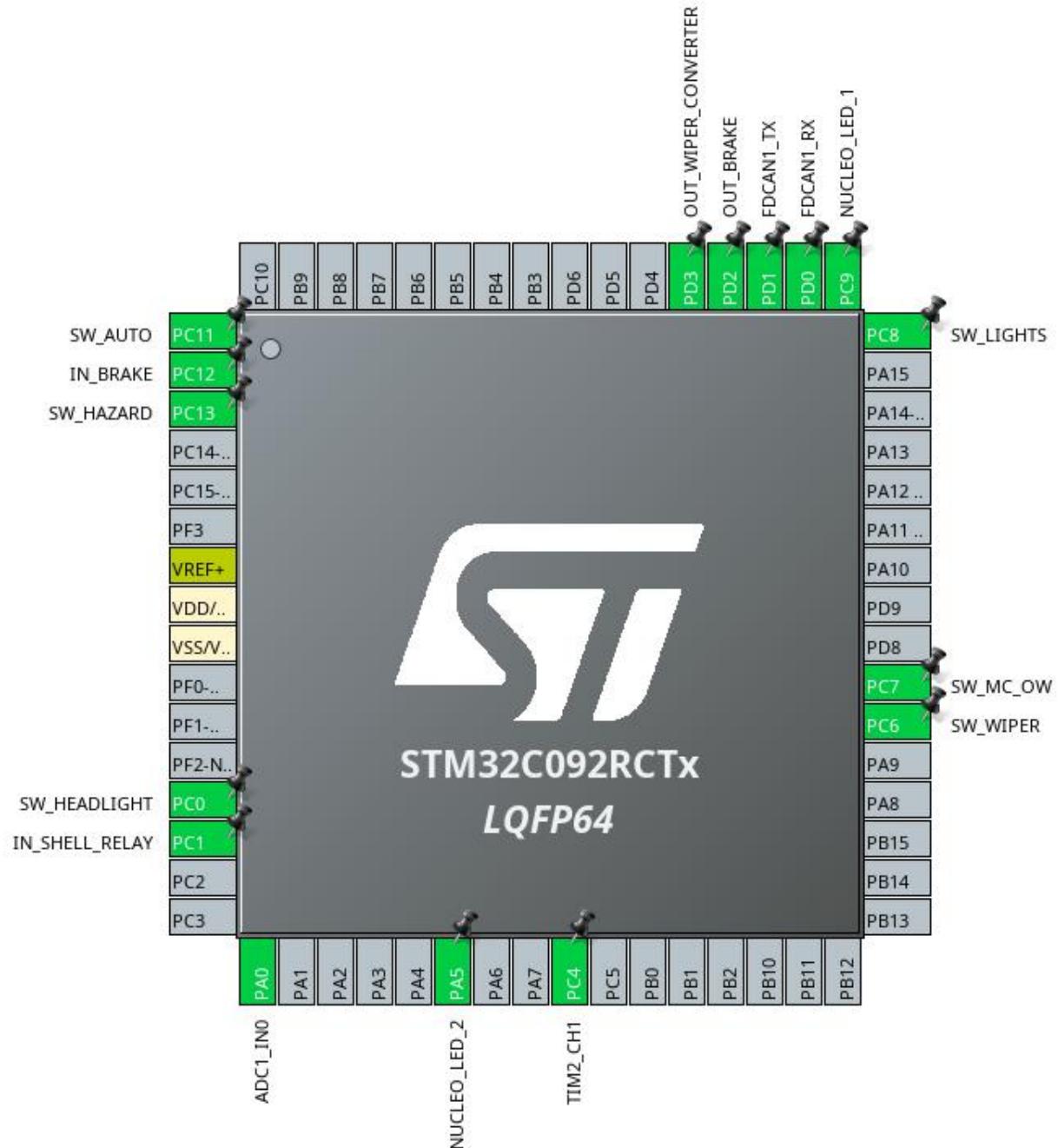
1.2. MCU

MCU Series	STM32C0
MCU Line	STM32C0x2
MCU name	STM32C092RCTx
MCU Package	LQFP64
MCU Pin number	64

1.3. Core(s) information

Core(s)	ARM Cortex-M0+

2. Pinout Configuration
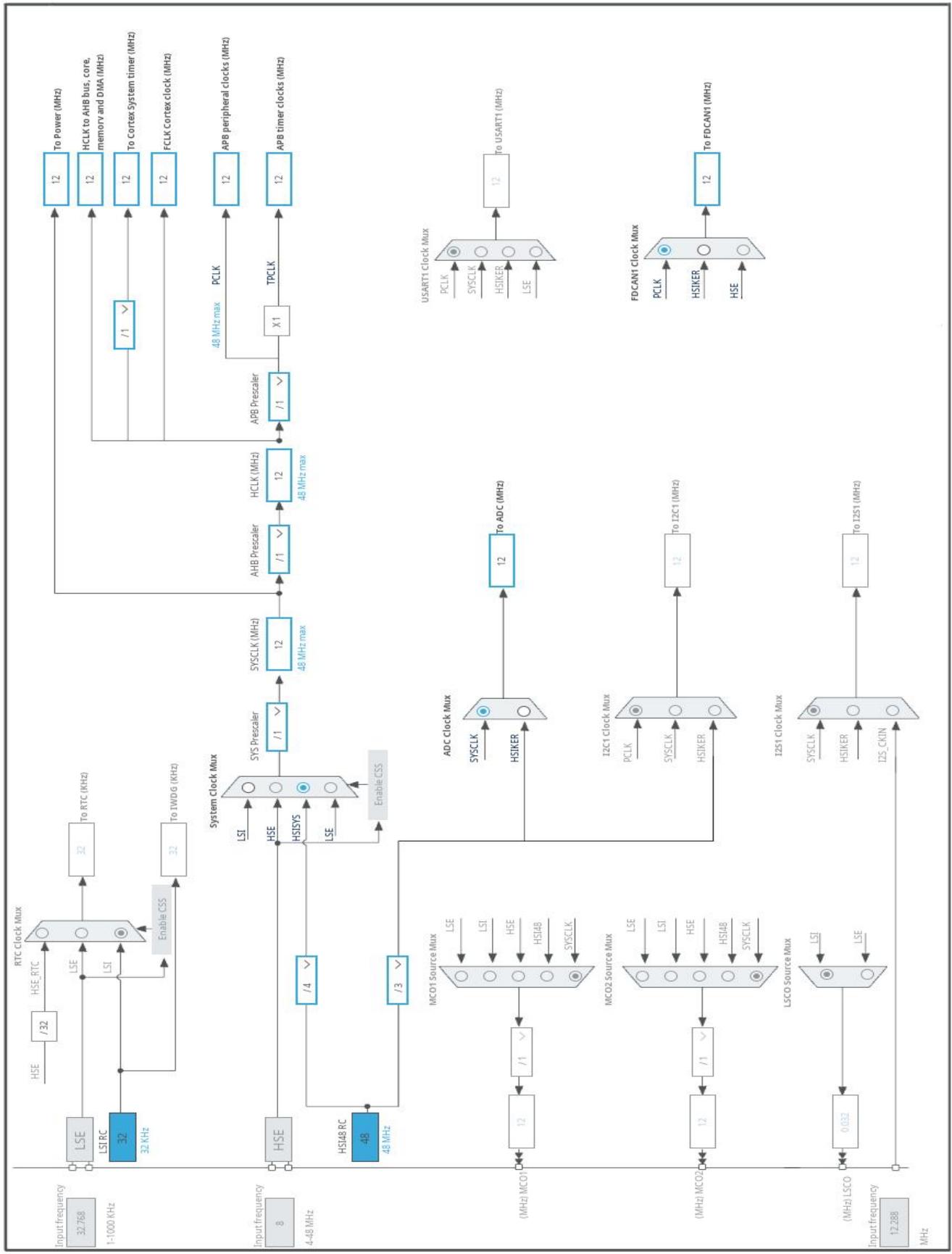
3. Pins Configuration

Pin Number LQFP64	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
1	PC11 *	I/O	GPIO_Input	SW_AUTO
2	PC12 *	I/O	GPIO_Input	IN_BRAKE
3	PC13 *	I/O	GPIO_Input	SW_HAZARD
7	VREF+	MonoIO		
8	VDD/VDDA	Power		
9	VSS/VSSA	Power		
13	PC0 *	I/O	GPIO_Input	SW_HEADLIGHT
14	PC1 *	I/O	GPIO_Input	IN_SHELL_RELAY
17	PA0	I/O	ADC1_IN0	
22	PA5 *	I/O	GPIO_Output	NUCLEO_LED_2
25	PC4	I/O	TIM2_CH1	
38	PC6 *	I/O	GPIO_Input	SW_WIPER
39	PC7 *	I/O	GPIO_Input	SW_MC_OW
48	PC8 *	I/O	GPIO_Input	SW_LIGHTS
49	PC9 *	I/O	GPIO_Output	NUCLEO_LED_1
50	PD0	I/O	FDCAN1_RX	
51	PD1	I/O	FDCAN1_TX	
52	PD2 *	I/O	GPIO_Output	OUT_BRAKE
53	PD3 *	I/O	GPIO_Output	OUT_WIPER_CONVERTER

* The pin is affected with an I/O function

4. Clock Tree Configuration

1. Power Consumption Calculator report

1.1. Microcontroller Selection

Series	STM32C0
Line	STM32C0x2
MCU	STM32C092RCTx
Datasheet	DS14720_Rev1

1.2. Parameter Selection

Temperature	25
Vdd	3.0

1.3. Battery Selection

Battery	Li-SOCL2(AAA700)
Capacity	700.0 mAh
Self Discharge	0.08 %/month
Nominal Voltage	3.6 V
Max Cont Current	10.0 mA
Max Pulse Current	30.0 mA
Cells in series	1
Cells in parallel	1
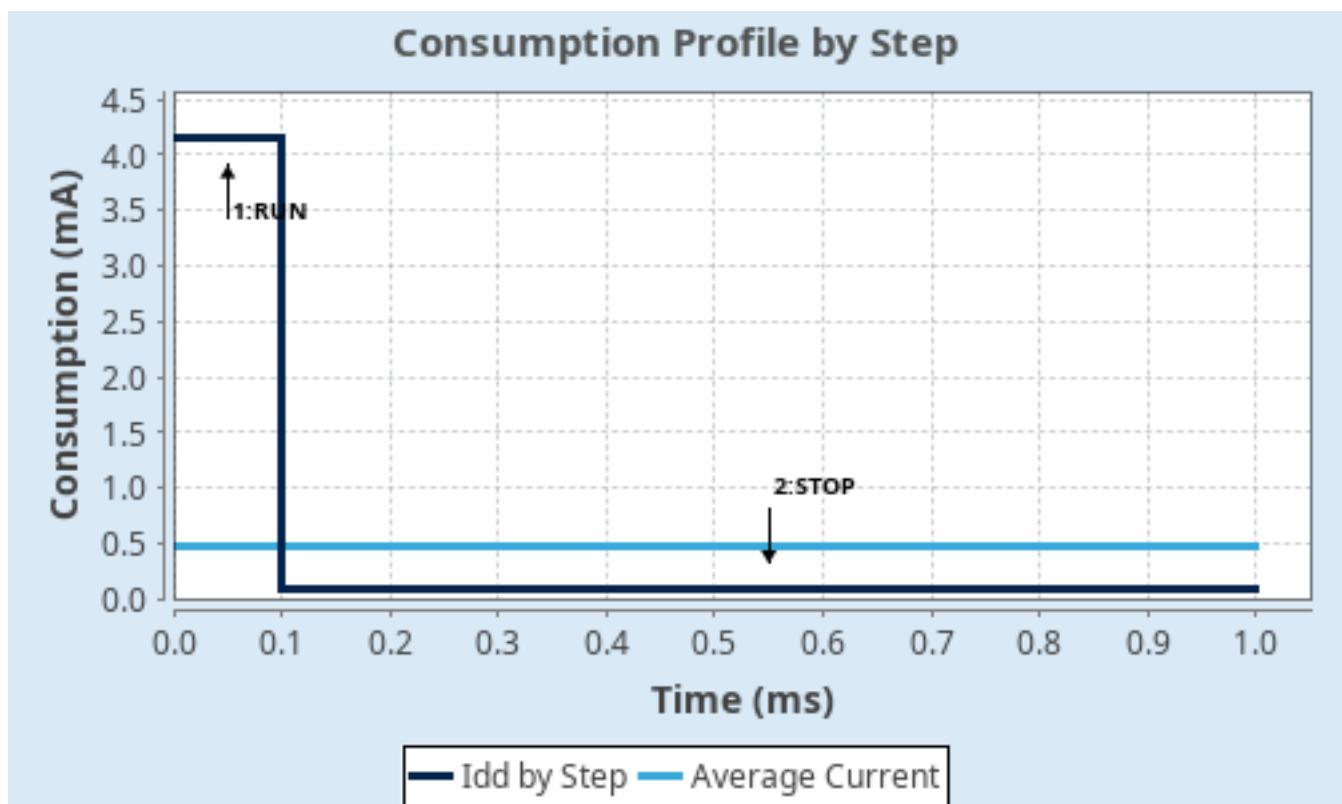
1.4. Sequence

Step	Step1	Step2
Mode	RUN	STOP
Vdd	3.0	3.0
Voltage Source	Battery	Battery
Range	NaN/SMPS	NaN/SMPS
Fetch Type	FLASH/Cache/PREFETCH	Flash-PowerDownStop
CPU Frequency	48 MHz	0 Hz
Clock Configuration	HSI	ALL_CLOCKS_OFF
Clock Source Frequency	48 MHz	0 Hz
Peripherals		
Additional Cons.	0 mA	0 mA
Average Current	4.15 mA	79 µA
Duration	0.1 ms	0.9 ms
DMIPS	60.0	0.0
Ta Max	129.5	129.99
Category	In DS Table	In DS Table

1.5. Results

Sequence Time	1 ms	Average Current	486.1 µA
Battery Life	1 month, 29 days, 11 hours	Average DMIPS	60.0 DMIPS

1.6. Chart

Consumption Profile by Step

2. Software Project

2.1. Project Settings

Name	Value
Project Name	sw_table_stm32
Project Folder	/home/varma01/Documents/szenergy/stm32/sw_table_stm32
Toolchain / IDE	STM32CubeIDE
Firmware Package Name and Version	STM32Cube FW_C0 V1.4.0
Application Structure	Advanced
Generate Under Root	Yes
Do not generate the main()	No
Minimum Heap Size	0x200
Minimum Stack Size	0x400

2.2. Code Generation Settings

Name	Value
STM32Cube MCU packages and embedded software	Copy only the necessary library files
Generate peripheral initialization as a pair of '.c/.h' files	No
Backup previously generated files when re-generating	No
Keep User Code when re-generating	Yes
Delete previously generated files when not re-generated	Yes
Set all free pins as analog (to optimize the power consumption)	No
Enable Full Assert	No

2.3. Advanced Settings - Generated Function Calls

Rank	Function Name	Peripheral Instance Name
1	SystemClock_Config	RCC
2	MX_GPIO_Init	GPIO
3	MX_FDCAN1_Init	FDCAN1
4	MX_ADC1_Init	ADC1
5	MX_TIM1_Init	TIM1
6	MX_TIM2_Init	TIM2

3. Peripherals and Middlewares Configuration

3.1. ADC1

mode: IN0

3.1.1. Parameter Settings:

ADC_Settings:

Clock Prescaler	Synchronous clock mode divided by 1
Resolution	ADC 12-bit resolution
Data Alignment	Right alignment
Sequencer	Sequencer set to not fully configurable
Scan Conversion Mode	Forward
Continuous Conversion Mode	Disabled
Discontinuous Conversion Mode	Disabled
DMA Continuous Requests	Disabled
End Of Conversion Selection	End of single conversion
Overrun behaviour	**Overrun data overwritten ***
Low Power Auto Wait	Disabled
Auto Off	Disabled
Oversampling Mode	Disabled

ADC_Regular_ConversionMode:

SamplingTime Common 1	1.5 Cycles
External Trigger Conversion Source	Regular Conversion launched by software
External Trigger Conversion Edge	None
Trigger Frequency	High frequency

Analog Watchdog 1:

Enable Analog WatchDog1 Mode	false

Analog Watchdog 2:

Watchdog Mode	Multiple channels
Number Of Channel can be monitored	1
1st Channel	None

Analog Watchdog 3:

Watchdog Mode	Multiple channels
Number Of Channel can be monitored	1
1st Channel	None

3.2. FDCAN1

mode: Activated

3.2.1. Parameter Settings:

Basic Parameters:

Clock Divider	Divide kernel clock by 1
Frame Format	Classic mode
Mode	Normal mode
Auto Retransmission	Disable
Transmit Pause	Disable
Protocol Exception	Disable
Nominal Sync Jump Width	**2 ***
Data Prescaler	1
Data Sync Jump Width	**11 ***
Data Time Seg1	**12 ***
Data Time Seg2	**11 ***
Std Filters Nbr	**2 ***
Ext Filters Nbr	0
Tx Fifo Queue Mode	FIFO mode

Bit Timings Parameters:

Nominal Prescaler	**1 ***
Nominal Time Quantum	**83.33333333333333 ***
Nominal Time Seg1	**21 ***
Nominal Time Seg2	**2 ***
Nominal Time for one Bit	**2000 ***
Nominal Baud Rate	**500000 ***

3.3. RCC
3.3.1. Parameter Settings:

System Parameters:

VDD voltage (V)	3.3
Instruction Cache	Enabled
Prefetch Buffer	Disabled
Data Cache	Enabled
Flash Latency(WS)	0 WS (1 HCLK cycle)

RCC Parameters:

HSI Calibration Value	64
HSE Startup Timout Value (ms)	100
LSE Startup Timout Value (ms)	5000

3.4. SYS

Timebase Source: SysTick

3.5. TIM1

Clock Source   : Internal Clock

3.5.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	**1 ***
Counter Mode	Up
Counter Period (AutoReload Register - 16 bits value)	**20000-1 ***
Internal Clock Division (CKD)	No Division
Repetition Counter (RCR - 16 bits value)	0
auto-reload preload	Disable

Trigger Output (TRGO) Parameters:

Master/Slave Mode (MSM bit)	Disable (Trigger input effect not delayed)
Trigger Event Selection TRGO	Reset (UG bit from TIMx_EGR)
Trigger Event Selection TRGO2	Reset (UG bit from TIMx_EGR)

3.6. TIM2

Clock Source   : Internal Clock

Channel1: PWM Generation CH1

3.6.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	**4-1 ***
Counter Mode	Up
Counter Period (AutoReload Register - 32 bits value)	**60000-1 ***
Internal Clock Division (CKD)	No Division
auto-reload preload	Disable

Trigger Output (TRGO) Parameters:

Master/Slave Mode (MSM bit)	Disable (Trigger input effect not delayed)
Trigger Event Selection TRGO	Reset (UG bit from TIMx_EGR)

Clear Input:

Clear Input Source	Disable

PWM Generation Channel 1:

Mode	PWM mode 1
Pulse (32 bits value)	0
Output compare preload	Enable
Fast Mode	Disable
CH Polarity	High

* User modified value

4. System Configuration

4.1. GPIO configuration

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
ADC1	PA0	ADC1_IN0	Analog mode	No pull-up and no pull-down	n/a	
FDCAN1	PD0	FDCAN1_RX	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PD1	FDCAN1_TX	Alternate Function Push Pull	No pull-up and no pull-down	Low	
TIM2	PC4	TIM2_CH1	Alternate Function Push Pull	No pull-up and no pull-down	Low	
GPIO	PC11	GPIO_Input	Input mode	**Pull-down ***	n/a	SW_AUTO
	PC12	GPIO_Input	Input mode	**Pull-down ***	n/a	IN_BRAKE
	PC13	GPIO_Input	Input mode	**Pull-down ***	n/a	SW_HAZARD
	PC0	GPIO_Input	Input mode	**Pull-down ***	n/a	SW_HEADLIGHT
	PC1	GPIO_Input	Input mode	**Pull-down ***	n/a	IN_SHELL_RELAY
	PA5	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	NUCLEO_LED_2
	PC6	GPIO_Input	Input mode	**Pull-down ***	n/a	SW_WIPER
	PC7	GPIO_Input	Input mode	**Pull-down ***	n/a	SW_MC_OW
	PC8	GPIO_Input	Input mode	**Pull-down ***	n/a	SW_LIGHTS
	PC9	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	NUCLEO_LED_1
	PD2	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	OUT_BRAKE
	PD3	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	OUT_WIPER_CONVERTER

4.2. DMA configuration

nothing configured in DMA service

4.3. NVIC configuration

4.3.1. NVIC

Interrupt Table	Enable	Preenmption Priority	SubPriority
Non maskable interrupt	true	0	0
Hard fault interrupt	true	0	0
System service call via SWI instruction	true	0	0
Pendable request for system service	true	0	0
System tick timer	true	3	0
TIM1 break, update, trigger and commutation interrupts	true	0	0
FDCAN1 interrupt 0	true	0	0
Flash global interrupt	unused		
RCC global interrupt	unused		
ADC1 interrupt	unused		
TIM1 capture compare interrupt	unused		
TIM2 global interrupt	unused		
FDCAN1 interrupt 1	unused		

4.3.2. NVIC Code generation
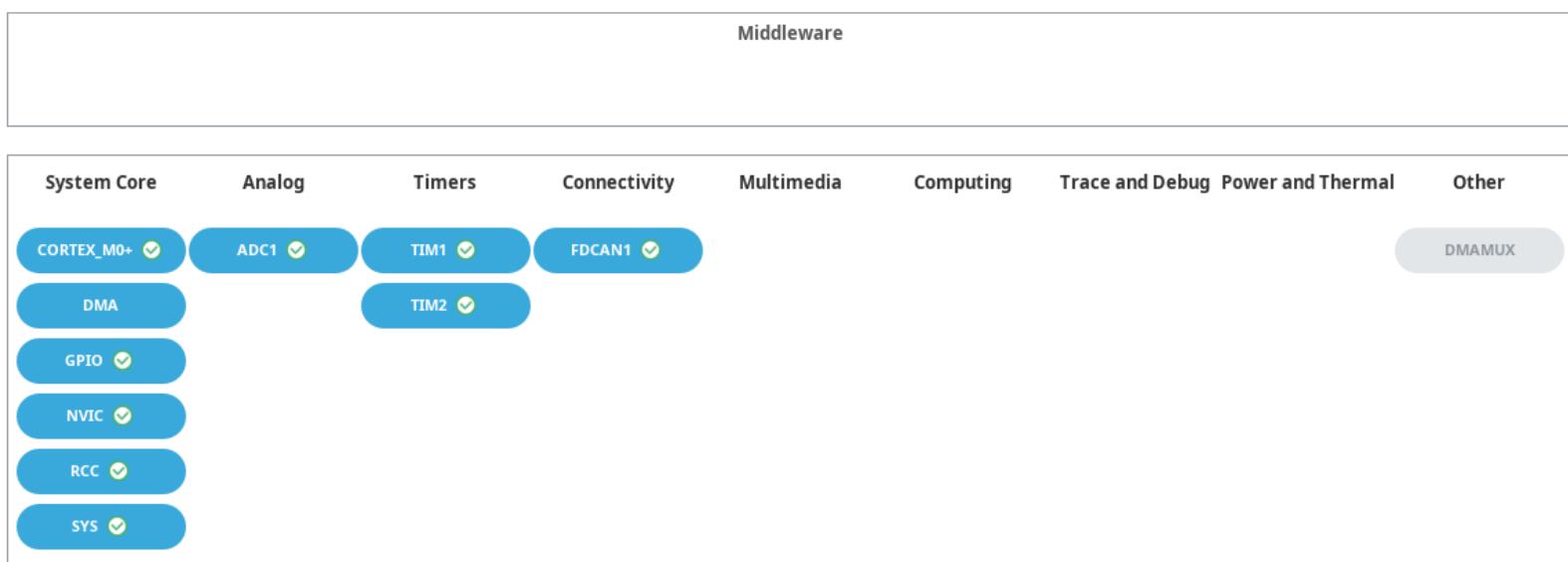
Enabled interrupt Table	Select for init sequence ordering	Generate IRQ handler	Call HAL handler
Non maskable interrupt	false	true	false
Hard fault interrupt	false	true	false
System service call via SWI instruction	false	true	false
Pendable request for system service	false	true	false
System tick timer	false	true	true
TIM1 break, update, trigger and commutation interrupts	false	true	true
FDCAN1 interrupt 0	false	true	true

* User modified value

5. System Views

5.1. Category view

5.1.1. Current

								Middleware

System Core	Analog	Timers	Connectivity	Multimedia	Computing	Trace and Debug	Power and Thermal	Other
CORTEX_M0+ ✓	ADC1 ✓	TIM1 ✓	FDCAN1 ✓					DMAMUX
DMA		TIM2 ✓						
GPIO ✓								
NVIC ✓								
RCC ✓								
SYS ✓								

6. Docs & Resources

Type   Link