FML a VM implemented in SML

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1 Introduction

For our project we have decided to build a virtual machine(VM) in SML. The name FML is just an arbitrary thre letter name and has no meaning or interpertation. The VM is a RISC machine using a Von-Neuman architecture. It has a very minimalistic instruction set. The design of FML resembles those of older 8-bit architectures such as the MOS 6510 and the Z80 microprocessors commonly in use during the late 70s and early 80s. The FML machine has no "bus width" and works exclusivley with signed integers[1]. The lack of a physical bus enables the VM to do things wich an ordinary CPU could not achive such as reading from two registers at the same time. Even though the cpu have very few operations (only 27) a very effective instruction set architecture makes these operations very flexibels and there are roughly 600 accepted instructions.

So even though FML is a very minimalistic machine it is quite powerfull.

We have allso built a fully featured assembler for the FML machine.

[1] The details of the integers used are dependent on which SML implementation is used