Taylor **Lloyd**

Software Developer · Computer Scientist

Seattle, Washington

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Work Experience

Amazon.com, Robotics - Industrial Internet of Things (IIoT)

Seattle, Washington, USA

Software Development Engineer II — *May '19 - Present*

- Designed and implemented a DSP and GPU-accelerated image processing pipeline for mobile SoCs.
- Designed and implemented a serverless corporate device management solution using AWS IoT and Lambda.
- Designed and implemented Android OS modifications to expose custom hardware peripherals.
- Implemented a realtime projected-light augmented reality system for sortation use-cases.
- Mentored teammates and interns through work review and weekly 1-on-1s

Amazon.com, Alexa for Business

Seattle, Washington, USA

Software Development Engineer I — *May '18 - May '19*

- Designed and implemented Polycom video conferencing integration with Alexa for Business.
- Implemented Full-CD policies for team, including testing requirements and automated deployments.

IBM Canada, Compilers Group / Cloud Innovation Lab

Toronto, Ontario, Canada

CAS Student Fellow / Co-op Software Developer — *Dec. '15 - May '16, May '14 - June '15*

- Implemented GPU data transfer for OpenMP 4.5 in the XL compiler.
- Prototyped and shipped novel GPU loop optimizations, speeding GPU execution by 25%.
- Developed a functional programming language (IBM Dash) and compiler for GPU execution. Wrote language specifications, compiler optimizations, and language runtime extensions.
- Implemented automated testing and continuous deployment on projects across the team with GitLab and Jenkins.

Amazon.com, Fulfillment Technologies

Seattle, Washington, USA

Software Development Engineer Intern — *Sept. '13 - Mar. '14, June '15 - Aug. '15*

- Designed, implemented, and supported an Android chat application with Microsoft Lync integration.
- Designed and implemented bandwidth-aware security camera tablet application, monitoring thousands of warehouse cameras.
- Worked with a small (4-6) person team under an Agile continuous delivery process to support and update thousands of Android devices.

Projects

GPUCheck

Static GPU Performance Analysis

GPUCheck detects GPU performance problems like non-coalescable memory accesses and divergent branches through LLVM analysis. GPUCheck improves benchmark performance up to 25%, and can be integrated into the build process of any GPU executable compiled using LLVM.

Wedding RFID

Tracking/Guidance for Guests

Guests are issued an RFID tag, used at terminals throughout the event. Tags are tied to guests by web API, while touchscreens and RFID sensors allow interaction. The terminals allow sign-in, direct guests to seats, and track engagement.

Skills

Programming Languages

C/C++, Java, CUDA, Golang, Python, LaTeX

Platforms & Frameworks

Lambda, AWS IoT, LLVM/Clang, OpenMP, OpenCL, Android, Linux

Areas of Interest

Heterogeneous Computing, Mobile Development, GPU Acceleration, Compiler Optimizations

Education

M.Sc. Computing Science

University of Alberta

- Specialization in Compiler Optimizations for GPU Computing
- GPA 4.0/4.0

B.Sc. Specialization in Computing Science

University of Alberta

- GPA 3.6/4.0

Publications & Presentations

Memory-access-aware Safety and Profitability Analysis for Transformation of Accelerator-bound OpenMP Loops
ACM Transactions on Architecture and Code Optimization - ACO — *July '19*

Program Analysis and Compiler Transformations for Computational Accelerators — *Edmonton, Alberta, Canada*
University of Alberta Master's Thesis — *May '18*

GPUCheck: Detecting CUDA Thread Divergence with Static Analysis
Education & Research Archive - ERA — *March '18*

Automated GPU Grid Geometry Selection for OpenMP Kernels — *Lyon, France*
Workshop on Applications for Multi-Core Architectures - WAMCA — *Sept '18*

Run-Length Base-Delta Encoding for High-Speed Compression — *Eugene, Oregon, USA*
International Conference on Parallel Processing - ICPP — *Aug '18*

Divergence and Arithmetic Control Form: Analyzing GPU Applications — *Markham, Ontario, Canada*
16th Compiler-Driven Performance Workshop - CASCON — *Nov '17*

Run-length base-delta encoding for high-speed compression
US Patent US11070230B2 — *Nov '17*

A Case for Better Integration of Host and Target Compilation When Using OpenCL for FPGAs — *Ghent, Belgium*
FPGAs for Software Programmers - FSP — *Sept '17*

GPGPU Offloading with OpenMP 4.5 in the IBM XL Compiler — *Markham, Ontario, Canada*
15th Compiler-Driven Performance Workshop - CASCON — *Nov '16*

Minimizing execution time of a compute workload based on adaptive complexity estimation
US Patent US10389800B2 — *Oct '16*

Modern analytics with the IBM Dash Compiler — *Markham, Ontario, Canada*
13th Compiler-Driven Performance Workshop - CASCON — *Nov '14*

Honors & Awards

2018 **Outstanding Thesis Award - Runner-up**, University of Alberta — *Edmonton, AB*
2017 **Queen Elizabeth II Graduate Scholarship - Master's Level**, University of Alberta — *Edmonton, AB*
2013, 2015 **Dean's Honor Roll**, University of Alberta — *Edmonton, AB*
2013 **Undergraduate Student Research Award(USRA)**, NSERC — *Edmonton, AB*
2013 **Amdahl Academic Scholarship in Computing Science**, University of Alberta — *Edmonton, AB*
2011, 2012 **Jason Lang Academic Excellence**, University of Alberta — *Edmonton, AB*
2010 **Academic Excellence**, University of Alberta — *Edmonton, AB*
2009 **First Place - Iverson Computing Science Exam**, University of Alberta — *Edmonton, AB*