NMOS Switched Voltage Controlled Oscillator

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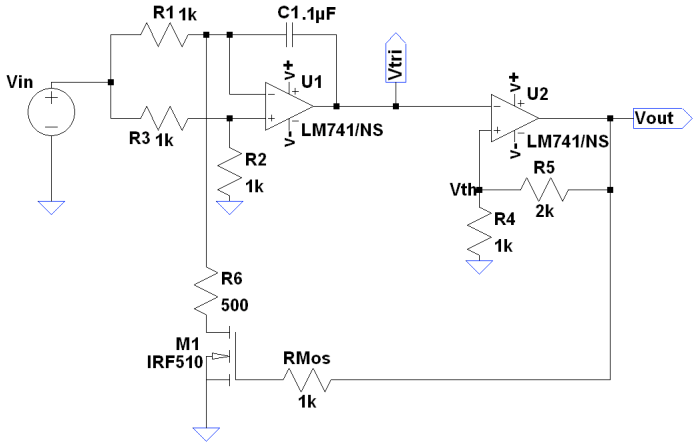


Fig. 1. MOSFET Switched DC Voltage to Frequency Converter

I. Introduction

Voltage controlled oscillators, i.e. voltage to frequency converters, are used in a wide range of applications. Some of these applications include audio synthesizers, phase locked loops, digital clocks, function generators, and communication circuits. This paper presents a NMOS switched, two op-amp voltage controlled relaxation oscillator, figure 1. The operation of this circuit will be discussed, as well as a method for deriving an expression for the output frequency as a function of input voltage. Factors affecting the circuit's output frequency are discussed, and demonstrated through simulation and experimentation.

II. Principles of Operation

The voltage to frequency converter shown in figure 1 consists of three main stages. The first stage is an integrator, the second a Schmitt trigger, and the final stage is an NMOS "switch". The input to the circuit is a DC voltage. This input voltage can range from 0.5V to 30V, as tested. A qualitative overview for the operation of this circuit will be divided into three sections. Each stage of the circuit will be examined in each of these sections. An analysis for determining the frequency of oscillation will be presented in a later section.

A. Startup

1) Integrator: It is assumed that the circuit is at "rest" upon startup. The startup conditions consist of a DC input voltage source being turned on. This action has the s-domain equivalent of a step function, $\frac{1}{s}$. Superposition was used to find the transfer function of the integrator stage, see Equation 1.

$$H(s)_{integrator} = \frac{1 \times 10^{-4}s - 1}{2 \times 10^{-4}s} \tag{1}$$

The step response of the first stage is :

$$H(s)_{integrator} = \frac{1 \times 10^{-4}s - 1}{2 \times 10^{-4}s^2} \tag{2}$$

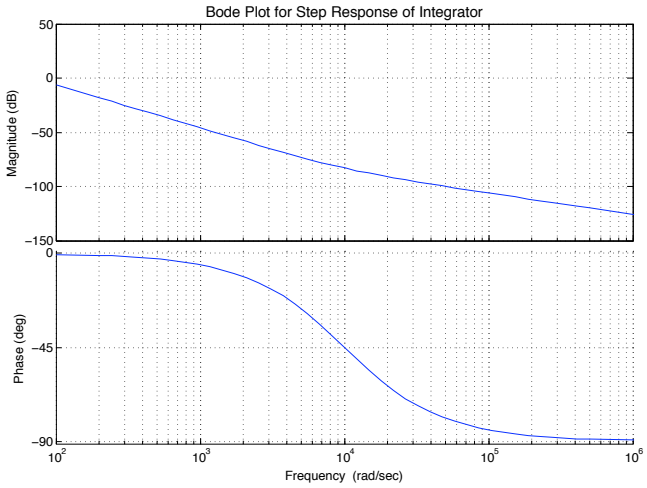
A frequency domain and time domain plot of this step response can be seen in figure 2. The bode plot shows a frequency response very similar to an ideal integrator's. The time domain plot shows that the integrator will produce a negative ramp. This ramp represents the capacitor's integration of the current. The end result is an increasingly negative voltage at the integrator output over time.

2) Schmitt Trigger: Initially, the output of the Schmitt trigger is at the negative rail of the op-amp. This means the threshold voltage, V_{th}, is negative as well. In order for the comparator output to change state to the positive rail, the voltage at it's inverting terminal, V_n, must become more negative. The output of this comparator can be determined by using Equation 4.

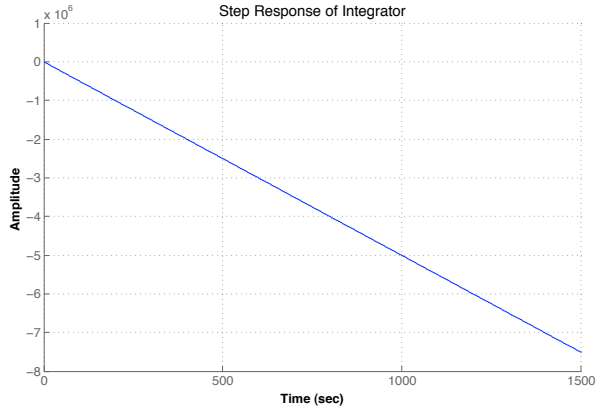
$$V_{O_{Comparator}} = A_o(V_{th} - V_n) \tag{3}$$

$$= A_o(\frac{V_s \cdot R_4}{R_4 + R_5} - V_n) \tag{4}$$

The voltage at V_n of the Schmitt Trigger is the output of the integrator, V_{tri}.



(a) Bode Plot of Integrator Step Response



(b) Integrator Step Response in Time Domain

Fig. 2. Time and Frequency Step Response of Integrator

3) NMOS Switch: At start up the switch is open. The voltage at it's gate is the output voltage of the Schmitt trigger. The condition $V_{gs} > V_t$ is not met; therefore, the transistor remains in the "cutoff" region of it's operation, i.e. switch is "open".

B. Transition of Switch from "Open" to "Closed"

1) Schmitt Trigger: The input voltage to the inverting terminal of the Schmitt Trigger is the output of the integrator. As seen previously, this voltage is becoming more negative over time. Eventually, the voltage at V_n of the Schmitt Trigger will fall below V_{th}. This will cause the comparator output to swing to the positive rail, see equation 4. The polarity of V_{th} will then change from negative to positive.

2) NMOS Switch: The NMOS will be analyzed as an ideal switch, meaning the impedance at it's drain is equivalent to that of a short. The condition $V_{gs} > V_t$ will be met after the comparator changes it's output state. This will drive the transistor into saturation; which effectively "closes" the switch. V_n is always equal to V_p in an ideal op-amp. The circuit in figure 1 shows that V_p and V_n of the integrator are equal to $\frac{1}{2}V_{in}$; as determined by the voltage divider network at V_p. Therefore, the current through the switch, i_d, is $\approx$ twice that flowing through R_1. For an input voltage of 1, this equates to a $500\mu A$ current through R_1, and a $1mA$ current through R_6. The remaining $500\mu A$ must come through the capacitor, C_1. This means the current through C_1 changes direction when the switch is closed.

3) Integrator: Previous to the switch closing, the current through the capacitor was flowing from V_n of the integrator to the output of the integrator. Therefore, a negative voltage developed on the side of the capacitor with respect to the integrator output. After the switch closes, the current changes direction and flows from the output of the integrator to V_n. The output of the integrator will begin to rise from $\approx -V_{th}$, as it is the integral of the current through the capacitor, see equation 5.

$$\Delta v_{cap} = \frac{1}{C_1}\int i_{cap}dt \tag{5}$$

C. Transition of Switch from "Closed" to "Open"

1) Schmitt Trigger: The ramping voltage at the output of the integrator will eventually rise to the positive V_{th} of the Schmitt Trigger. When this voltage becomes more positive than V_{th} the output of the Schmitt Trigger will go to the negative rail of the op-amp, see equation 4.

2) NMOS Switch: The negative rail voltage at the output of the Schmitt Trigger will cause the NMOS to go into the cutoff region of it's operation. This action is equivalent to opening the switch.

3) Integrator: The opening of the switch allows all of the current flowing through R_1, to again flow through the C_1. The change in current direction will cause integrator's output voltage to ramp down. This behavior is the same as that described in the section on the startup behavior of the integrator. However, the voltage is now ramping down from approximately positive V_{th}. Eventually, this voltage will reach negative V_{th}, and the cycle will repeat again.

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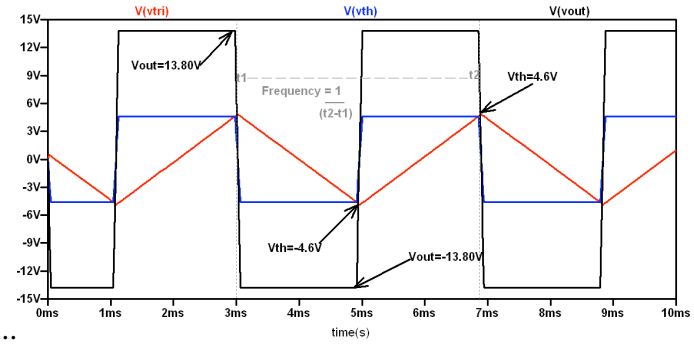


Fig. 3. SPICE Simulated Voltage Waveforms

D. Operation Summary

The following list is a summary of the circuit's operation. See figure 3 to view the waveforms associated with these steps:

1) After startup, the output voltage of the integrator, V_{tri}, ramps in the negative direction.
2) When $V_{tri} < V_{th}$, V_{out} will go from negative to positive rail.
3) V_{out} is at positive rail; therefore, V_{th} becomes positive.
4) The NMOS switch closes when V_{out} rails positive.
5) Current through the capacitor changes direction.
6) V_{tri} ramps in the positive direction.
7) When $V_{tri} > V_{th}$, V_{out} will rail negative.
8) The NMOS switch opens
9) The current through the capacitor changes direction; causing V_{tri} to ramp negative.
10) Go to step 2 and Repeat

Repeating steps 2 to 10 results in oscillation. The periodically produced negative and positive voltage ramps at the output of the integrator results in a symmetrical triangle wave. The swinging of the Schmitt Trigger output from negative to positive rail produces a symmetrical square wave, i.e. 50% duty cycle.

III. Theoretical Analysis

An equation for the relationship between the DC input voltage and output frequency of the circuit shown in figure 1 is now found. In order to find this equation, four initial assumptions about the circuit are made:

1) Circuit oscillates.
2) Op-amps are ideal.
3) Triangle and Square waves are symmetrical.
4) NMOS "switch" was closed, and is now open.

The startup transient of the circuit is not of interest, since it is assumed to be oscillating. Analyzing the circuit using the ideal op-amp model simplifies the process of finding the said equation. Real op-amp limitations such as input impedance, slew rate, and saturation voltages are not taken into account. Assuming symmetrical triangle and square waves also simplify the process of finding the equation, as will be shown. This symmetry implies that the time it takes to complete half of these waveforms is equivalent to $\frac{T}{2}$. This symmetry also allows us to analyze the circuit as it transitions from one state to the next. The circuit could very well be analyzed from the point in time when the NMOS switch was open and is closing. However, the opposite condition has been assumed.

The assumptions listed above lead to the following conditions in the circuit:

$$V_{th}(0^-) = V_s^+ \frac{R_4}{R_4 + R_5} = \frac{V_s^+}{3} \tag{6}$$

$$V_{th}(0^+) = V_s^- \frac{R_4}{R_4 + R_5} = \frac{V_s^-}{3} \tag{7}$$

$$V_{cap}(i) = V_{cap}(0^{-/+}) = V_{th}(0^-) \tag{8}$$

The change in V_{th} is due to the change in state of the comparator output, from positive rail to negative rail. However, the voltage across the capacitor cannot change instantaneously; therefore it's voltage stays the same right after the switch opens.

The non-inverting, V_p, and inverting, V_n, inputs in an ideal op-amp maintain the same voltage. Therefore, the voltages at the inputs of the integrator in figure 1 are equal, see equation 9.

$$V_n = V_p = V_{in} \frac{R_2}{R_2 + R_3} = \frac{V_{in}}{2} \tag{9}$$

Keeping the above assumptions, and observations in mind, it is now possible to get an equation for the relationship between the input voltage and output frequency. A step by step approach will be taken.

1) Find the Current through the Capacitor: The input impedance of an ideal op-amp is infinite; therefore, the current through R_1 is equivalent to the current through C_1, see equations 10 - 12.

$$i_{cap} = \frac{V_{in} - \frac{V_{in}}{2}}{R_1} = \frac{V_{in}}{2R_1} \tag{10}$$

$$i_{cap} = C_1 \frac{dv}{dt} \tag{11}$$

$$C_1 \frac{dv}{dt} = -\frac{V_{in}}{2R_1} \tag{12}$$

Current is traveling from V_n to the output of the first op-amp. Therefore, the voltage at the integrator output will be the same as the negative voltage developing across C_1. This explains where the negative sign comes from in the last line of equation 12.

2) Solve for Time: The time variable, t, in equation 12 can now be solved for.

$$\int_{V_{cap_i}}^{V_{cap_f}} dv = \int_0^t -\frac{V_{in}}{2R_1C_1} dt \tag{13}$$

$$V_{cap_f} - V_{cap_i} = -\frac{V_{in}t}{2R_1C_1} \tag{14}$$

V_{cap_f} will be approximately equal to $V_{th}(0^+)$, the voltage required to change the state of the Schmitt trigger. V_{cap_i} will be equal to $V_{th}(0^-)$, the initial voltage across the capacitor when the switch opened. Therefore, the left side of last line in equation 14 is equal to $-2V_{th}$. It was stated earlier that the circuit is being analyzed for half the period of oscillation; therefore $t = \frac{T}{2}$. Substituting these into equation 14 lead to the final expressions of the period and frequency of oscillation.

$$-2V_{th} = -\frac{V_{in}T}{4R_1C_1} \tag{15}$$

$$T = \frac{8V_{th}R_1C_1}{V_{in}} \tag{16}$$

$$f = \frac{V_{in}}{8V_{th}R_1C_1} \tag{17}$$

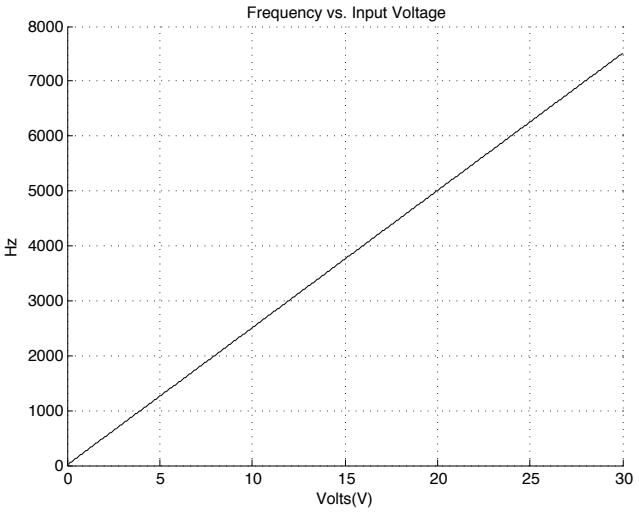


Fig. 4. Theoretical Frequency Output vs. Input Voltage

3) Frequency: Equation 17 provides a great deal of information about what affects the output frequency. DC input voltage, V_{in} is linearly proportional to frequency. Also, frequency can be increased by reducing R_1, C_1, and V_{th}. Placing the circuit elements values in the expression for f in equation 17 yields the following for the circuit in figure 1.

$$f = \frac{V_{in}}{4 \times 10^{-3}} = V_{in} \cdot 250 \tag{18}$$

Equation 18 shows that the output frequency will be a multiple of 250Hz. Equation 18 was plotted in MATLAB. Figure 4 shows that the theoretical output frequency is perfectly linear with respect to the voltage input.

IV. SPICE Simulation

The circuit in figure 1 was simulated in LT SPICE. Op-amp models for the LM741 were used. A default NMOS component was used to model the IRF510 transistor. The frequency of the output, and it's linearity, were measured for input voltages between 0V to 30V.

A. Waveforms

Figure 3 shows voltage waveforms for three points of interest: V_{th} (blue), V_{tri} (red), and V_{out} (black), for a V_{in} of 1V. This figure also shows how the frequency of the output is determined. The values for the three voltages listed differ from those

obtained with ideal models. This is expected. The Schmitt Trigger output is limited by the saturation voltage of the LM741, in this case $13.8V$. V_{th} is therefore $\frac{1}{3}$ of this, $4.6V$. It is also apparent from figure 3 that V_{out} does not change instantaneously.

B. Results

Figure 5 shows that as input voltage increases, output frequency changes less and less. Figure 6 shows that the simulated LM741 output deviates up to 60% from theoretical values.

The linearity of the VCO is an indicator of it's performance. The data for a discrete derivative of the frequency with respect to the input voltage was calculated in SPICE. This data was then exported to MATLAB to perform a linear regression. The result of this operation can be seen in figure 7. The data in figure 7 appears to vary greatly. This variation is due to precision limitations in the frequency difference calculation. It is well known that exceeding the precision for a certain number of bits results in overflow, or signed results. The linear regression was performed to correct for these errors. The fitted linear regression shows the frequency changes less and less as input voltages increase. This is evident by the negative slope of the red line.

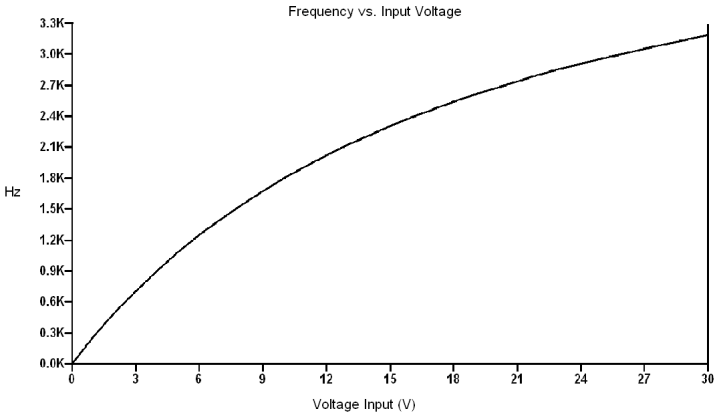


Fig. 5. SPICE Results for Frequency Output vs. Input Voltage

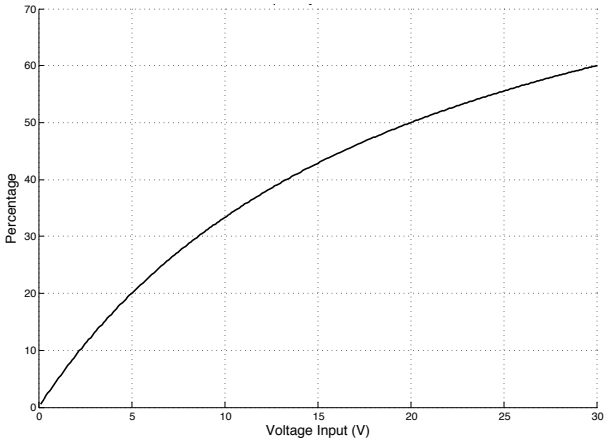


Fig. 6. Gain Error of SPICE Results vs. Theoretical Results

C. Discussion

The rise and fall time of V_{out} from positive to negative saturation, and vice versa, introduces a time delay. This is a deviation from ideal operation, see equation 18. This time delay is due to the slew rate of the LM741,$\approx \frac{.3V}{\mu s}$. The slew rate can be used to calculate the time delay per period, see equation 19.

$$t_{delay} = 2 \cdot \frac{s}{0.3V \times 10^6} \cdot 27.6V = 184\mu s \quad (19)$$

This time delay can be added to the period calculation in equation 17 to find a closer approximation of the output frequency, see equation 20.

$$T_{SPICE} = \frac{8 \cdot 4.6V \cdot 1k\Omega \cdot 0.1\mu F}{V_{in}} + 184\mu s \quad (20)$$

Equation 20 explains the results seen in figures 5, 6, and 7. The delay introduced by the slew rate of the Schmitt Trigger op-amp limits the rate at which the NMOS can be switched open or closed. Figure 8 shows that it takes $\approx 44\mu s$ after V_{tri} crosses V_{th} for V_{out} to reach the voltage required to open the switch. It then takes $\approx 44\mu s$ for V_{out} to reach the negative rail. These delays occur twice per period. Therefore, the total is approximately the delay value seen in equation 20. The slew rate of the op-amp is the biggest limitation to the linear performance of this VCO. It is clear from the results shown above that performance of the simulated circuit is far worse than the ideal model.

V. Experimental

A. Materials

A B&K Precision power supply was used to supply the input voltages. The input voltage values were recorded with a Summit 35 digital multimeter. A Tektronix TDS2004 oscilloscope was used to measure the output frequency and capture the input and output waveforms of the circuit. Circuit elements consisted of thin film resistors with a 5% tolerance, mylar capacitor, IRF510 NMOS, and

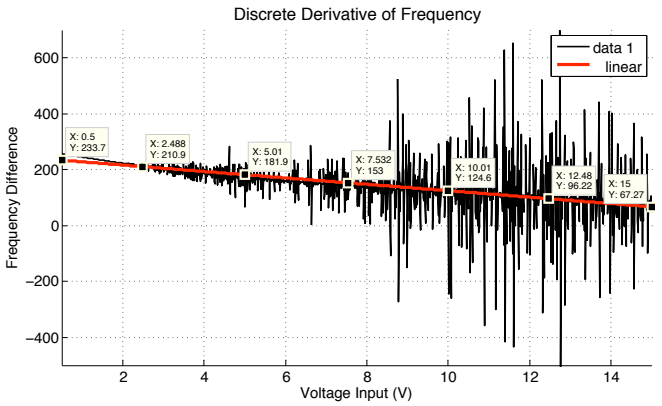


Fig. 7. Linearity of SPICE Simulated VCO

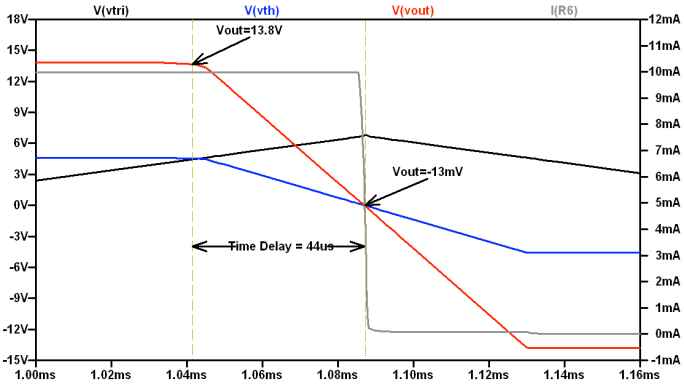


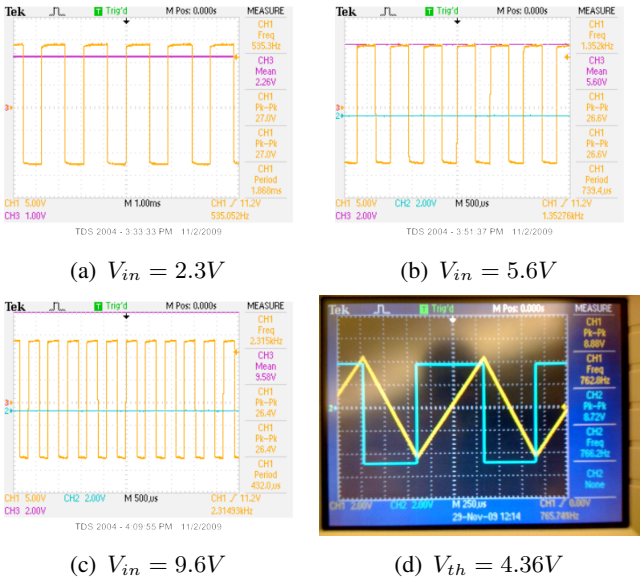
Fig. 8. Effect of Slew Rate on NMOS Switch

a Texas Instruments TL082 dual op-amp IC. The TL082 dual op-amp IC was used in order to observe changes in performance due to an increased slew rate. The data sheet for the TL082 reports a slew rate of $\frac{13V}{\mu s}$.

B. Waveforms

The circuit in figure 1 was built and tested at over 200 input voltage values. Experimental waveforms for various input voltages are shown in figure 9.

Figure 9(a) shows that the op-amp saturates at $\approx 13.5V$. Figure 9(d) shows $V_{th} \approx 4.36V$. The triangle wave in figure 9(d) overshoots V_{th} by $80mV$. This value is much smaller than those overshoots obtained with a LM741, see figure 8. The decrease in overshoot is due to the increase in slew rate; which translates into quicker switching of the NMOS.



(a) $V_{in} = 2.3V$ (b) $V_{in} = 5.6V$

(c) $V_{in} = 9.6V$ (d) $V_{th} = 4.36V$

Fig. 9. Experimental Waveforms and Output at Different Voltages

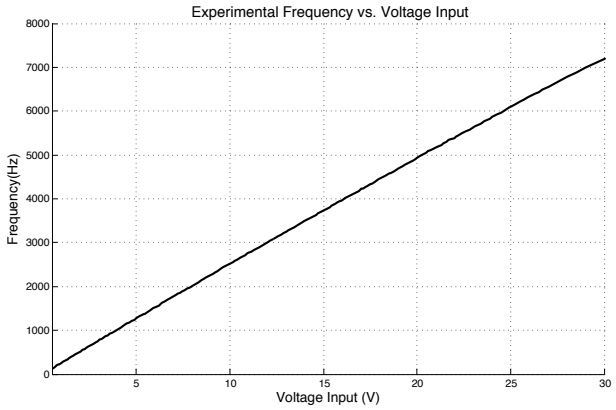


Fig. 10. Experimental Results for Frequency Output vs. Input Voltage

C. Results and Discussion

Figure 10 shows a plot of the measured output frequencies over a voltage ranges of 0V to 30V. It is readily apparent that the TL082 performs much better than the simulated LM741. The constant delay in the LM741 circuit was approximated to be $184\mu s$. The constant delay and oscillation period for the TL082 circuit can be calculated with equation 21.

$$t_{delay} = 2 \cdot \frac{s}{13V \times 10^6} \cdot 27V = 4.25\mu s \quad (21)$$

$$T_{Exp} = \frac{8 \cdot 4.43V \cdot 1k\Omega \cdot 0.1\mu F}{V_{in}} + 4.25\mu s \quad (22)$$

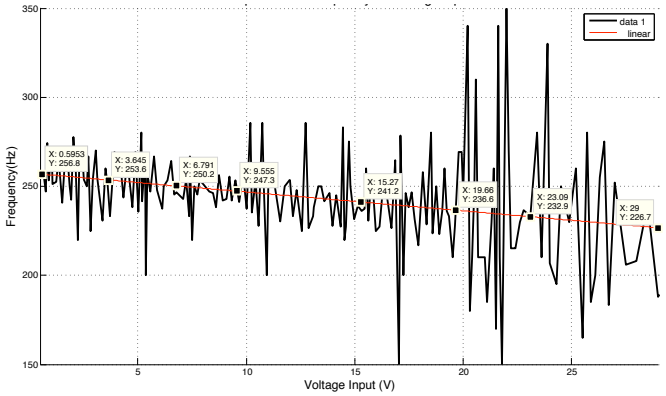


Fig. 11. Linearity of Experimental Results for TL082 VCO

The results for the TL082 more closely match the ideal linear model for this VCO, see equation 17. The linearity of the output can be seen in figure 11. Again, linear regression was used to correct for precision errors in the discrete differences. Figure 11 shows that the TL082 circuit is more linear than the simulated LM741.

Table I compares the ideal, SPICE, and experimental results. The results for the LM741 stray further and further away from ideal calculations as the input voltage increases. This is due to the slew rate. The experimental values consistently exceed those calculated for the ideal model. This is due to the difference in the values for V_{th}, see equation 17. The ideal model assumes saturation at 15V. However, a real op-amp saturates below this. V_{th} is a ratio of the saturation voltage. It is also worthwhile to not that saturation voltages depend on the voltage supply at the rail of the op-amp. Therefore, decreasing power supply voltages of the op-amps in this circuit actually cause a greater output frequency than predicted. It is expected that the experimental error with respect to the ideal model will be much smaller than those calculated for the SPICE simulated LM741.

TABLE I
RESULT COMPARISON

Input Voltage	Ideal (Hz)	SPICE (Hz)	Experimental (Hz)
1	250	258	279
2	500	492	520
3	750	706	782
4	1000	902	1000
5	1250	1082	1279
6	1500	1247	1556
7	1750	1400	1796
8	2000	1542	2023
9	2250	1674	2293
10	2500	1797	2523
11	2750	1911	2766
12	3000	2023	3012
13	3250	2119	3268
14	3500	2214	3526
15	3750	2303	3770

VI. CONCLUSION

The analysis of a voltage controlled oscillator, or any circuit, is best done by using the ideal models of components contained in that circuit. This type of analysis makes it easier to understand how the circuit operates. Making reasonable assumptions about the state of the circuit also helps. The ideal model for the op-amp, and assuming the circuit was oscillating, made it possible to derive the expression seen in equation 17. This type of analysis also makes it easier to identify non-idealities in the circuit. Such non-idealities show up when the circuit is simulated, or built on the bench. In the case of the circuit presented, the main non-ideality was identified as the slew-rate. It was also found that frequency output increases by reducing Vth. Vth is based on the saturation value of an op-amp; and saturation voltage depends on power supply voltages. This translates into faster frequencies with smaller power supply voltages. When the main limitation to the performance of a circuit is found, only then can a designer choose components with parameters that will more closely match ideal operation of that circuit. This paper has shown this.