Digital issues

domingo, 3 de outubro de 2021 19:40

What is good / is being worked on:

- Communication between disciplines
- Geometrical deliveries flow (floorplan, abstract, layout)

What is lacking:

- Better understanding of the flow of the other discipline (what you do that affects the other?)
- Interface definition, synchronization and electrical constraints during project
- Record of processes being generated that reach some level of maturity (like geometrical flow)
- Formalization of key processes with discipline interactions
- Documentation planning
- Requirement engineering

Issues:

- **Silo-like structure**: Both disciplines have a good communication and will to help, but each one treats the other as a black-box most of the time. Context, perspective and opinion of the other are not considered on many situations, causing rework, frustration, delays and quality problems. Even though Chipus was originally an analog IC company, the existence of an ever-growing digital discipline apparently did not change the culture of digital being an external service provider.
  The main consequences are:
  - No consideration for important factors or practices of digital flow
  - No consideration of change impacts on digital (changes may be not as simple as it seems)
  - Lack of top-level view and participation of digital designers (mainly until later in the project)
  - Lack of resource sharing view, causing server or license unavailability

- **Weak interface agreement**: Pins require a strong agreement between both disciplines, where the main interaction points are pin existence, nomenclature, position, properties and electrical characteristics. However, it is common to occur uninformed changes and name mismatches on both sides, as well as bad property assignment by analog team (power, signal, etc) and lack of timing/capacitance discussions for digital design (usually use arbitrary values instead of receiving it or requests to analog designer without context/guides). Pin placement refinement has an process that has been evolving along the projects, but is not yet well consolidated on the company and is undocumented.
  The main consequences are:
  - Digital wrapper required due port name mismatches or index rerouting on analog top
  - Lack of important pin constraints that can be critical to digital design
  - Rework due constant changes and late decisions that can cause great impacts

- **Informal digital-analog hand-off activities**: Documents do not specify any mixed or digital-analog integration activities, guides or risks. Versioning on analog side is being introduced already with success cases, but is still incipient. Even considering undocumented processes followed by most of the company (like geometrical deliveries), it is not present well defined specifications and checks on the discipline interactions. Electrical and functional abstraction level interaction between disciplines are still not being worked on and are current challenges, having clear interest points to be worked on like definition of timing / capacitance of digital pins and digital models of analog blocks for top simulation. Informal interactions are not condemned, but key points that present high risk (affects multiple actors, influences architecture or behaviour, etc) must be better defined.
  The main consequences are:

    - Lack of context, guides, checks and important points to consider on hand-off activities
    - No alignment of expectations on what, how and why of activities
    - Informal communication of critical points, causing loss and occlusion of information

- **Loosely defined requirements**: Requirements and design decisions are center pieces of projects. It's common that mixed-signal requests or activities don't have a very clear scope and constraints. Even though most designers have an overall notation of what to do, details or alignment of expectations aren't well defined in most cases, like the level of abstraction of models, what/how/why of tasks and low priority on requirement mapping. In summary, there is a lack of requirement engineering between disciplines. This causes unclear, unnoticed and unimplemented system requirements. No essential features have always worked at silicon, what might be giving a false sense of security once it's common to have unessential features not working and workarounds being necessary to successfully use critical features.
  The main consequences are:
    - Unmapped and unclear requirements that affects final product quality
    - Poorly specified requests between disciplines causing rework and frustration

Analog issues

domingo, 3 de outubro de 2021 19:40

What is good / is being worked on:

- Communication with teams
- Versioning of digital deliverables
- Earlier top activities with someone responsible for them
- Abstract interactions with digital

What is lacking:

- Valid deliverables from digital (mainly layout)
- Requirements regarding deliveries and requests to digital
- Earlier digital interaction and deliveries
- Better follow-up of changes and current top-level view
- Management (update, adoption) of project flow
- Shift efforts left in the project

Issues:

- **Silo-like structure**: Even though teams have a good communication, it is often not considered that challenges and benefits from the other discipline. Digital usually delivers their artifacts (mainly layout) too close to the project deadline and they always present problems when integrating on analog tools. This is mainly caused because physical verification flows are distinct between teams, creating DRC problems (digital tech with vias, substrate voltage, rules not being respected) and LVS issues (port order, third-party IPs, digital layout/schematic files). At the same time, requests and inputs from analog to digital often miss important information or definitions, which may cause the late and invalid deliveries. The lack of a shared-vision and well-defined interaction has a high impact on cross-functional teams, resulting at projects delayed and/or with less quality, as well as stress, frustration and anxiety among designers.
  The main consequences are:
  - Layout deliveries not working at integration team tools
  - Suboptimal implementations
  - Excessive iterations to fix or understand problems

- **Late digital interactions**: The digital portion of systems is commonly started at the middle or end of projects, when most of analog portion is completed or very mature. For most of the time, an abstract or analog functional models are used instead of digital deliveries, while those are not ready. When digital provides them, it is often close to project deadline and there is not much time to solve integration problems, which range from physical verification bugs to interface or behaviour misalignments between teams. A thorough top-level verification also gets affected because only higher priority issues and main cases are possible to be covered in the short time after digital release.
  The main consequeces are:
  - Huge workload at end of projects
  - Bugs, misunderstandings and flow incompatibilities found late
  - Possible undetected bugs
  - Stress, furstration, ansiety, extra work hours
  - Unclear which are the responsabilities of the digital team

- **Narrow-sighted implementation**: An overview of the project usually (not always) occur at the start of the project with all designers involved. An initial top-level view is given and responsibilities are defined. During the development, decisions and changes are made, which are not always informed to everyone. This makes not only designers to loose top-level view (at least the macro block it is involved with), but also teams to have blocks with incompatibilities (interface, behaviour, pin position, etc). This scenario is fairly common considering initial

specification is usually very basic and further elaborated during project execution. This is more likely to occur between digital and analog teams, but can also occur between analog design and layout members. This causes less people to be able to discuss the system as a whole, increases the chance of integration issues and miss the opportunity to improve the experience of some collaborators.
The main consequences are:
    - Less voices for top-level discussion
    - More integration issues
    - Reduce opportunity of professional growth

- **No robust continuous improvement of development process**: Improvements to analog flow are done to solve past problems, like the introduction of abstract interactions with digital team to shift-left some integration activities before digital layout or early LVS checks of third-party circuits (IO cells, memory IPs) to reduce physical verification issues late in the project. However, some activities that commonly have problems don't have guidelines to be followed, like abstract deliveries or request specification to digital and verification scope at top/digital level. Not only that, recurring problems that are known and have solution don't have a clear approach to be dealt with, like power up simulations, missing level shifters or missing vias due digital technology library. Most of the time those tasks depend of someone remembering to do that or solutions on previous projects to be forgotten.
  The main consequences are:
    - Lack of lessons learned retention in the process
    - Unmapped required activities

Manager issues

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What is good / is being worked on:

- Top role with more independency (even with "flexible" responsibilities)
- Shift-left of integration activities
- Overload on layout team
- Delivery versioning and hand-off
- Knowledge of problems between teams

What is lacking:

- Consensus of top and shared-vision visibility interest, requirement and relevance
- Delivery requirements (elicitation, clarity and verification)
- Deliveries validity
- Requirement changes treatment (once they are inevitable)
- Late interactions between teams
- Late digital deliveries
- System-level verification planning and alignment
- Shift-left and alignment of physical verification strategies
- More prevention-based approach
- Early and continuous follow-up of project status
- Continuous improvement of process

Issues:

- **Silo-like structure**: Communication between designers is good when it happens, but are not as frequent or clear as expected. The flow of the other team is most of the time unknown, causing unclear requests, misunderstandings between designers or high-effort tasks that would be very low effort to the other team. Failing deliveries, mainly digital backend layouts, occur because of different non-compatible physical verification strategies not aligned before or during project. The late participation of digital team in the project and the perspective of it as a third-party IP provider reenforce that separation of disciplines. A low interaction between analog designers and layouters was also informed.
  The main consequences are:
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- **No strategy for changing requirements**: Projects have the characteristic of constantly changing requirements and incipient initial specifications. The missing information during initialization is apparently common on the client side in the sector and not a poor elicitation problem (not confirmed) and most of requirements are discovered during implementation. However, no explicit strategy exists to plan management and mitigation of them.

- **Lack of top-level view**: Many

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Other issues

segunda-feira, 4 de outubro de 2021 10:03

Mapped issues unrelated to team interactions.

- **Undocumented processes**: Projects follow the Chipus' standard document POP-006 and each discipline contains their own reference document (DR-002 for digital and DR-006 for analog). However, POP-006 presents a very broad overview, not specifying assurance, monitoring and control activities or any mechanisms to help managers. The geometrical flow between teams (like floorplan, abstract and layout) has evolved over the years, but it is not recorded and not present on all projects.
  The main consequences are:
  - Flow inconsistencies between projects
  - Divergent standards that causes additional work and confusion
  - Late integration and top-level verification due lack of planning

- **Low documentation priority**: Some documents are planned and generated during projects, but are often neglected. The lack of a proper time during and after the project for fully document design and respective decisions is recurring on multiple cases, causing problems mainly on new versions of past projects were designers don't remember decisions/details or are not more employees at Chipus. Unplanned documentation activities are usually left for "when there is time", causing loss of information and consultancy of outdated or incomplete documents.
  The main consequences are:
  - Loss of information regarding implementation and design decisions
  - Rework due outdated documentation that was considered updated

Final coding

domingo, 3 de outubro de 2021 18:41

Constructs

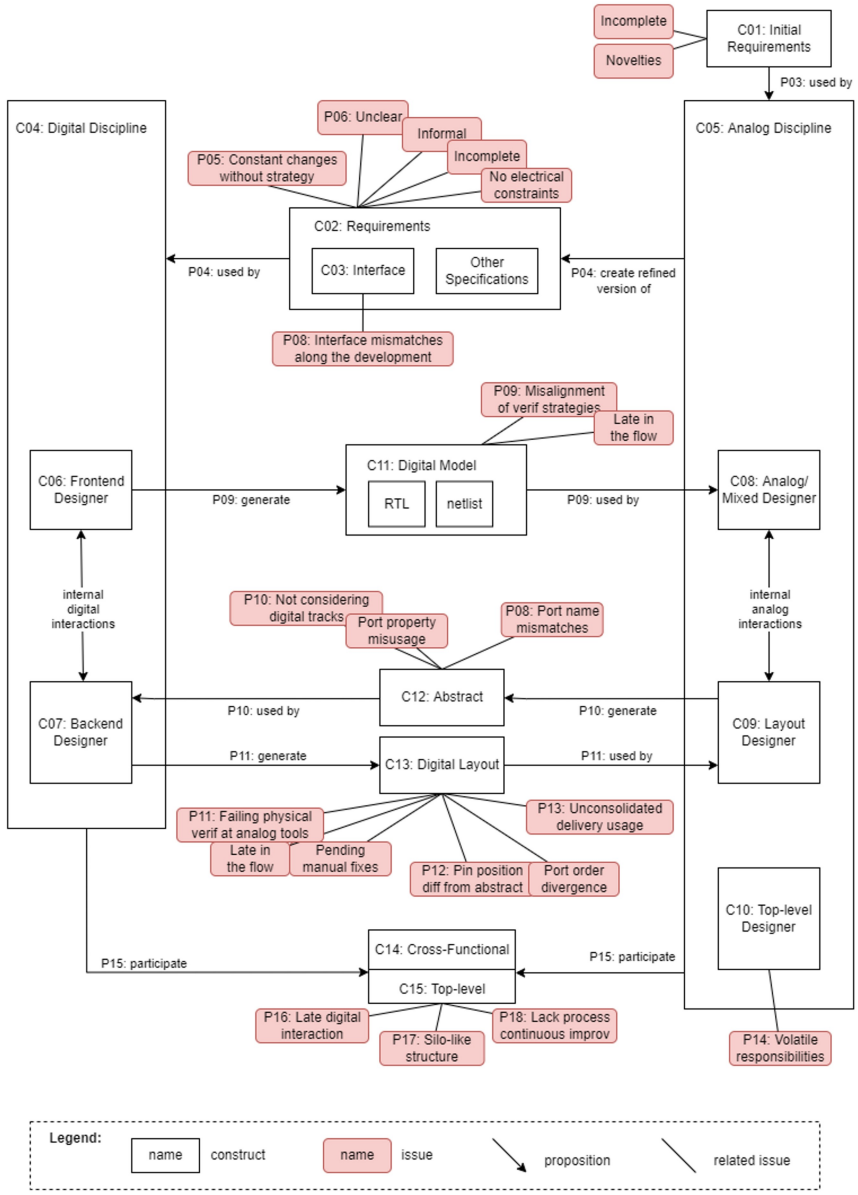
C??	Digital Discipline
C??	Analog Discipline
C??	Frontend Designer (Model, Verification, Logic Synthesis)
C??	Backend Designer (Floorplan, Layout, Physical Verification)
C??	Analog/Mixed-Signal Designer (Model, Schematic, Verification)
C??	Layout Designer (Layout, Physical Verification)
C??	Top-level Designer (Mixed-signal model and Verification, Integration)
C??	Manager
C??	Client (External stakeholder that specified product or service)
C??	Communicate (exchange of information between designers)
C??	Request (ask an artefact from another discipline)
C??	Deliver (send an artefact requested to another discipline)
C??	Versioning (usage of SVN and SoS for delivery versions)
C??	Model (software that mimick circuit behaviour; High-level, RTL)
C??	Abstract (representation of size, shape and pin of a circuit; LEF/DEF)
C??	Layout (drawing of physical circuit)
C??	Physical verification (layout integrity and validity using LVS and DRC)
C??	Functional verification (model integrity and validity)
C??	Resources (servers, licenses)
C??	Requirement (Stakeholders need of the project)
C??	Initial requirement (information from client about project)
C??	Requirement change (addition, removal or modification on previous spec)
C??	Digital electrical constraints (timing, capacitance, power)
C??	Interface (bundle of ports used to interconnect blocks of systems)
C??	Port (block access point for input, output or both of analog or digital signals)
C??	Pin (physical representation of a port, with position and size well defined)
C??	Port order (list with the sequence of port names of a block)
C??	Port property (in/out/inout, power/signal, name)
C??	Discipline process (steps of discipline in order to produce planned deliverables)
C??	Process continuous improvement (update of predefined process for future use)
C??	Process adoption (attachment to predefined process, avoiding deviations)
C??	Formalization (standard guidelines, templates and procedures)
C??	Rework (repeat a completed or partially completed task)
C??	Negative impact on designer (frustration, extra hours, weekend work)
C??	Negative impact on project (cost, quality)

Propositions

P??	Designers can be Frontend, Backend, Analog/Mixed-Signal or Top-level Designers
P??	Digital Discipline contains Frontend and Backend Designers
P??	Analog Discipline contains Analog/Mixed-Signal and Layout Designers
P??	Mixed-signal Discipline contains Manager and Top-level Designers
P??	Disciplines can request or deliver artefacts to another discipline, which commonly use a versioning tool.
P??	Client defines Initial requirements, often incomplete.
P??	Analog/Mixed-Signal Designers develop models and refine initial requirements.
P??	Analog/Mixed-Signal Designers (or Client a few times) delivers Requirements for the Digital Discipline designers, which also include interface specification.
P??	Interface contains a group of ports that have characteristics like pin information, properties and order.
P??	Frontend Designers use arbitrary digital electrical constraints, but can request from Analog/Mixed-signal Designers or Top-level Designers
P??	Requests for digital electrical constraints usually are poorly specified and usage/context is not clear for who delivers.
P??	

Conceptual diagram

terça-feira, 28 de junho de 2022 17:47



Conceptual refinement

terça-feira, 28 de junho de 2022 17:53