



FARE - ICS905– 2021-2022

Digital-to-Analog Conversion
Analog-to-Digital Conversion

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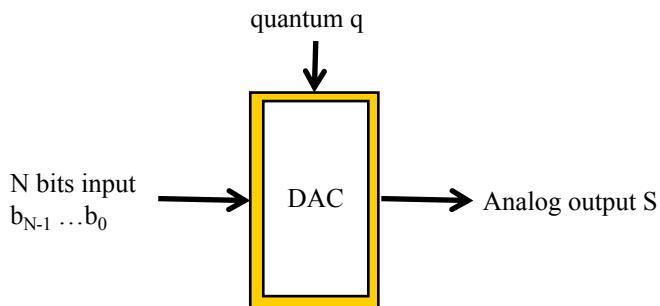
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Digital to Analog Conversion

- Definition
- Main features
- DAC test
- Weighted network parallel DAC
- High resolution parallel DAC
- Algorithmic DAC
- Conclusion

Definition



$$S = q(2^{N-1}b_{N-1} + 2^{N-2}b_{N-2} + \dots + 2^1b_1 + 2^0b_0)$$

$$q = K \frac{V_{\text{réf}}}{2^N}$$

$KV_{\text{réf}}$ represents full scale output voltage of the converter.

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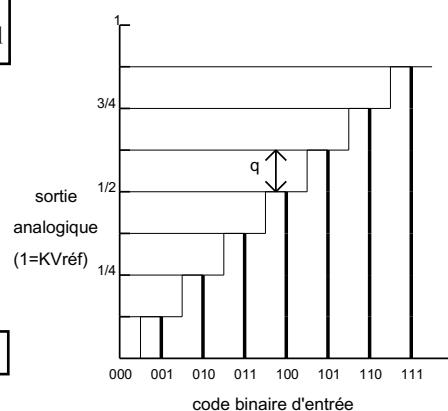
Definition

$$S = KV_{\text{réf}}(2^{-1}b_{N-1} + 2^{-2}b_{N-2} + \dots + 2^{-N+1}b_1 + 2^{-N}b_0)$$

$$S_{\text{Max}} = KV_{\text{réf}} \frac{2^N - 1}{2^N} = KV_{\text{réf}} - q$$

Transfer characteristic of a 3-bits DAC

$$S_{\text{min}} = 0$$



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Main features

Resolution :

Output voltage smallest variation q in response to input digital code change \leftrightarrow number 2^N of reachable output levels.

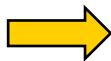
$$\text{For a } N\text{-bits resolution converter : } q = K \frac{V_{\text{réf}}}{2^N}$$

Example : $N=16$ bits and $FS=2V \rightarrow q=30\mu V$

Accuracy :

Expression of the error ΔV_e between the real measured value and the ideal theoretical value.

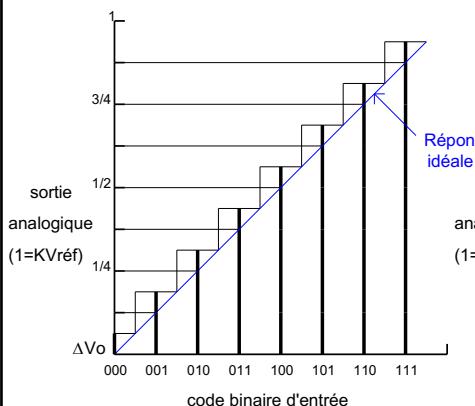
$$\text{For a } N \text{ bits accuracy converter : } \Delta V_e \leq K \frac{V_{\text{réf}}}{2^{N+1}}$$



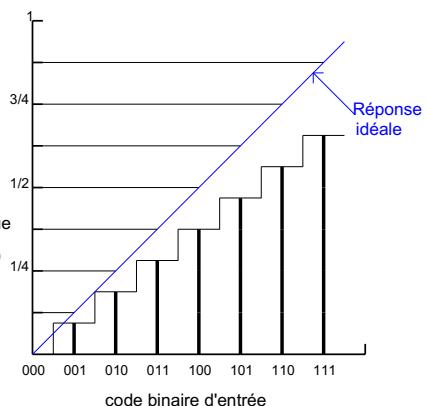
Resolution and accuracy are not necessarily equal.

Main error terms

Offset error :



Gain error :



Overall shift of the real transfer characteristic compared with the ideal one.

Difference between real transfer characteristic slope and ideal slope.

Main error terms

Non linearity errors :

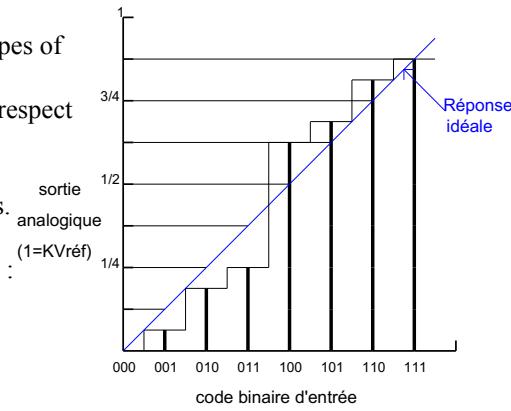
Non linearity concept includes two types of distortion :

- overall distortion: expresses the non respect of proportionality condition
- local distortion: expresses the non consistency of successive output steps.

Thus two types of non linearity errors :

Integral Non Linearity or INL

Differential Non Linearity or DNL

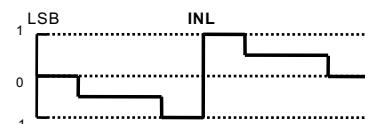


Transfer characteristic after offset and gain errors correction.

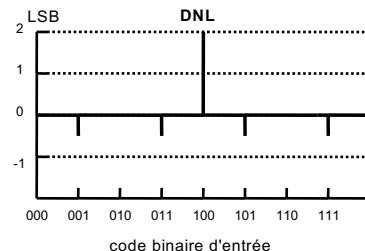
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Non linearity errors

INL : difference between the real output value and the reference straight line value (linear regression straight line)



DNL : difference between each step height and the ideal step value of one quantum for one LSB



Converter specifications state INL and DNL errors which are generally smaller than $\frac{1}{2}$ LSB.

Main features

Monotonicity :

Property meaning that the analog output always increases or remains constant as the digital input increases.

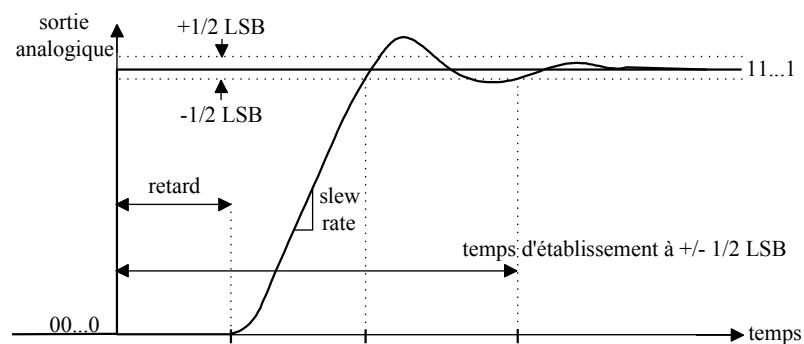
Making an significant impact when the converter locks a feedback loop.

Operating range :

DAC performances changes with time, temperature, supply voltage. Thus, gain, offset, non linearities and monotonicity must be given for a specified range of temperature and supply voltage.

Main features

Settling time :



Time elapsed from the application of an ideal instantaneous full scale step input to the time at which the analog output (voltage or current) has entered and remained within a specified error band (typically $\pm 1/2$ LSB) around the final value.

Main features

Converter bandwidth :

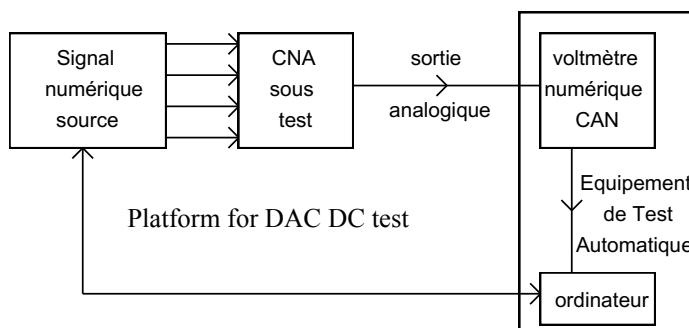
The required amount of time for processing data within converters determines a maximal operation frequency or maximal sampling rate.

- When the application only needs that the analog output remains within a specified error band around the final value before a new digital input code could be processed :

$$\text{Sampling Rate}_{\max} = \frac{1}{\text{Settling time}}$$

- In general, evaluation of converter bandwidth relies on the curve plotting of the Effective Number Of Bits (ENOB) in function of the sampling rate. As soon as the ENOB falls of 1/2 compared to the low frequency resolution, nominal accuracy is not guaranteed anymore and thus the maximal bandwidth of the converter is reached.

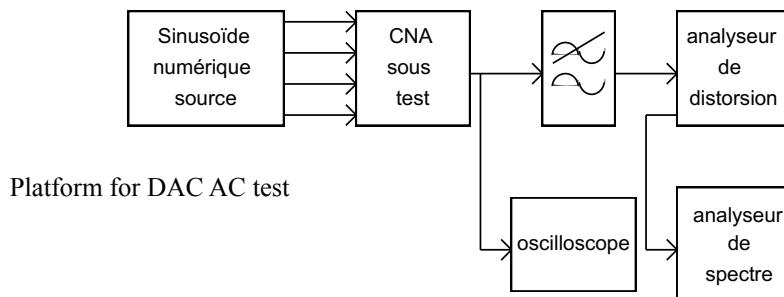
DC characteristics test



Digital voltmeter accuracy must be much greater than converter under test accuracy.

DC characteristics test is done for several temperatures and several supply voltages (minimum, nominal, maximum).

DC characteristics test by FFT



Spurious Free Dynamic Range(SFDR) : ratio in dB of the RMS value of the carrier frequency (maximum signal component) at the output of the DAC to the RMS value of the next largest noise or harmonic distortion component (which is referred to as a “spurious” or a “spur”).

Effective number of bits (ENOB) :
$$ENOB = \frac{SNDR_{dB} - 1,76}{6,02}$$

Tapez une équation ici.DAC/ADC ICS905– Patricia DESGREYS

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Digital to Analog Conversion

Definition

Main features

DAC test

Weighted network parallel DAC

High resolution parallel DAC

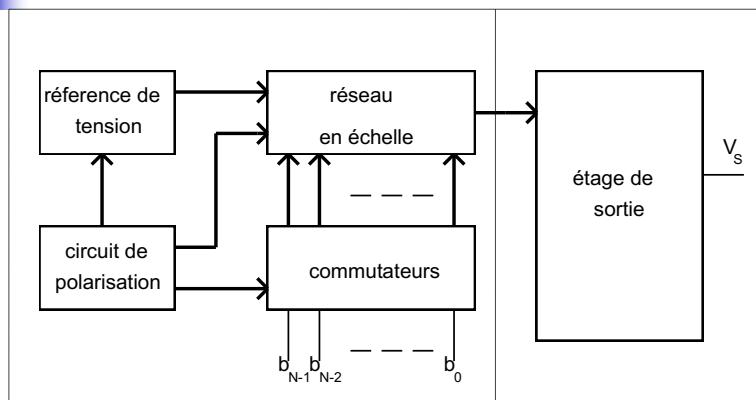
Algorithmic DAC

Conclusion

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Weighted network DAC



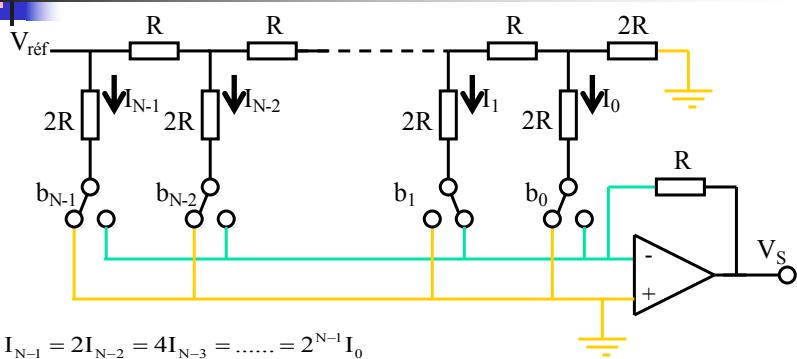
Principle : The output is the sum of weighted analog references (ex : binary network) selected by the input digital code bits. The references are calibrated sources of current, voltage or charge.

Advantage : rapidity – reachable bandwidth = 500 MHz → a few GHz

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R-2R network DAC

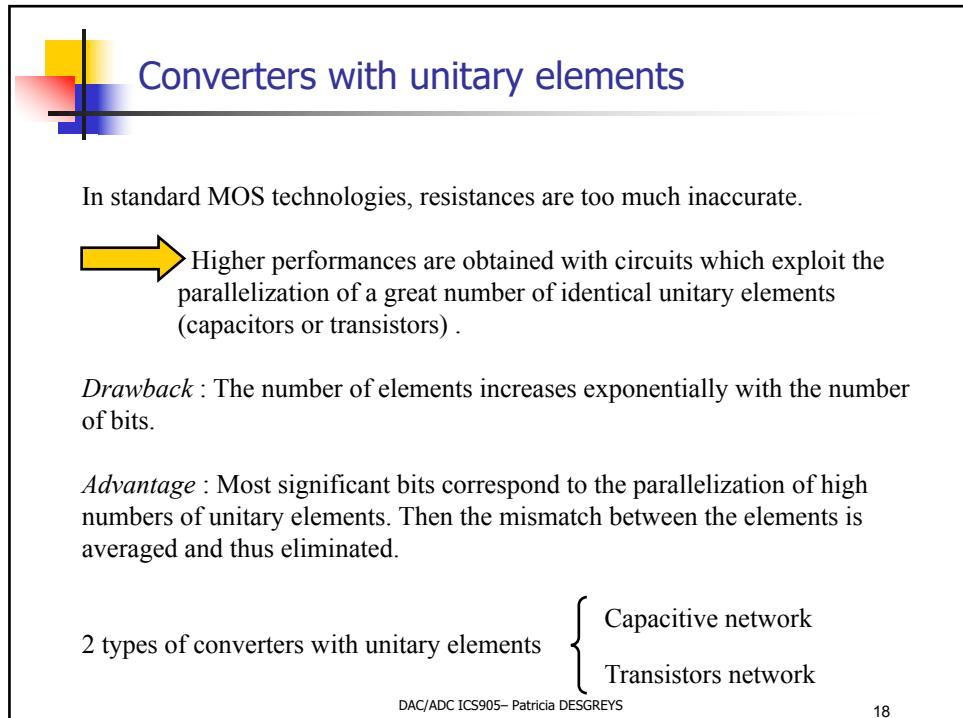
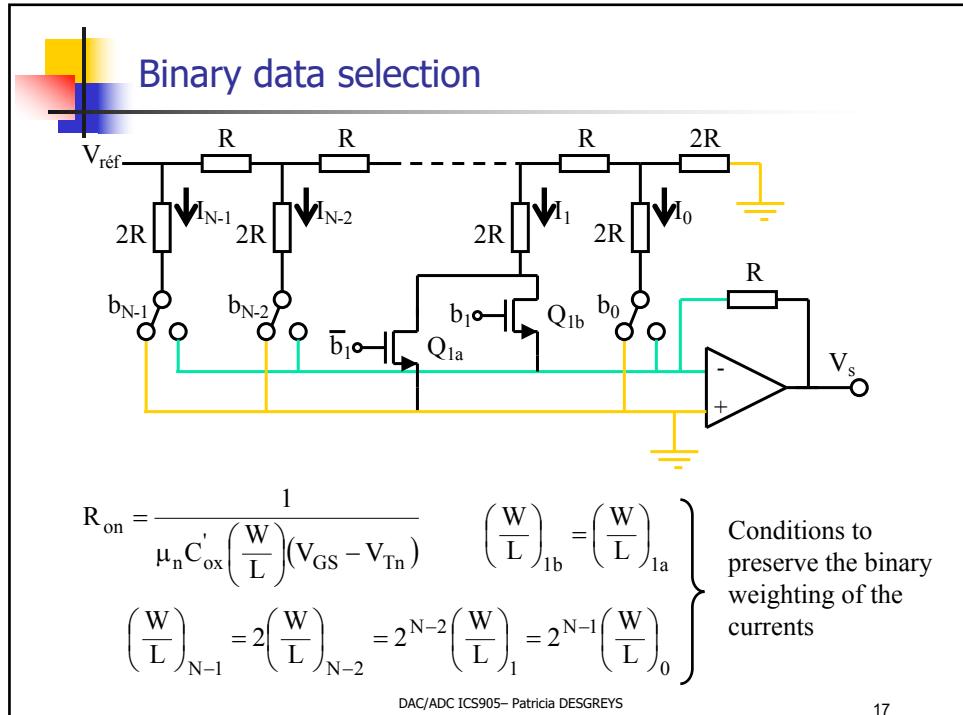


A single value of resistance is used
Identical resistors are matched as well as possible to 0.1% } Max. accuracy 10 bits

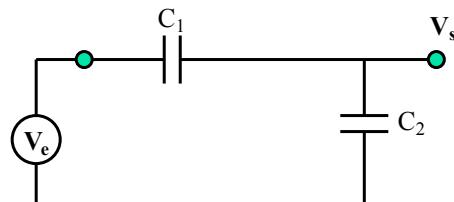
+ laser adjustment : max. accuracy 12 bits

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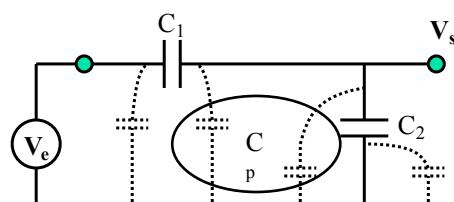
Capacitive divider



$$\frac{V_s}{V_e} = \frac{C_1}{C_1 + C_2}$$

- Advantages* ➔ Power consumption is strongly reduced since no current circulates in the divider.
- ➔ DC and AC behaviors can be managed separately.
- ➔ Capacity ratios can be carried out with accuracy.

Capacitive divider



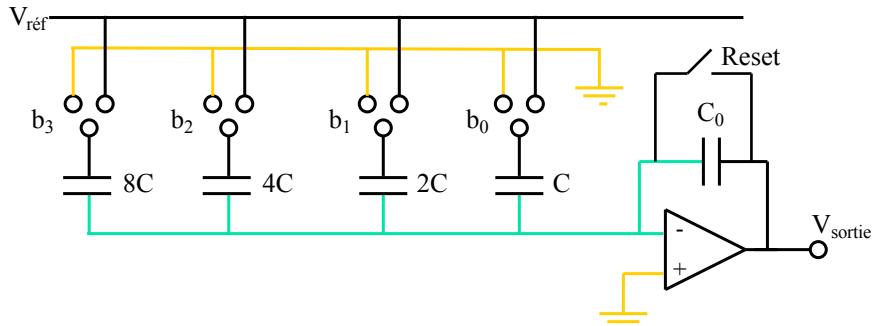
$$\frac{V_s}{V_e} = \frac{C_1}{C_1 + C_2 + C_p}$$

- Advantages* ➔ Power consumption is strongly reduced since no current circulates in the divider.
- ➔ DC and AC behaviors can be managed separately.

Drawback : Capacitive dividers are strongly sensitive to parasitic capacitances.

$$\frac{V_s}{V_e} = \frac{C_1}{C_1 + C_2 + C_p}$$

Charge transferring converter

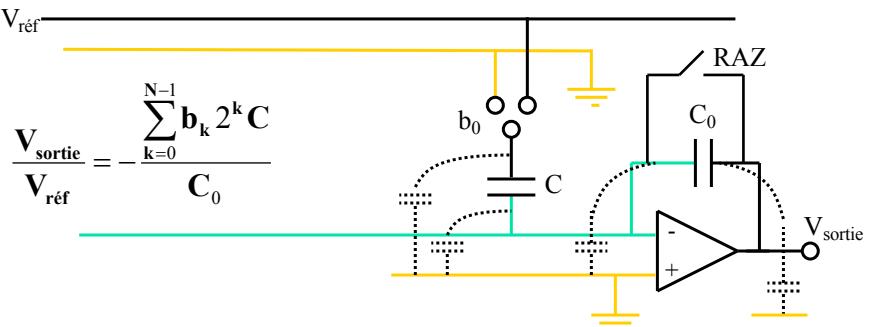


1st phase : Reset

2nd phase : Action of bits $b_3 b_2 b_1 b_0$

$$\frac{V_{\text{sortie}}}{V_{\text{réf}}} = - \frac{\sum_{k=0}^{N-1} b_k 2^k C}{C_0}$$

Charge transferring converter

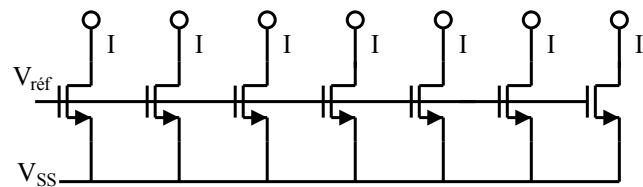


Parasitic capacitances doesn't affect this converter.

Thus, this converter resolution can reach 10 bits.

Transistor network

A row of unitary current sources can act as a row of unitary capacities.



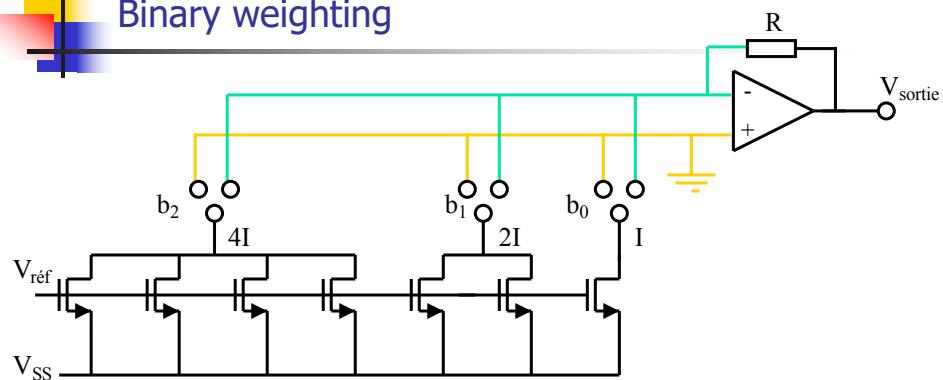
Two combining types are carried out

$\left\{ \begin{array}{l} \text{Binary weighting} \\ \text{Thermometer coding} \end{array} \right.$

Transistor networks use only identical transistors.

Mismatching limits the accuracy of transistor network DAC to 10 bits.

Binary weighting

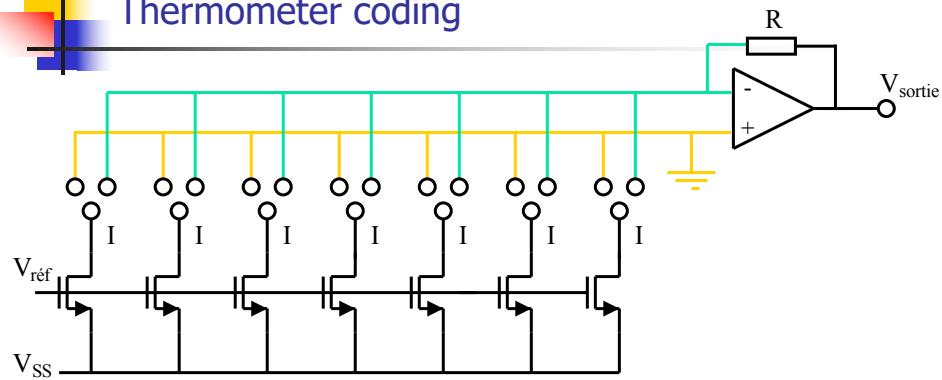


In this case, transistors are connected together in order to form binary weighted current sources.

Advantage : easy switch control.

drawback : Risk of high DNL error.

Thermometer coding



In this second case, transistors are added in parallel one by one to produce a current proportional to the digital word. Greater inputs imply more transistors in parallel.

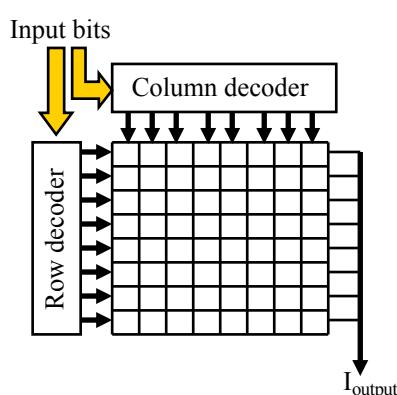
Advantages : guaranteed monotonicity and high DNL performance.

Drawback : reaching each unitary transistor leads to more complexity in the switch control.

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Thermometer coding



Converter organized like a RAM memory :

Advantage : automatic design

Drawback : control complexity

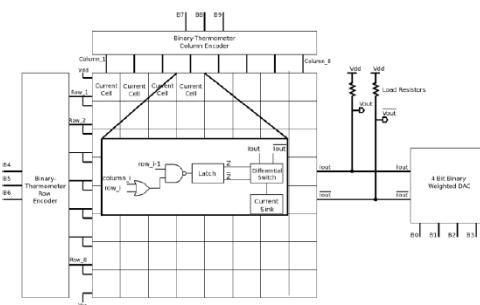
🚫 Too large occupied surface area

For optimum performances in resolution and surface area, a good solution consist in combining thermometer coding and binary coding.

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Partially Thermometer coding



Resolution	10 bits
Technology	CMOS 90 nm
INL	0,41 LSB
DNL	-0,031 LSB
Supply voltage	1,2 V

10 bit current steering DAC in 90 nm technology, Aerospace and Electronics Conference, NAFCON 2014 - IFFE National, Issue Date: 24-27 June 2014, Written by: Moody, T.; Saiyu Ren; Ewing, R.

Input signal frequency	Sampling frequency	SFDR
250 MHz	1 GS/s	69 dB

Limitations of weighted network DAC

Weighted network DAC are not appropriate beyond 10 bits because matching conditions are not feasible.

- Too high inaccuracy of resistances in R-2R network
- Too high number of elements (exponential increase) for the conversion based on identical unitary elements.

→ { Two techniques for high resolution parallel DA conversion :
Dynamic current division
Segment converter (or by pieces)

Digital to Analog Conversion

Definition

Main features

DAC test

Weighted network parallel DAC

High resolution parallel DAC

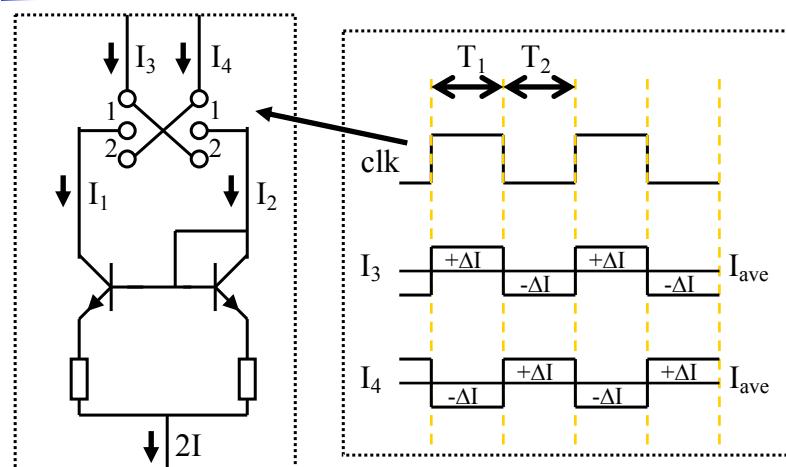
Algorithmic DAC

Conclusion

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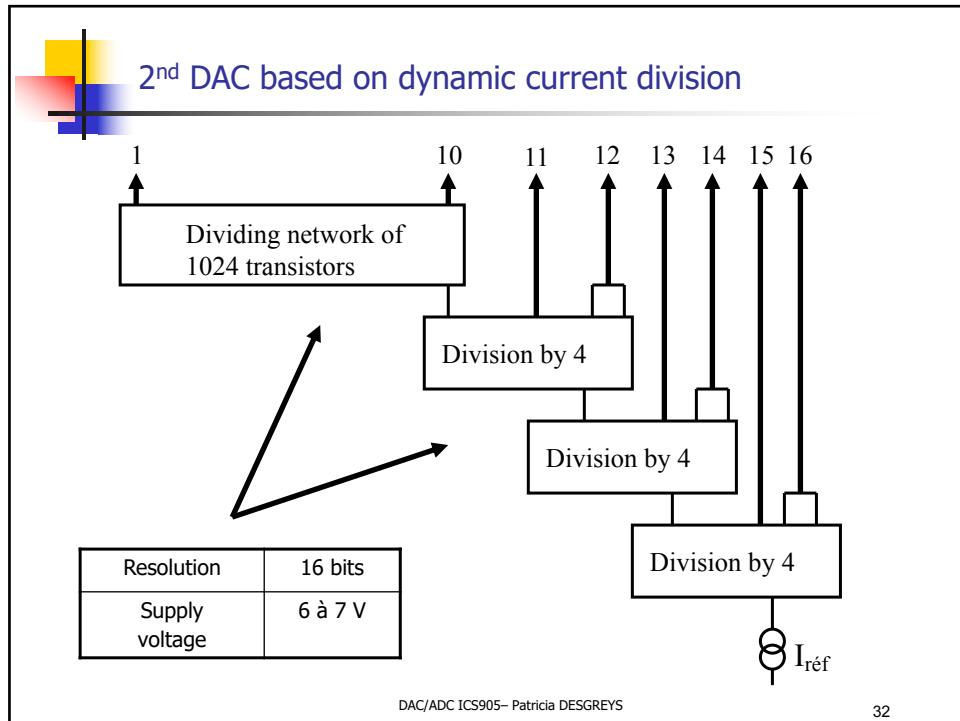
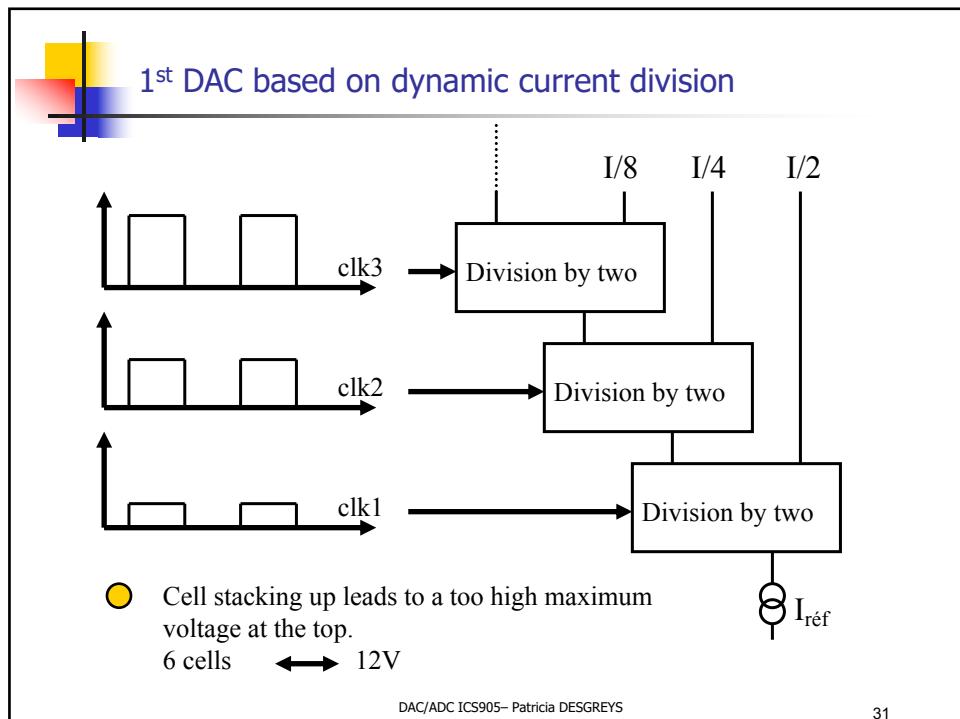
Principle of dynamic current division

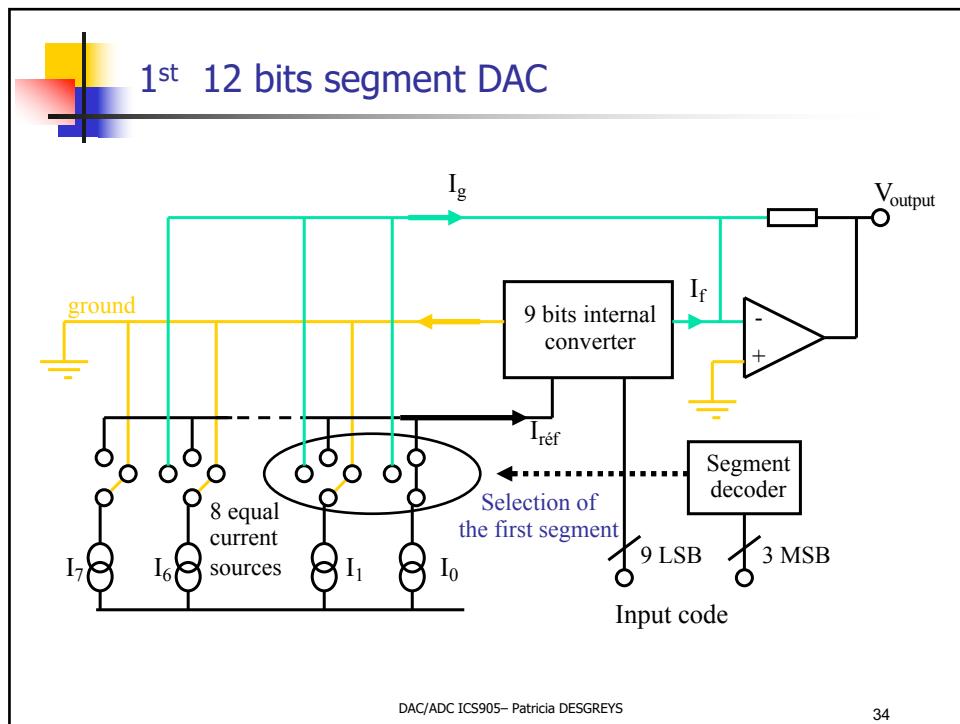
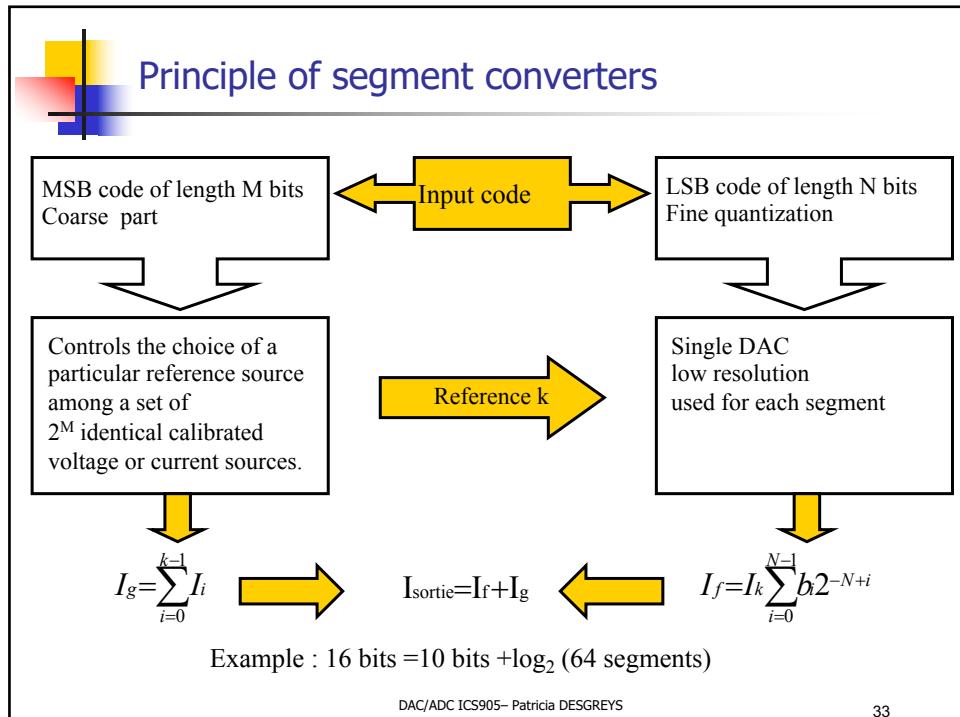


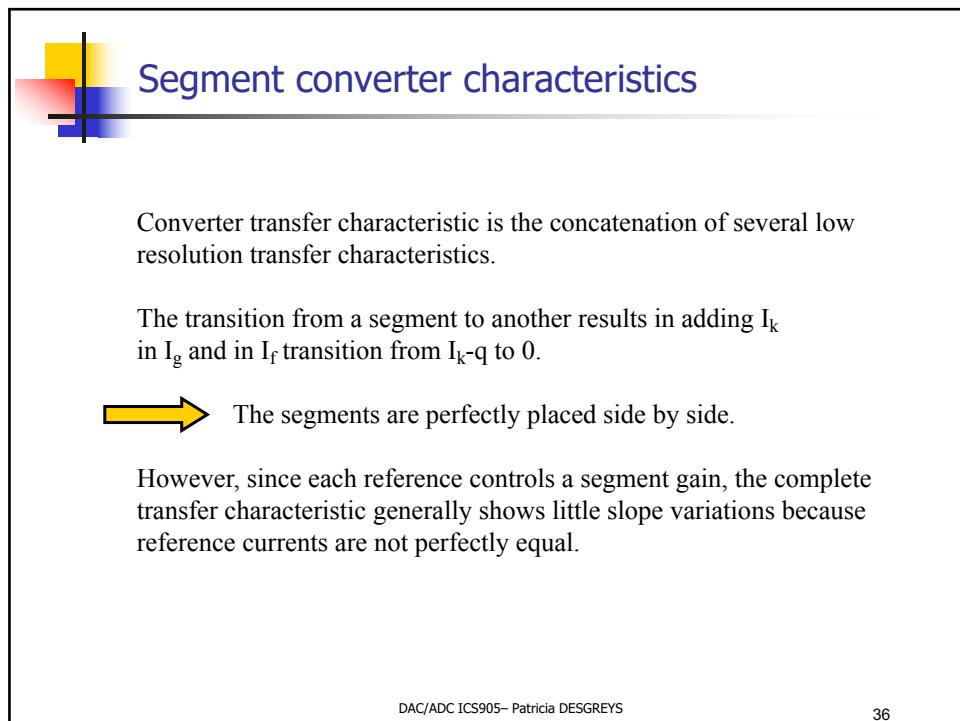
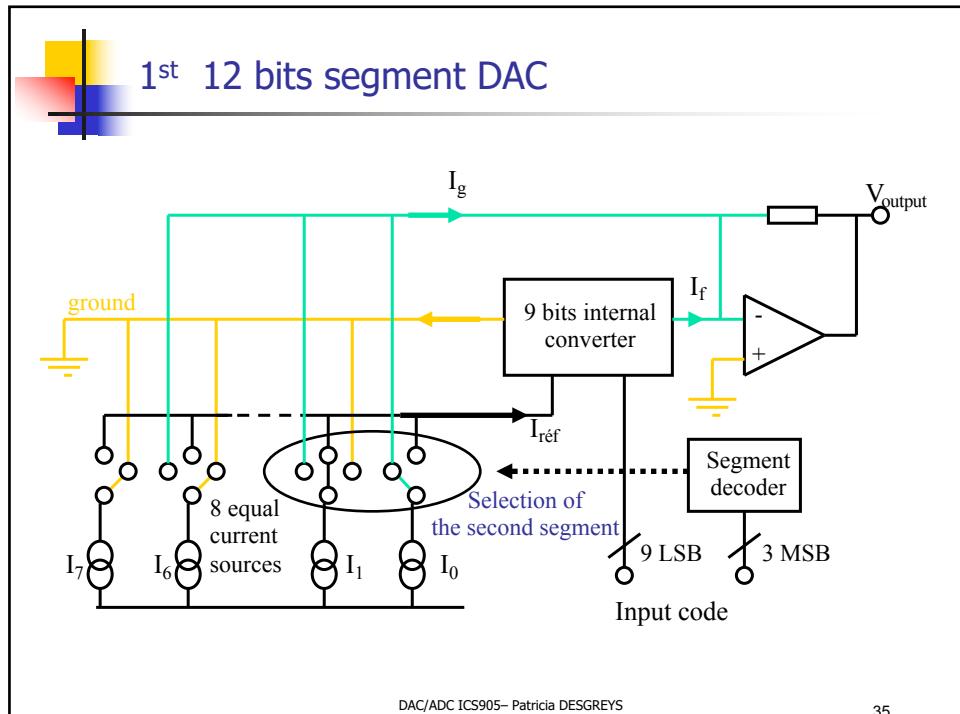
Gain of a factor 10^3 to 10^4

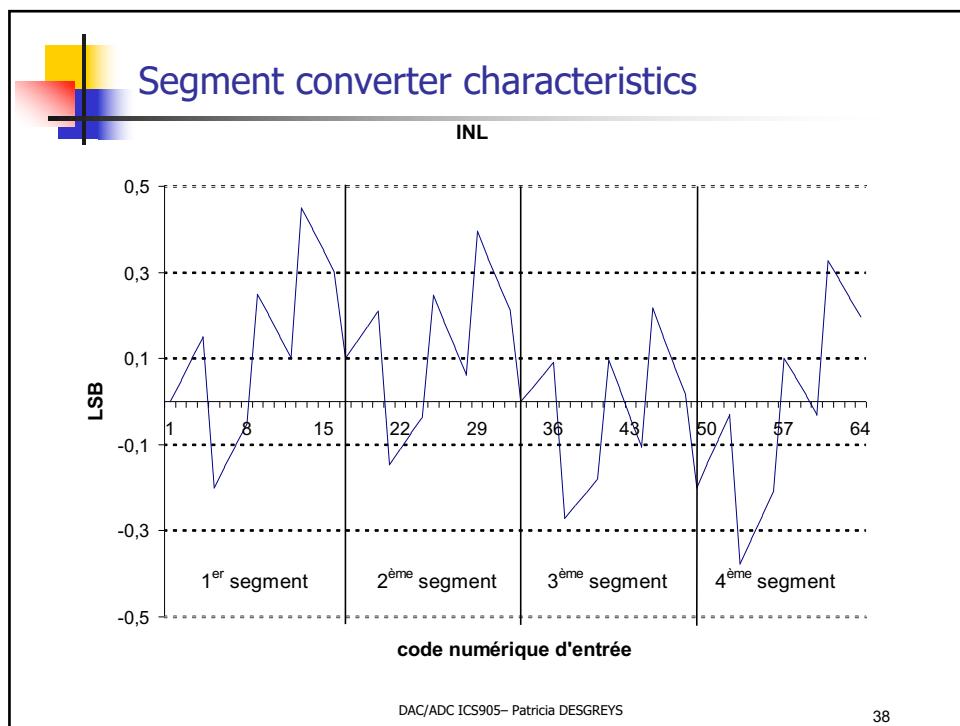
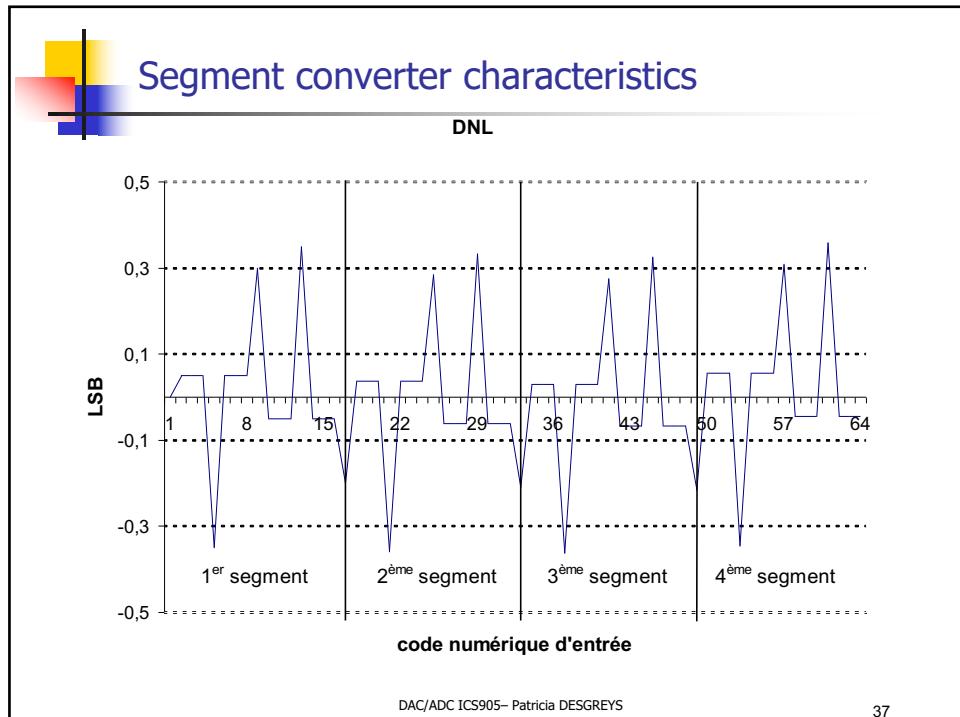
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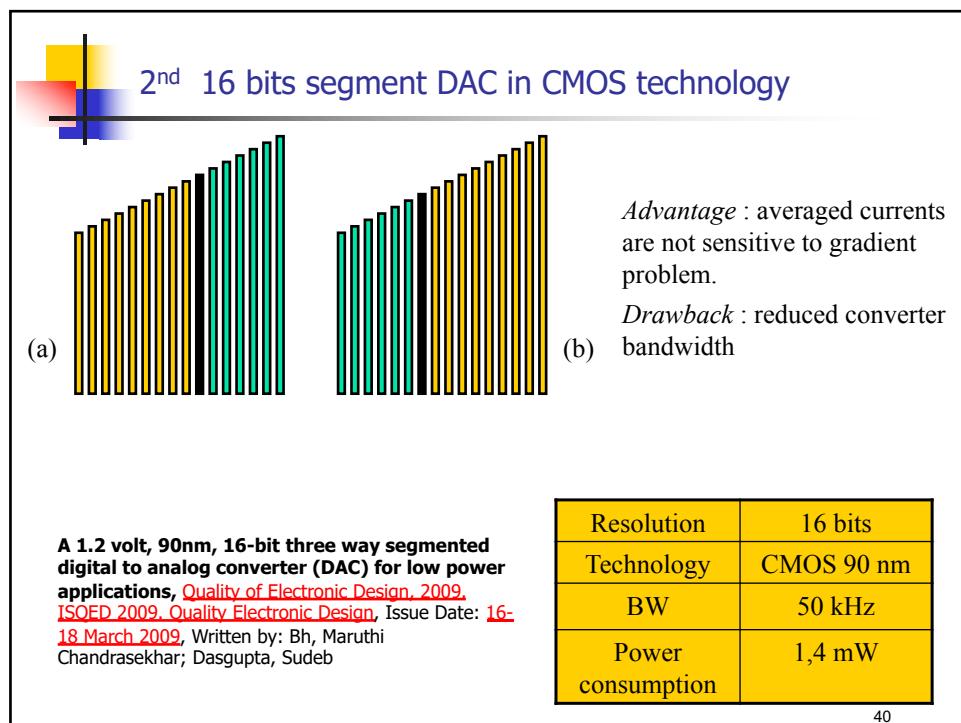
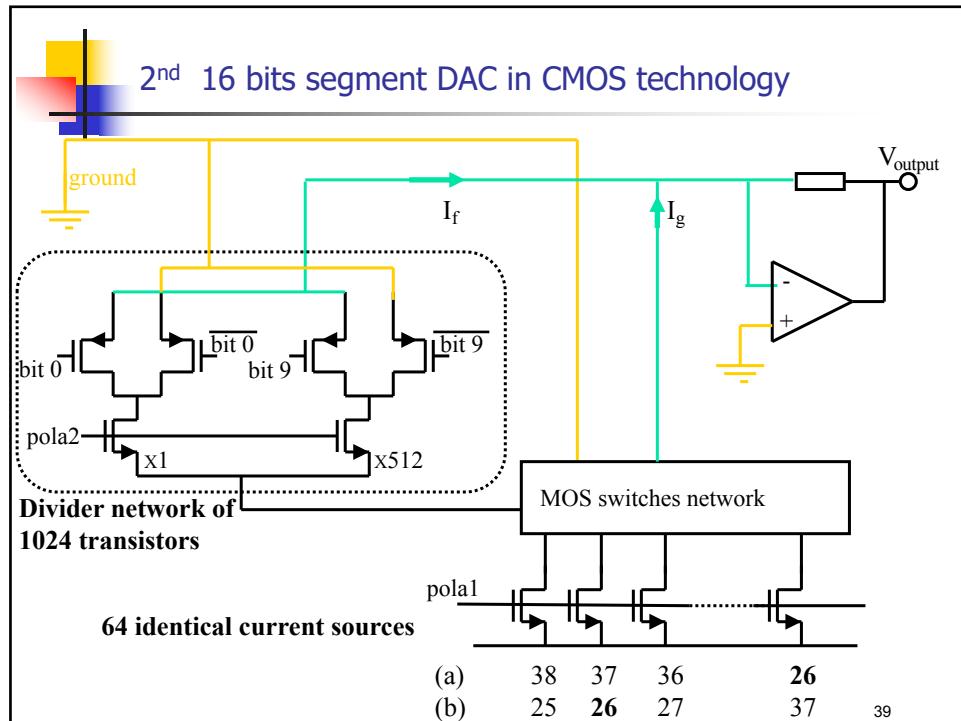
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Digital to Analog Conversion

Definition

Main features

DAC test

Weighted network parallel DAC

High resolution parallel DAC

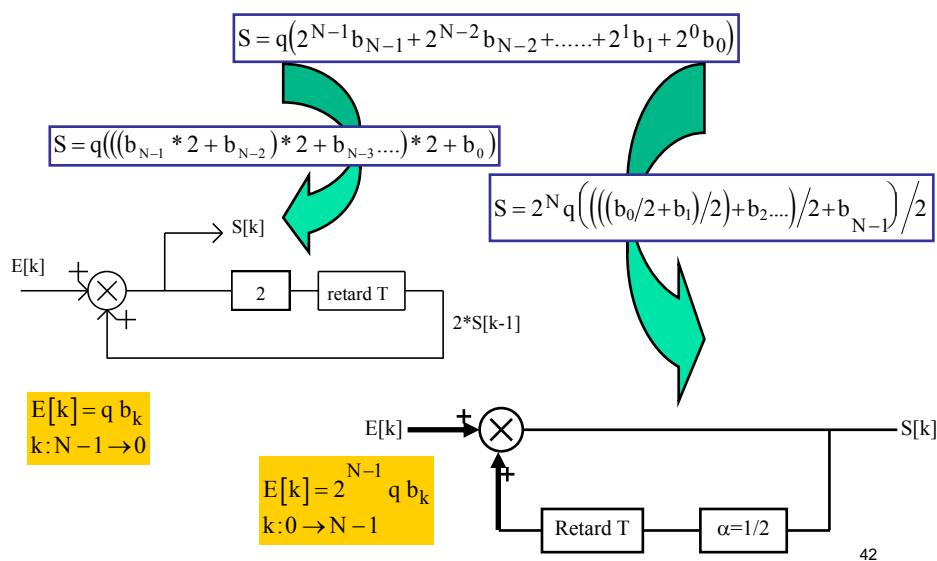
Algorithmic DAC

Conclusion

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Algorithmic DAC



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Algorithmic DAC

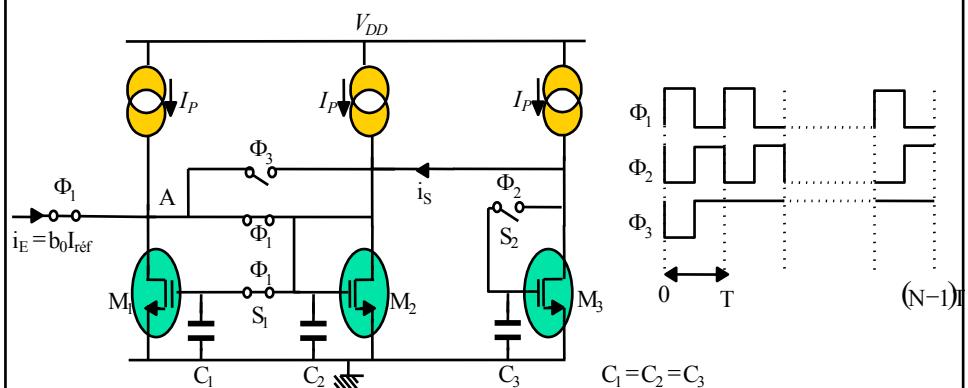
Conclusion : Only three basic operations are required to implement an algorithmic DAC :

1. Addition
2. Multiplication or division by two
3. One period delay

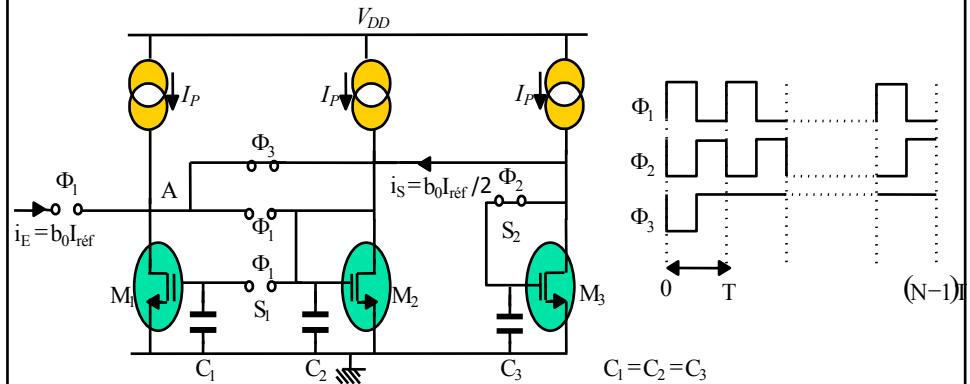
Advantages : low occupied die area
low power consumption

Drawbacks : low conversion speed
accuracy limited to 12-14 bits

Implementation in switched current (SI) technique



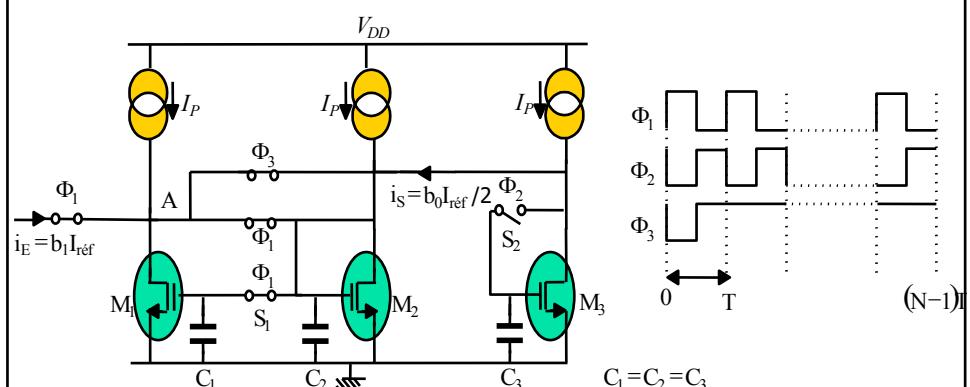
Implementation in switched current (SI) technique



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Implementation in switched current (SI) technique



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Conclusions

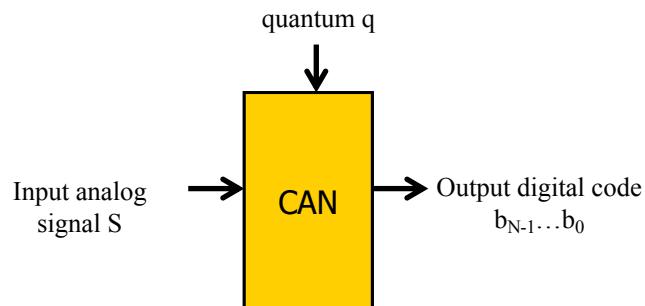
DAC type	Performances	advantages	drawbacks
R-2R network (with MOS)	8 to 10 bits a few GHz	Very fast Low power consumption	Low resolution
Binary network commuting currents	10 to 14 bits a few GHz	Very fast	Resolution limited to 10 unless calibration method is used
Thermometer network commuting currents	10 bits a few GHz	Good resolution (low DNL)	High occupied die area beyond 8 bits
Segment architecture	10 to 16 bits a few GHz	Very fast for 10 bits (\rightarrow 10 GHz)	Average power consumption
Algorithmic or cyclic	12 to 14 bits a few MHz	Low power consumption Low occupied die area	low conversion speed

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Analog to Digital Conversion

- Definition
- Sampling and Hold
- Successive approximation ADC
- Algorithmic ADC
- Flash ADC
- Oversampling technique and $\Sigma\Delta$ conversion
- ADC performance: State-of-the-art

Definition



$$S = q(2^{N-1}b_{N-1} + 2^{N-2}b_{N-2} + \dots + 2^1b_1 + 2^0b_0) + e$$

Main characteristics: resolution, accuracy, offset error, gain error, INL, DNL...

Sample and Hold circuit is required

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Characteristic equation

$$V_{\text{analogique}} = N \times V_{\text{référence}} + e$$

Code Reference voltage Quantization error

$$-\frac{q}{2} \leq e < +\frac{q}{2} \quad q : \text{quantization step}$$

N : digital code on n bits : { b_{n-1}, ..., b_0 }

n : converter resolution

$$q = \frac{V_{\text{référence}}}{2^n}$$

$$N = \frac{b_{n-1}}{2} + \frac{b_{n-2}}{2^2} + \dots + \frac{b_0}{2^n}$$

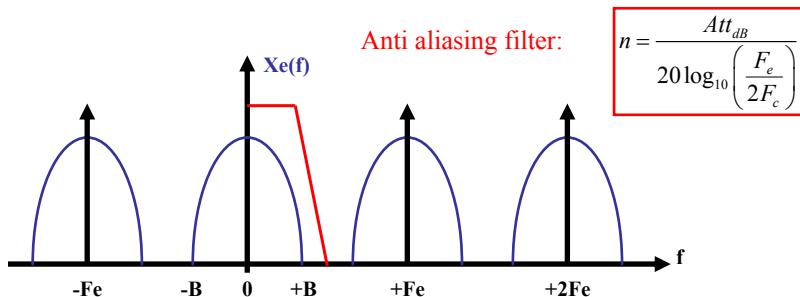
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Sampling

$$x_e(t) = x(t) \sum_{n=-\infty}^{n=+\infty} \delta(t - nT_e) = \sum_{n=-\infty}^{n=+\infty} x(nT_e) \delta(t - nT_e) \quad \delta_{T_e}(t) = \frac{1}{T_e} \sum_{n=-\infty}^{n=+\infty} e^{j \frac{2\pi}{T_e} nt}$$

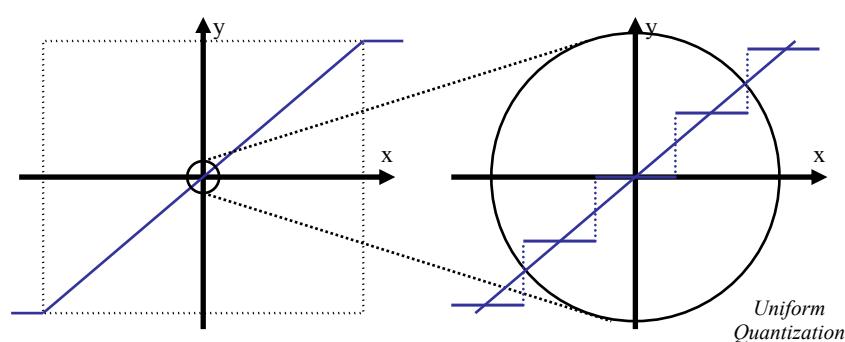
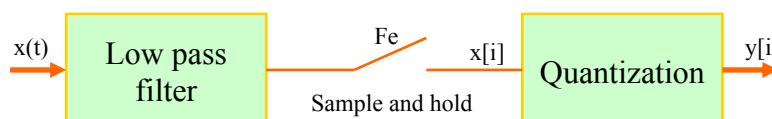
$$X_e(f) = \frac{1}{T_e} X(f) * \sum_{n=-\infty}^{n=+\infty} \delta(f - nF_e) = \frac{1}{T_e} \sum_{n=-\infty}^{n=+\infty} X(f - nF_e)$$



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« Nyquist type » conversion



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Analog to Digital Conversion

Definition

Sampling and Hold

Successive approximation ADC

Algorithmic ADC

Flash ADC

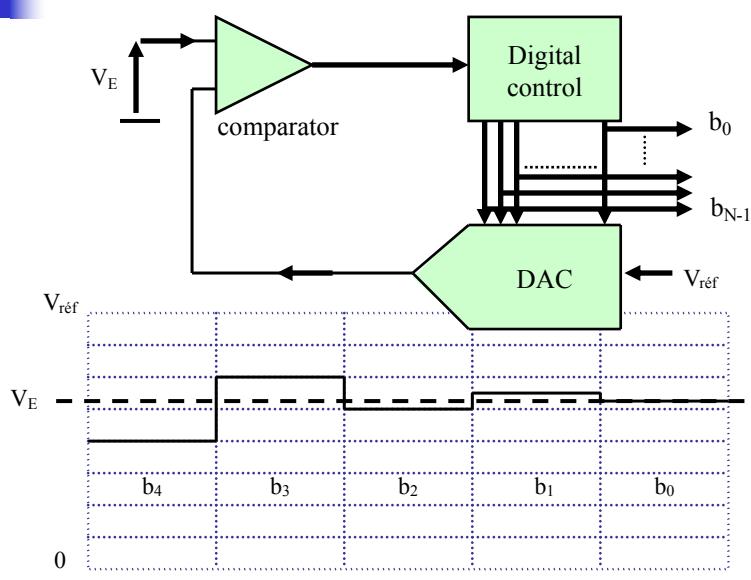
Oversampling technique and $\Sigma\Delta$ conversion

ADC performance: State-of-the-art

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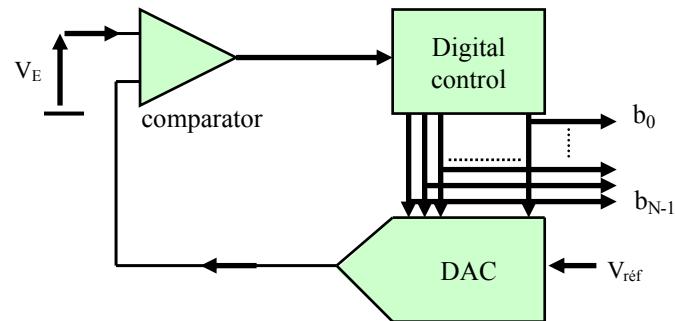
Successive approximation ADC



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Successive approximation ADC



Drawback : low converters

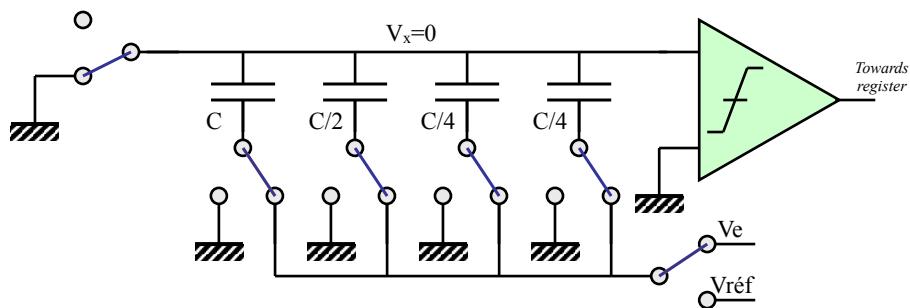
*Advantages : good performances
not expensive to design and implement*

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Charge redistribution ADC

1. Sampling mode

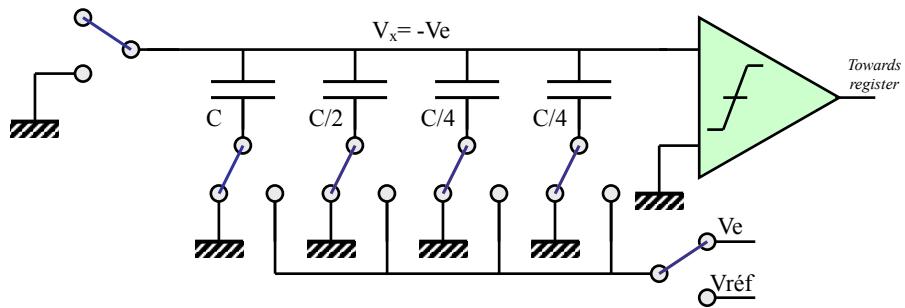


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Charge redistribution ADC

2. Hold mode

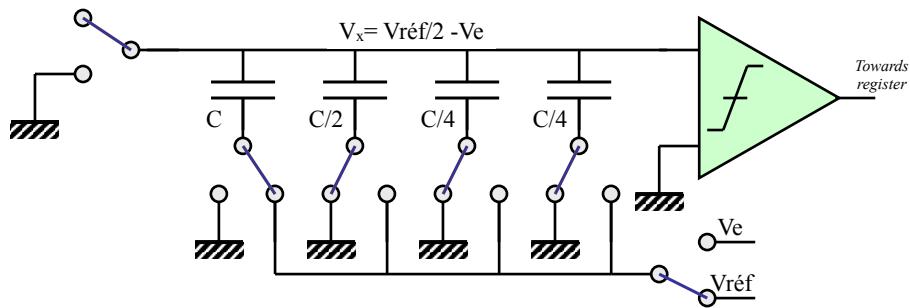


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Charge redistribution ADC

3. Test from MSB to LSB

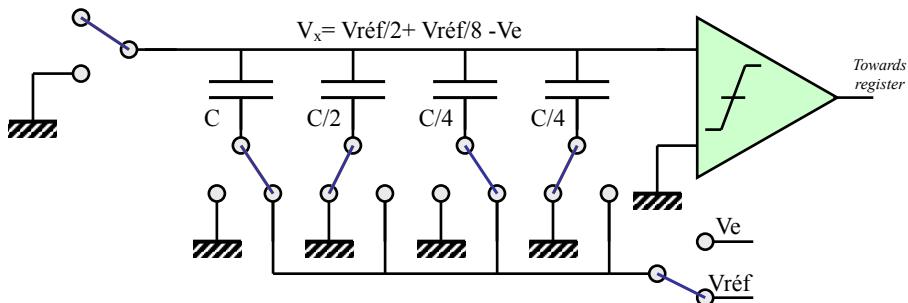


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Charge redistribution ADC

Eventually, V_x is smaller than one LSB



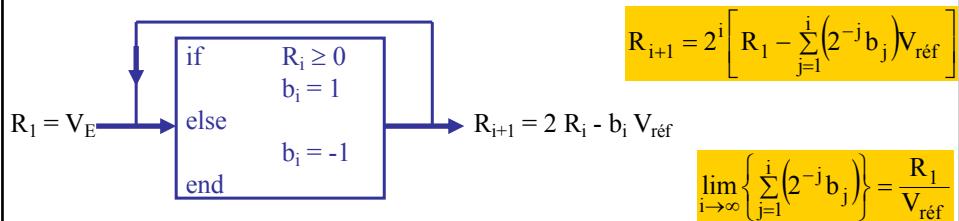
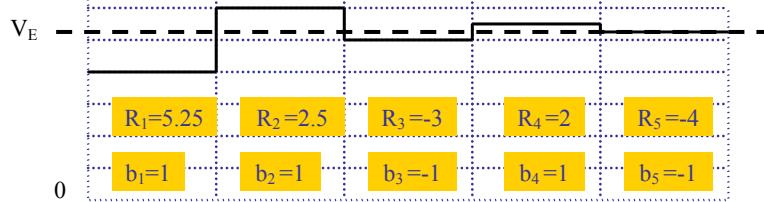
→ Converter insensitive to parasitic capacitances

→ The charge $2CV_e$ initially distributed onto all the capacities has been ‘redistributed’ only onto the capacities linked to $V_{\text{réf}}$.

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Algorithmic ADC

$$V_E = \left(\sum_{i=1}^N b_i 2^{-i} \right) V_{\text{réf}} \quad \text{where } b_i \text{ is equal to } \pm 1$$

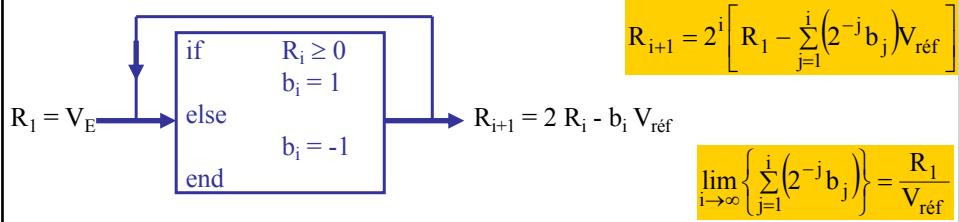


Algorithmic ADC

Advantages : low power consumption
low occupied die area

Drawback : low conversion speed

Resolution : 13 to 14 bits

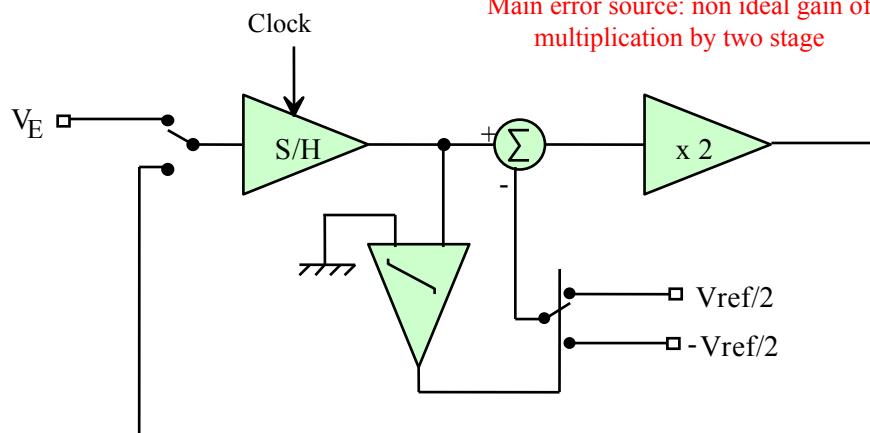


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Algorithmic ADC

Main error source: non ideal gain of multiplication by two stage



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Analog to Digital Conversion

Definition

Sampling and Hold

Successive approximation ADC

Algorithmic DAC

Flash DAC

Oversampling technique and $\Sigma\Delta$ conversion

ADC performance: State-of-the-art

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Fast AD conversion

Aimed sampling frequencies: a few MS/s to a few **100 MS/s** (to a few GS/s)
Applications : telecommunications, video, medical imaging, radars, network analyzers.

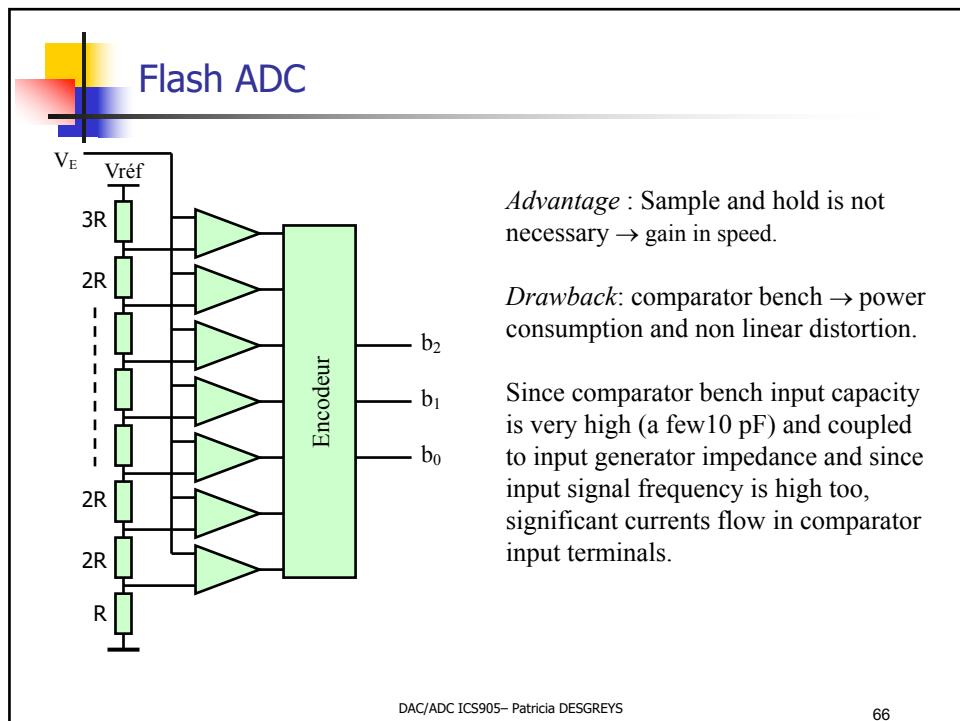
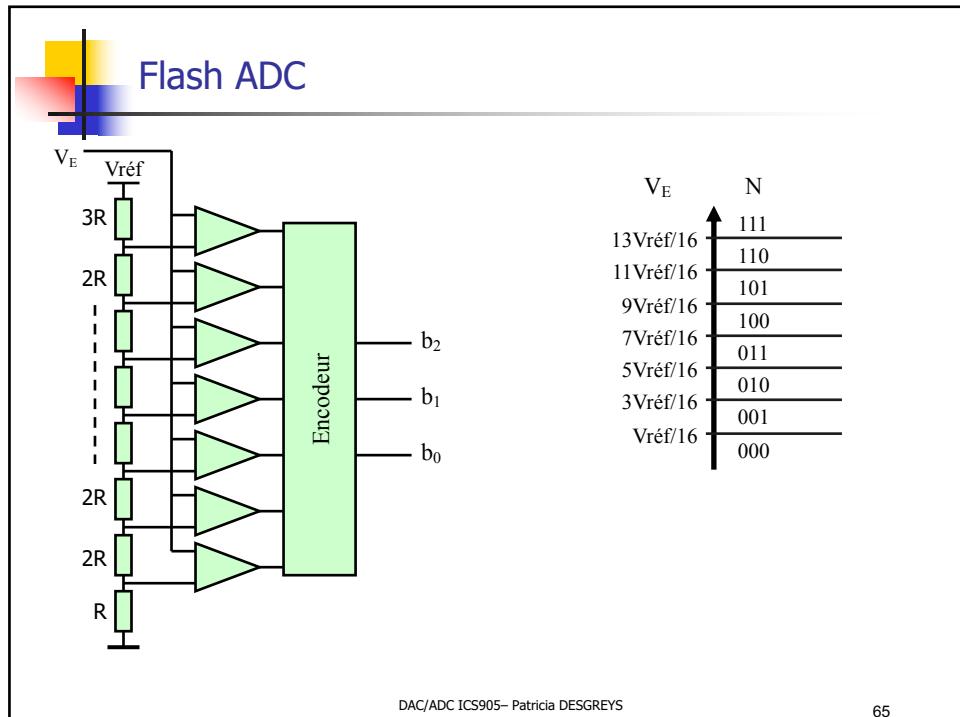
- ➡ require a parallel conversion in one clock cycle
- ➡ AD-equivalent of thermometer coded network DAC

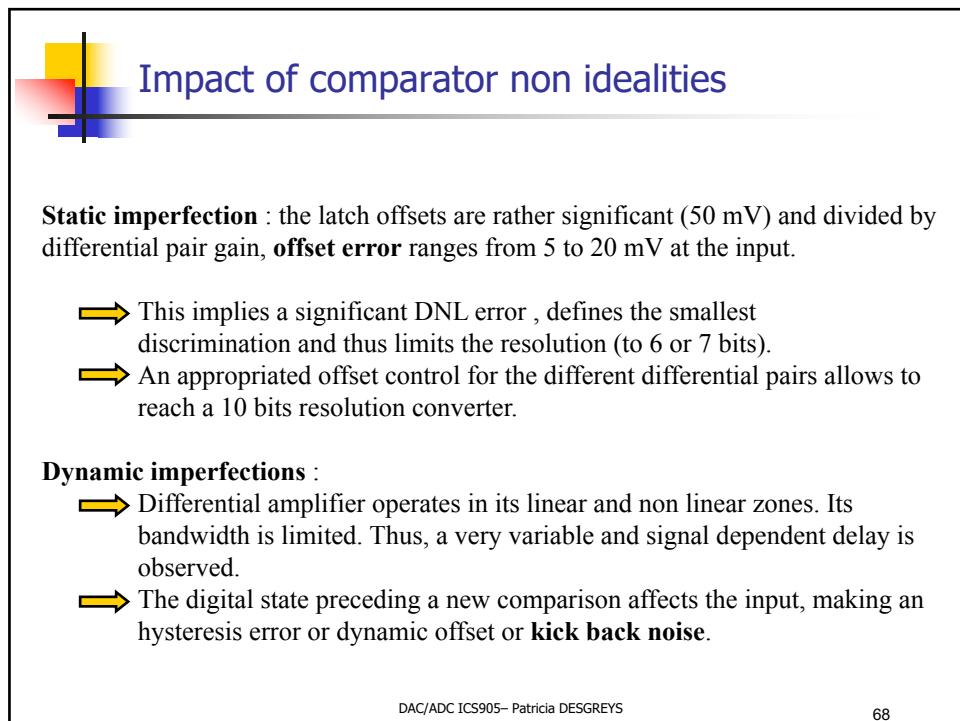
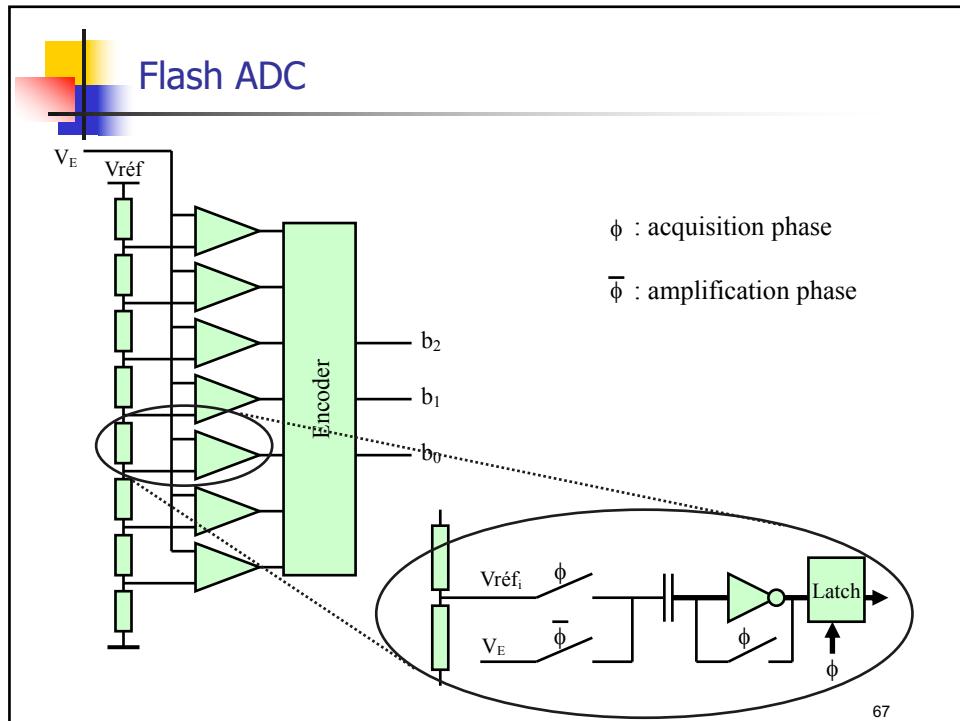
The only converters that really operate in one clock cycle are **the flash converters**.

Others converters (half-flash converters, pipeline converters) combine low resolution flash converters and algorithmic architectures to decrease the power consumption at the price of 2 or 3 clock cycles.

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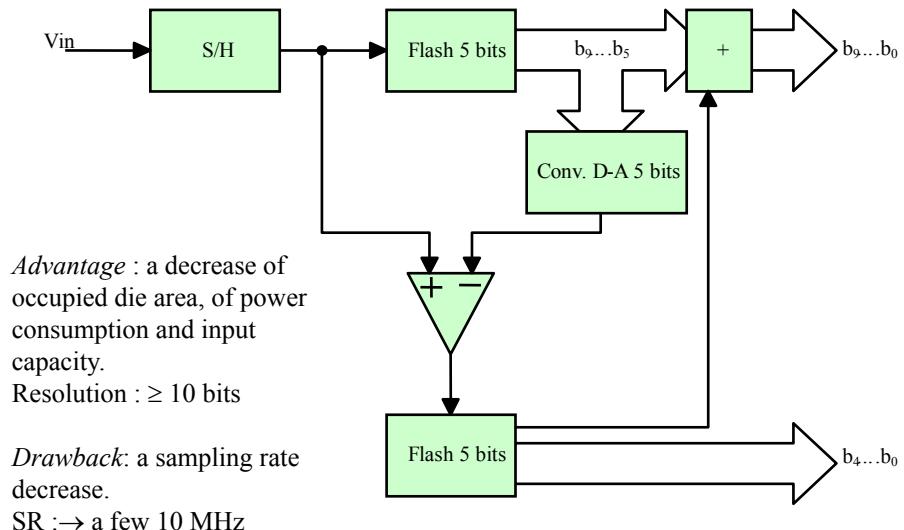




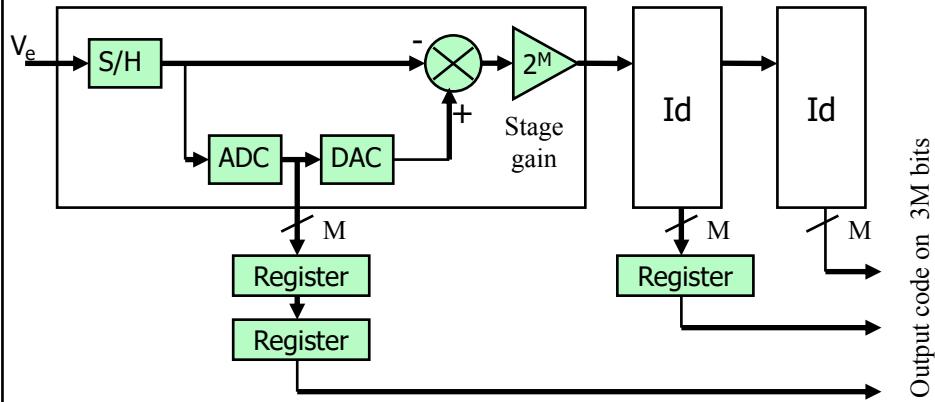
Other sources of non linear distortion

- The reference scale also defines the smallest discrimination and thus limits the resolution. Polysilicium features a resistance of a few $10 \Omega/\square$ but reproducibility isn't very satisfying.
There is a direct consequence on INL error but DNL error is negligible and no monotonicity error appears.
Max. resolution : 8 bits (or 10 bits if laser adjustment)
- Clock Jitter
Comparator noise
Layout

Half-flash ADC



Pipeline architecture



Advantage : an increase of the resolution (14-16 bits) without a decrease of the sampling rates (a few 10 MS/s) with a limitation of occupied die area and power cosumption.

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Limited resolution architectures

Adc type	Performances	advantages	drawbacks
Successives approximations	10 to 12 bits a few MHz	Low cost	Low speed of conversion
Algorithmic or cyclic	12 to 14 bits a few MHz	Low consumption Low occupied area	Low speed of conversion
Flash	8 to 10 bits a few GHz	Very fast	High power consumption
Half-flash	12 to 14 bits a few 100 MHz	Consumption, occupied area and conversion speed average	
Pipeline	14 to 16 bits a few 100 MHz	Good resolution, Low consumption for 10 bits	

For all these converters, accuracy is limited by component matching. With a standard CMOS technology, mismatching on integrated capacitances or resistors limits the accuracy at 10-12 bits (+2 if laser adjustment).

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Analog to Digital Conversion

Definition

Sampling and Hold

Successive approximation ADC

Algorithmic DAC

Flash DAC

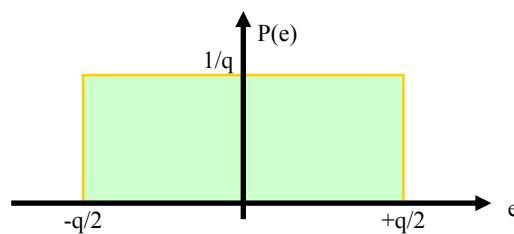
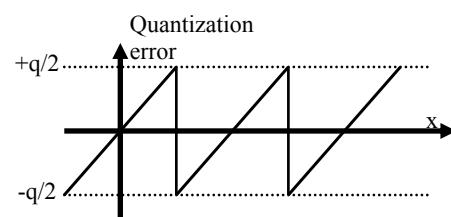
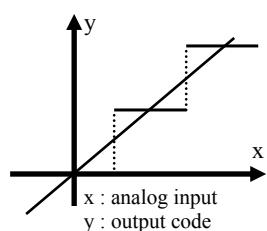
cube **Oversampling technique and $\Sigma\Delta$ conversion**

ADC performance: State-of-the-art

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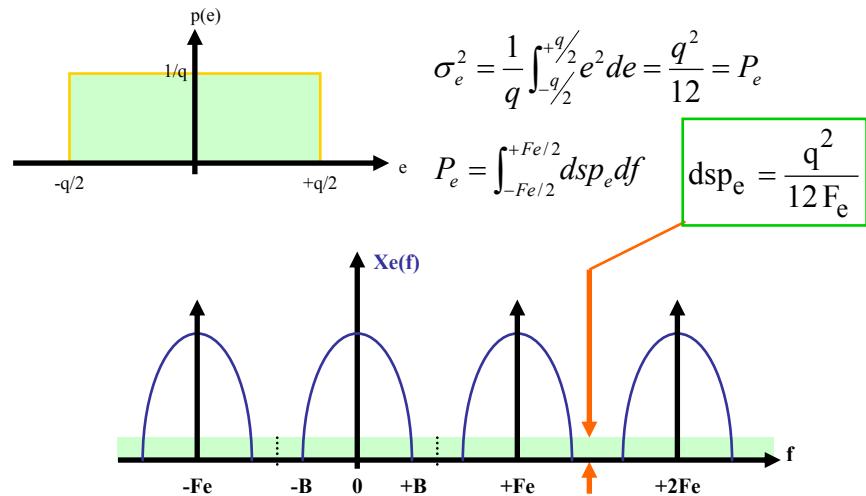
Quantization error



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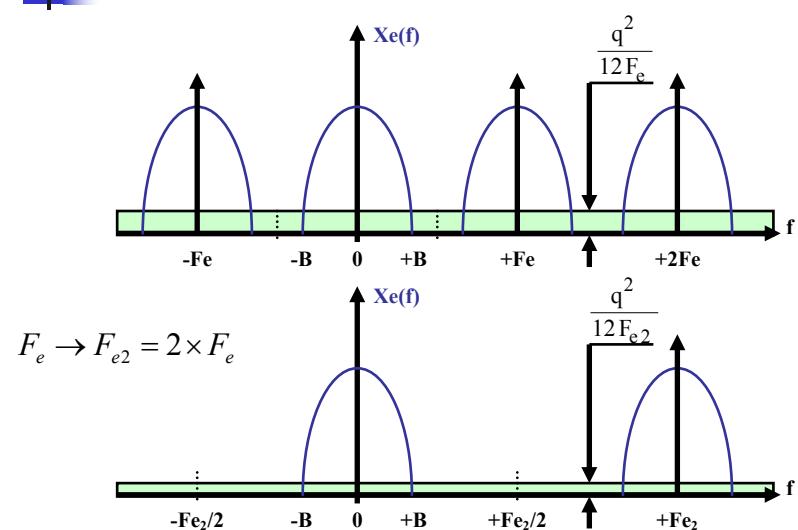
Quantization noise



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Oversampling effect



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Signal to noise ratio (1)

Sinusoidal signal : $x(t) = a \cdot \sin(2\pi f_s t)$ $P_x = \frac{a^2}{2}$

$$P_{e \text{ bande utile}} = \int_{-F_s}^{+F_s} ds p_e df = \frac{q^2}{12 F_s} \cdot 2 F_{\text{Nyquist}} = \frac{q^2}{12 OSR}$$

$$q = \frac{2 \cdot a_0}{2^n - 1}$$

$$SNR = 10 \log \left(\frac{P_x}{P_{e.b.u.}} \right) = 10 \log \frac{3}{2} + 20 \log \frac{a}{a_0} + 20 \log (2^n - 1) + 10 \log OSR$$

Signal to noise ratio (2)

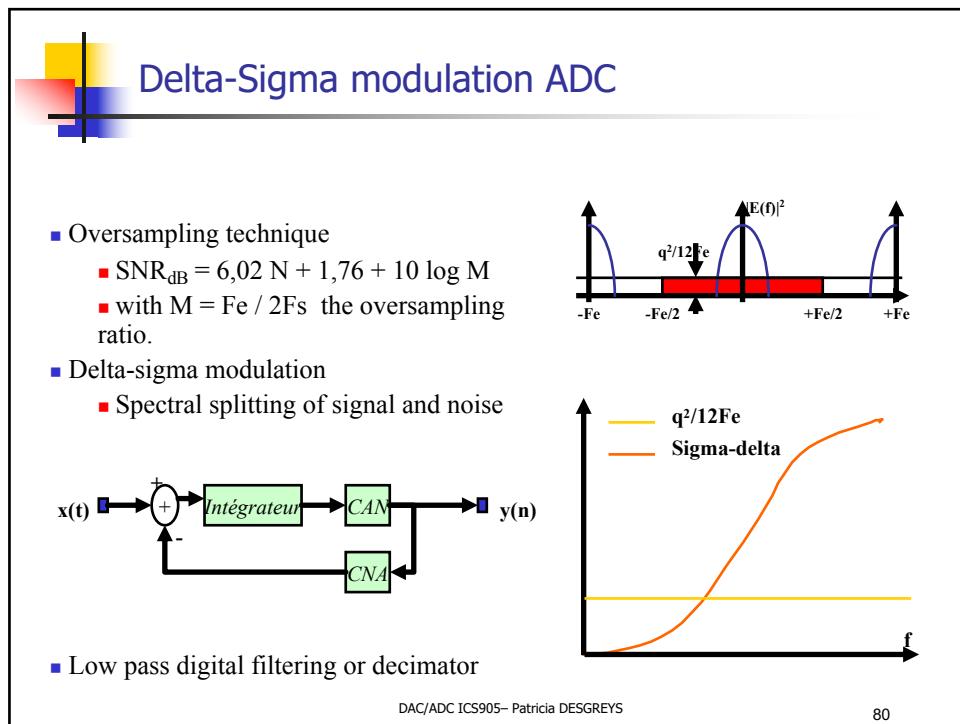
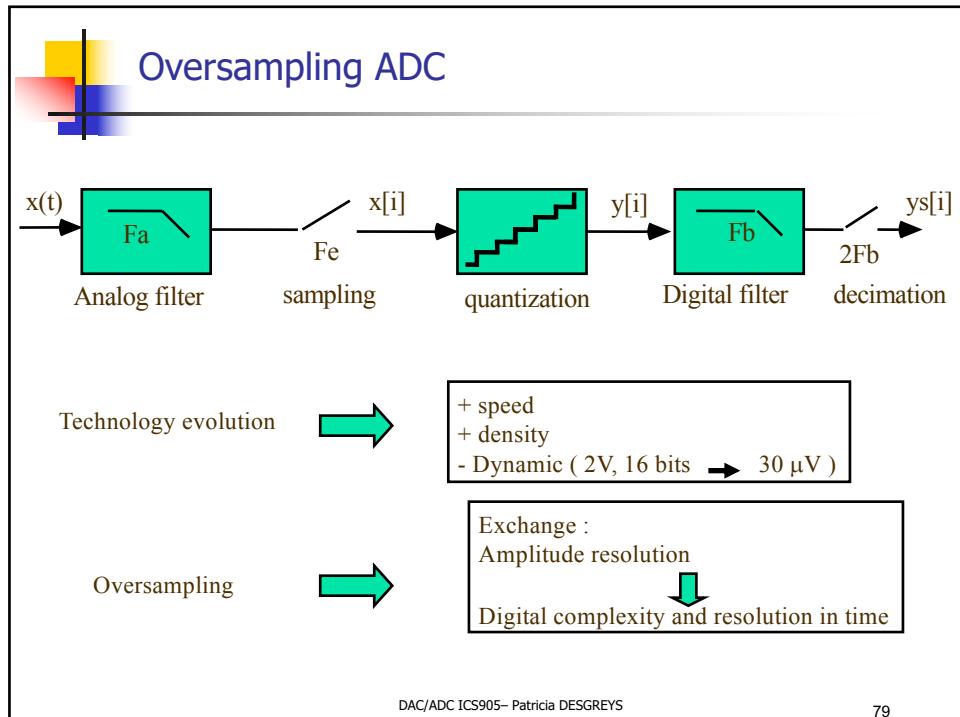
Assumptions : $a = a_0$

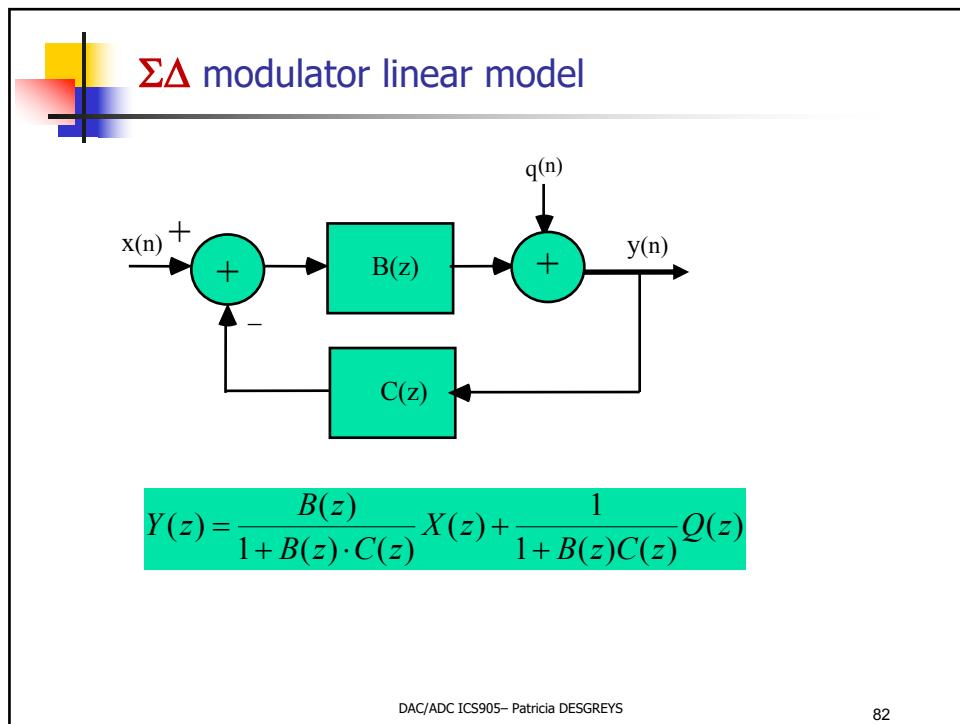
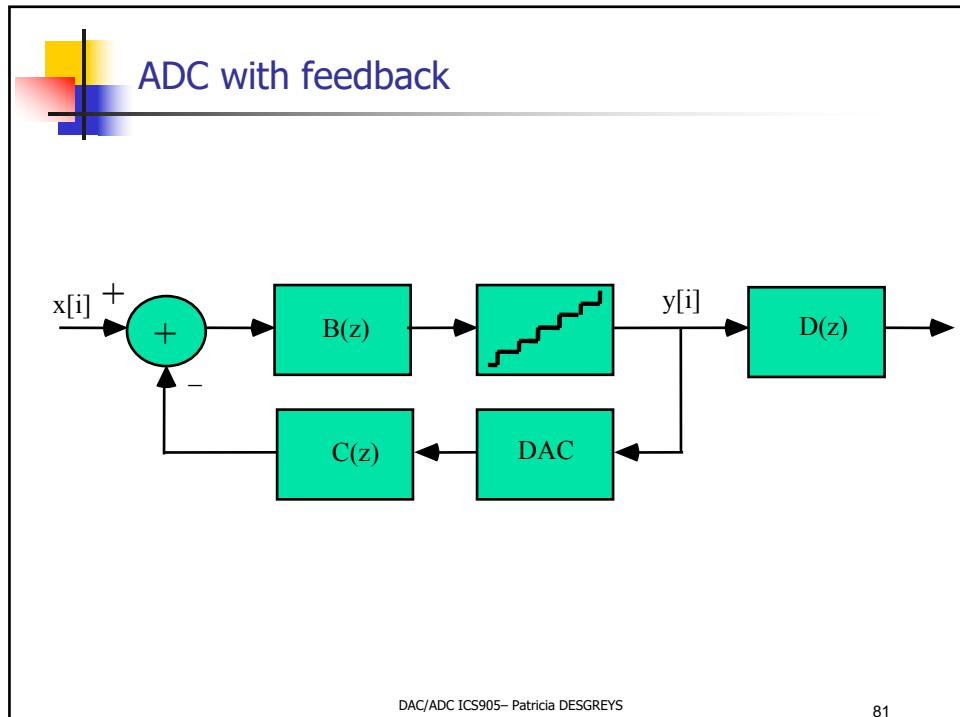
$$OSR = 2^L$$

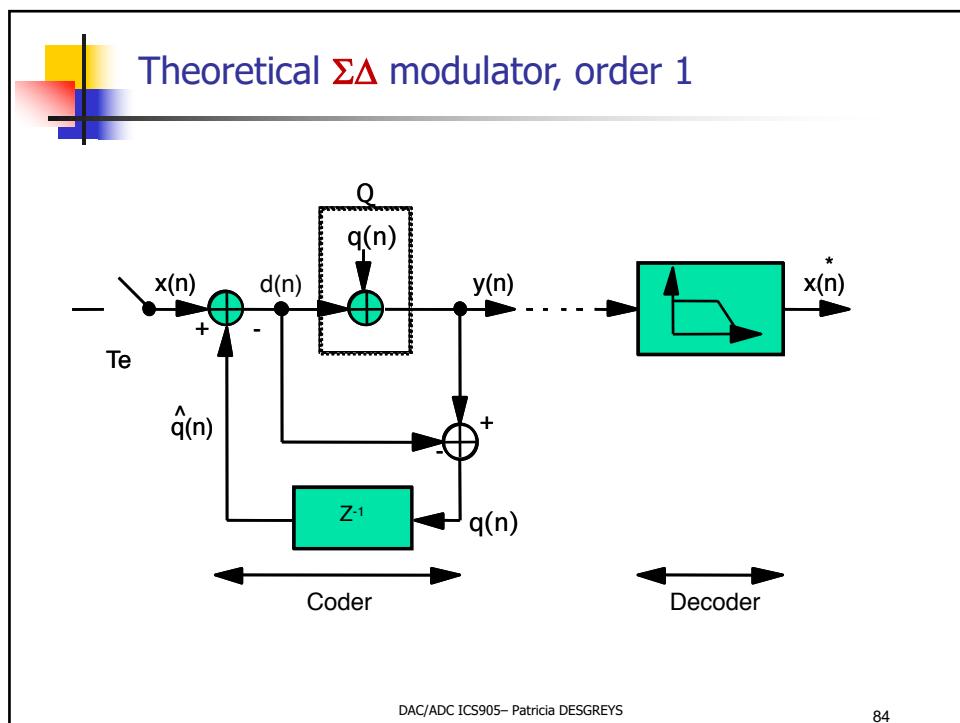
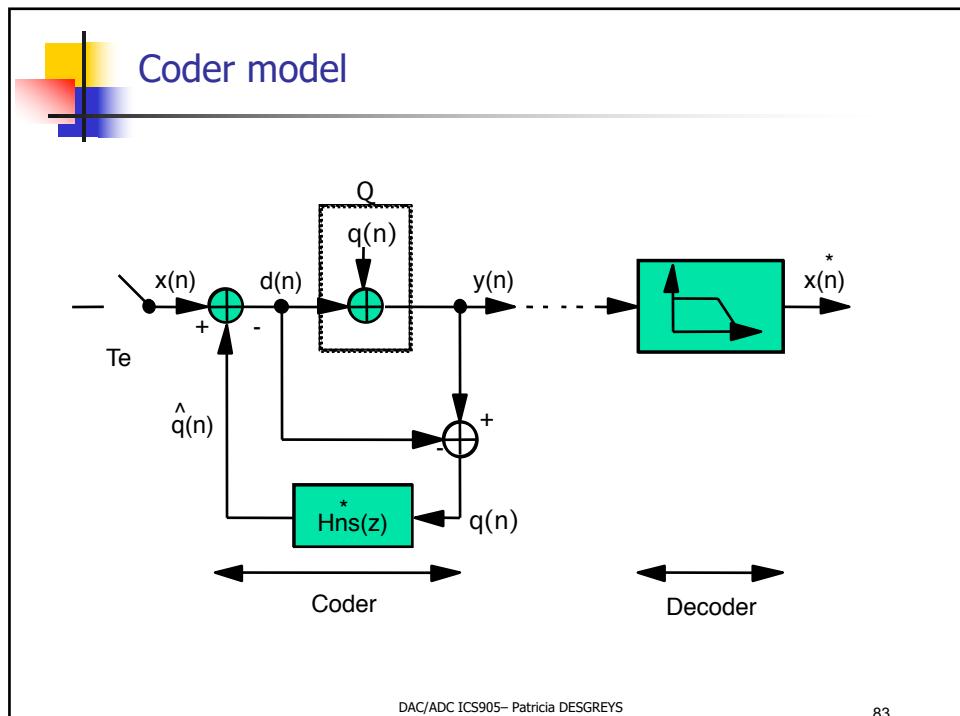
$$n \text{ tel que } 2^n \gg 1$$

$$SNR_{(dB)} = 10 \log \left(\frac{P_x}{P_{e.b.u.}} \right) \approx 1,76 + 6,02 \cdot n + 3,01 \cdot L$$

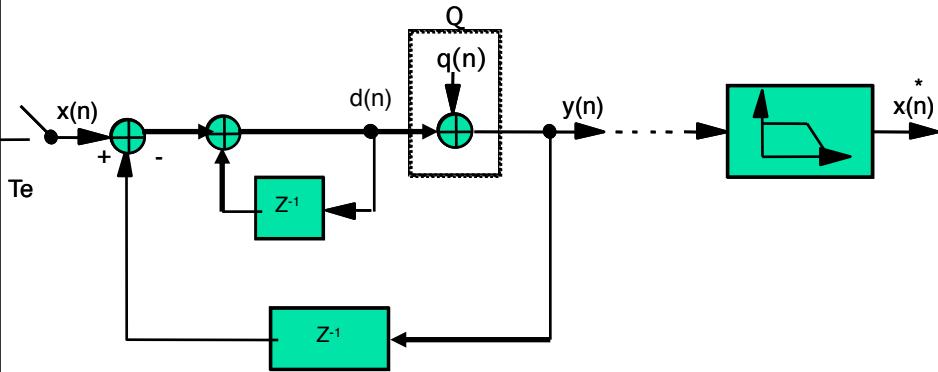
It is necessary to quadruple the sampling frequency to gain the equivalent of one bit of quantization.







Real $\Sigma\Delta$ modulator, order 1

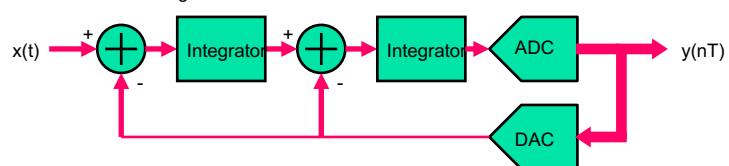


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Generalization to any order

Second order Sigma Delta Modulator



$$Y(z) = z^{-1} \cdot S(z) + z^{-1} \cdot (1 - z^{-1})^2 \cdot E(z)$$

$$DSP_Q(f) = DSP_E(f) \cdot 16 \cdot \sin^4 \left(\pi \frac{f}{f_e} \right)$$

□ N order :

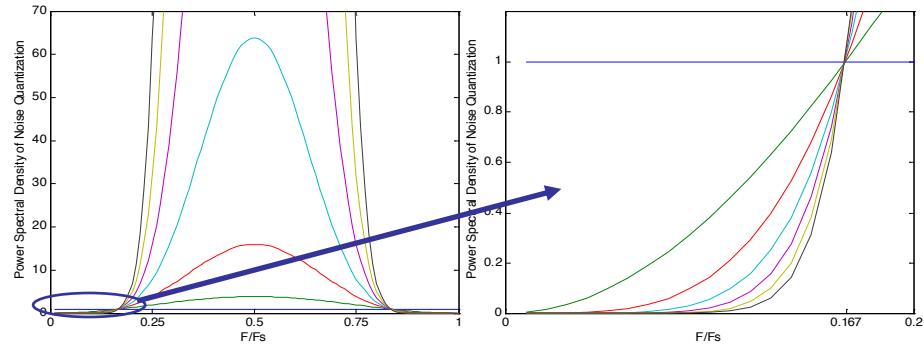
$$Y(z) = z^{-1} \cdot S(z) + z^{-1} \cdot (1 - z^{-1})^N \cdot E(z)$$

$$DSP_Q(f) = DSP_E(f) \cdot 2^{2 \cdot N} \cdot \sin^{2 \cdot N} \left(\pi \frac{f}{f_e} \right)$$

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Noise shaping effect



$$DSP_Q(f) = DSP_E(f) \cdot 2^{2N} \cdot \sin^{2N} \left(\pi \frac{f}{f_e} \right)$$

Signal Noise Ratio of the $\Sigma\Delta$ modulator

$$SNR = \frac{P_{signal}}{P_{bruit}}$$

$$P_{signal} = \frac{S_{max}^2}{2}$$

$$OSR = \frac{fe}{2f_s} = 2^L$$

$$P_Q = \frac{\Delta^2}{12} \cdot \frac{\pi^{2N}}{2 \cdot N + 1} \cdot OSR^{-(2N+1)}$$

$$SNR = SNR_{quantiser} + \Delta SNR$$

$$\Delta = \frac{2 \cdot ref}{2^n - 1}$$

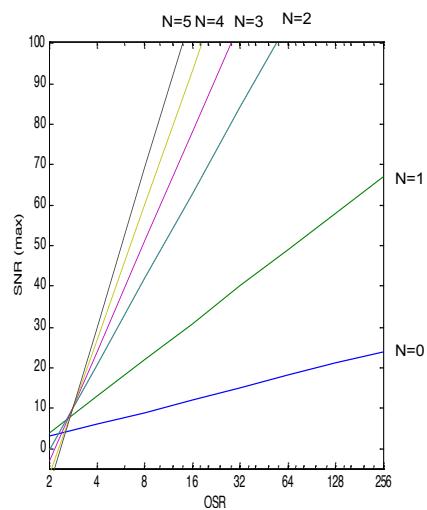
$$\Delta SNR = 10 \cdot \log(2 \cdot N + 1) - N \cdot 20 \cdot \log \pi + L \cdot N \cdot 20 \cdot \log 2$$

$$SNR_{quantiser} = 10 \cdot \log \frac{3}{2} + 20 \cdot \log \frac{S_{max}}{ref} + 20 \cdot \log(2^n - 1) + L \cdot 10 \cdot \log 2$$

Quantization noise and oversampling effects

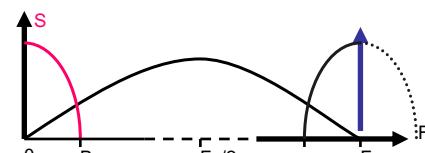
- Only oversampling effect
 - $N=0; L=\log_2 OSR$
 - +3.01dB/octave of F_s
- Oversampling and Noise Shaping effects
 - $N=1$
 - +9.03dB/octave of F_s
 - $N=2$
 - +15.05dB/octave of F_s
 - $N=3$
 - +21.07dB/octave of F_s
 - $N=4$
 - +27.09dB/octave of F_s

$$S_{max} = ref, n = 1$$

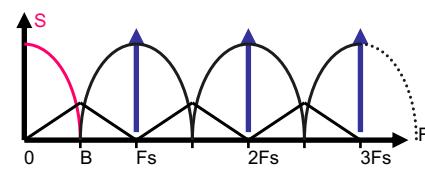


Decimation and digital filter

- Filter
 - Delete any signal and noise out of band

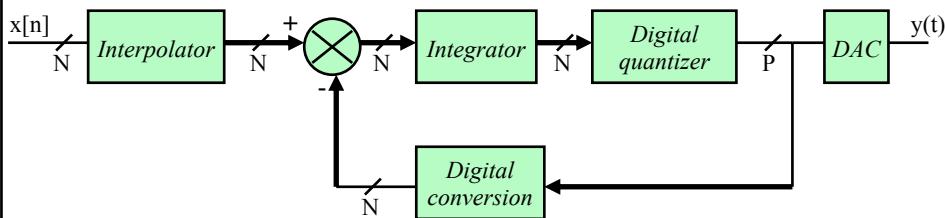


- Decimation
 - Reduce the sampling rate to $F_s=2 \times B$



Delta-Sigma modulation DAC

$P < N$ (at the limit $P=1$)



+ Low pass analog filtering of $y(t)$

Delta-Sigma converters are an attractive alternative for high resolution converters (16 bits or more). They compensate the accuracy loss inherent to the implementation of analog circuits in digital technologies thanks to faster signal processing and more digital circuits. Thus, they benefit of both analog circuit speed and digital circuit accuracy.

Drawback : Oversampling limits input signal bandwidth (a few MHz)

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Analog to Digital Conversion

Definition

Sampling and Hold

Successive approximation ADC

Algorithmic DAC

Flash DAC

Oversampling technique and $\Sigma\Delta$ conversion

ADC performance: State-of-the-art

Performance parameters

■ Speed :

- Nyquist sampling rate : F_N
 - Bandwidth : BW
 - Over Sampling Ratio : OSR
- $$F_N = 2BW$$
- $$OSR = \frac{F_s}{2BW}$$

■ Accuracy :

- Stated resolution : N
 - Signal to Noise and Distortion Ratio : SNDR
 - Effective number of bits : ENOB
 - Spurious Free Dynamic Range : SFDR
- $$ENOB = \frac{SNDR - 1.76}{6.02}$$

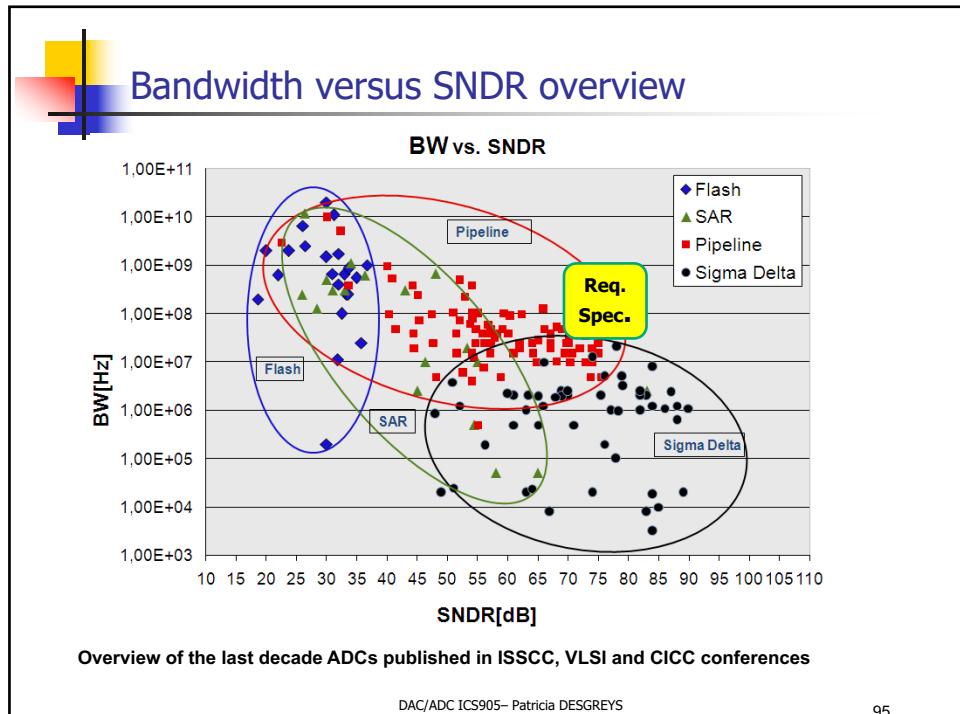
■ Power :

- Power consumption : P_{diss}
 - Figure of Merit : FoM
- $$FoM = \frac{P_{diss}}{2^{ENOB} \cdot 2BW} \text{ [pJ/step]}$$

Required specifications on the ADC

→ Analog-to-digital converters are key blocks in modern communication systems.

- 70 to 80 dB of SNR
- more than 50dB of SFDR
- 100 MHz -1 GHz of Bandwidth
- 0.1 pJ by conversion step



- ## Conclusion : Promising Techniques
- For future 5G radio requirements :
 - $\Delta\Sigma$ converters and CT implementations
 - Pipeline converters
 - Parallel implementation and increasing use of calibration and digital correction
 - For multi-channel cable receiver :
 - TI SAR converters
 - An attractive solution:
 - CT BP $\Delta\Sigma$ converters and Parallelism
- DAC/ADC ICS905– Patricia DESGREYS
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