Frequency Synthesis

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Summary

- Digital Transceiver RF Front-end
- RF oscillators
- PLLs
- Indirect frequency synthesis

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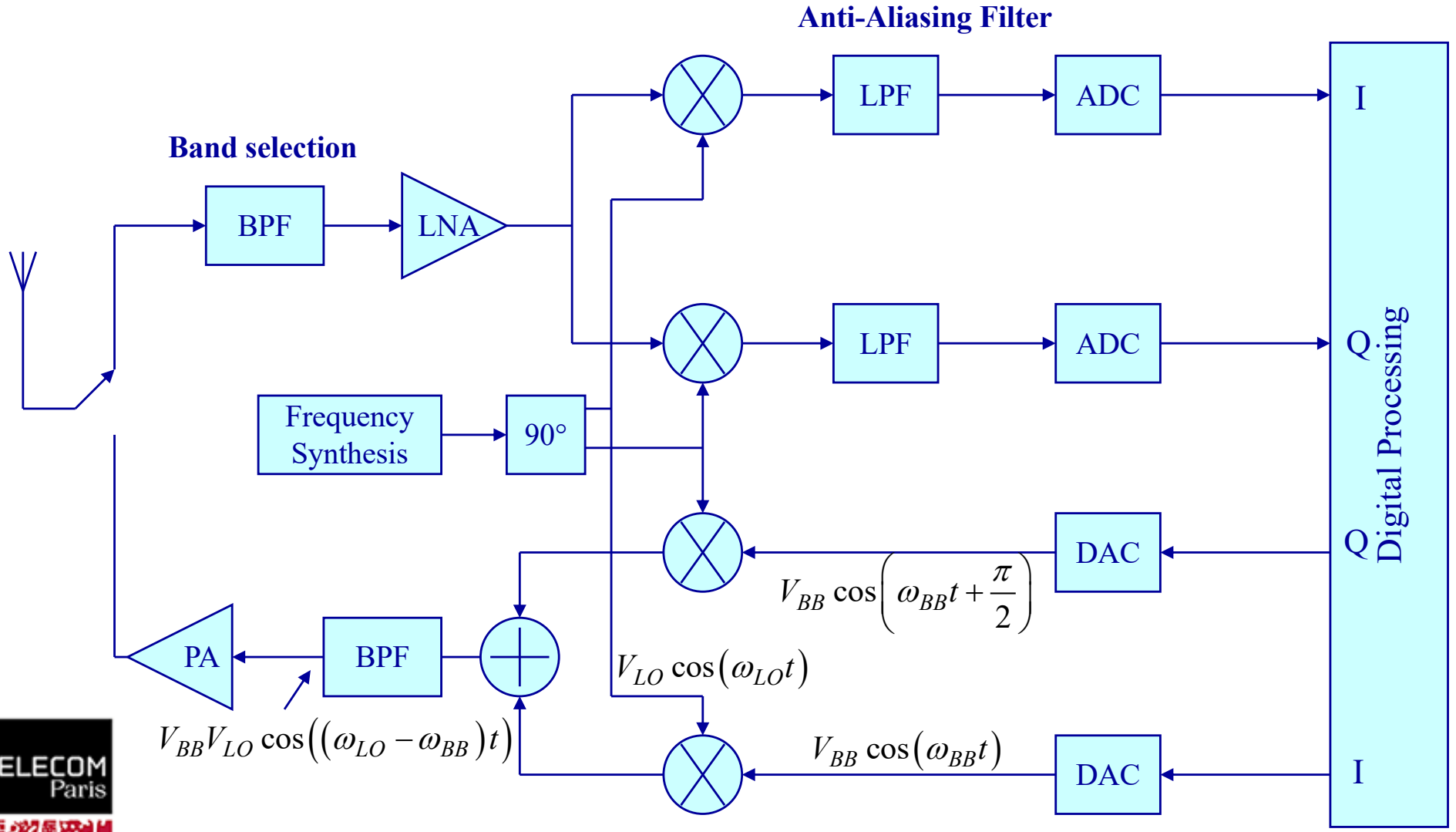
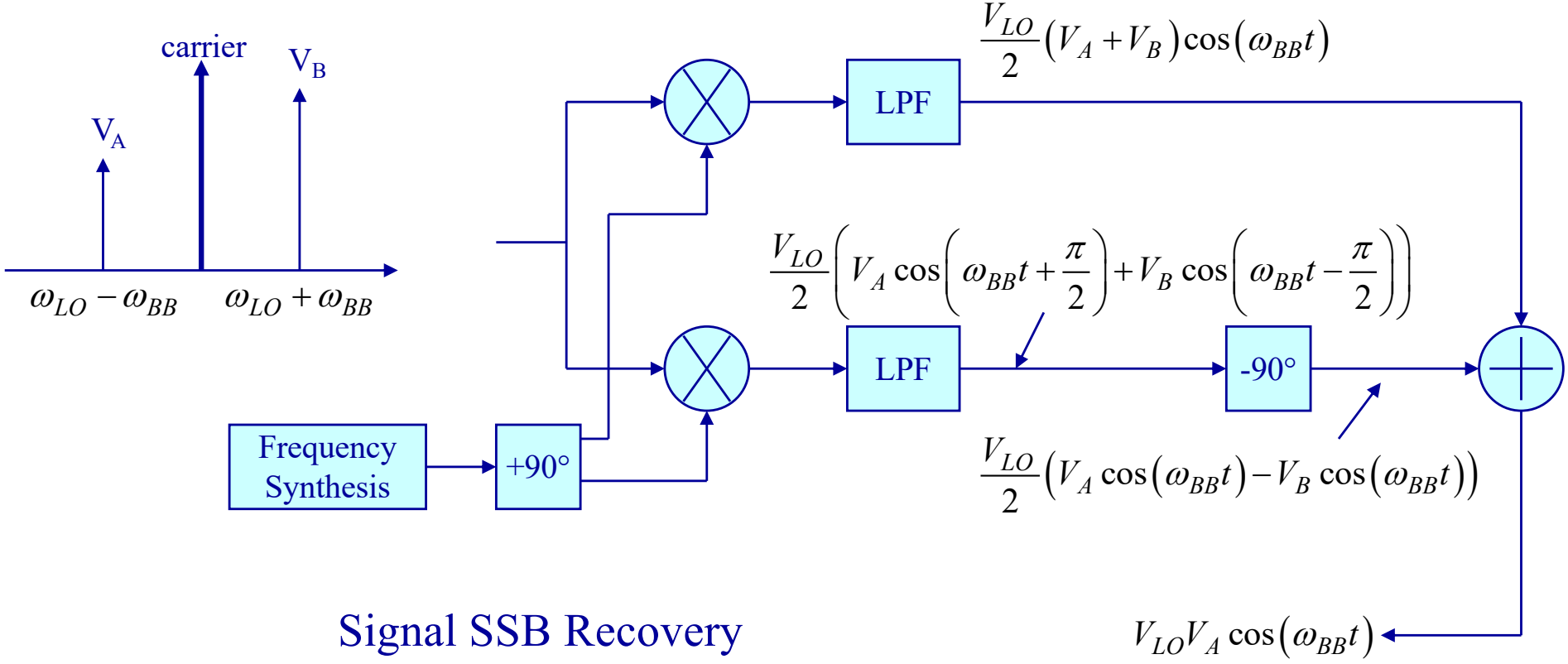
Transceiver chain



Direct conversion transceiver SSB

Single-Side Band Transceiver



Signal SSB Recovery

RF frequency synthesis: RF oscillator, PLL

$$f_{LO} = f_0 + k\, f_{ch}$$ Chanel selection

Mixer converts signal band around carrier frequency down to DC (baseband)

Key functions

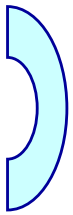
Almost all the functions are implemented in digital signals :

- Coding/decoding
- Modulation/demodulation (amplitude, frequency or phase)
- Pulses shaping (raised cosine filtering)

A few analog functions remain unavoidable :

- LNA, Mixers
- Power amplifiers
- Filters
- ADC & DAC

- RF oscillators
- PLLs
- Frequency synthesizers



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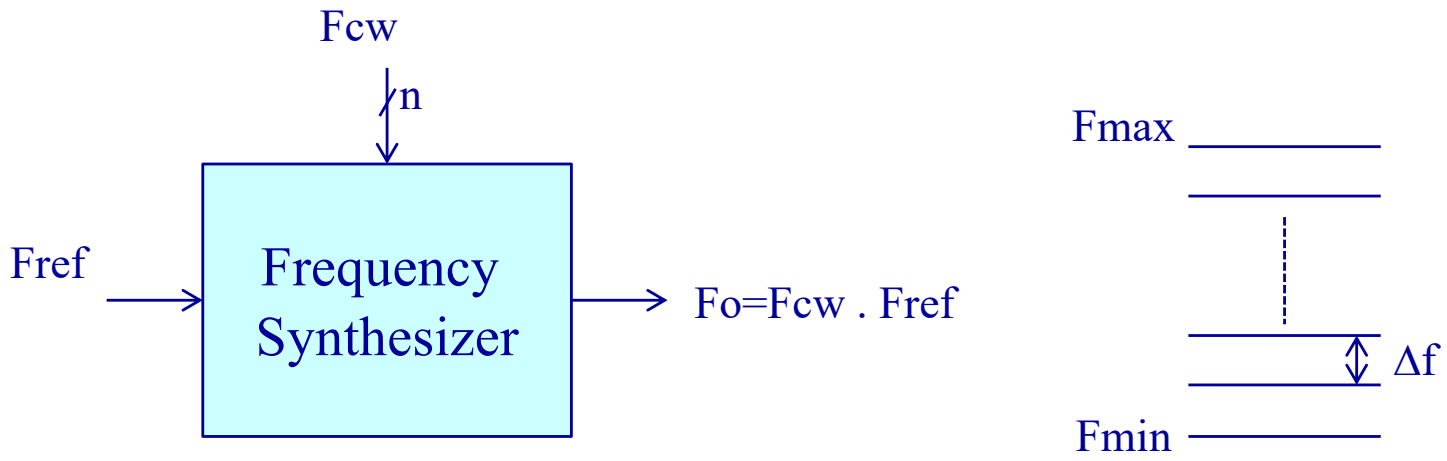
Frequency synthesizer

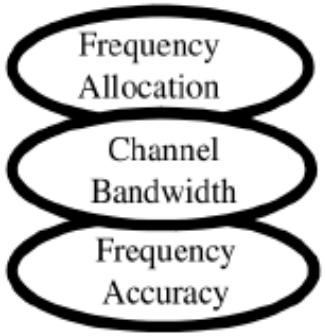
The “black box” view of a frequency synthesizer is a block getting a very stable reference frequency (usually provided by quartz oscillator) and delivering a set of frequencies between F_{min} and F_{max} with a resolution of Δf :



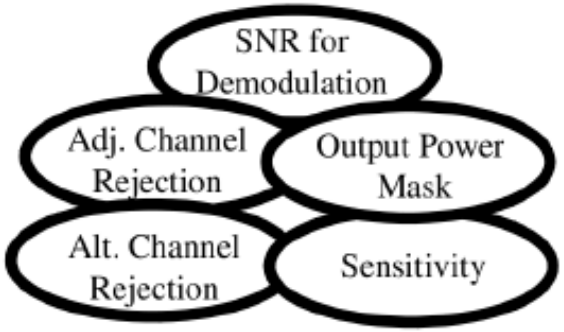
The frequency range [F_{min}, F_{max}] and the resolution Δf are synthesizer fundamental specifications which depend on the application.

Main specifications

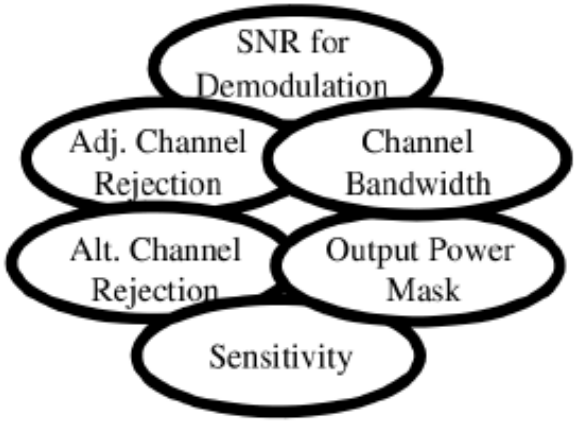
- Frequency range
- Resolution
- Accuracy
- Settling time
- Reference frequency
- Spurs
- Power consumption
- Temperature stability
- Phase noise



Frequency Synthesis



Spur Rejection



Phase Noise

Settling Time

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Summary

- Digital Transceiver RF Font-end
- RF oscillators
- PLLs
- Indirect frequency synthesis

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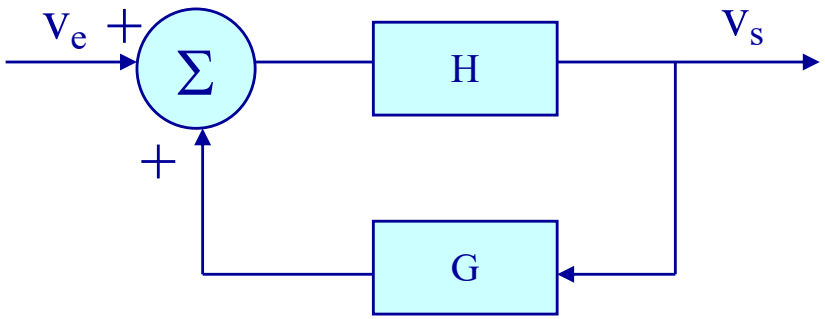
RF oscillators - Introduction

An oscillator must provide a self-sustaining periodic signal

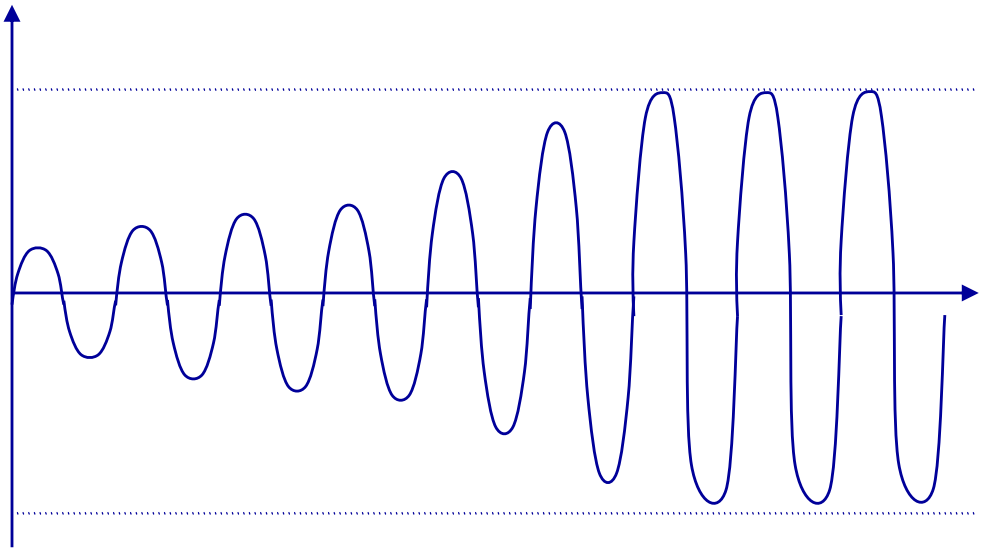


Positive feedback system

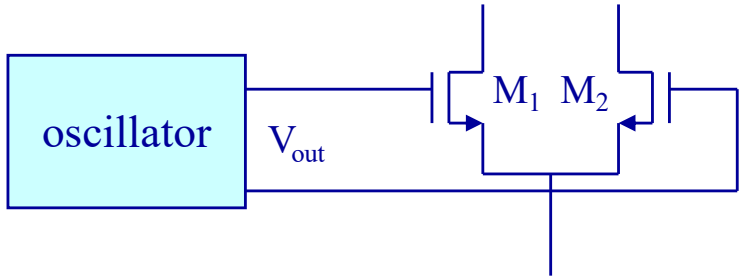
$$V_s = \frac{H(j\omega)}{1 - G(j\omega)H(j\omega)} V_e$$

Barkhausen criterion

$$\begin{cases} |G(j\omega_0)||H(j\omega_0)| = 1 \\ \arg\{G(j\omega_0)H(j\omega_0)\} = 0 \end{cases}$$



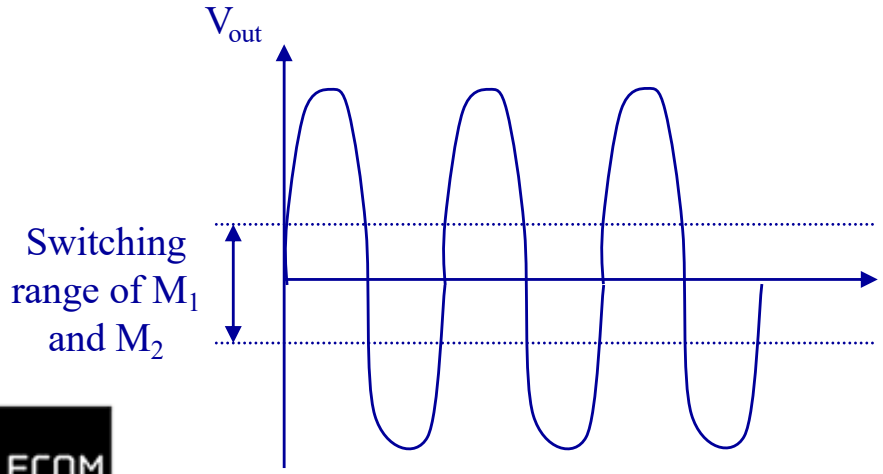
RF oscillators – Output waveform



Input stage of an active CMOS mixer

Mixer good behavior is favored if the waveform of the local oscillator (LO) exhibits abrupt transitions and if the duty cycle is equal to 50%

Ideal waveform = Square wave signal



Approximation of a square wave signal with a large amplitude sinusoid

- Large amplitude wave
- Differential topology for duty cycle of 50%

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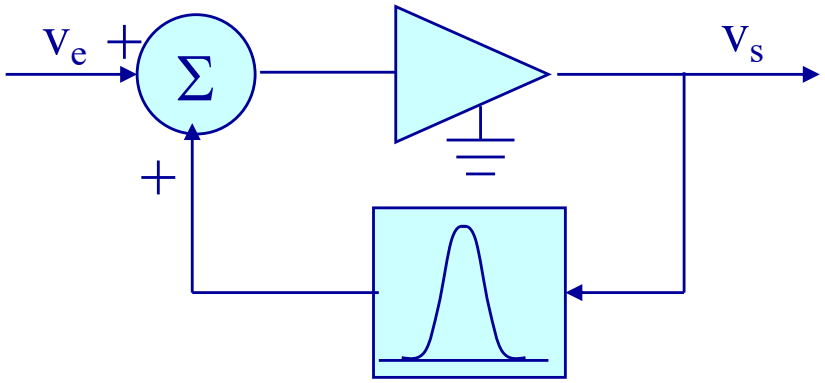
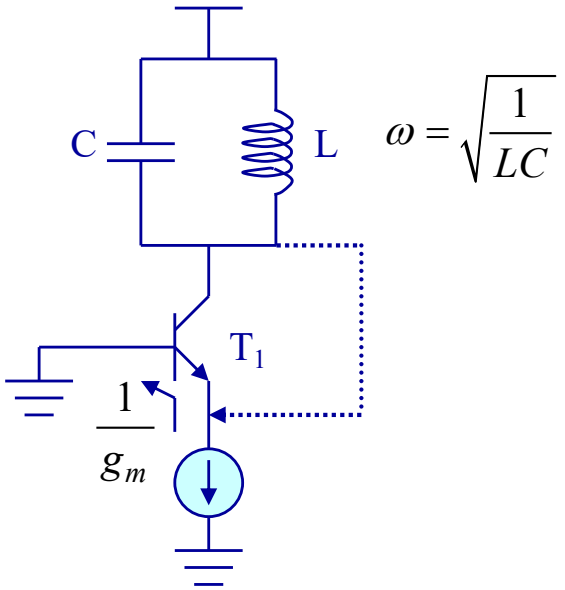
RF oscillators – Frequency selection

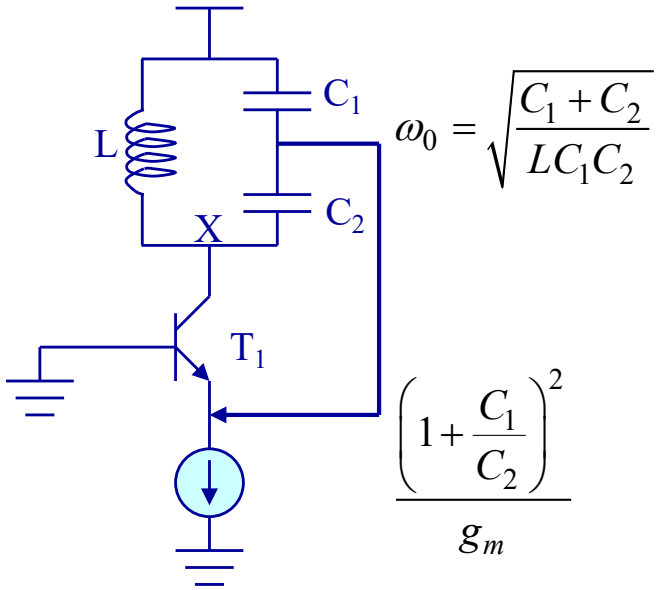


Frequency selective network or resonator

The system oscillations frequency is determined by the characteristics of the selective circuit.



Direct return from collector to emitter



Colpitts oscillator

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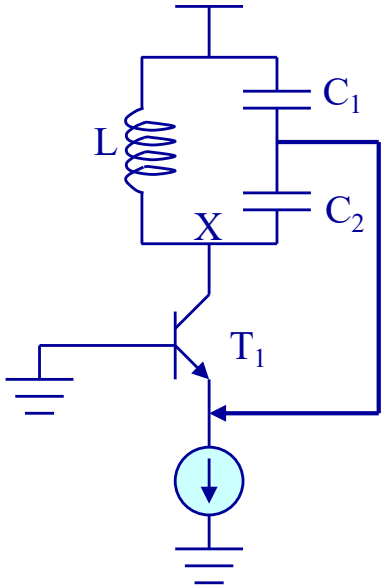
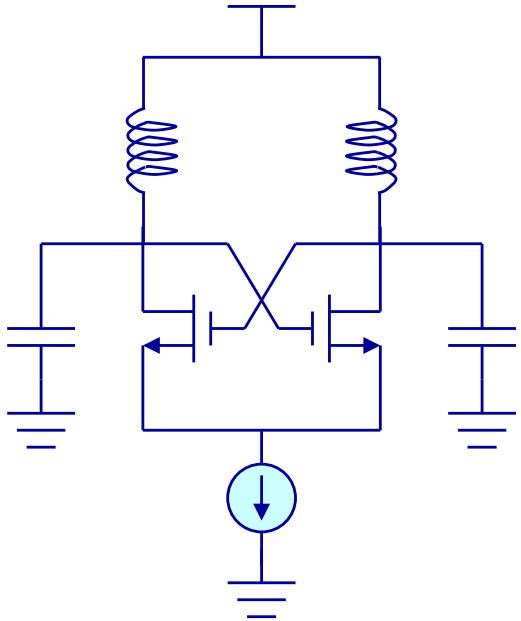
RF oscillators – LC Architecture



Colpitts oscillator



CMOS differential architecture

Pros : High quality factor
One single inductor

Cons : Large ratio C_1/C_2
One terminal output

Pros : High quality factor
Differential output

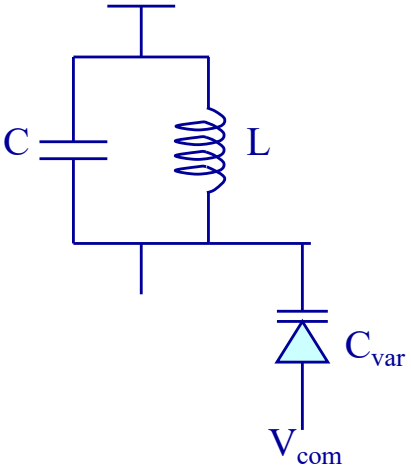
Cons : Matching of the two LC cells

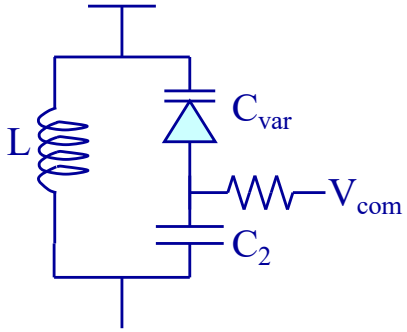
Voltage Controlled RF oscillators (VCO)

- Need to obtain an adjustable frequency RF oscillation for channel selection :

$$f_{LO} = f_0 + k\, f_{ch}$$

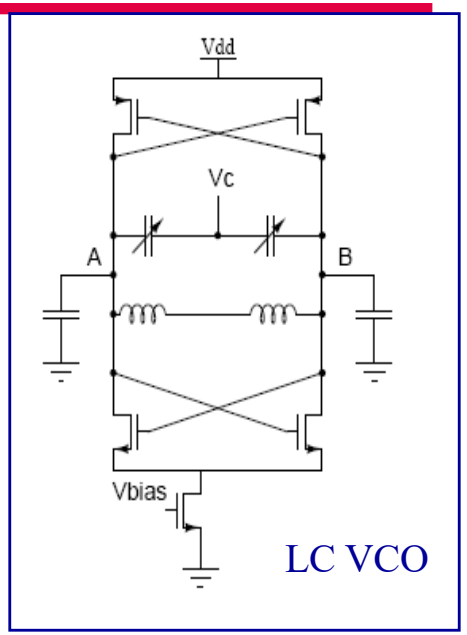
- Frequency value controlled by a voltage





$$C_{\text{var}}(V_{com}) = \frac{C_0}{\left(1 - \frac{V_{com}}{V_{diff}}\right)^{\frac{1}{2}}}$$

Use of a varicap diode in the LC cell



Voltage Controlled RF oscillators (VCO)

- VCO mathematical model

$$\omega_{LO} = \omega_{FR} + K_{VCO} V_{com} = \frac{d\Phi}{dt}$$

$$X(t) = V_{LO} \cos(\Phi) = V_{LO} \cos\left(\omega_{FR} t + K_{VCO} \int V_{com} dt\right)$$

- If the control voltage is constant, the frequency is shifted by $K_{VCO}V_{com}$

$$V_{com} = V_0$$

$$X(t) = V_{LO} \cos\left((\omega_{FR} + K_{VCO} V_0) t + \phi_0\right)$$

- The VCO is a frequency modulator

$$V_{com} = V_m \cos(\omega_m t)$$

$$X(t) = V_{LO} \cos\left(\omega_{FR} t + \frac{K_{VCO}}{\omega_m} V_m \sin(\omega_m t)\right)$$

⇒ Rejection of the control voltage HF components

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RF oscillators – Phase noise

- Origin : internal noise of components constituting the oscillator
  example : amplifier thermal noise (use of a single transistor to minimize)

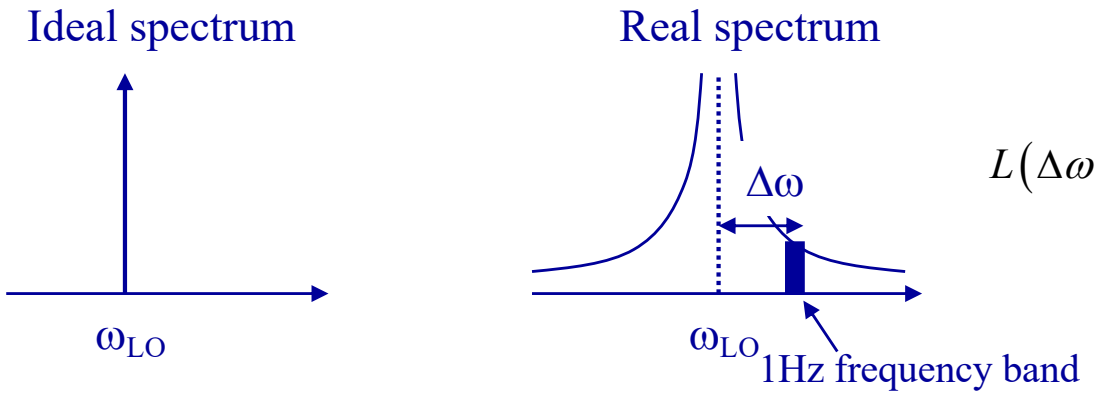
- Main effect : Random deviation of output wave frequency

$$X(t) = V_{LO}\cos\left(\omega_{LO}t + \Phi_n(t)\right)$$

$\Phi_n(t)$: phase noise

$$si \quad \left|\Phi_n(t)\right| << 1 \quad , \quad X(t) \approx V_{LO}\left\{\cos\left(\omega_{LO}t\right) - \Phi_n(t)\sin\left(\omega_{LO}t\right)\right\}$$

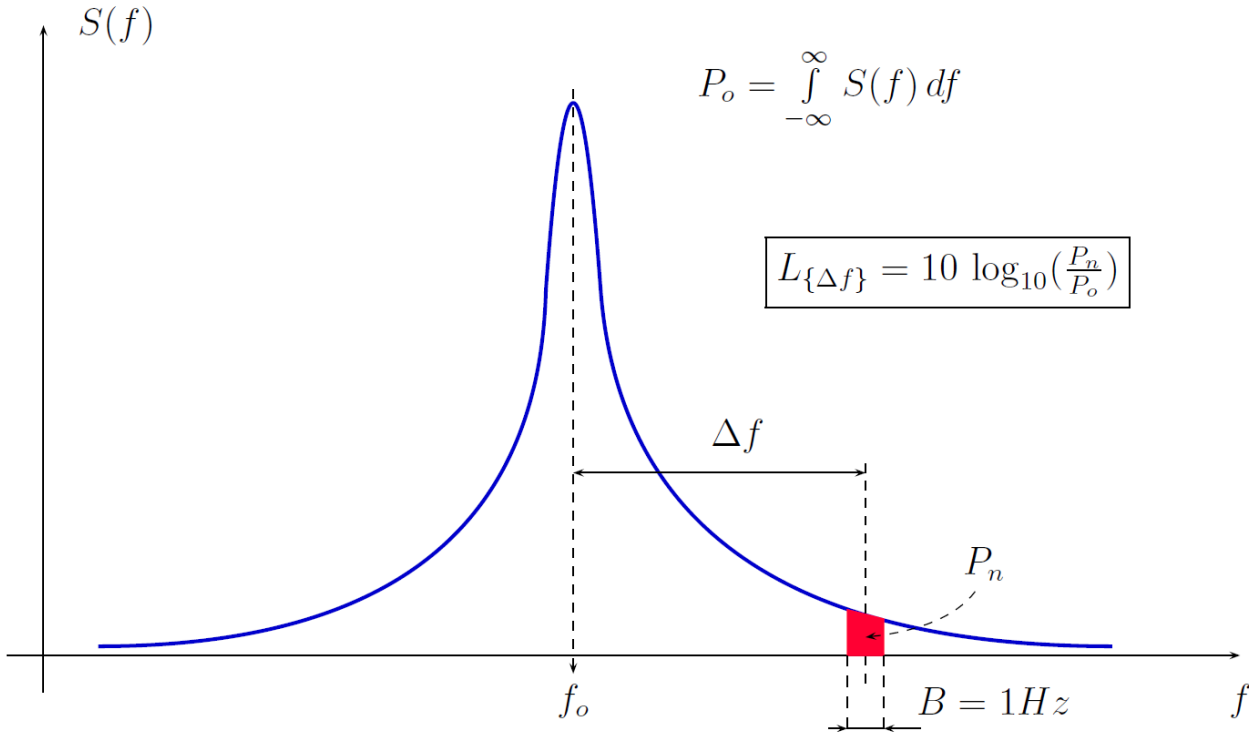
- Frequency domain characterization for RF applications :



$$L(\Delta\omega) = 10\log\left(\frac{P_n}{P_{LO}}\right) \quad [dBc/Hz]$$

Spectral characterization

- Thus, because of the different noise sources (thermal, 1/f…) the Power Spectral Density (PSD) spreads around f_0

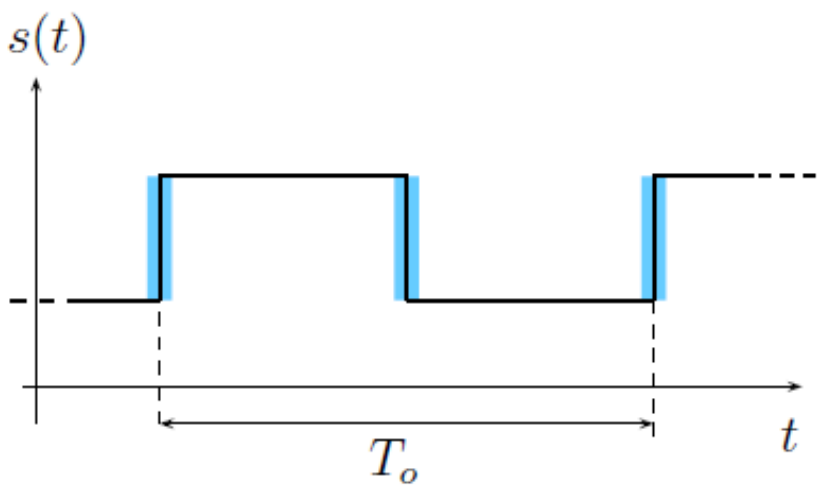


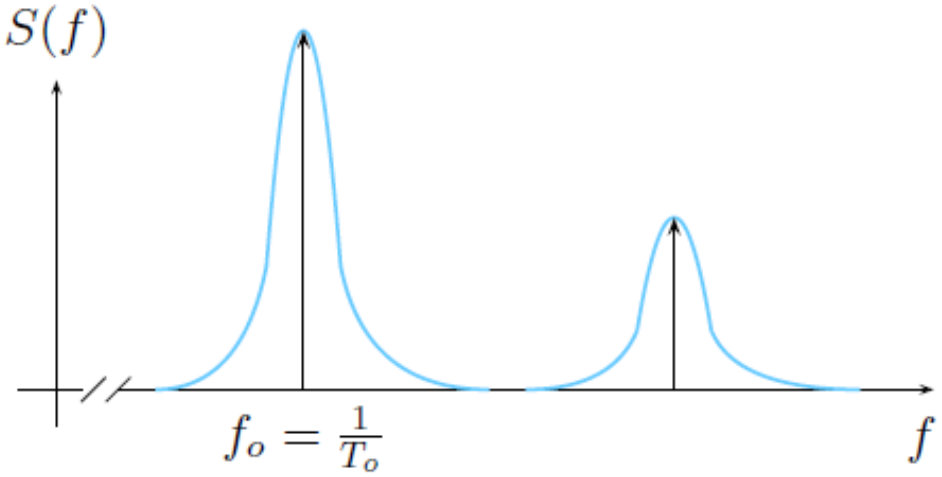
Example (DECT standard) : -97dBc/Hz @ 1,8 MHz

Phase noise and Jitter

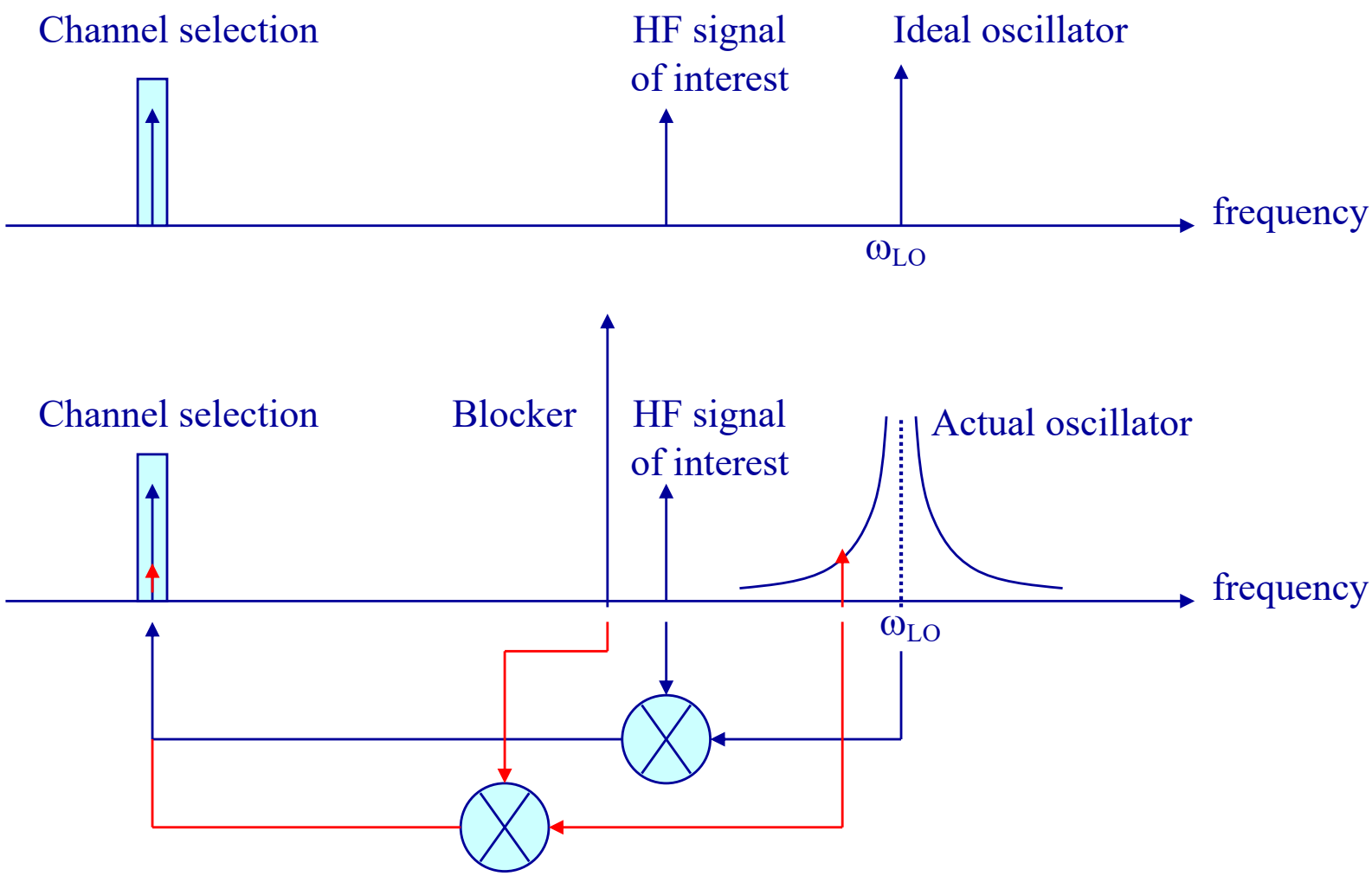
- Phase noise and jitter are two manifestations of an unique phenomena : random fluctuations of the oscillator period.

- Phase noise is associated to spectral representation whereas jitter is associated to time representation of these fluctuations





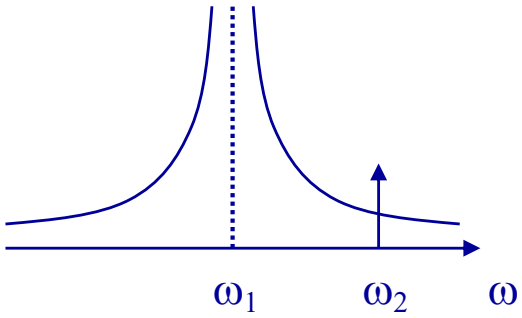
Phase noise – Reciprocal mixing



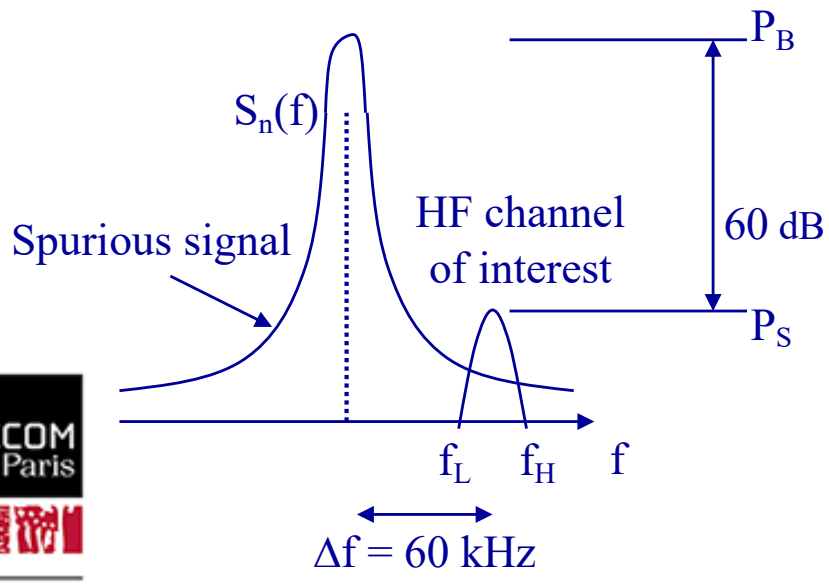
Addition of noise during down-conversion to reception

Phase noise – Specification example

Real spectrum of the transmitter



Adding noise during up-conversion to transmission



Calculation of a phase noise specification for the RF oscillator :

Bandwidth of interest : $f_H - f_L = 30$ kHz

Assumption : $S_n(\Delta f)$ is constant in this band

$$S_n(\Delta f) = S_0 \quad [dBc/Hz]$$

What is the maximum value of S_0 that guarantees an SNR in the channel of interest greater than 15 dB?

?

Summary

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- PLLs
- Indirect frequency synthesis

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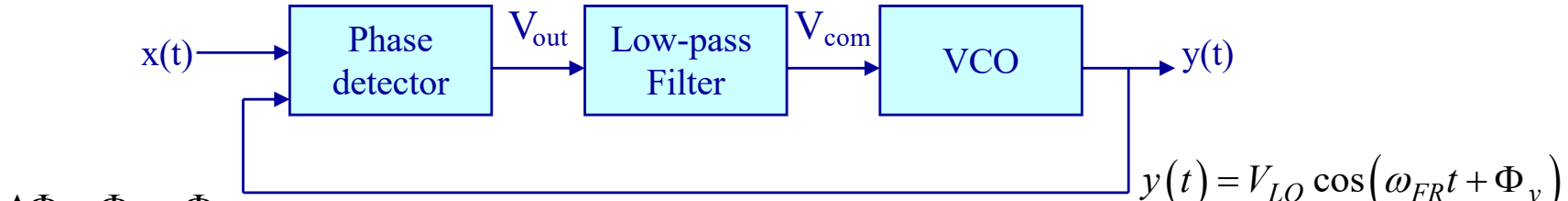
PLL – Presentation



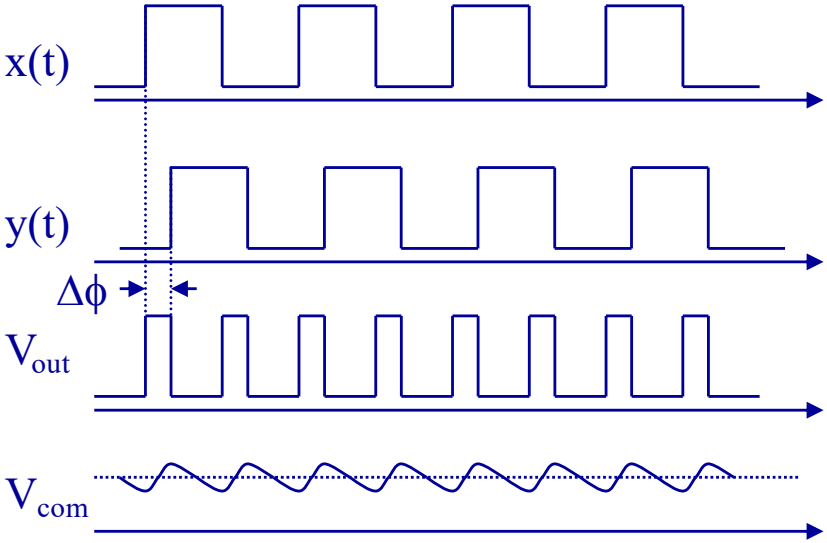
$$\Delta\Phi = \Phi_x - \Phi_y$$

$$V_{com} = K_{DP}\Delta\Phi$$

$$y(t) = V_{LO}\cos\left(\omega_{FR}t + \Phi_y\right)$$

$$\Phi_y = K_{VCO}\int V_{com}dt$$

Basic Phase Locked Loop



PLL waveforms

The loop is locked when $\Delta\Phi$ is constant, which corresponds to the equality of the input and output frequencies.

$$\omega_y = \omega_{FR} + K_{VCO}V_{com} = \omega_x$$

$$\Delta\Phi = \frac{V_{com}}{K_{DP}} = \frac{\omega_x - \omega_{FR}}{K_{DP}\cdot K_{VCO}}$$

The frequency are exactly equal !

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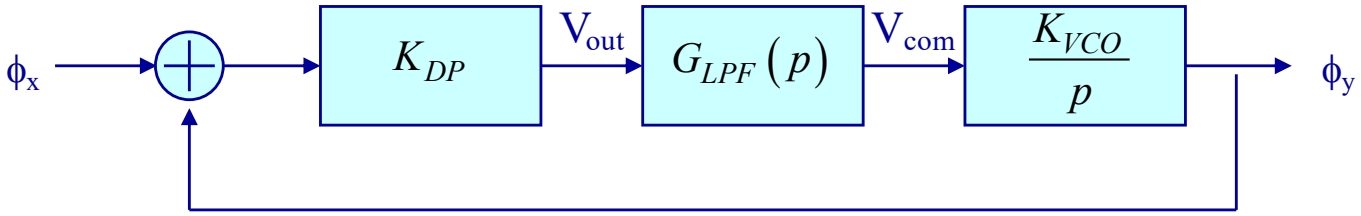
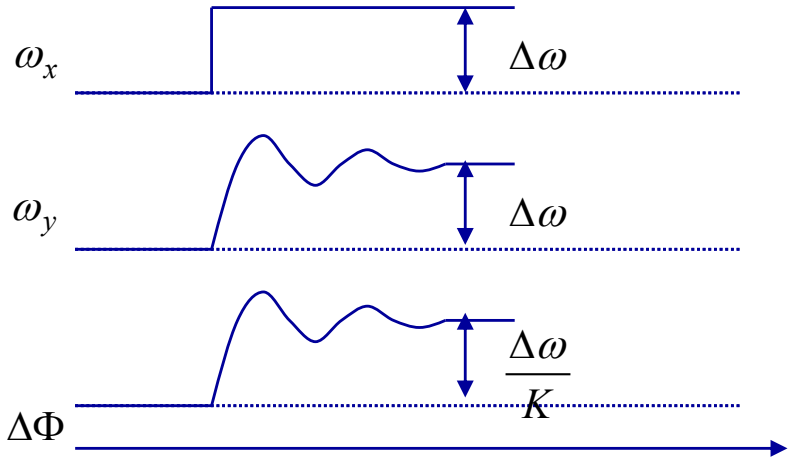
PLL – Dynamic behavior



Closed loop transfer function: $H(p) = \frac{\Phi_y(p)}{\Phi_x(p)} = \frac{K\, G_{LPF}(p)}{p + K\, G_{LPF}(p)}$ *avec* $K = K_{DP} K_{VCO}$

with first order low-pass filter: $G_{LPF}(p) = \frac{1}{1 + \frac{p}{\omega_{LPF}}}$, we obtain a classical second order system:



$$H(p) = \frac{\omega_n^2}{p^2 + 2\zeta\omega_n p + \omega_n^2}$$

avec $\omega_n = \sqrt{\omega_{LPF} K}$

et $\zeta = \frac{1}{2}\sqrt{\frac{\omega_{LPF}}{K}}$

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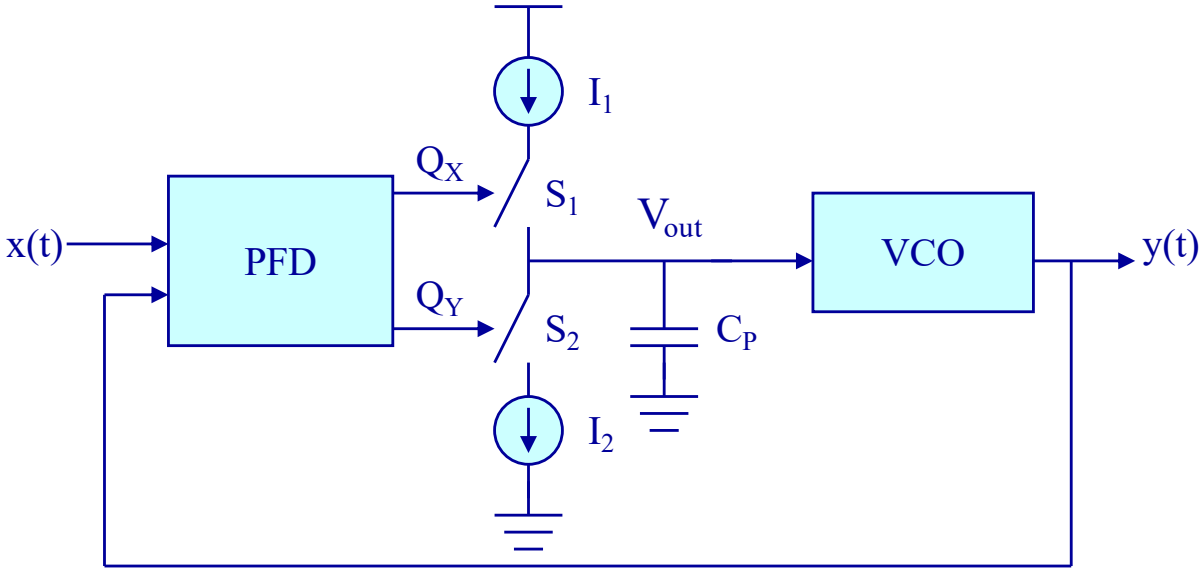
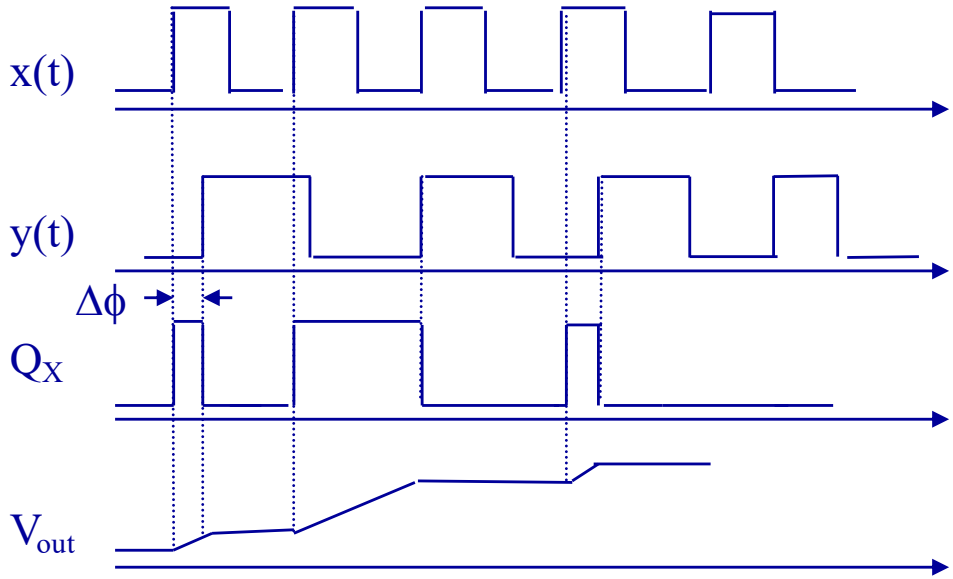
Charge Pump PLL



Architecture with 3-state phase/frequency detector and charge pump circuit

$$I_1 = I_2 = I$$



Waveforms in CPPLL with $\omega_x > \omega_y$ in closed loop :

$$V_{out} \quad cons\tan t$$
$$\omega_y = \omega_{FR} + K_{VCO} V_{out} = \omega_x$$
$$\Delta\Phi = \Phi_x - \Phi_y = 0$$
$$Q_X = Q_Y = 0$$

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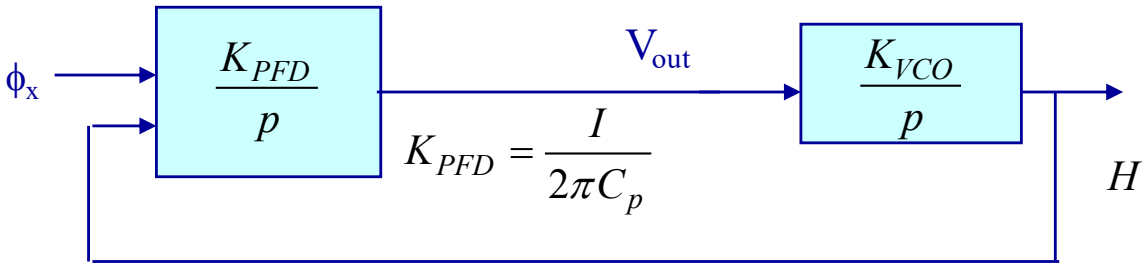
Charge Pump PLL

Assuming that the bandwidth of the loop is much lower than the input frequency:



$$H(p) = \frac{\Phi_y(p)}{\Phi_x(p)} = \frac{K}{p^2 + K} \quad avec \quad K = K_{PFD} K_{VCO}$$

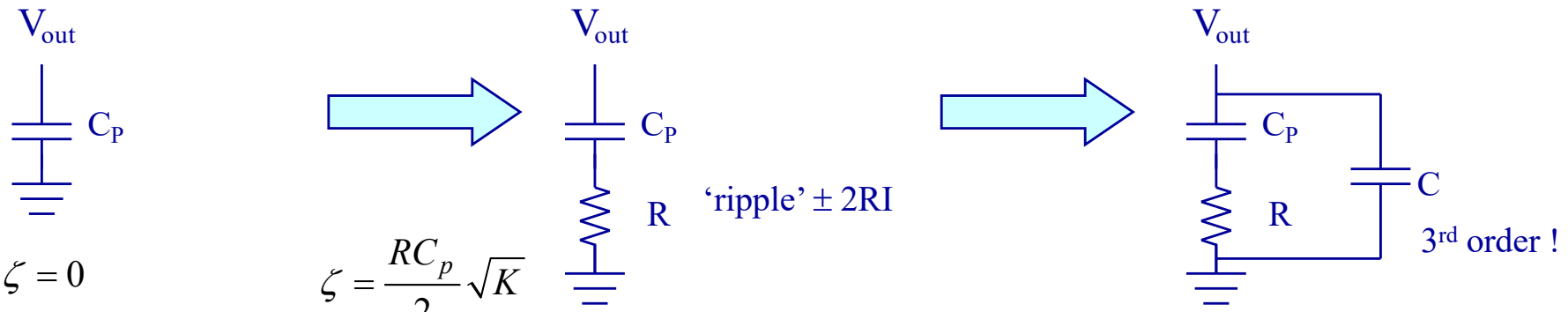
Main difference : two poles at zero in open loop

Pros :

- Maximum extension of the capture range,
- Increase of the locking speed,
- Zero static phase error (if ideal circuits).

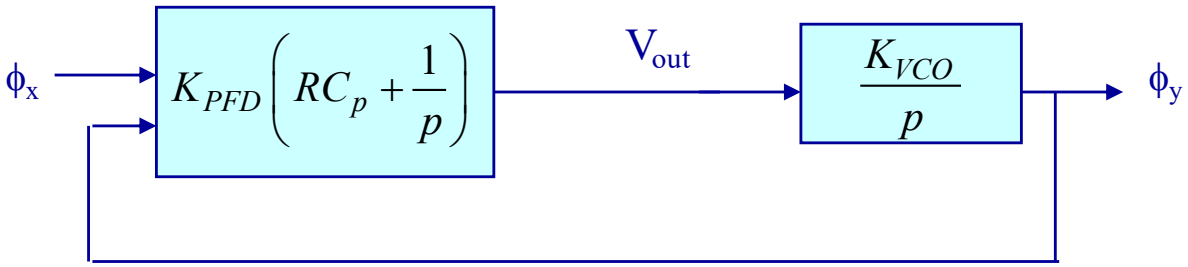
Cons :

- Instability issue



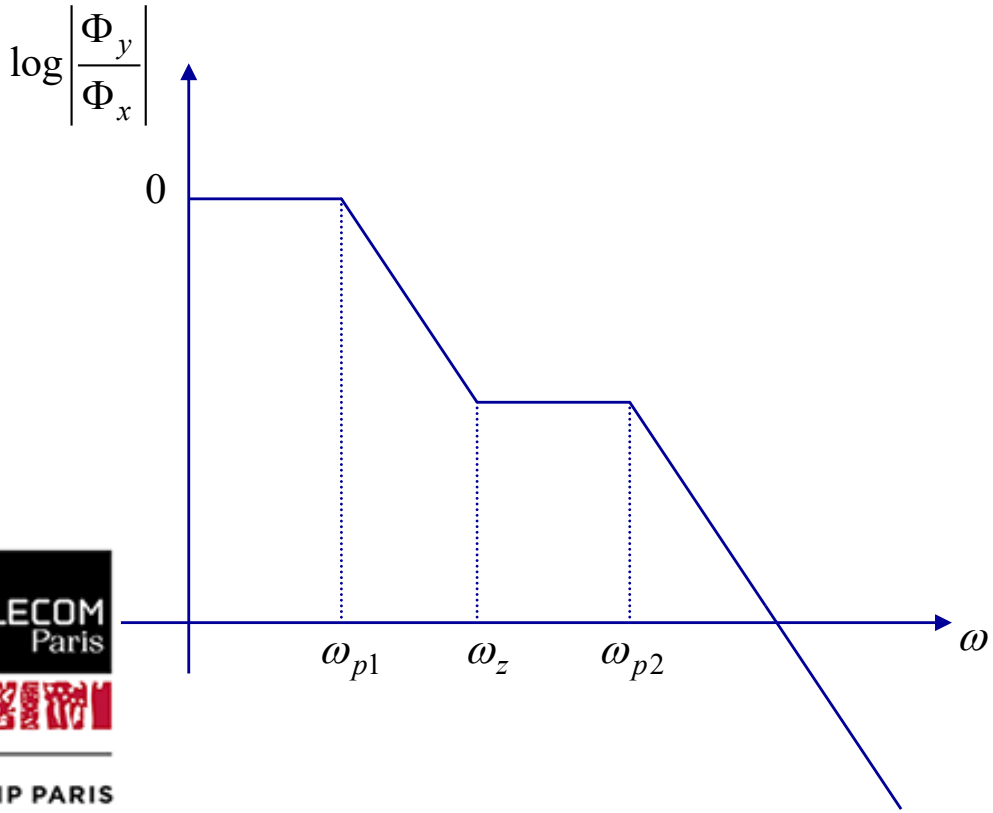
CPPLL – Input phase noise filtering

Transfer function of a second-order CPPLL with a stabilization zero :



$$H(p)=\frac{\Phi_y(p)}{\Phi_x(p)}=\frac{\omega_n^2\left(1+p/\omega_z\right)}{p^2+2\zeta\omega_n p+\omega_n^2}$$

$$avec\ \begin{cases}\omega_n^2=K=K_{PFD}K_{VCO}\\ \omega_z=1/RC_p\end{cases}$$



$$\Phi_x=\phi_0+\Phi_n(t)$$
$$\Phi_y=\phi_0+\Phi_{out}(t)$$

$\Phi_n(t)$: phase noise

- Slow variations of the phase noise are reproduced at the output.
- HF noise is eliminated at the output.

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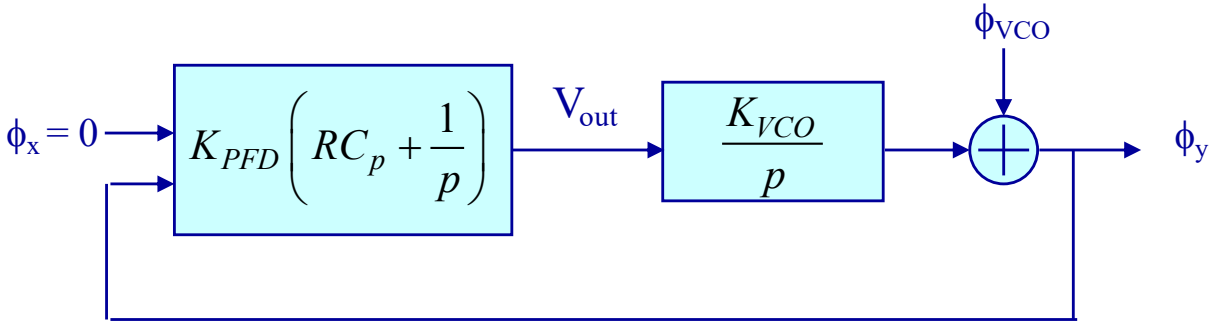
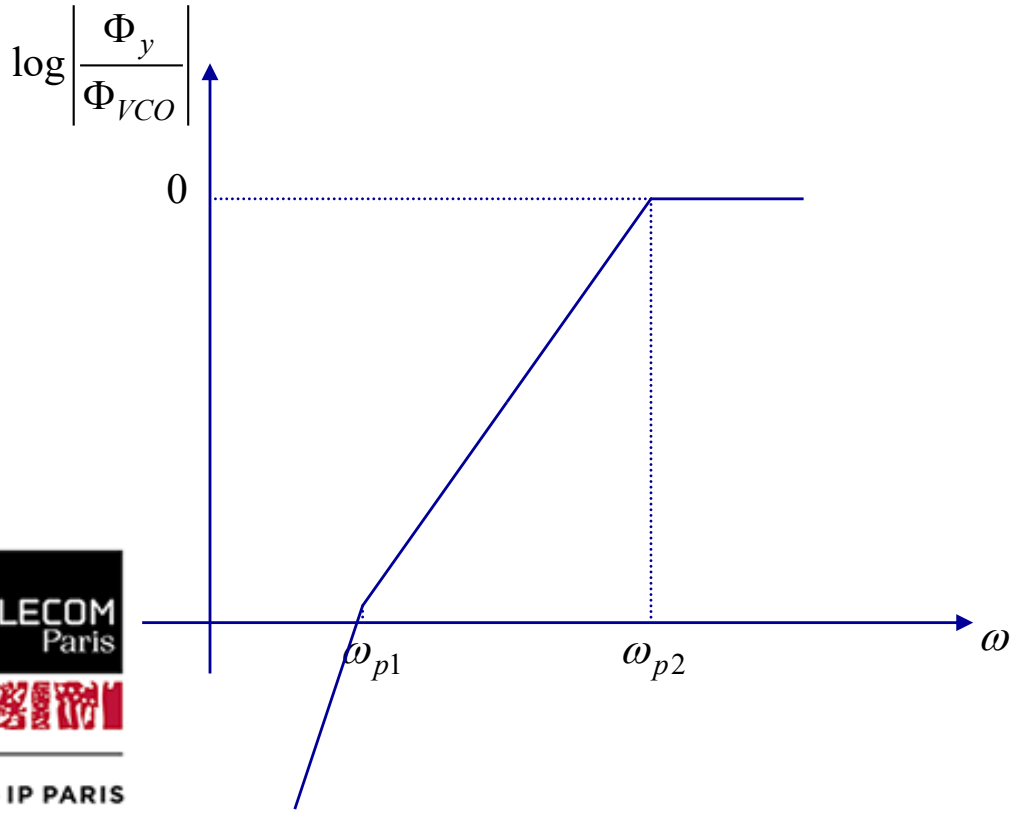
CPPLL – VCO phase noise filtering



$$\frac{\Phi_y(p)}{\Phi_{VCO}(p)} = \frac{p^2}{p^2 + 2\zeta\omega_n p + \omega_n^2}$$



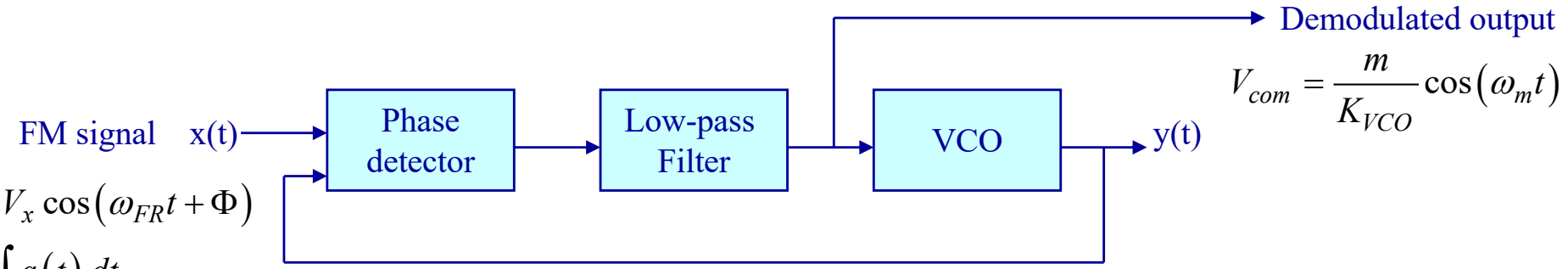
$$\Phi_{VCO} = \Phi_n(t)$$
$$\Phi_y = \Phi_{out}(t)$$

$\Phi_n(t)$: phase noise

- The transfer function is a high-pass filtering
- An increase in the bandwidth of the PLL decreases the phase noise of the VCO

PLL – Applications

RF signal demodulation



$$x(t) = V_x \cos(\omega_{FR} t + \Phi)$$

$$\Phi = m \int a(t)\, dt$$

$$a(t) = \cos(\omega_m t)$$

$$x(t) = V_x \cos\left(\omega_{FR} t + \frac{m}{\omega_m} \sin(\omega_m t)\right)$$

The frequency are exactly equal :

$$\omega_y = \omega_x$$

$$\omega_{FR} + K_{VCO} V_{com} = \omega_{FR} + m \cos(\omega_m t)$$

Important: Loop bandwidth large enough !

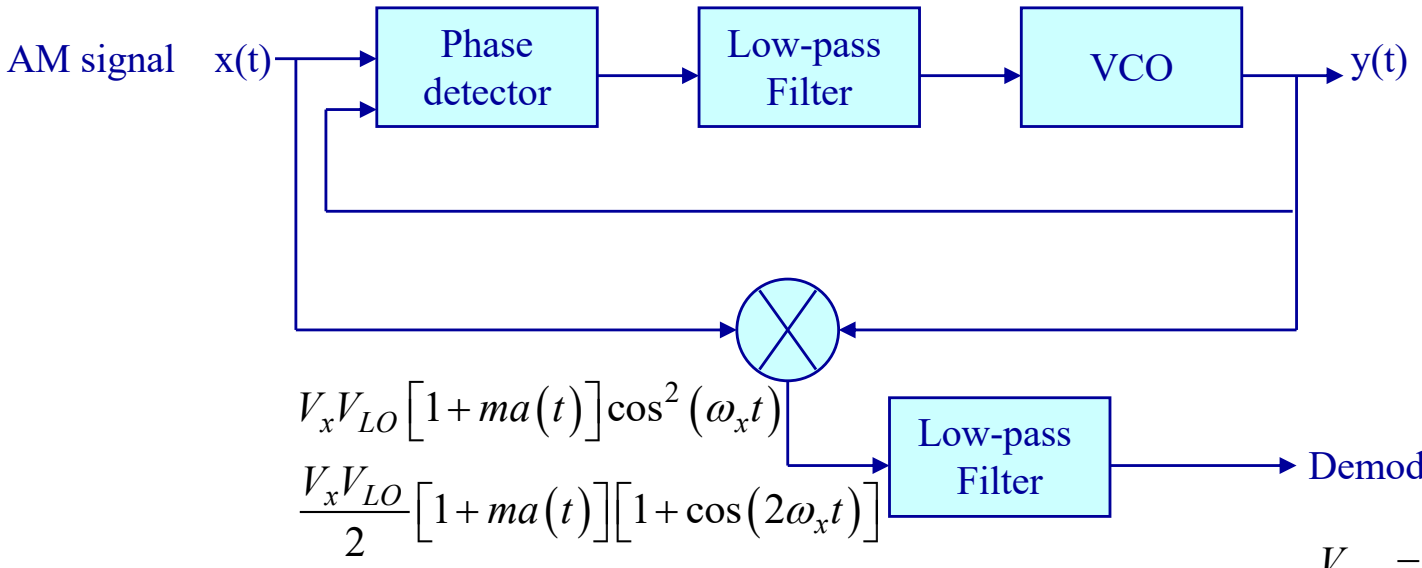
Phase-locked loop for FM demodulator

PLL – Applications

RF signal demodulation

$x(t) = V_x\left[1 + ma(t)\right]\cos(\omega_x t)$

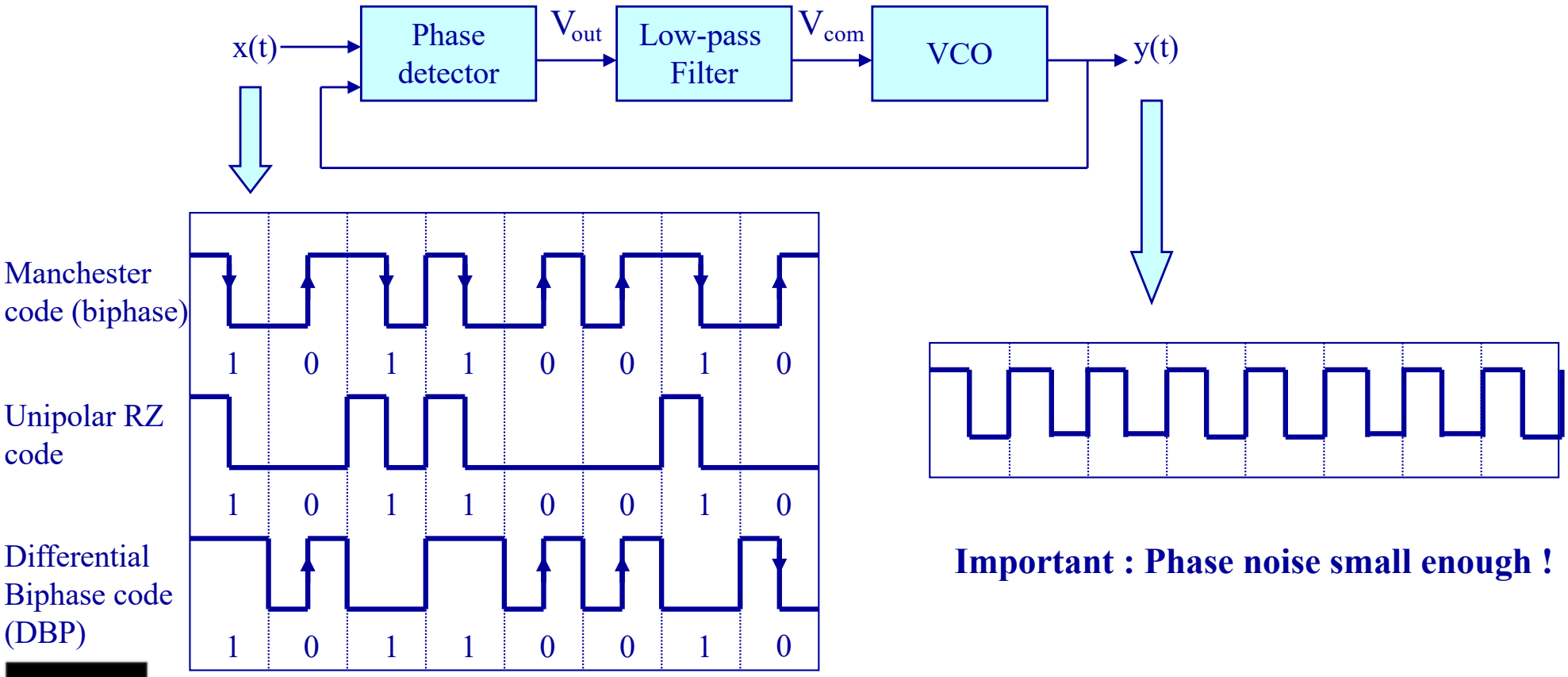
$y(t) = V_{LO}\cos(\omega_x t)$



Phase-locked loop for AM coherent demodulator

PLL – Applications

Clock recovery



Important : Phase noise small enough !

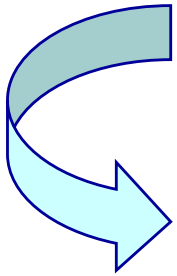
Phase-locked loop for clock recovery from an encoded signal

PLL - Conclusion

Phase locked loops are key elements in digital communications systems. Their design and optimization are complex (trade-off between speed, precision, stability).

Main features are :

- **Locking and Capture Ranges**
- **Agility (locking speed)**
- **Phase noise**
- **Bandwidth**
- **Settling time**



Major application for the RF front end

RF frequency synthesis : RF oscillator, PLL

$$f_{LO} = f_0 + k\, f_{ch}$$ Channel selection

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Summary

- Digital Transceiver RF Font-end
- RF oscillators
- PLLs
- Indirect frequency synthesis

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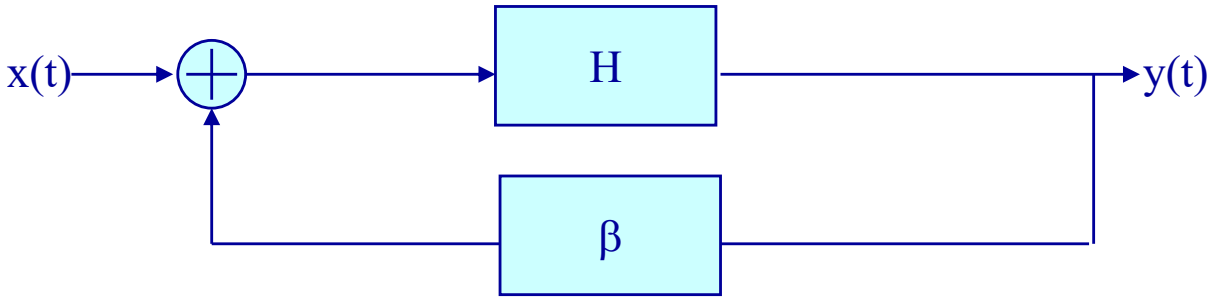
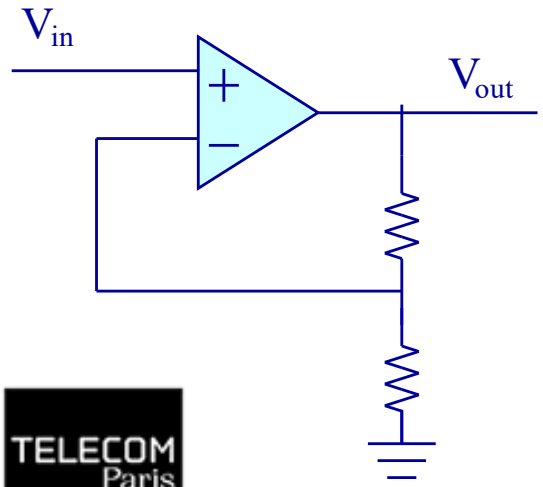
Frequency multiplication

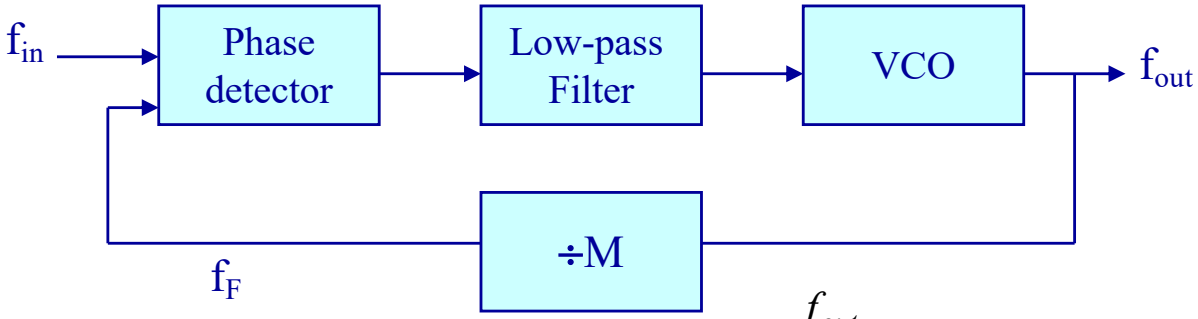


$$\frac{y}{x} = \frac{H}{1+\beta H} = \frac{1}{\beta}$$

Basic loop system



Voltage amplifier



$$\frac{f_{out}}{f_{in}} = M$$

Frequency multiplier

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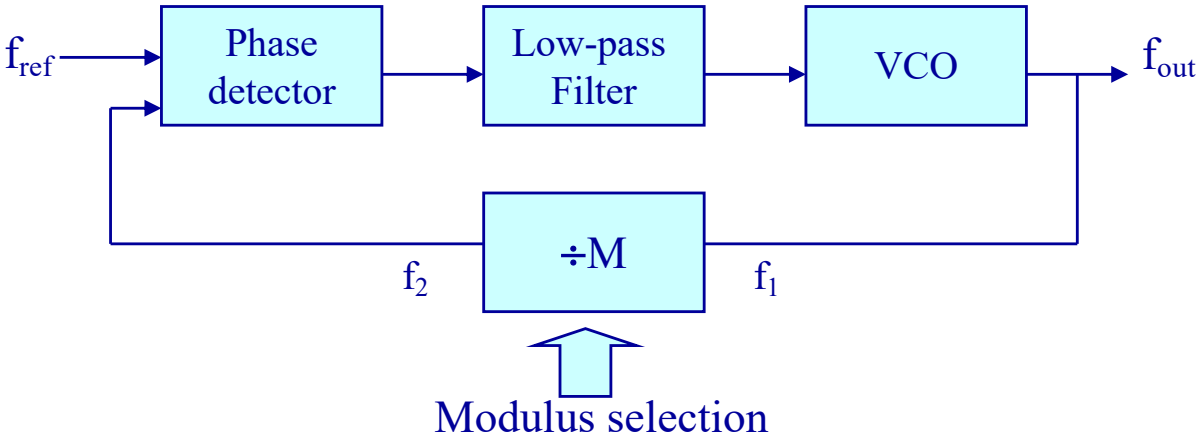
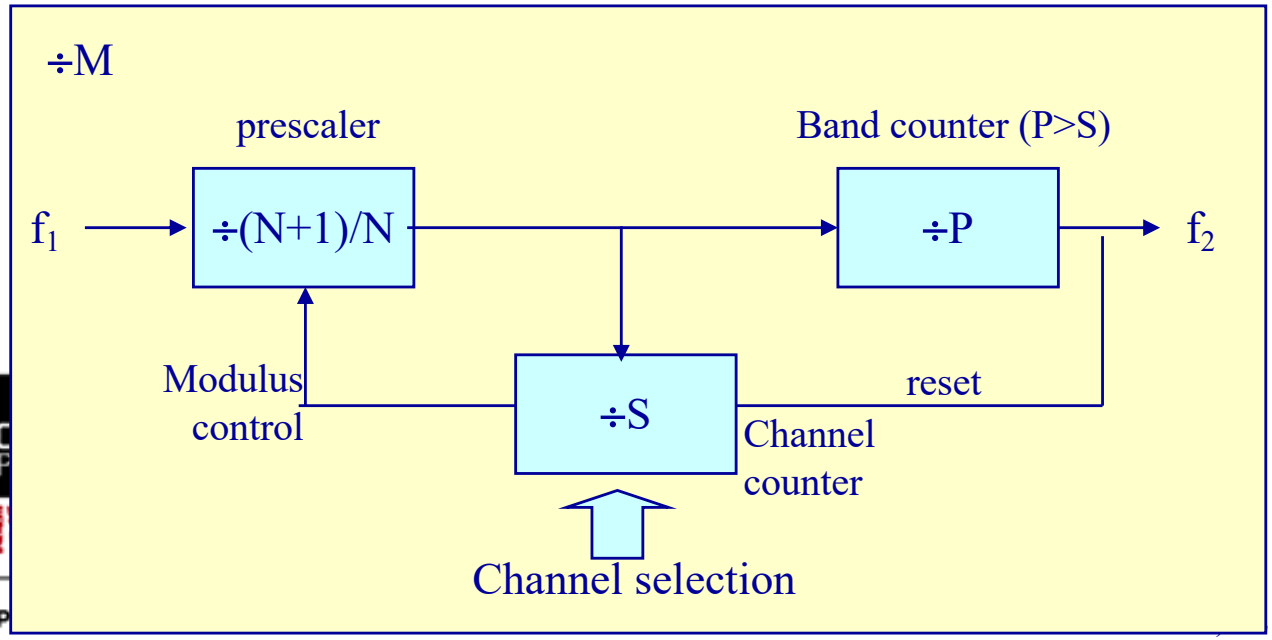
Integer Modulus Synthesizer



$$f_{out} = Mf_{réf} = f_0 + kf_{ch}$$
$$M_L \le M \le M_H$$
$$f_0 = M_L f_{réf}$$
$$f_{ch} = f_{réf}$$

The reference input frequency must be equal to the channel spacing.

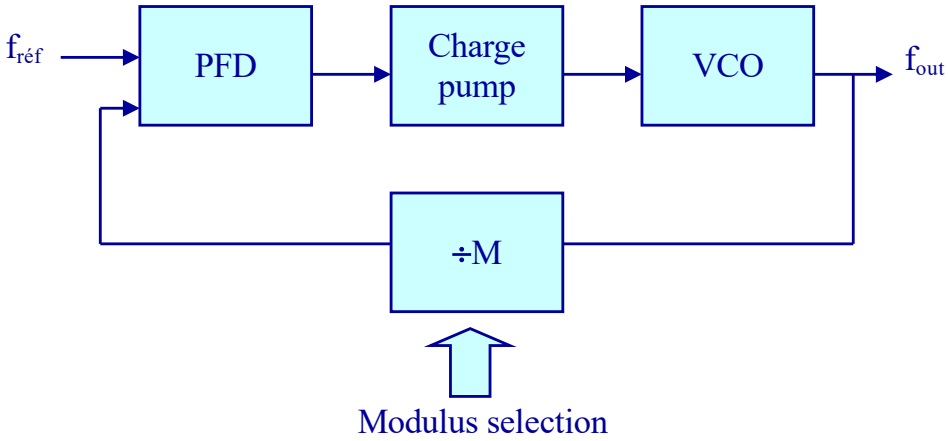


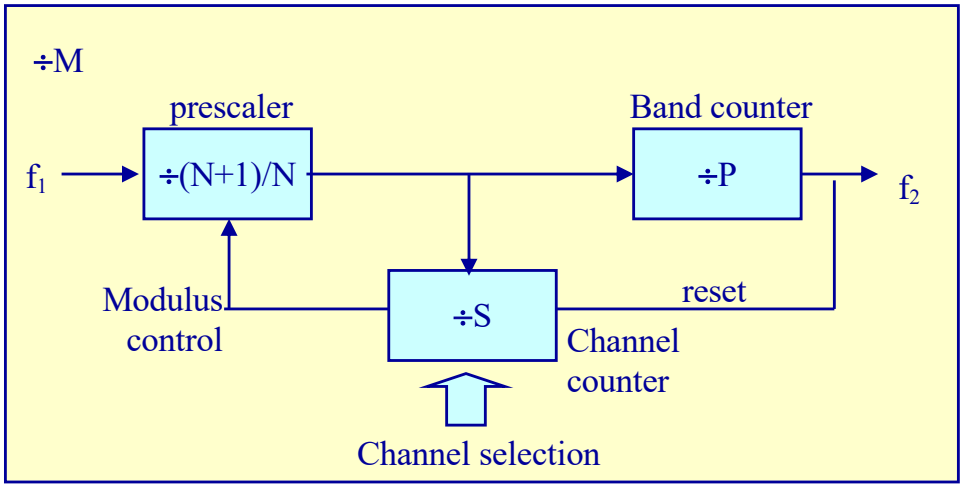
Frequency divider by pulse counting

One output cycle occurs at the end of (N + 1) * S + N * (P-S) input cycles.

$$f_2 = \frac{f_1}{NP + S}$$

Integer Modulus Synthesizer





- *Main advantage*: architecture simplicity

- *Implementation* in RF system :

Band counter, channel counter, PFD, charge pump

VCO
prescaler
} a single die in deeply submicronic CMOS technology

- *Main drawback*:

The reference frequency has a small value.
The bandwidth of PLLs is limited to 1/10 of the input frequency to ensure stability
} The bandwidth of the loop is limited!

ex : GSM inter-channel spacing : 200kHz
Settling time 100 µs or more

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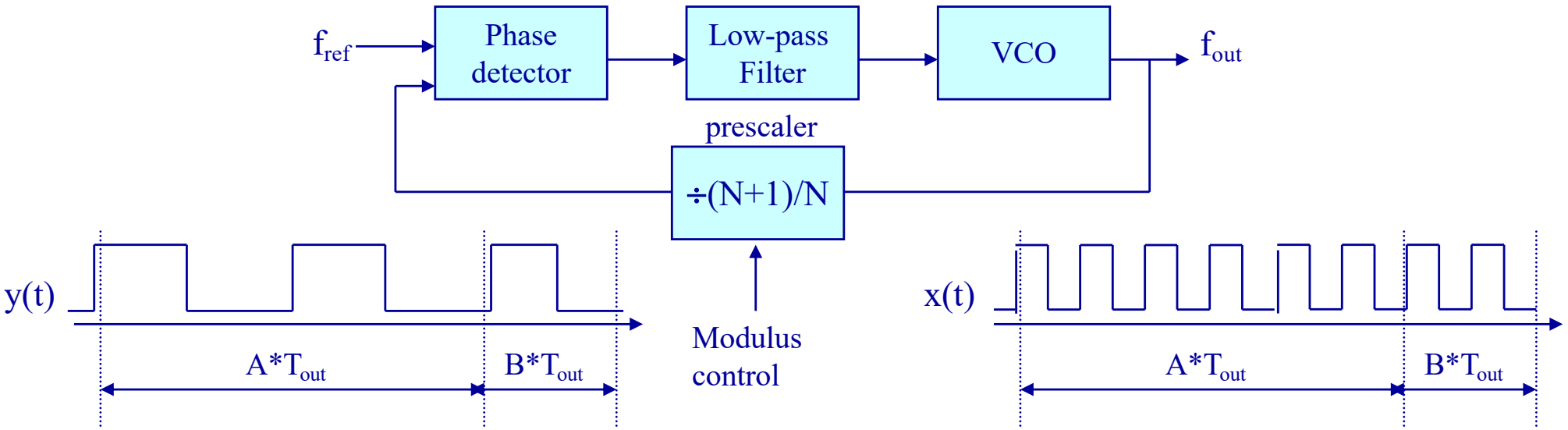
Fractional Modulus Synthesizer



Number of pulses during the time $(A+B)T_{out}$:

$A/(N+1) + B/N$

'Average' or equivalent frequency of y(t) :

$(A/(N+1) + B/N) \ / \ ((A+B)\ T_{out})$

$= f_{out} / M$

Locked loop :

$f_{réf} = f_{out} / M$

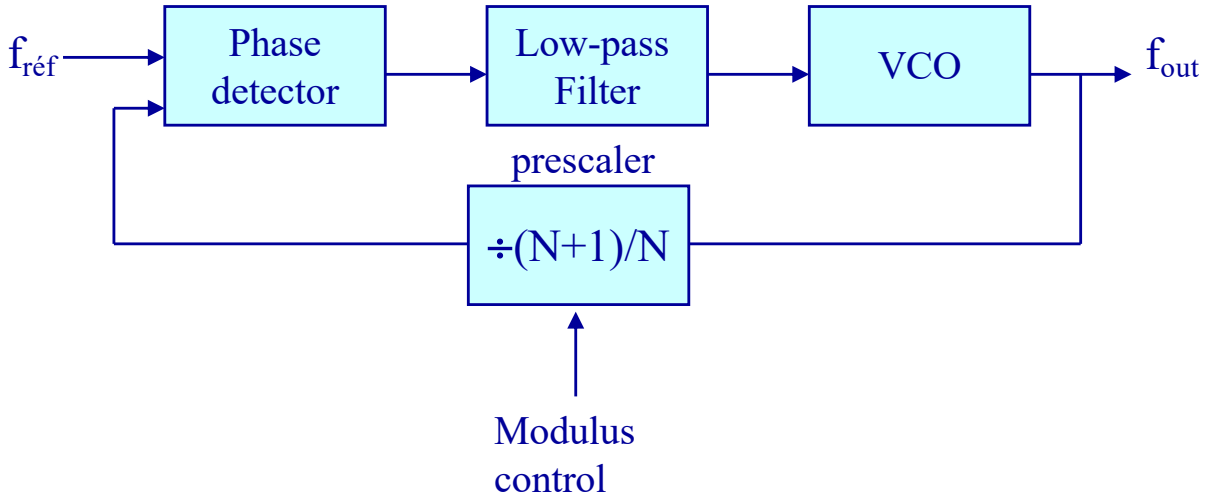
$f_{out} = M * f_{réf}$

$$M = \frac{A+B}{\frac{A}{N+1}+\frac{B}{N}}$$

$$N < M < N+1$$

Use of a two-modulus frequency divider

Fractional Modulus Synthesizer



EXAMPLE :

Let's Consider a synthesizer for which the reference frequency is provided by a 1MHz oscillator. The expected output frequency is:

$$f_{out} = f_0 + kf_{ch}$$

with f_0=10 MHz and f_{ch}=100kHz for k= 0, 1, 2,…9, 10.

What is the value of N?

What are the minimum possible values for A and B to address the different channels?

?