LM4809 Boomer® Audio Power Amplifier Series Dual 105mW Headphone Amplifier with Active-Low Shutdown Mode

Check for Samples: LM4809, LM4809LQBD

FEATURES

- **Active-Low Shutdown Mode**
- **"Click and Pop" Reduction Circuitry**
- **Low Shutdown Current**
- **WSON, MSOP, and SOIC Surface Mount Packaging**
- **No Bootstrap Capacitors Required**
- **Unity-Gain Stable**

APPLICATIONS

- **Headphone Amplifier**
- **Personal Computers**
- **Microphone Preamplifier**
- **PDA's**

KEY SPECIFICATIONS

- **THD+N at 1kHz at 105mW Continuous Average Power into 16Ω 0.1% (typ)**
- **THD+N at 1kHz at 70mW Continuous Average Power into 32Ω 0.1% (typ)**
- **Shutdown Current 0.4µA (typ)**

DESCRIPTION

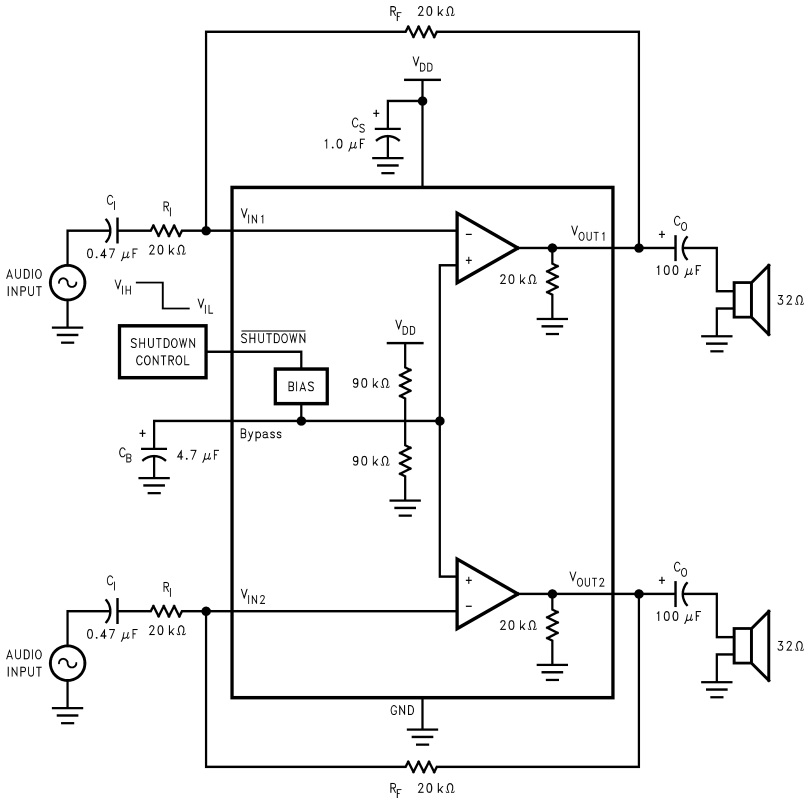
The LM4809 is a dual audio power amplifier capable of delivering 105mW per channel of continuous average power into a 16Ω load with 0.1% (THD+N) from a 5V power supply.

Boomer audio power amplifiers were designed specifically to provide high quality output power with a minimal amount of external components. Since the LM4809 does not require bootstrap capacitors or snubber networks, it is optimally suited for low-power portable systems.

The unity-gain stable LM4809 can be configured by external gain-setting resistors.

The LM4809 features an externally controlled, active-low, micropower consumption shutdown mode, as well as an internal thermal shutdown protection mechanism.

Typical Application



*Refer to Application Information for information concerning proper selection of the input and output coupling capacitors.

Figure 1. Typical Audio Amplifier Application Circuit

Connection Diagrams

Top View

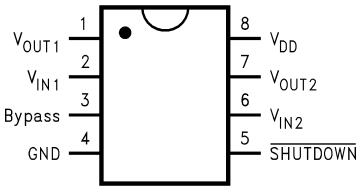


Figure 2. VSSOP Package
See Package Number DGK0008A

Top View

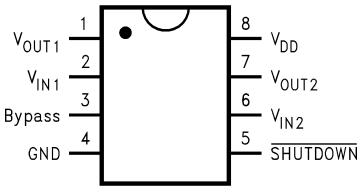


Figure 3. SOIC Package
See Package Number D0008A

Top View

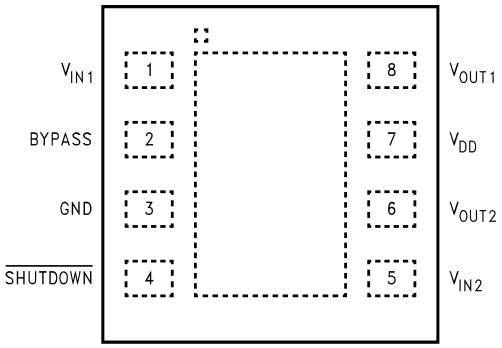


Figure 4. WSON Package
See Package Number NGL0008B

Top View

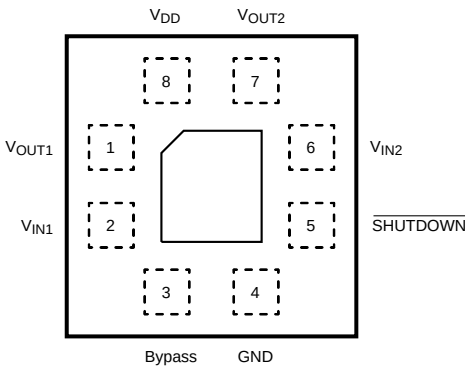


Figure 5. WSON Package
See Package Number NGP0008A

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Absolute Maximum Ratings (1)(2)

Supply Voltage			6.0V
Storage Temperature			−65°C to +150°C
ESD Susceptibility (3)			3.5kV
ESD Machine model (4)			250V
Junction Temperature (T_J)			150°C
Soldering Information	SOIC Package	Vapor Phase (60 sec.)	215°C
		Infrared (15 sec.)	220°C
Thermal Resistance		θ_{JA} (SOIC)	170°C/W
		θ_{JC} (SOIC)	35°C/W
		θ_{JA} (MSOP)	210°C/W
		θ_{JC} (MSOP)	56°C/W
		θ_{JA} (WSON)	117°C/W (5)
		θ_{JA} (WSON)	150°C/W (6)
		θ_{JC} (WSON)	15°C/W

(1) *Absolute Maximum Ratings* indicate limits beyond which damage to the device may occur.
(2) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/ Distributors for availability and specifications.
(3) Human body model, 100pF discharged through a 1.5kΩ resistor.
(4) Machine Model ESD test is covered by specification EIAJ IC-121-1981. A 200pF cap is charged to the specified voltage, then discharged directly into the IC with no external series resistor (resistance of discharge path must be under 50Ohms).
(5) The given θ_{JA} is for an LM4809 packaged in an NGL0008B wit the Exposed-Dap soldered to a printed circuit board copper pad with an area equivalent to that of the Exposed-Dap itself.
(6) The given θ_{JA} is for an LM4809 packaged in an NGL0008B with the Exposed-Dap not soldered to any printed circuit board copper.

Operating Ratings

Temperature Range	$T_{MIN} \le T_A \le T_{MAX}$	$-40°C \le T_A \le 85°C$
Supply Voltage (V_{CC})		$2.0V \le V_{CC} \le 5.5V$

Electrical Characteristics V_{DD} = 5V (1)(2)

The following specifications apply for V_{DD} = 5V unless otherwise specified, limits apply to T_A = 25°C.

Parameter		Test Conditions	LM4809		Units (Limits)
			Typ (3)	Limit (4)	
V_{DD}	Supply Voltage			2.0 5.5	V (min) V (max)
I_{DD}	Supply Current	V_{IN} = 0V, I_O = 0A	1.4	3	mA (max)
I_{SD}	Shutdown Current	V_{IN} = 0V, $V_{SHUTDOWN}$ = GND	0.4	2	µA(max)
V_{OS}	Output Offset Voltage	V_{IN} = 0V	4.0	50	mV(max)
P_O	Output Power	THD+N = 0.1%, f = 1kHz			
		R_L = 16Ω	105		mW
		R_L = 32Ω	70	65	mW (min)
THD+N	Total Harmonic Distortion	P_O = 50mW, R_L = 32Ω f = 20Hz to 20kHz	0.3		%
Crosstalk	Channel Separation	R_L = 32Ω; P_O = 70mW	70		dB
PSRR	Power Supply Rejection Ratio	C_B = 1.0µF; V_{RIPPLE} = 200mV_{PP}, f = 1kHz; Input terminated into 50Ω	70		dB

(1) *Absolute Maximum Ratings* indicate limits beyond which damage to the device may occur.
(2) All voltages are measured with respect to the ground pin, unless otherwise specified.
(3) Typical specifications are specified at +25OC and represent the most likely parametric norm.
(4) Datasheet min/max specification limits are ensured by design, test, or statistical analysis.

Electrical Characteristics V_{DD} = 5V (1)(2) (continued)

The following specifications apply for V_{DD} = 5V unless otherwise specified, limits apply to T_A = 25°C.

Parameter		Test Conditions	LM4809		Units (Limits)
			Typ (3)	Limit (4)	
V_{SDIH}	Shutdown Voltage Input High			0.8 x V_{DD}	V (min)
V_{SDIL}	Shutdown Voltage Input Low			0.2 x V_{DD}	V (max)

Electrical Characteristics V_{DD} = 3.3V (1)(2)

The following specifications apply for V_{DD} = 3.3V unless otherwise specified, limits apply to T_A = 25°C.

Parameter		Test Conditions	LM4809		Units (Limits)
			Typ (3)	Limit (4)	
I_{DD}	Supply Current	V_{IN} = 0V, I_O = 0A	1.1		mA
I_{SD}	Shutdown Current	V_{IN} = 0V, $V_{SHUTDOWN}$ = GND	0.4		µA
V_{OS}	Output Offset Voltage	V_{IN} = 0V	4.0		mV
P_O	Output Power	THD+N = 0.1%, f = 1kHz			
		R_L = 16Ω	40		mW
		R_L = 32Ω	28		mW
THD+N	Total Harmonic Distortion	P_O = 25mW, R_L = 32Ω f = 20Hz to 20kHz	0.4		%
Crosstalk	Channel Separation	R_L = 32Ω; P_O = 25mW	70		dB
PSRR	Power Supply Rejection Ratio	C_B = 1.0µF; V_{RIPPLE} = 200mV_{PP}, f = 1kHz; Input terminated into 50Ω	70		dB
V_{SDIH}	Shutdown Voltage Input High			0.8 x V_{DD}	V (min)
V_{SDIL}	Shutdown Voltage Input Low			0.2 x V_{DD}	V (max)

(1) *Absolute Maximum Ratings* indicate limits beyond which damage to the device may occur.
(2) All voltages are measured with respect to the ground pin, unless otherwise specified.
(3) Typical specifications are specified at +25OC and represent the most likely parametric norm.
(4) Datasheet min/max specification limits are ensured by design, test, or statistical analysis.

Electrical Characteristics V_{DD} = 2.6V (1)(2)

The following specifications apply for V_{DD} = 2.6V unless otherwise specified, limits apply to T_A = 25°C.

Parameter		Test Conditions	LM4809		Units (Limits)
			Typ (3)	Limit (4)	
I_{DD}	Supply Current	V_{IN} = 0V, I_O = 0A	0.9		mA
I_{SD}	Shutdown Current	V_{IN} = 0V, $V_{SHUTDOWN}$ = GND	0.2		µA
V_{OS}	Output Offset Voltage	V_{IN} = 0V	4.0		mV
P_O	Output Power	THD+N = 0.1%, f = 1kHz			
		R_L = 16Ω	20		mW
		R_L = 32Ω	16		mW
THD+N	Total Harmonic Distortion	P_O = 15mW, R_L = 32Ω f = 20Hz to 20kHz	0.6		%
Crosstalk	Channel Separation	R_L = 32Ω; P_O = 15mW	70		dB
PSRR	Power Supply Rejection Ratio	C_B = 1.0µF; V_{RIPPLE} = 200mV_{PP}, f = 1kHz; Input terminated into 50Ω	70		dB
V_{SDIH}	Shutdown Voltage Input High			0.8 x V_{DD}	V (min)
V_{SDIL}	Shutdown Voltage Input Low			0.2 x V_{DD}	V (max)

(1) *Absolute Maximum Ratings* indicate limits beyond which damage to the device may occur.
(2) All voltages are measured with respect to the ground pin, unless otherwise specified.
(3) Typical specifications are specified at +25OC and represent the most likely parametric norm.
(4) Datasheet min/max specification limits are ensured by design, test, or statistical analysis.

External Components Description

Components	Functional Description (See Figure 1)
1. R_i	The inverting input resistance, along with R_f, set the closed-loop gain. R_i, along with C_i, form a high pass filter with $f_c = 1/(2\pi R_i C_i)$.
2. C_i	The input coupling capacitor blocks DC voltage at the amplifier's input terminals. C_i, along with R_i, create a highpass filter with $f_C = 1/(2\pi R_i C_i)$. Refer to the section, **Selecting Proper External Components**, for an explanation of determining the value of C_i.
3. R_f	The feedback resistance, along with R_i, set closed-loop gain.
4. C_S	This is the supply bypass capacitor. It provides power supply filtering. Refer to the **Application Information** section for proper placement and selection of the supply bypass capacitor.
5. C_B	This is the BYPASS pin capacitor. It provides half-supply filtering. Refer to the section, **Selecting Proper External Components**, for information concerning proper placement and selection of C_B.
6. C_O	This is the output coupling capacitor. It blocks the DC voltage at the amplifier's output and forms a high pass filter with R_L at $f_O = 1/(2\pi R_L C_O)$

Typical Performance Characteristics

THD+N vs Frequency

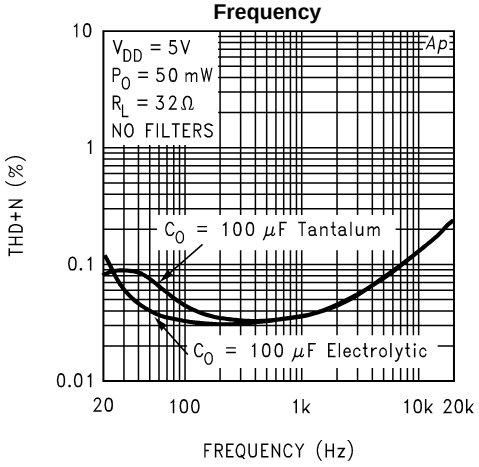


Figure 6.

THD+N vs Frequency

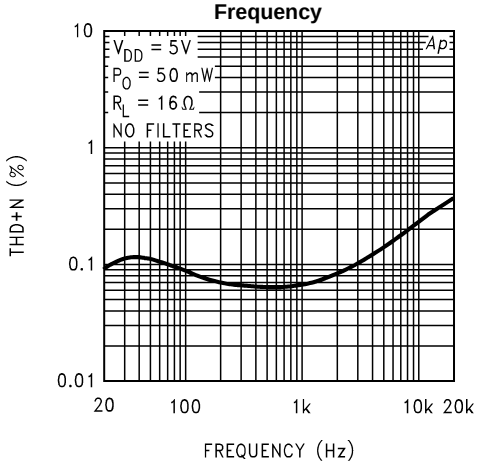


Figure 7.

THD+N vs Frequency

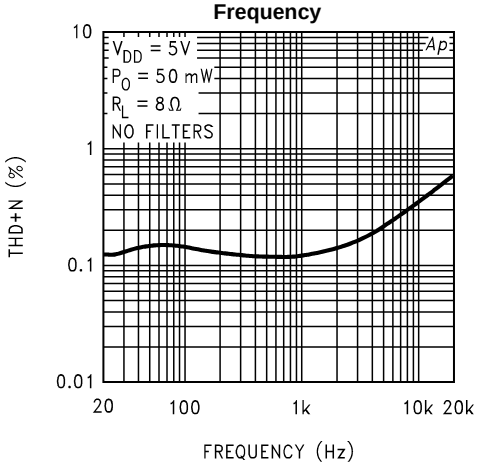


Figure 8.

THD+N vs Frequency

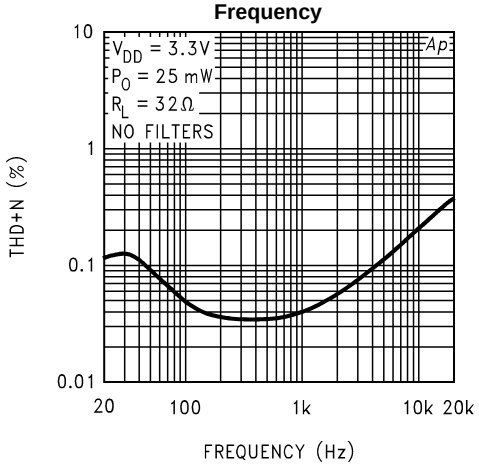


Figure 9.

THD+N vs Frequency

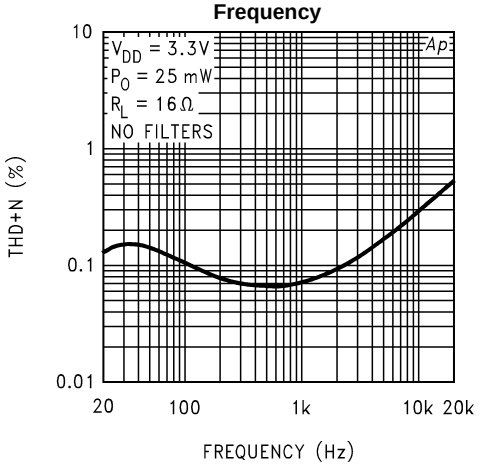


Figure 10.

THD+N vs Frequency

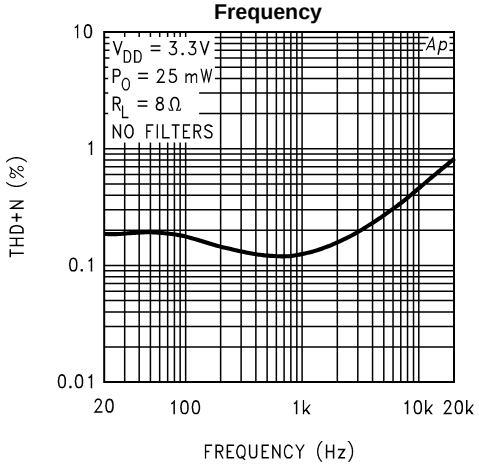


Figure 11.

Typical Performance Characteristics (continued)

THD+N vs Frequency

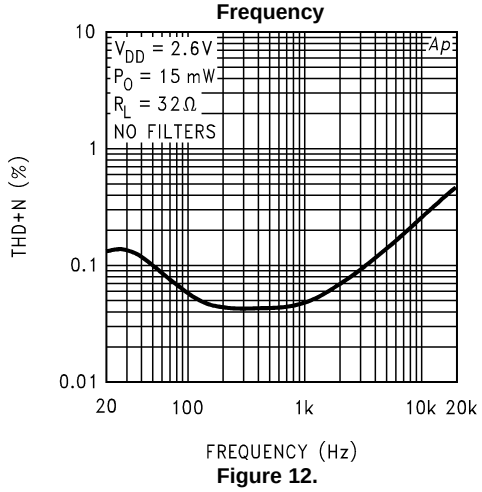


Figure 12.

THD+N vs Frequency

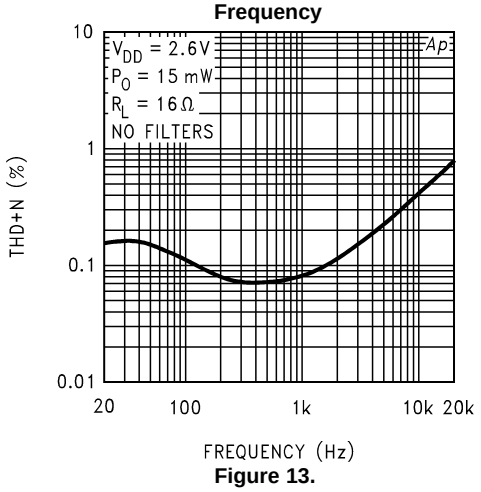


Figure 13.

THD+N vs Frequency

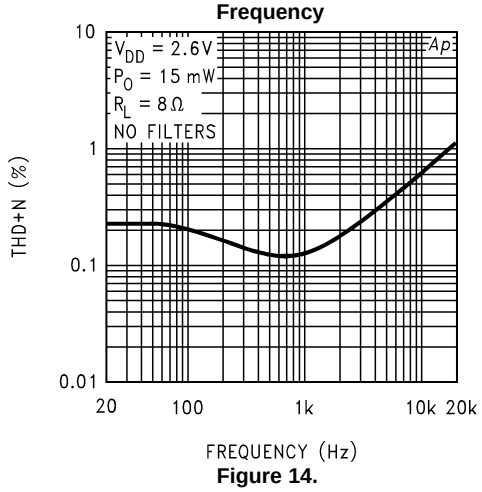


Figure 14.

THD+N vs Frequency

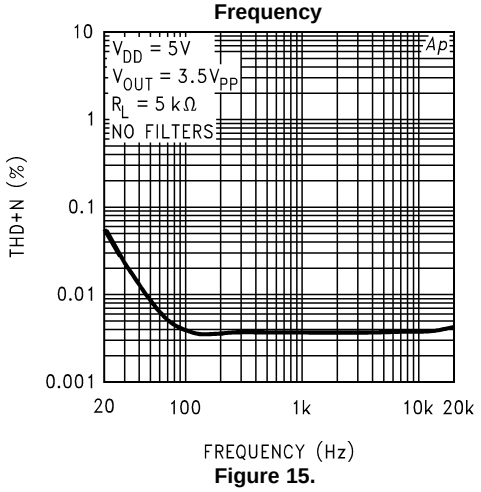


Figure 15.

THD+N vs Output Power

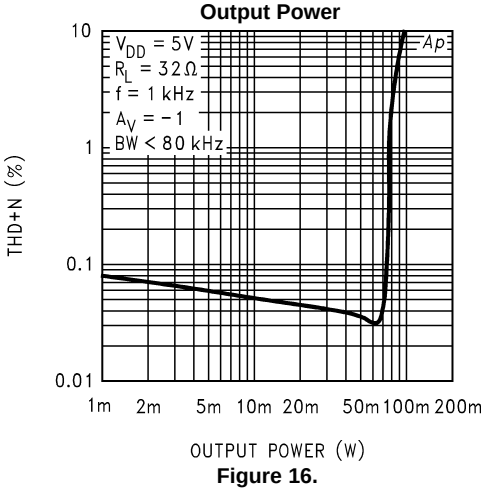


Figure 16.

THD+N vs Output Power

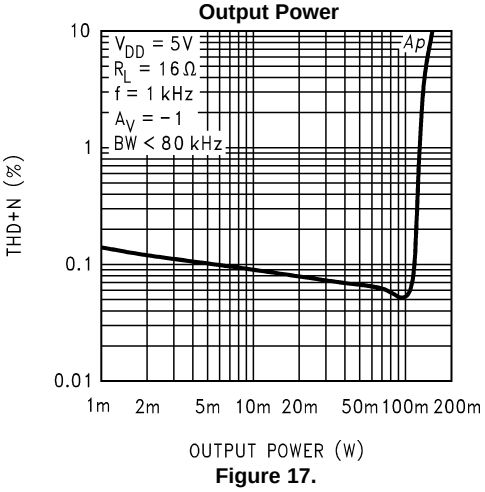


Figure 17.

Typical Performance Characteristics (continued)

THD+N vs Output Power

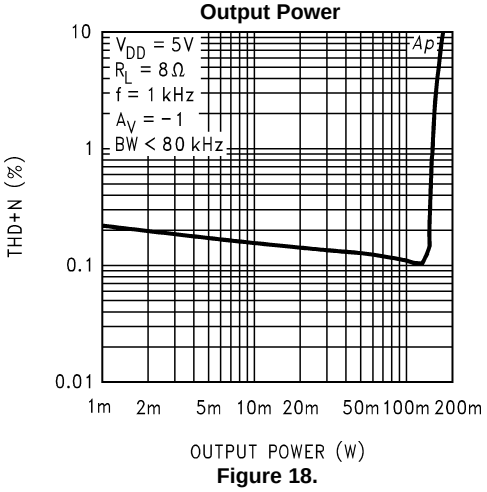


Figure 18.

THD+N vs Output Power

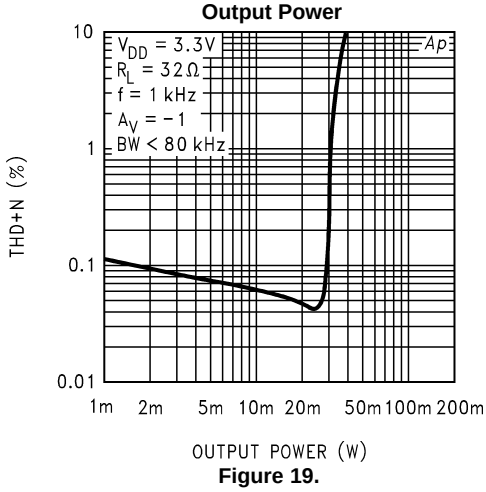


Figure 19.

THD+N vs Output Power

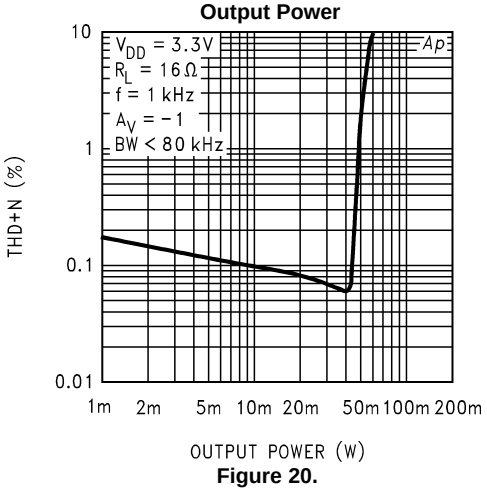


Figure 20.

THD+N vs Output Power

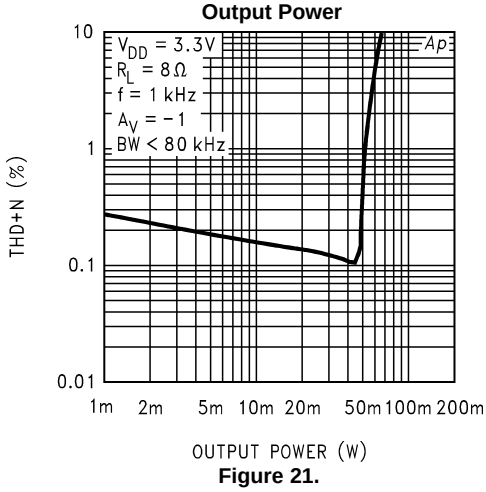


Figure 21.

THD+N vs Output Power

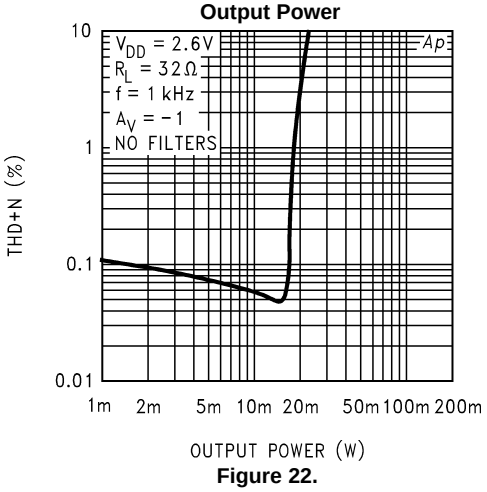


Figure 22.

THD+N vs Output Power

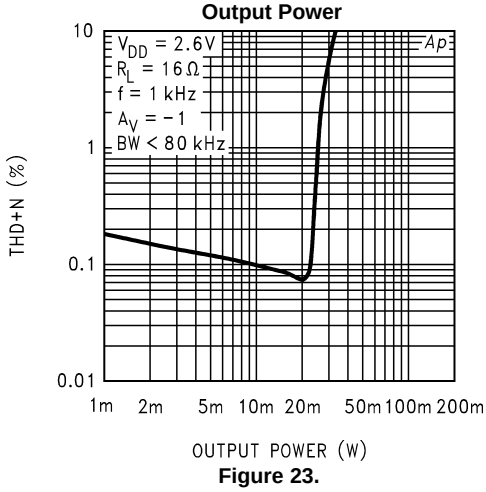


Figure 23.

Typical Performance Characteristics (continued)

THD+N vs Output Power

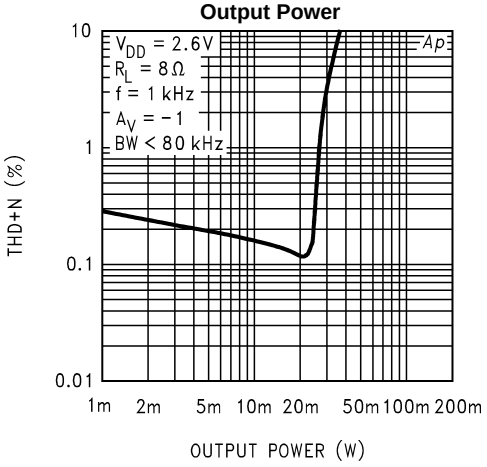


Figure 24.

Output Power vs Load Resistance

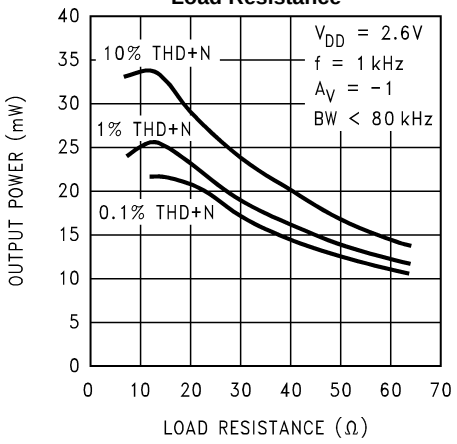


Figure 25.

Output Power vs Load Resistance

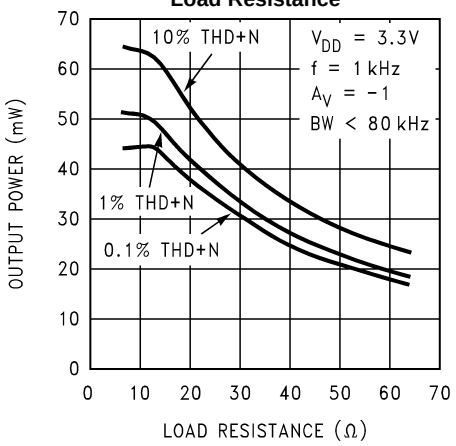


Figure 26.

Output Power vs Load Resistance

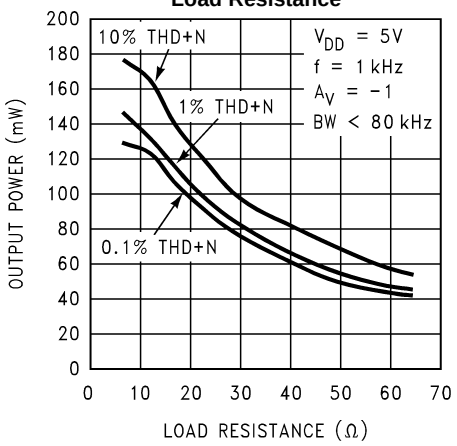


Figure 27.

Output Power vs Supply Voltage

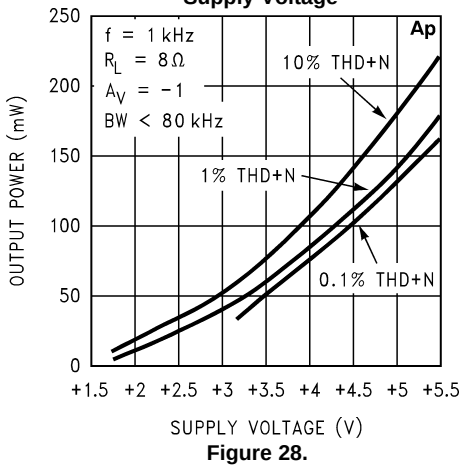


Figure 28.

Output Power vs Power Supply

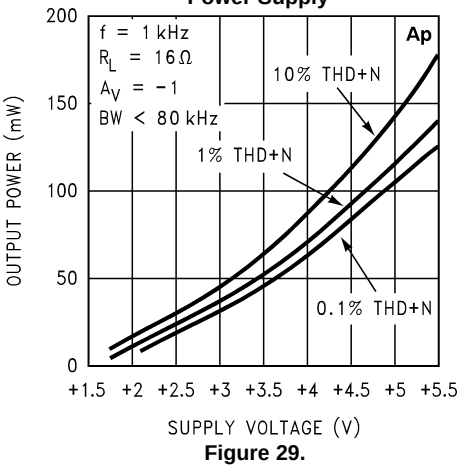


Figure 29.

Typical Performance Characteristics (continued)

Output Power vs Power Supply

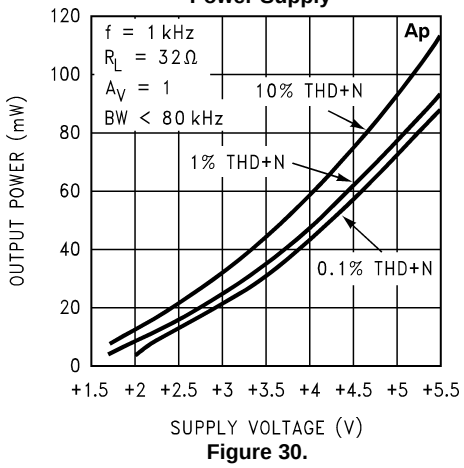


Figure 30.

Dropout Voltage vs Supply Voltage

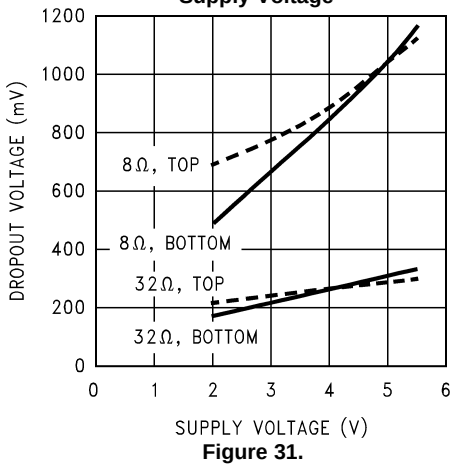


Figure 31.

Power Dissipation vs Output Power

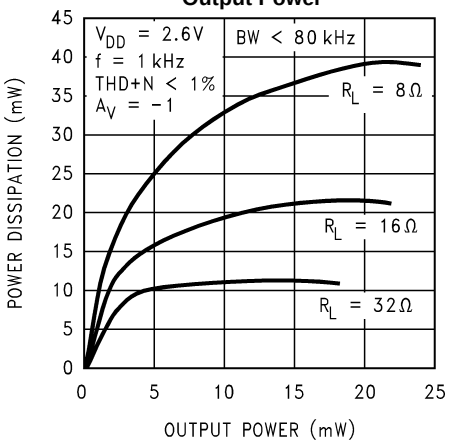


Figure 32.

Power Dissipation vs Output Power

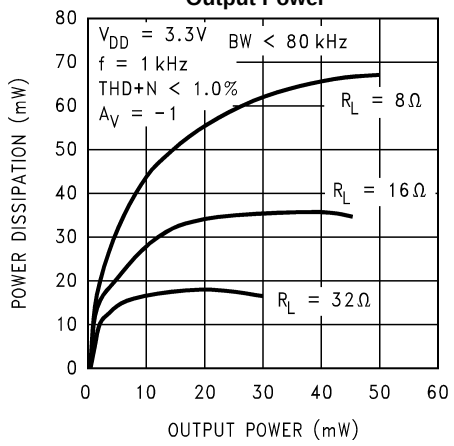


Figure 33.

Power Dissipation vs Output Power

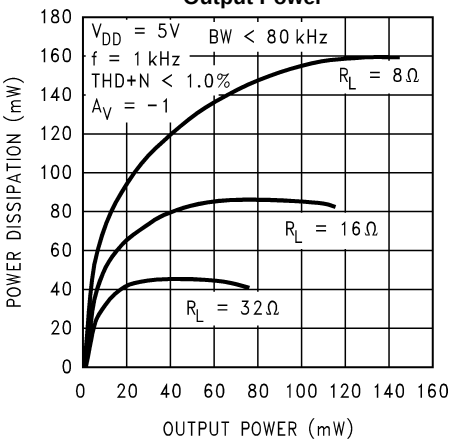


Figure 34.

Channel Separation

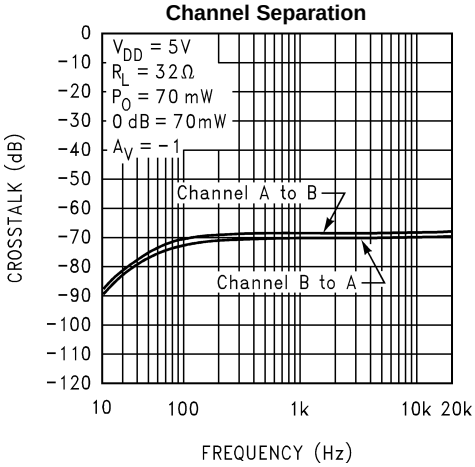


Figure 35.

Typical Performance Characteristics (continued)

Noise Floor

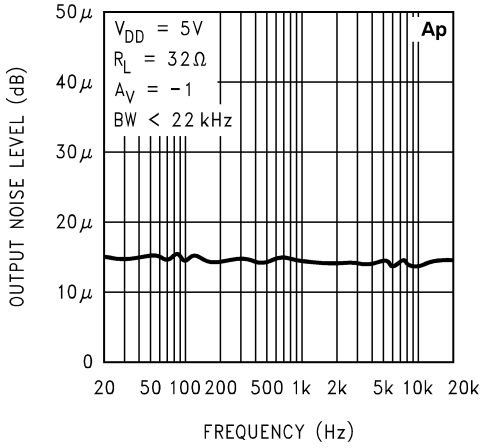


Figure 36.

Power Supply Rejection Ratio

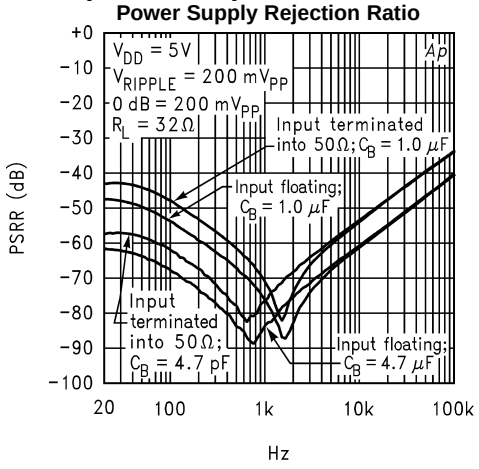


Figure 37.

Open Loop Frequency Response

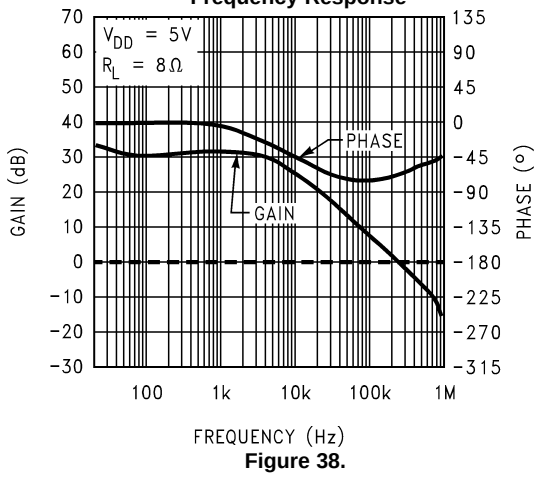


Figure 38.

Open Loop Frequency Response

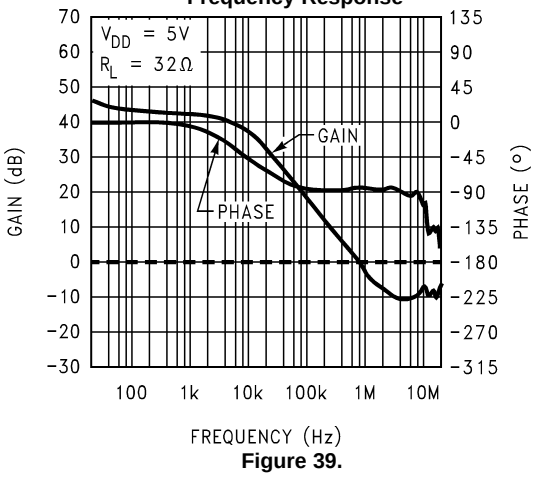


Figure 39.

Open Loop Frequency Response

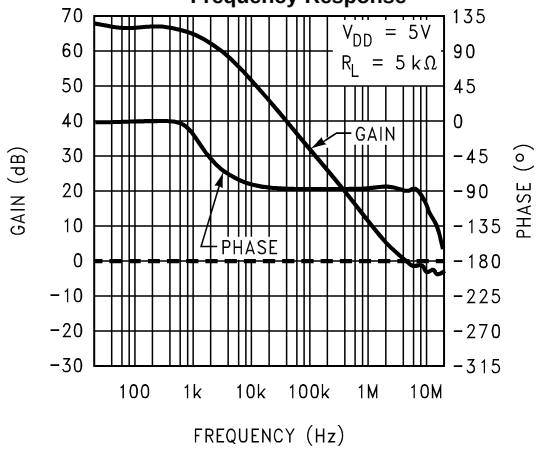


Figure 40.

Supply Current vs Supply Voltage

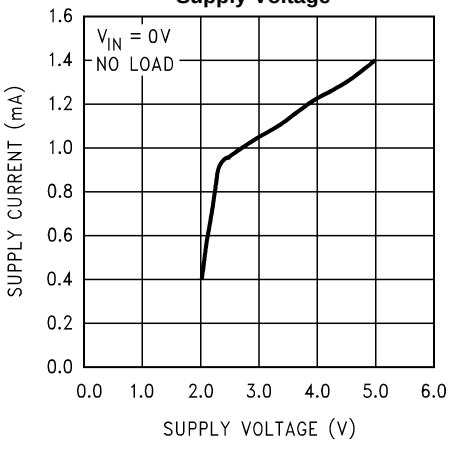


Figure 41.

APPLICATION INFORMATION

MICRO-POWER SHUTDOWN

The voltage applied to the $\overline{\text{SHUTDOWN}}$ pin controls the LM4809's shutdown function. Activate micro-power shutdown by applying a logic low voltage to the $\overline{\text{SHUTDOWN}}$ pin. The logic threshold is typically $V_{DD}/2$. When active, the LM4809's micro-power shutdown feature turns off the amplifier's bias circuitry, reducing the supply current. The low 0.4µA typical shutdown current is achieved by applying a voltage that is as near as GND as possible to the $\overline{\text{SHUTDOWN}}$ pin. A voltage that is above GND may increase the shutdown current.

There are a few ways to control the micro-power shutdown. These include using a single-pole, single-throw switch, a microprocessor, or a microcontroller. When using a switch, connect an external 100kΩ pull-down resistor between the $\overline{\text{SHUTDOWN}}$ pin and GND. Connect the switch between the $\overline{\text{SHUTDOWN}}$ pin and V_{DD}. Select normal amplifier operation by closing the switch. Opening the switch connects the $\overline{\text{SHUTDOWN}}$ pin to GND through the pull-down resistor, activating micro-power shutdown. The switch and resistor ensure that the $\overline{\text{SHUTDOWN}}$ pin will not float. This prevents unwanted state changes. In a system with a microprocessor or a microcontroller, use a digital output to apply the control voltage to the $\overline{\text{SHUTDOWN}}$ pin. Driving the $\overline{\text{SHUTDOWN}}$ pin with active circuitry eliminates the pull-down resistor.

EXPOSED-DAP PACKAGE PCB MOUNTING CONSIDERATION

The LM4809's exposed-Dap (die attach paddle) package (LD or LQ) provides a low thermal resistance between the die and the PCB to which the part is mounted and soldered. This allows rapid heat transfer from the die to the surrounding PCB copper traces, ground plane, and surrounding air.

The LD or LQ package should have its DAP soldered to a copper pad on the PCB. The DAP's PCB copper pad may be connected to a large plane of continuous unbroken copper. This plane forms a thermal mass, heat sink, and radiation area.

However, since the LM4809 is designed for headphone applications, connecting a copper plane to the DAP's PCB copper pad is not required. Figure 34 in Typical Performance Characteristics shows that the maximum power dissipated is just 45mW per amplifier with a 5V power supply and a 32Ω load.

Further detailed and specific information concerning PCB layout, fabrication, and mounting an NGL0008B or NGP0008A package is available from Texas Instruments' Package Engineering Group under application note AN1187.

POWER DISSIPATION

Power dissipation is a major concern when using any power amplifier and must be thoroughly understood to ensure a successful design. Equation 1 states the maximum power dissipation point for a single-ended amplifier operating at a given supply voltage and driving a specified output load.

$$P_{DMAX} = (V_{DD})^2 / (2\pi^2 R_L) \quad (1)$$

Since the LM4809 has two operational amplifiers in one package, the maximum internal power dissipation point is twice that of the number which results from Equation 1. Even with the large internal power dissipation, the LM4809 does not require heat sinking over a large range of ambient temperature. From Equation 1, assuming a 5V power supply and a 32Ω load, the maximum power dissipation point is 40mW per amplifier. Thus the maximum package dissipation point is 80mW. The maximum power dissipation point obtained must not be greater than the power dissipation that results from Equation 2:

$$P_{DMAX} = (T_{JMAX} - T_A) / \theta_{JA} \quad (2)$$

For package MUA08A, θ_{JA} = 210°C/W. T_{JMAX} = 150°C for the LM4809. Depending on the ambient temperature, T_A, of the system surroundings, Equation 2 can be used to find the maximum internal power dissipation supported by the IC packaging. If the result of Equation 1 is greater than that of Equation 2, then either the supply voltage must be decreased, the load impedance increased or T_A reduced. For the typical application of a 5V power supply, with a 32Ω load, the maximum ambient temperature possible without violating the maximum junction temperature is approximately 133.2°C provided that device operation is around the maximum power dissipation point. Power dissipation is a function of output power and thus, if typical operation is not around the maximum power dissipation point, the ambient temperature may be increased accordingly. Refer to the **Typical Performance Characteristics** curves for power dissipation information for lower output powers.

POWER SUPPLY BYPASSING

As with any power amplifier, proper supply bypassing is critical for low noise performance and high power supply rejection. Applications that employ a 5V regulator typically use a 10µF in parallel with a 0.1µF filter capacitors to stabilize the regulator's output, reduce noise on the supply line, and improve the supply's transient response. However, their presence does not eliminate the need for a local 1.0µF tantalum bypass capacitance connected between the LM4809's supply pins and ground. Keep the length of leads and traces that connect capacitors between the LM4809's power supply pin and ground as short as possible. Connecting a 4.7µF capacitor, C_B, between the BYPASS pin and ground improves the internal bias voltage's stability and improves the amplifier's PSRR. The PSRR improvements increase as the bypass pin capacitor value increases. Too large, however, increases the amplifier's turn-on time. The selection of bypass capacitor values, especially C_B, depends on desired PSRR requirements, click and pop performance (as explained in the section, **Selecting Proper External Components**), system cost, and size constraints.

SELECTING PROPER EXTERNAL COMPONENTS

Optimizing the LM4809's performance requires properly selecting external components. Though the LM4809 operates well when using external components with wide tolerances, best performance is achieved by optimizing component values.

The LM4809 is unity-gain stable, giving a designer maximum design flexibility. The gain should be set to no more than a given application requires. This allows the amplifier to achieve minimum THD+N and maximum signal-to-noise ratio. These parameters are compromised as the closed-loop gain increases. However, low gain demands input signals with greater voltage swings to achieve maximum output power. Fortunately, many signal sources such as audio CODECs have outputs of $1V_{RMS}$ ($2.83V_{P-P}$). Please refer to the **Audio Power Amplifier Design** section for more information on selecting the proper gain.

Input and Output Capacitor Value Selection

Amplifying the lowest audio frequencies requires high value input and output coupling capacitors (C_I and C_O in Figure 1). A high value capacitor can be expensive and may compromise space efficiency in portable designs. In many cases, however, the speakers used in portable systems, whether internal or external, have little ability to reproduce signals below 150Hz. Applications using speakers with this limited frequency response reap little improvement by using high value input and output capacitors.

Besides affecting system cost and size, C_i has an effect on the LM4809's click and pop performance. The magnitude of the pop is directly proportional to the input capacitor's size. Thus, pops can be minimized by selecting an input capacitor value that is no higher than necessary to meet the desired −3dB frequency. Please refer to the Optimizing Click and Pop Reduction Performance section for a more detailed discussion on click and pop performance.

As shown in Figure 1, the input resistor, R_I and the input capacitor, C_I, produce a −3dB high pass filter cutoff frequency that is found using Equation 3. In addition, the output load R_L, and the output capacitor C_O, produce a -3db high pass filter cutoff frequency defined by Equation 4.

$$f_{I\text{-}3db}=1/2\pi R_I C_I \quad (3)$$

$$f_{O\text{-}3db}=1/2\pi R_L C_O \quad (4)$$

Also, careful consideration must be taken in selecting a certain type of capacitor to be used in the system. Different types of capacitors (tantalum, electrolytic, ceramic) have unique performance characteristics and may affect overall system performance.

Bypass Capacitor Value Selection

Besides minimizing the input capacitor size, careful consideration should be paid to the value of C_B, the capacitor connected to the BYPASS pin. Since C_B determines how fast the LM4809 settles to quiescent operation, its value is critical when minimizing turn-on pops. The slower the LM4809's outputs ramp to their quiescent DC voltage (nominally 1/2 V_{DD}), the smaller the turn-on pop. Choosing C_B equal to 4.7µF along with a small value of C_i (in the range of 0.1µF to 0.47µF), produces a click-less and pop-less shutdown function. As discussed above, choosing C_i no larger than necessary for the desired bandwith helps minimize clicks and pops.

OPTIMIZING CLICK AND POP REDUCTION PERFORMANCE

The LM4809 contains circuitry that minimizes turn-on and shutdown transients or “clicks and pop”. For this discussion, turn-on refers to either applying the power supply voltage or when the shutdown mode is deactivated. During turn-on, the LM4809's internal amplifiers are configured as unity gain buffers. An internal current source charges up the capacitor on the BYPASS pin in a controlled, linear manner. The gain of the internal amplifiers remains unity until the voltage on the BYPASS pin reaches 1/2 V_{DD} . As soon as the voltage on the BYPASS pin is stable, the device becomes fully operational. During device turn-on, a transient (pop) is created from a voltage difference between the input and output of the amplifier as the voltage on the BYPASS pin reaches 1/2 V_{DD}. For this discussion, the input of the amplifier refers to the node between R_I and C_I. Ideally, the input and output track the voltage applied to the BYPASS pin. During turn-on, the buffer-configured amplifier output charges the input capacitor, C_I, through the input resistor, R_I. This input resistor delays the charging time of C_I thereby causing the voltage difference between the input and output that results in a transient (pop). Higher value capacitors need more time to reach a quiescent DC voltage (usually 1/2 V_{DD}) when charged with a fixed current. Decreasing the value of C_I and R_I will minimize turn-on pops at the expense of the desired -3dB frequency.

Although the BYPASS pin current cannot be modified, changing the size of C_B alters the device's turn-on time and the magnitude of “clicks and pops”. Increasing the value of C_B reduces the magnitude of turn-on pops. However, this presents a tradeoff: as the size of C_B increases, the turn-on time increases. There is a linear relationship between the size of C_B and the turn-on time. Here are some typical turn-on times for various values of C_B:

C_B	T_{ON}
0.1µF	80ms
0.22µF	170ms
0.33µF	270ms
0.47µF	370ms
0.68µF	490ms
1.0µF	920ms
2.2µF	1.8sec
3.3µF	2.8sec
4.7µF	3.4sec
10µF	7.7sec

In order eliminate “clicks and pops”, all capacitors must be discharged before turn-on. Rapidly switching V_{DD} may not allow the capacitors to fully discharge, which may cause “clicks and pops”. In a single-ended configuration, the output is coupled to the load by C_O. This capacitor usually has a high value. C_O discharges through internal 20kΩ resistors. Depending on the size of C_O, the discharge time constant can be relatively large. To reduce transients in single-ended mode, an external 1kΩ–5kΩ resistor can be placed in parallel with the internal 20kΩ resistor. The tradeoff for using this resistor is increased quiescent current.

AUDIO POWER AMPLIFIER DESIGN

Design a Dual 70mW/32Ω Audio Amplifier

Given:	
Power Output	70 mW
Load Impedance	32Ω
Input Level	1 Vrms (max)
Input Impedance	20kΩ
Bandwidth	100 Hz–20 kHz ± 0.50dB

The design begins by specifying the minimum supply voltage necessary to obtain the specified output power. One way to find the minimum supply voltage is to use Figure 28 in the **Typical Performance Characteristics** section. Another way, using Equation 5, is to calculate the peak output voltage necessary to achieve the desired output power for a given load impedance. To account for the amplifier's dropout voltage, two additional voltages, based on Figure 31 in **Typical Performance Characteristics** , must be added to the result obtained by Equation 5. For a single-ended application, the result is Equation 6.

$$V_{opeak} = \sqrt{(2R_L P_O)} \tag{5}$$

$$V_{DD} \geq (2V_{OPEAK} + (V_{ODTOP} + V_{ODBOT})) \tag{6}$$

Figure 28 for a 32Ω load indicates a minimum supply voltage of 4.8V. This is easily met by the commonly used 5V supply voltage. The additional voltage creates the benefit of headroom, allowing the LM4809 to produce peak output power in excess of 70mW without clipping or other audible distortion. The choice of supply voltage must also not create a situation that violates maximum power dissipation as explained above in the **Power Dissipation** section. Remember that the maximum power dissipation point from Equation 1 must be multiplied by two since there are two independent amplifiers inside the package. Once the power dissipation equations have been addressed, the required gain can be determined from Equation 7.

$$A_V \geq \sqrt{(P_O R_L)}/(V_{IN}) = V_{orms}/V_{inrms} \tag{7}$$

Thus, a minimum gain of 1.497 allows the LM4809 to reach full output swing and maintain low noise and THD+N perfromance. For this example, let A_V=1.5.

The amplifiers overall gain is set using the input (R_i) and feedback (R_f) resistors. With the desired input impedance set at 20kΩ, the feedback resistor is found using Equation 8.

$$A_V = R_f/R_i \tag{8}$$

The value of R_f is 30kΩ.

The last step in this design is setting the amplifier's −3db frequency bandwidth. To achieve the desired ±0.25dB pass band magnitude variation limit, the low frequency response must extend to at lease one−fifth the lower bandwidth limit and the high frequency response must extend to at least five times the upper bandwidth limit. The gain variation for both response limits is 0.17dB, well within the ±0.25dB desired limit. The results are an

$$f_L = 100Hz/5 = 20Hz \quad (9)$$

and a

$$f_H = 20kHz^*5 = 100kHz \quad (10)$$

As stated in the **Selecting Proper External Components** section, both R_i in conjunction with C_i, and C_o with R_L, create first order highpass filters. Thus to obtain the desired low frequency response of 100Hz within ±0.5dB, both poles must be taken into consideration. The combination of two single order filters at the same frequency forms a second order response. This results in a signal which is down 0.34dB at five times away from the single order filter −3dB point. Thus, a frequency of 20Hz is used in the following equations to ensure that the response is better than 0.5dB down at 100Hz.

$$C_i \geq 1 / (2\pi * 20k\Omega * 20Hz) = 0.397\mu F; \text{ use } 0.39\mu F. \quad (11)$$

$$C_o \geq 1 / (2\pi * 32\Omega * 20Hz) = 249\mu F; \text{ use } 330\mu F. \quad (12)$$

The high frequency pole is determined by the product of the desired high frequency pole, f_H, and the closed-loop gain, A_V. With a closed-loop gain of 1.5 and f_H = 100kHz, the resulting GBWP = 150kHz which is much smaller than the LM4809's GBWP of 900kHz. This figure displays that if a designer has a need to design an amplifier with a higher gain, the LM4809 can still be used without running into bandwidth limitations.

Demonstration Board Schematic

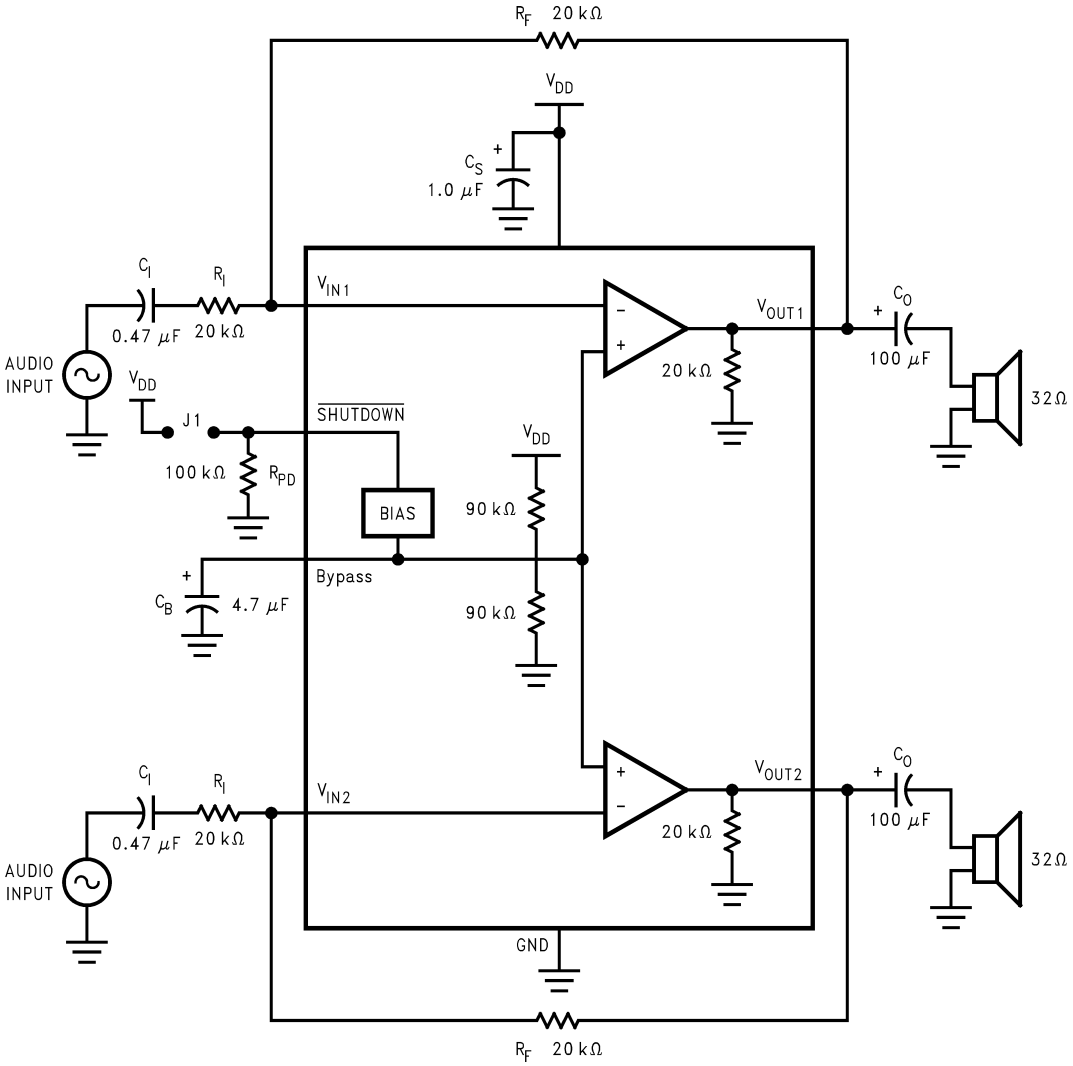


Figure 42. LM4809 Demonstration Board Schematic

Demonstration Board Layout

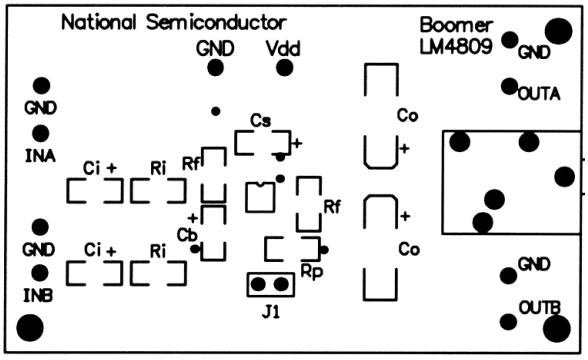


Figure 43. Recommended DGK0008A PC Board Layout Component-Side Silkscreen

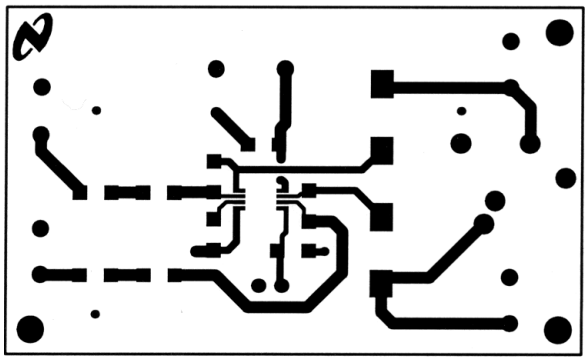


Figure 44. Recommended DGK0008A PC Board Layout Component-Side Layout

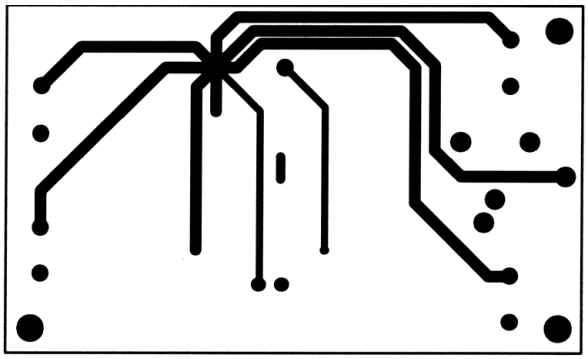


Figure 45. Recommended DGK0008A PC Board Layout Bottom-Side Layout

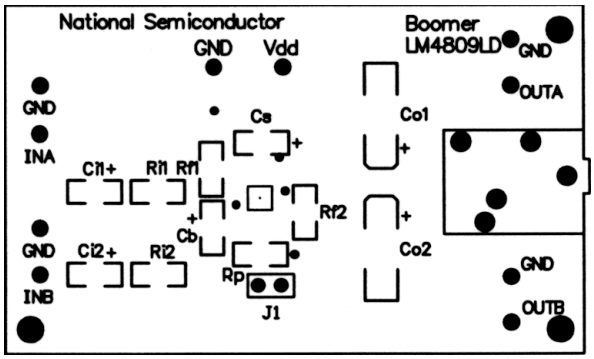


Figure 46. Recommended NGL0008B PC Board Layout Component-Side Silkscreen

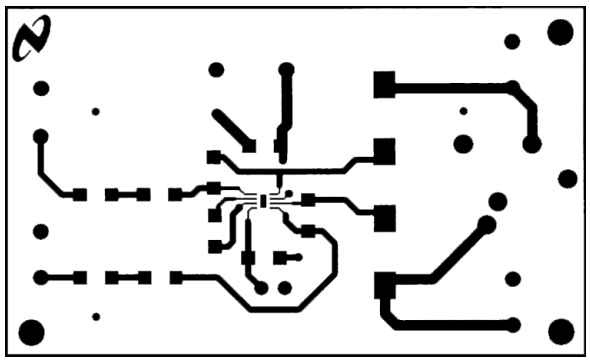


Figure 47. Recommended NGL0008B PC Board Layout
Component-Side Layout

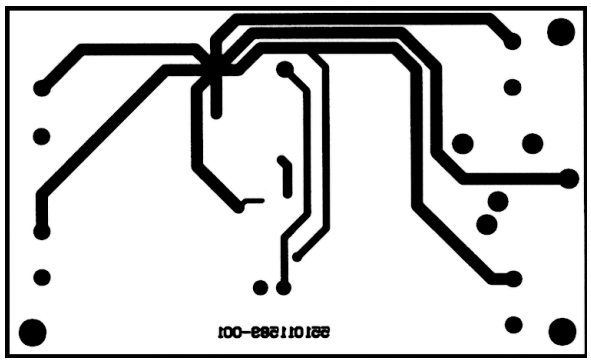


Figure 48. Recommended NGL0008B PC Board Layout
Bottom-Side Layout

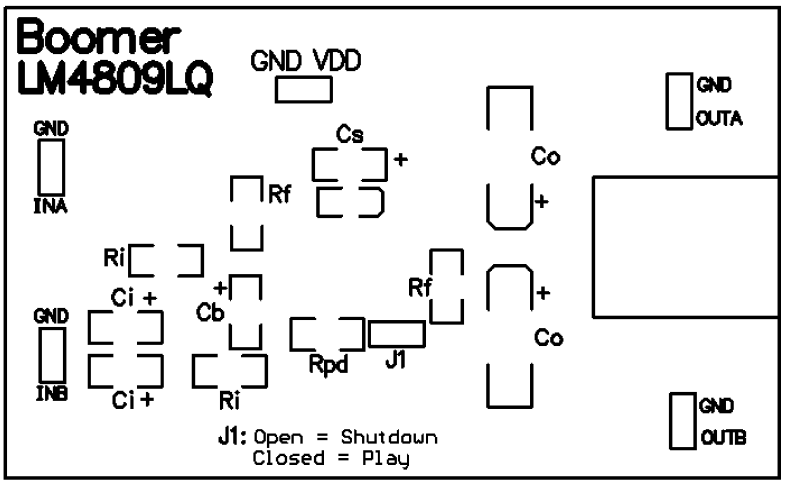


Figure 49. Recommended NGP0008A PC Board Layout
Component-Side Silkscreen

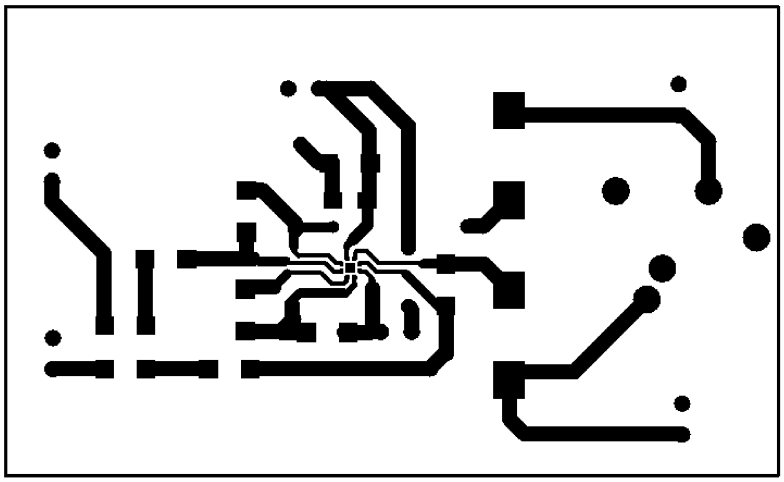


Figure 50. Recommended NGP0008A PC Board Layout
Component-Side Layout

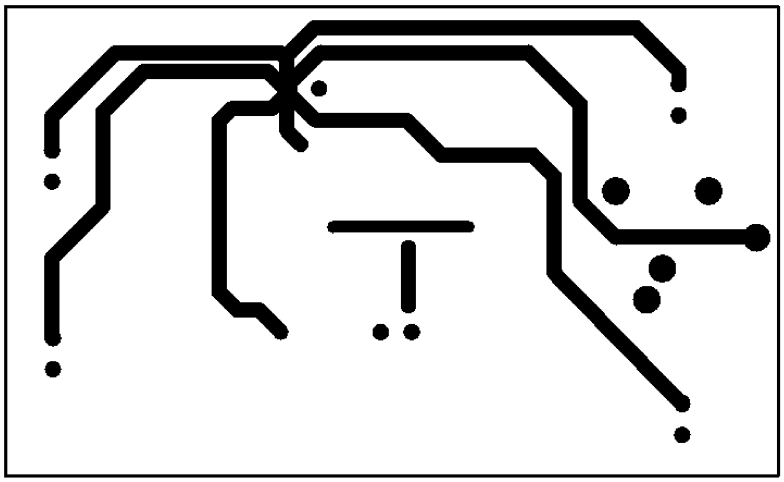


Figure 51. Recommended NGP0008A PC Board Layout
Bottom-Side Layout

REVISION HISTORY

Changes from Revision E (April 2013) to Revision F	Page
• Changed layout of National Data Sheet to TI format	21

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
LM4809LDX/NOPB	Active	Production	WSON (NGL) | 8	4500 | LARGE T&R	Yes	SN	Level-3-260C-168 HR	-40 to 85	G09
LM4809LDX/NOPB.A	Active	Production	WSON (NGL) | 8	4500 | LARGE T&R	Yes	SN	Level-3-260C-168 HR	-40 to 85	G09
LM4809LDX/NOPB.B	Active	Production	WSON (NGL) | 8	4500 | LARGE T&R	-	Call TI	Call TI	-40 to 85	
LM4809MM/NOPB	Active	Production	VSSOP (DGK) | 8	1000 | SMALL T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 85	G09
LM4809MM/NOPB.A	Active	Production	VSSOP (DGK) | 8	1000 | SMALL T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 85	G09
LM4809MMX/NOPB	Active	Production	VSSOP (DGK) | 8	3500 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 85	G09
LM4809MMX/NOPB.A	Active	Production	VSSOP (DGK) | 8	3500 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 85	G09

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

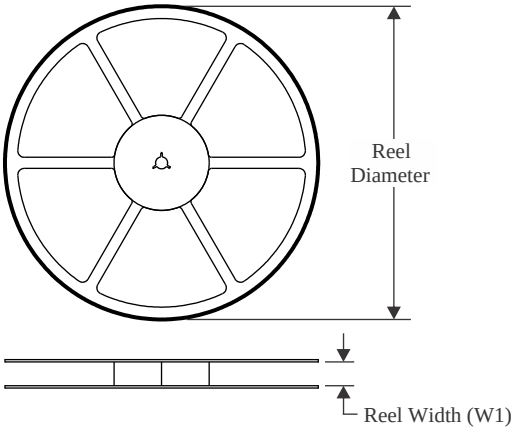
(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

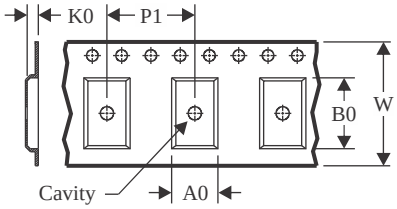
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

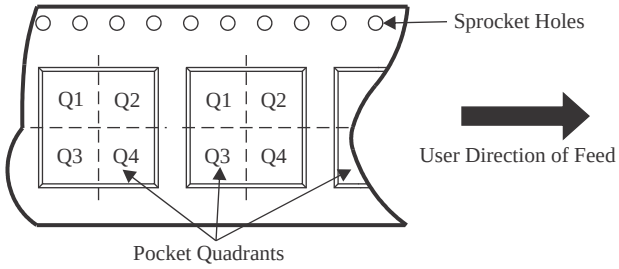


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

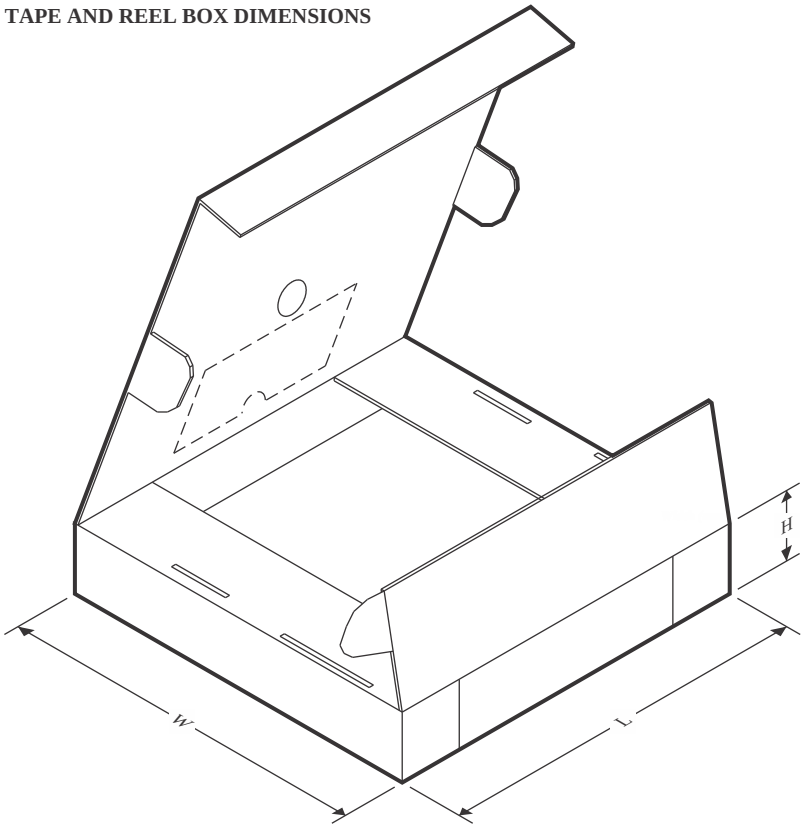
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LM4809LDX/NOPB	WSON	NGL	8	4500	330.0	12.4	2.8	2.8	1.0	8.0	12.0	Q1
LM4809MM/NOPB	VSSOP	DGK	8	1000	177.8	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LM4809MMX/NOPB	VSSOP	DGK	8	3500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1

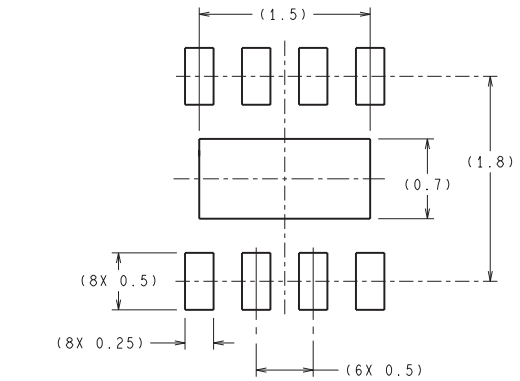
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

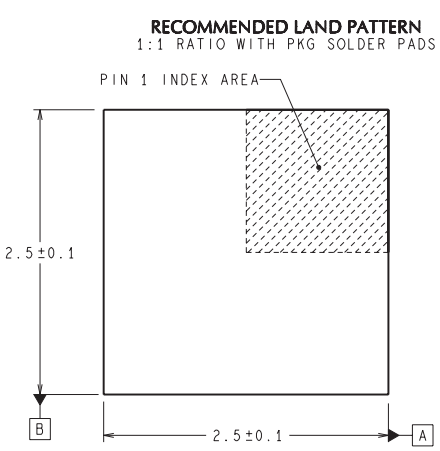
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LM4809LDX/NOPB	WSON	NGL	8	4500	356.0	356.0	36.0
LM4809MM/NOPB	VSSOP	DGK	8	1000	208.0	191.0	35.0
LM4809MMX/NOPB	VSSOP	DGK	8	3500	367.0	367.0	35.0

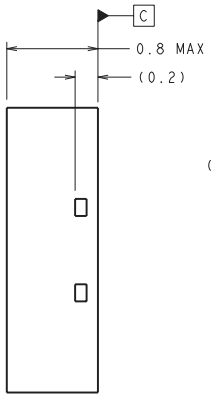
NGL0008B

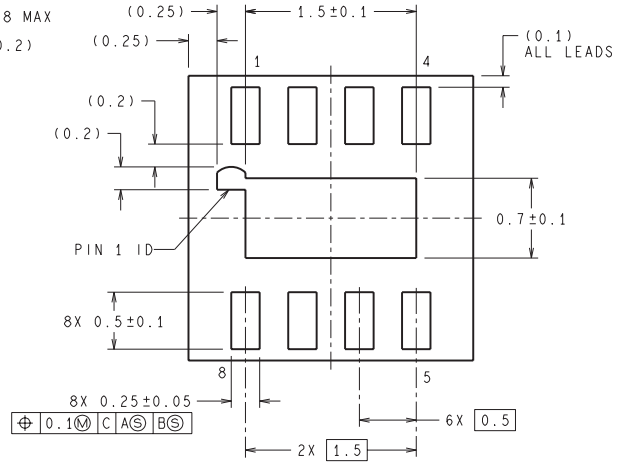


RECOMMENDED LAND PATTERN
1:1 RATIO WITH PKG SOLDER PADS

DIMENSIONS ARE IN MILLIMETERS
DIMENSIONS IN ( ) FOR REFERENCE ONLY







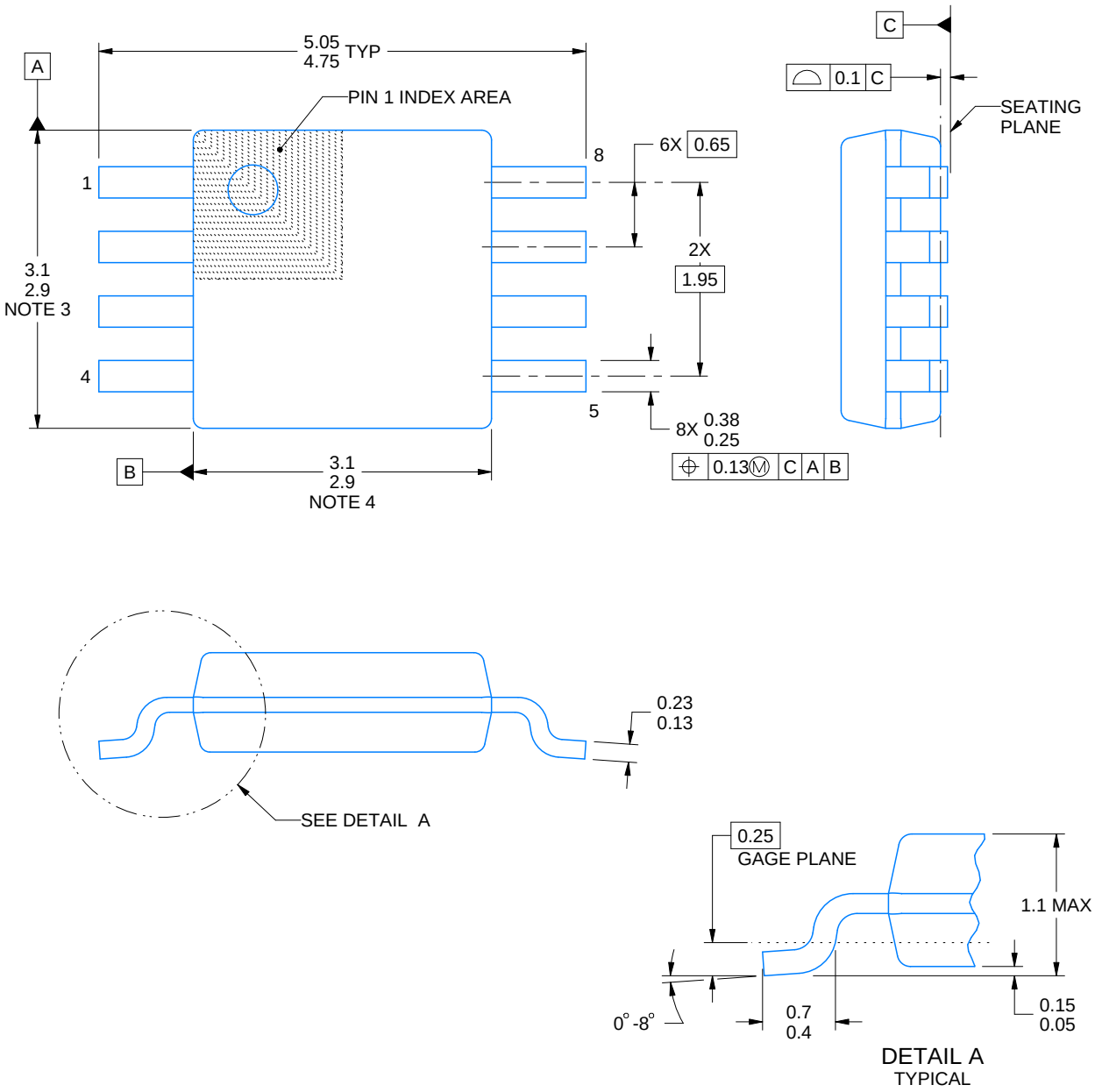
LDA08B (Rev B)

PACKAGE OUTLINE

DGK0008A

VSSOP - 1.1 mm max height

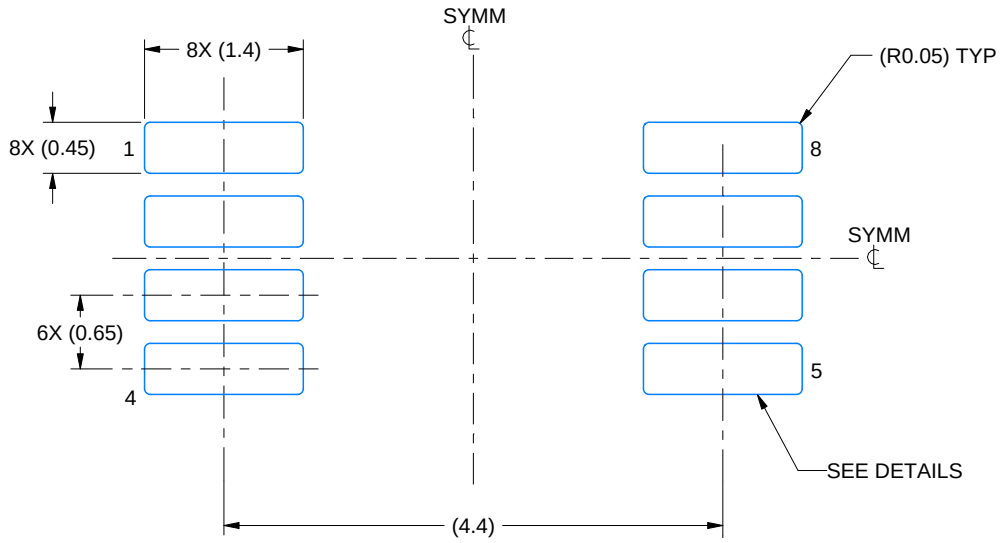
SMALL OUTLINE PACKAGE



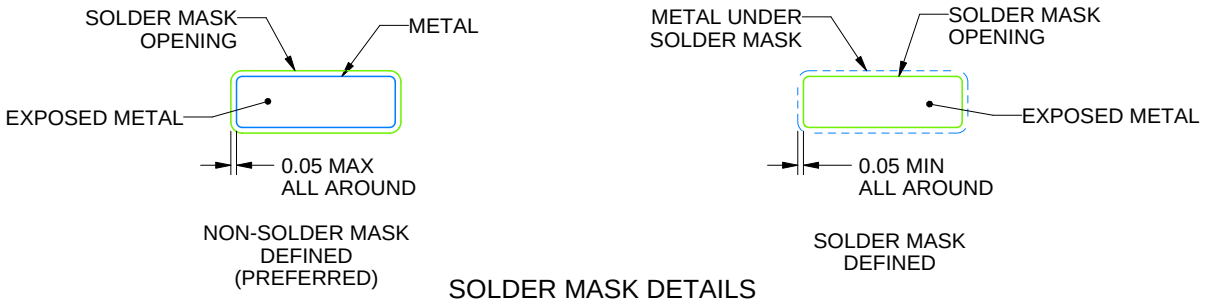
PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 15X

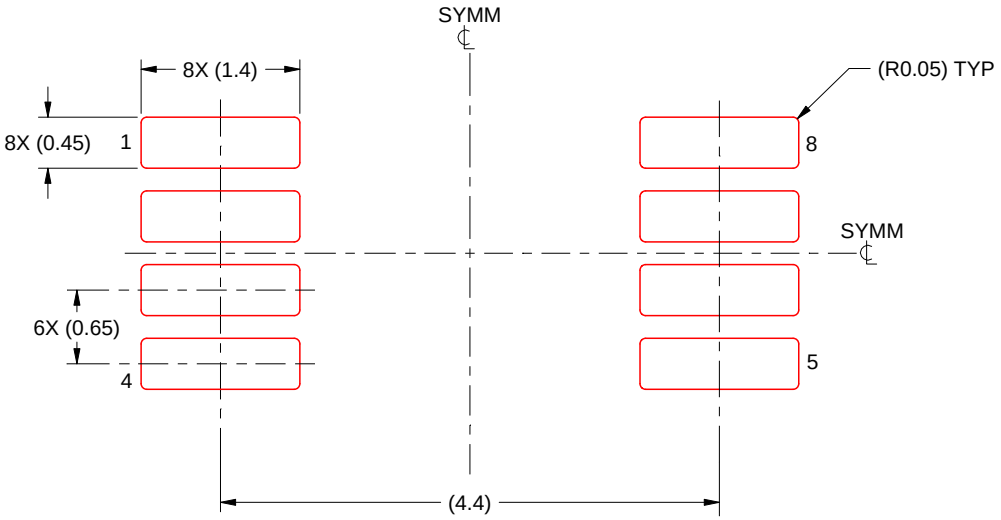


SOLDER MASK DETAILS

4214862/A 04/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.
9. Size of metal pad may vary due to creepage requirement.



SOLDER PASTE EXAMPLE
SCALE: 15X

4214862/A 04/2023

NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI’s products are provided subject to TI’s Terms of Sale or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI’s provision of these resources does not expand or otherwise alter TI’s applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265