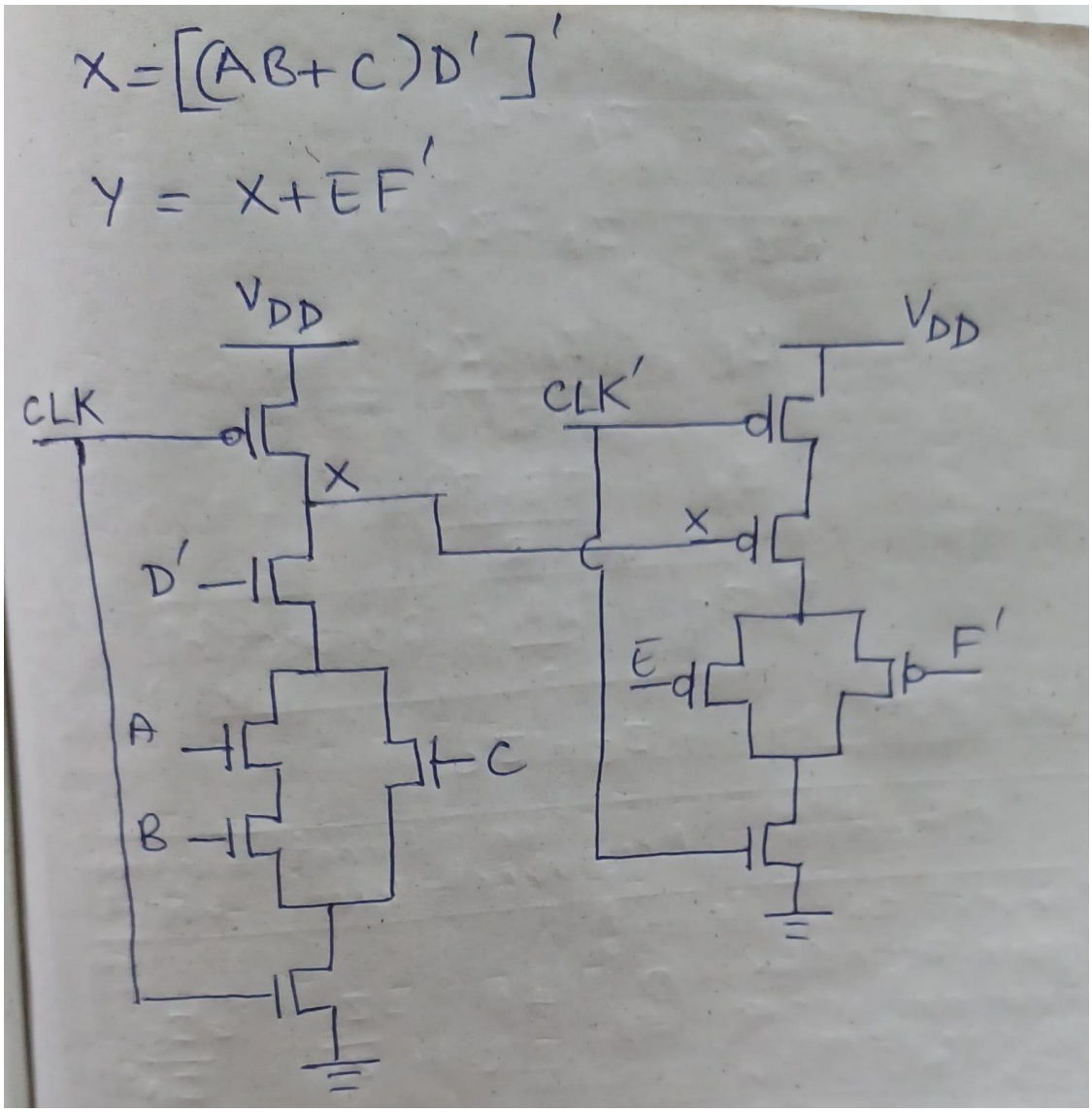
VLSI LAB Exercise-8 NORA Logic

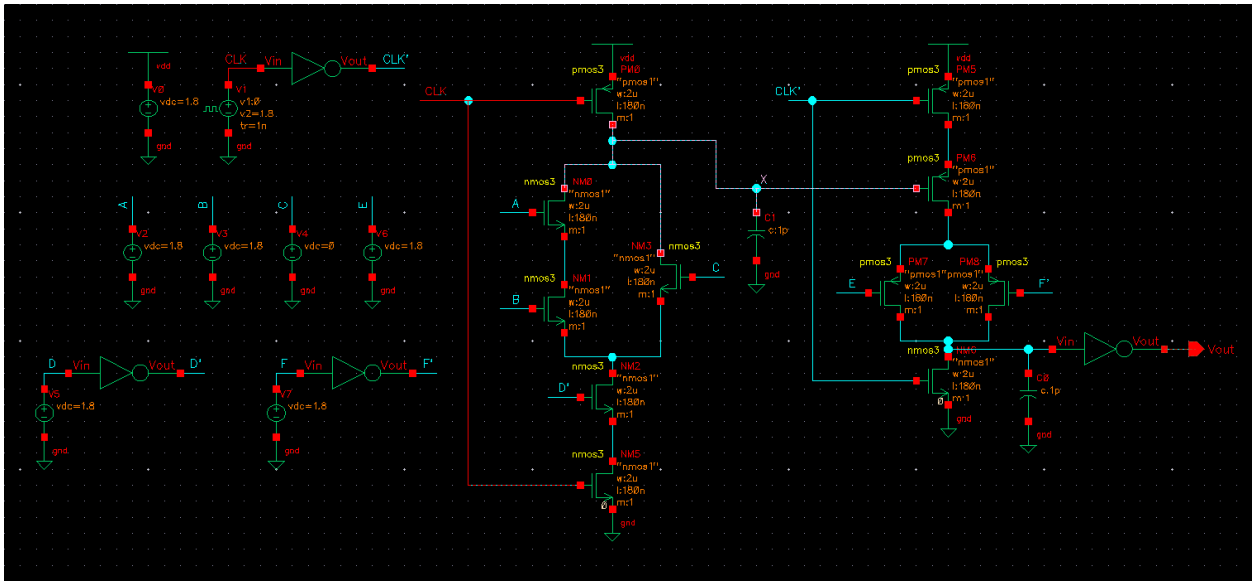
Group Number: 2

Group Members:
Thathapudi Sanjeev Paul Joel - 2020AAPS0120H
Aditya Anirudh - 2020AAPS0373H

Design Workout:

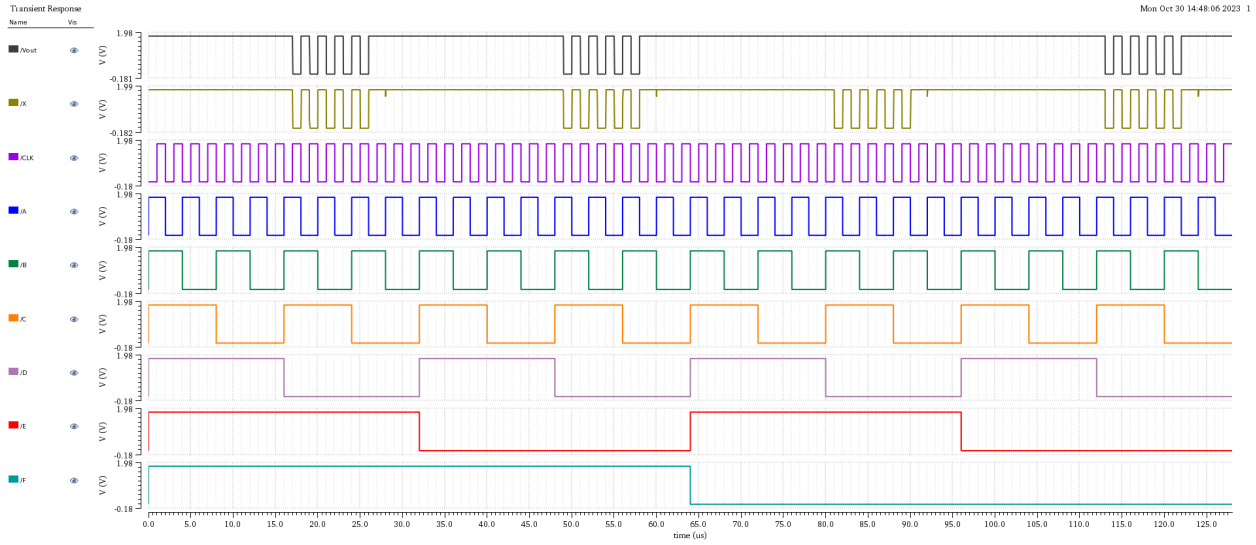


Schematics:



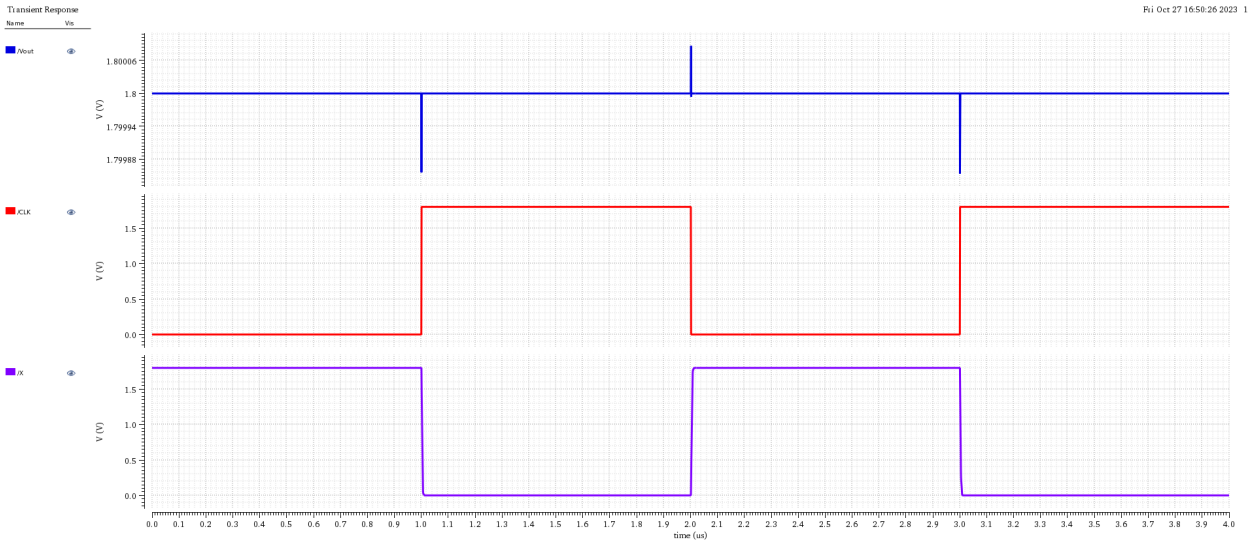
Waveforms:

Giving pulse excitations:-

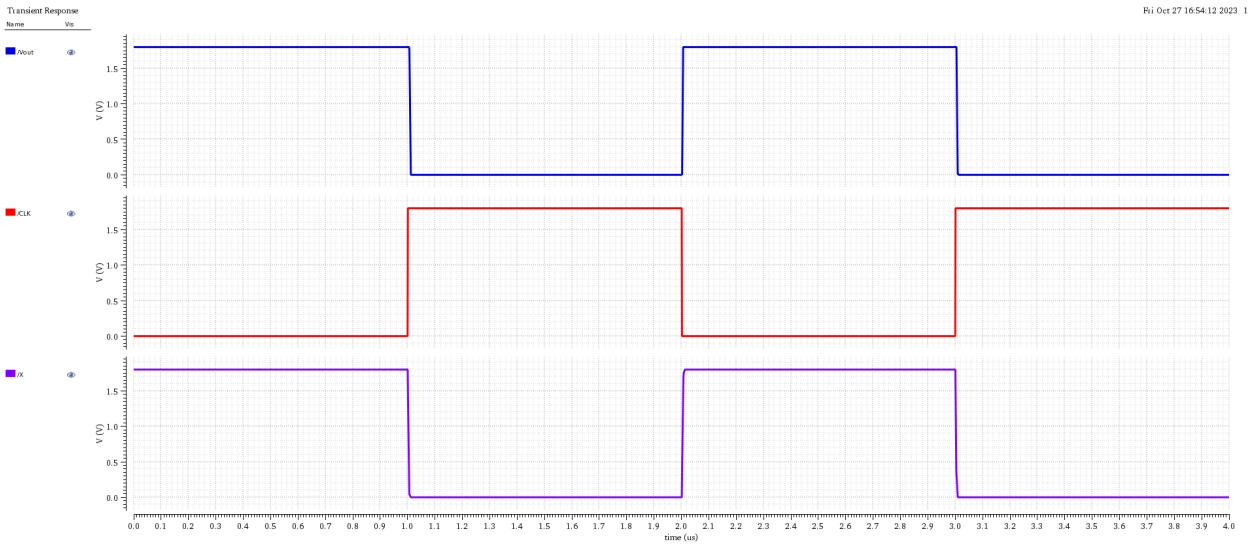


Giving constant excitations (to analyze the behavior):-

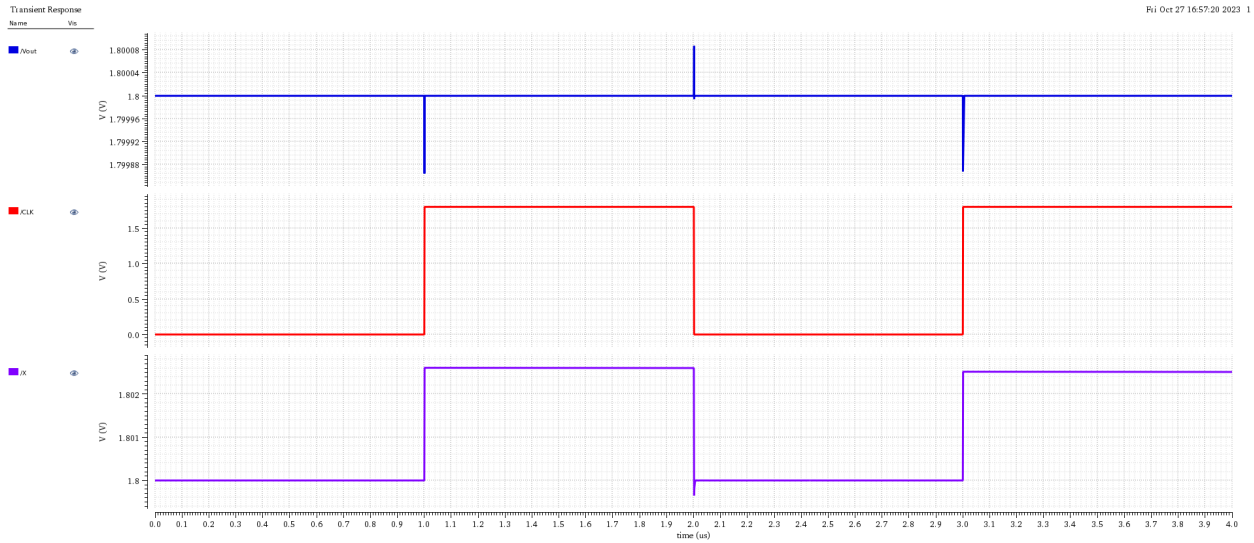
A = 1, B = 1, C = 0, D = 0, E = 1, F = 0



A = 1, B = 1, C = 0, D = 0, E = 1, F = 1



A = 1, B = 1, C = 0, D = 1, E = 1, F = 1



Inferences:

1. V_{out} = 1.8 V, whenever CLK = 0, because the **2nd stage is in the predischarge phase** in this period.
2. Three cases have been depicted while giving constant input excitations to the above circuit:
   a. The 1st stage is evaluated while the 2nd stage is not.
   b. Both the stages are evaluated.
   c. Both the stages are not evaluated.
3. While designing the NMOS and PMOS logic blocks, we have to ensure that, the **race condition for inputs is avoided** by **giving the input non-inverted to the second stage** as PMOS transistors are ON only when V_{in} = LOW, while the NMOS stage is initially pre-charged and not pre-discharged.

Conclusion:

In this experiment, we designed a combinational circuit by **cascading two stages** of **dynamic logic**: one using NMOS logic while the other using PMOS logic for the evaluation phase. This ensures that the **race condition is avoided (NORA Logic)**.