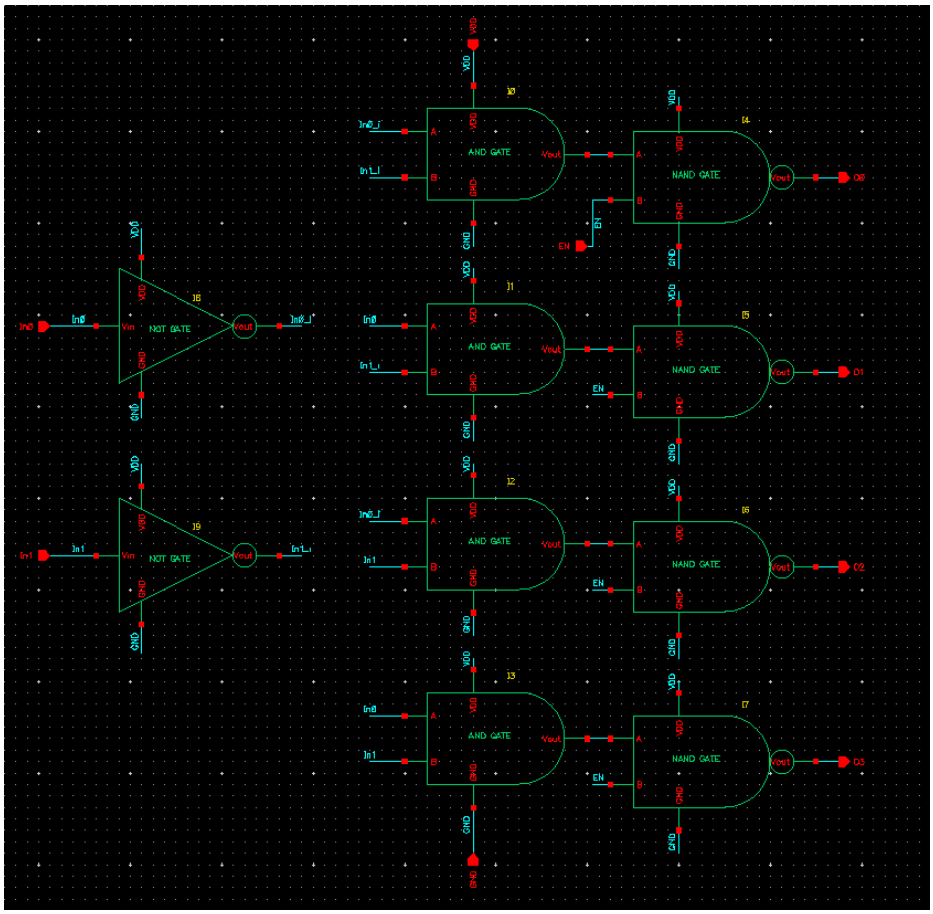
VLSI LAB Experiment-5 Combinational Logic Circuits

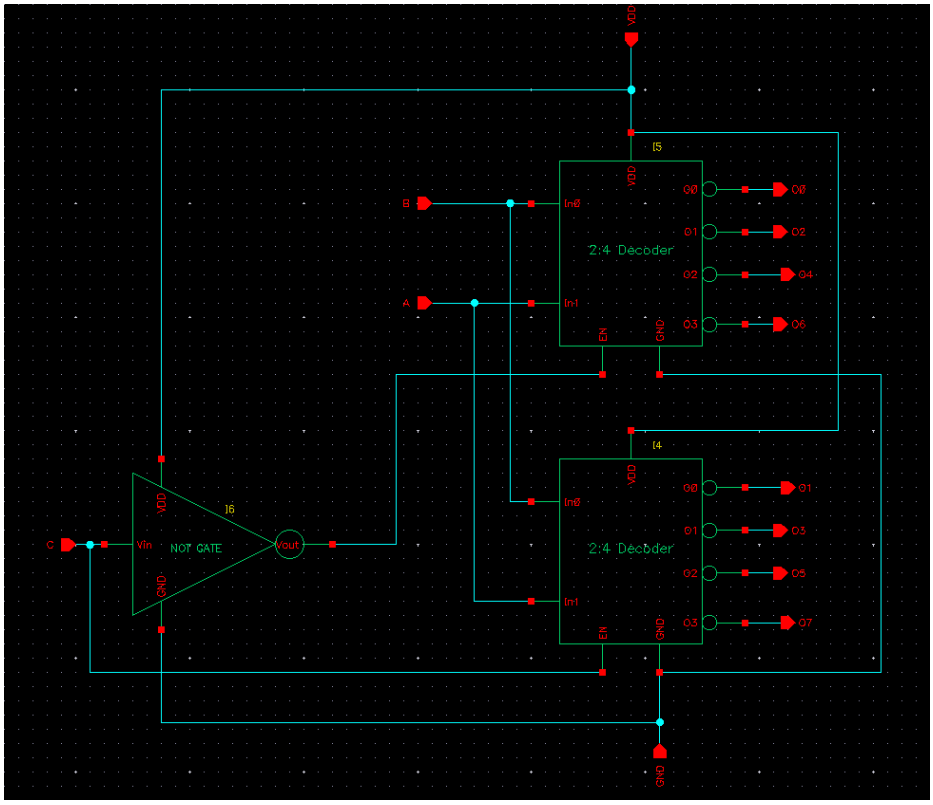
Group Number: 2

Group Members:
Thathapudi Sanjeev Paul Joel - 2020AAPS0120H
Aditya Anirudh - 2020AAPS0373H

Schematics:
Decoder:-



Demux:-



Design Workout:

Excitation Schematic:

Decoder:-

① 2:4 Decoder with active low output and Enable Pin

Truth table:

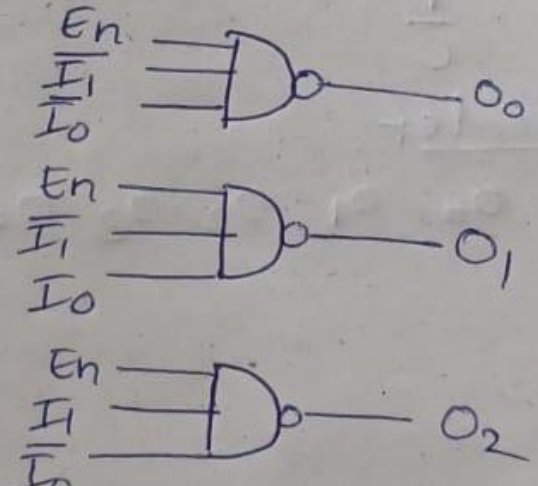
En	I_1	I_0	O_0	O_1	O_2	O_3
0	x	x	1	1	1	1
1	0	0	0	1	1	1
1	0	1	1	0	1	1
1	1	0	1	1	0	1
1	1	1	1	1	1	0

From the truth table above, we can write the following logic equations,

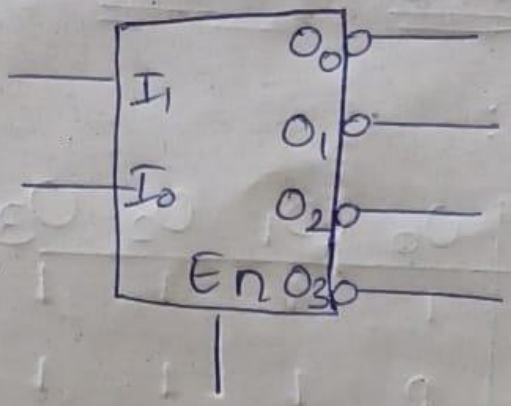
$O_0 = \overline{(En \cdot \bar{I}_1 \cdot \bar{I}_0)}$ $\quad O_2 = \overline{(En \cdot I_1 \cdot \bar{I}_0)}$

$O_1 = \overline{(En \cdot \bar{I}_1 \cdot I_0)}$ $\quad O_3 = \overline{(En \cdot I_1 \cdot I_0)}$

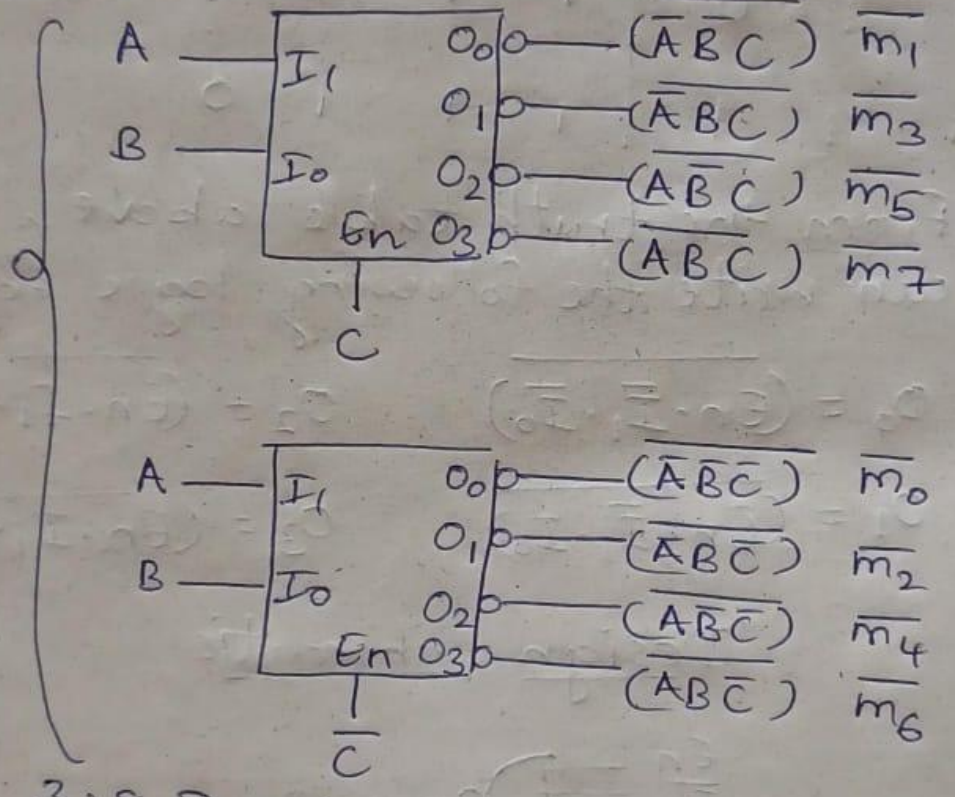
Design Schematic



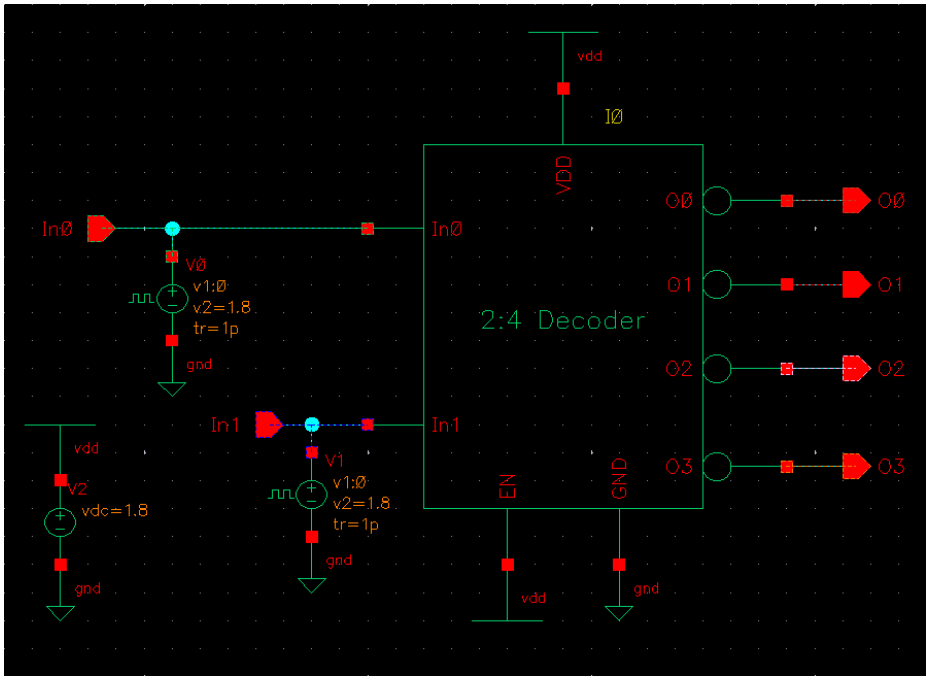
Symbol



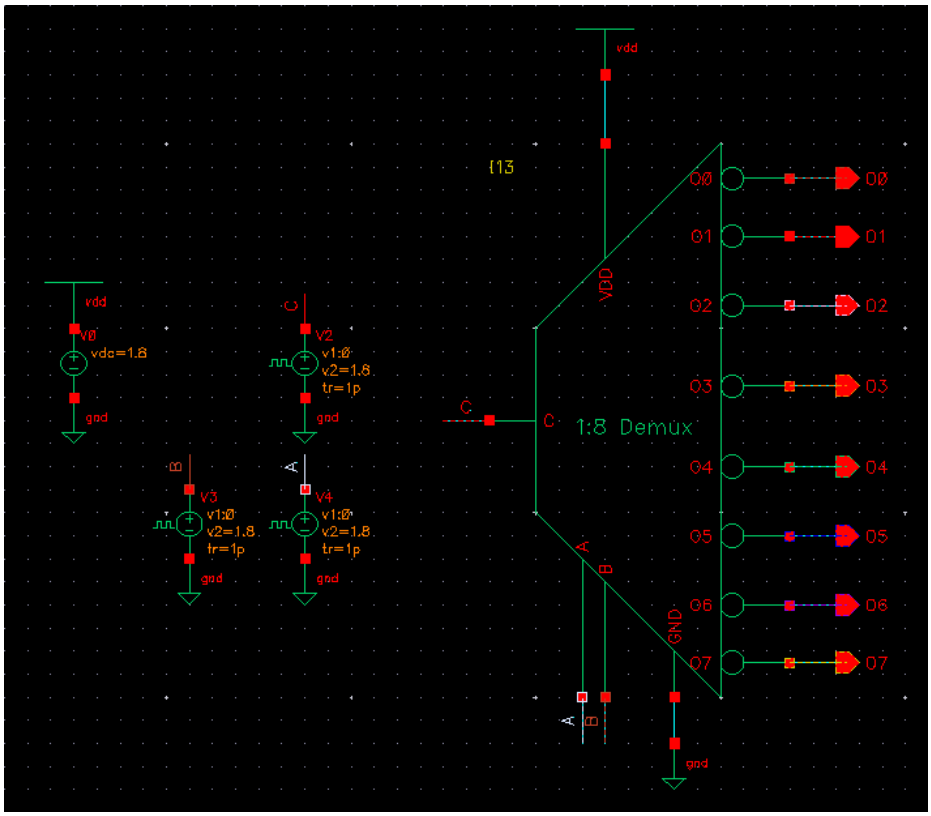
② 1:8 Demux -



3:8 Decoder.

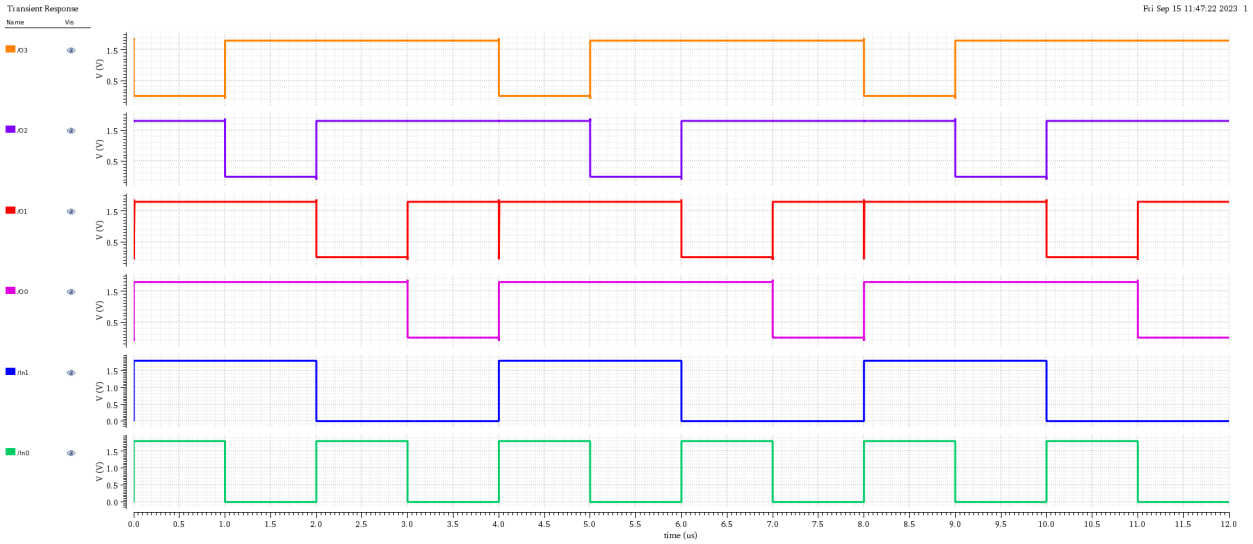


Demux:-

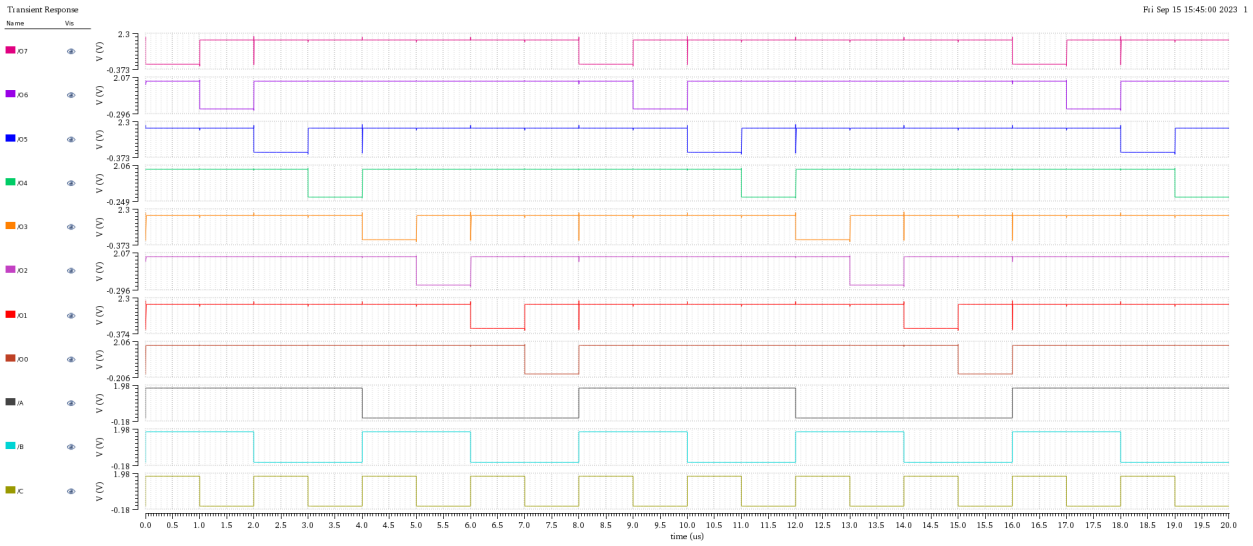


Waveforms:

Decoder:-



Demux:-



<u>Conclusion</u>:

In this experiment, we learnt how to design a 2:4 decoder using logic gates constructed in the previous experiment. Later by using the same decoder instance we designed a 1:8 demux in Cadence and simulated it for functional verification.