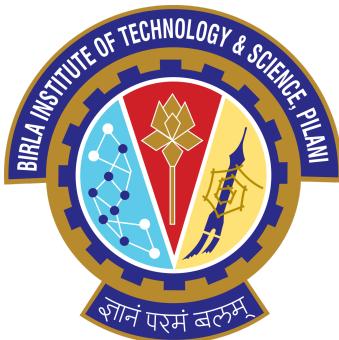


# Cadence Virtuoso Tutorial



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**MEL G621 - VLSI DESIGN**

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## 1. Basics

### Introduction

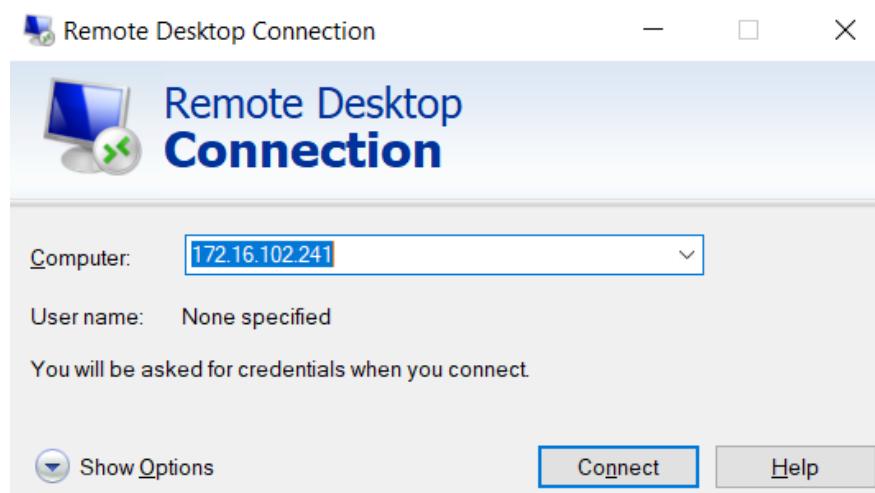
This manual introduces the basic steps in setting up the Cadence Virtuoso environment. It also explains the detailed process of creating a schematic, running a simulation, and measuring the performance metrics. Throughout the DC simulation, an NMOS transistor is used as a reference circuit. For transient simulation, an inverter is used as a reference circuit. This course makes use of a 180nm technology node.

### Server Login

**Step 1:** Click the Start menu on the desktop, and open Remote Desktop Connection.

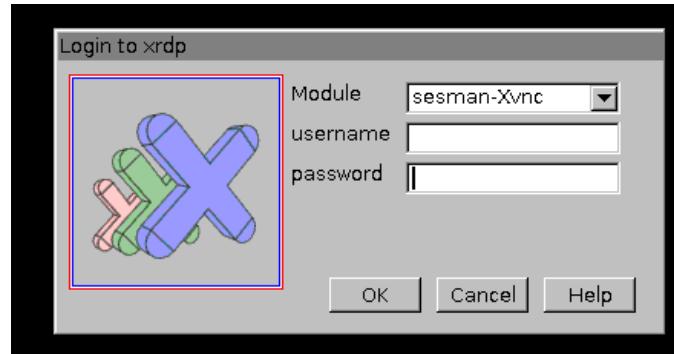
**Step 2:** Choose any one server node from the following and click Connect (Figure 1).

- 172.16.102.241
- 172.16.102.242
- 172.16.102.243
- 172.16.102.247
- 172.16.102.250



**Figure 1. Server Login**

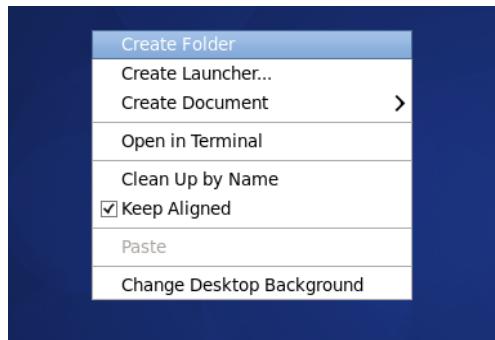
**Step 3:** Enter the group login credentials, i.e. username and password (Figure 2).



**Figure 2. Group Credentials**

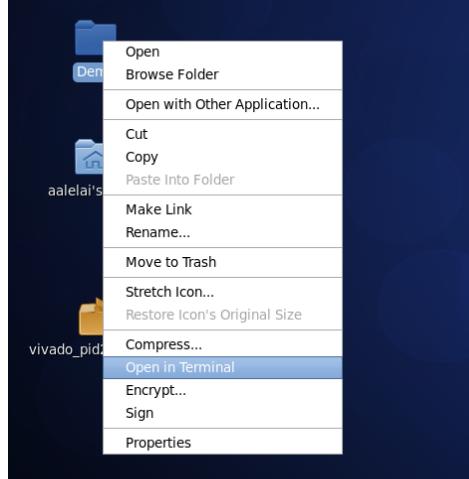
### Cadence Setup

**Step 1:** Right-click anywhere on the screen and create a new folder on the Linux desktop (Figure 3). The folder name must not contain any empty spaces.



**Figure 3. Folder Creation**

**Step 2:** Right-click on the created folder and select Open in Terminal



**Figure 4. Terminal Window**

**Step 3:** Type pwd for checking whether the working directory is correct. The directory path should appear as follows;

**/home/username/Desktop/Folder name**

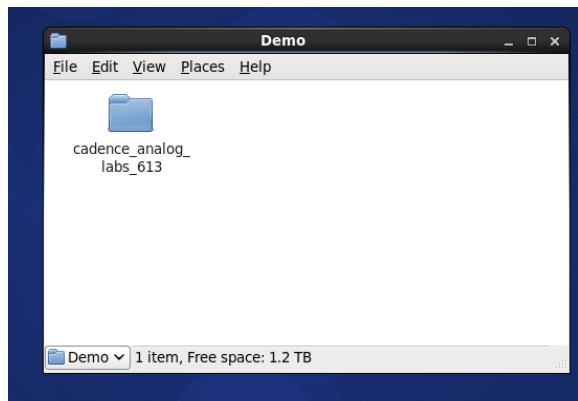
Ex: /home/Group1/Desktop/VLSILAB

**Step 4:** After checking the directory, the following command needs to be typed for installing the analog library folder into your own folder.

**scp -r /eesoft/tool\_library/cadence\_analog\_labs\_613 /directory path**

Ex: scp -r /eesoft/tool\_library/cadence\_analog\_labs\_613 /home/Group1/Desktop/VLSILAB

**Step 5:** If the analog library is properly installed, a folder named “cadence\_analog\_labs\_613” will be available inside the initially created folder (Figure 5).



**Figure 5. Analog Library Installation**

**Step 6:** After 2-3 minutes, close the terminal window

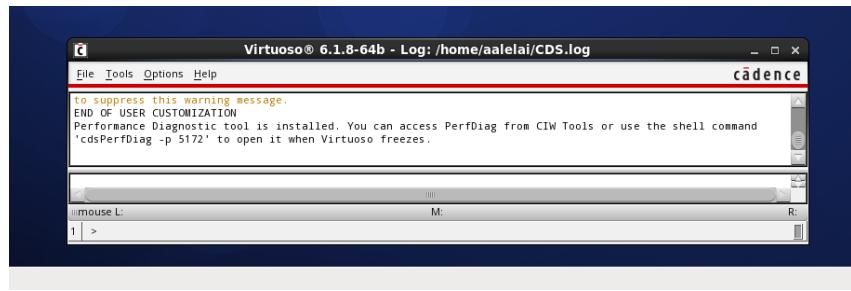
## **2. Schematic Design**

### *Library Creation*

**Step 1:** Right-click on the cadence\_analog\_labs\_613 folder and select Open in Terminal.

**Step 2:** In the terminal window, type the following command and a log window will be opened at the bottom of the screen (Figure 6).

**virtuoso &**

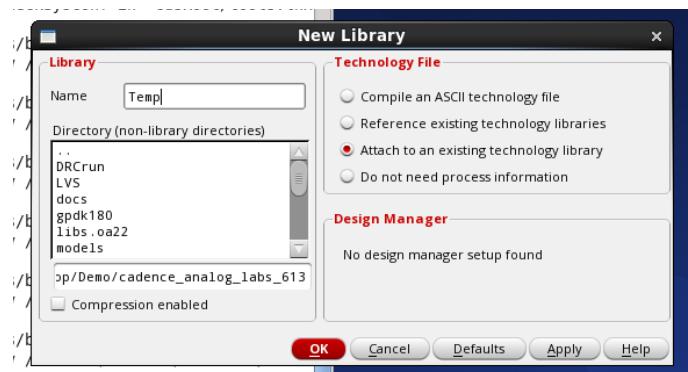


**Figure 6. Cadence Virtuoso Log Window**

**Step 3:** From the log window, Open File→New→Library

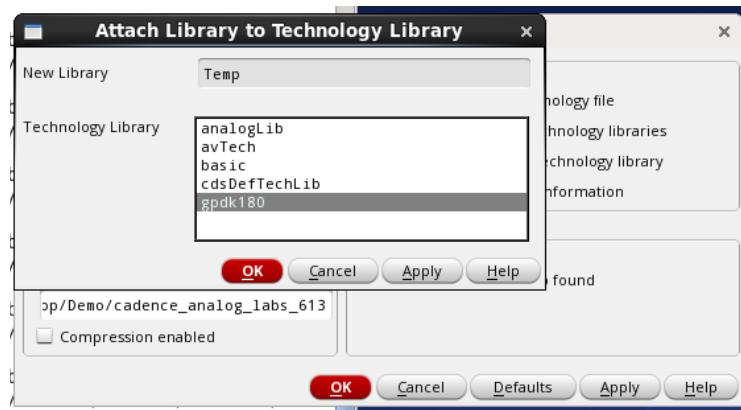
**Step 4:** Provide any library name

**Step 5:** Under Technology File, choose Attach to an existing technology library (Figure 7) and click OK.



**Figure 7. Library Creation**

**Step 6:** In the next dialog box, select gpdk180 (Figure 8) and click OK.

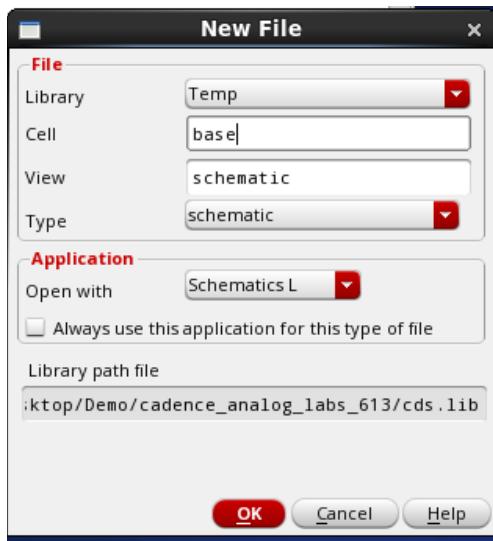


**Figure 8. GPDK Selection**

## Cellview Creation

**Step 1:** From the log window, Open File→New→Cellview

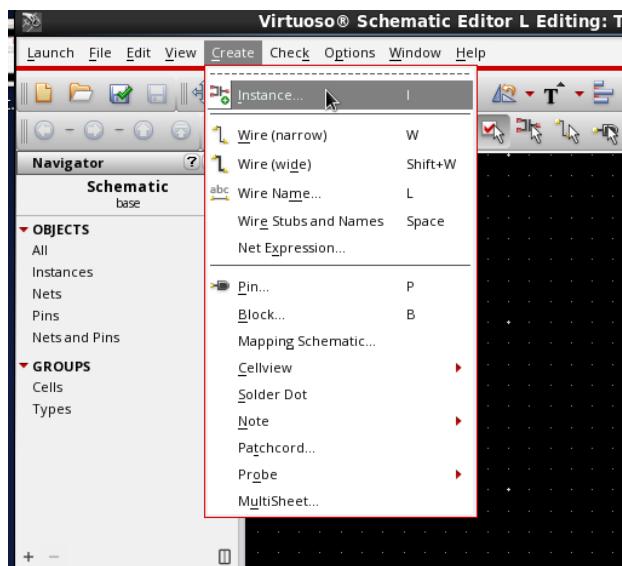
**Step 2:** In the New File dialog box, select the library, which has been created earlier and provide any cellview name (Figure 9), and click OK.



**Figure 9. Cellview Creation**

## Schematic Creation

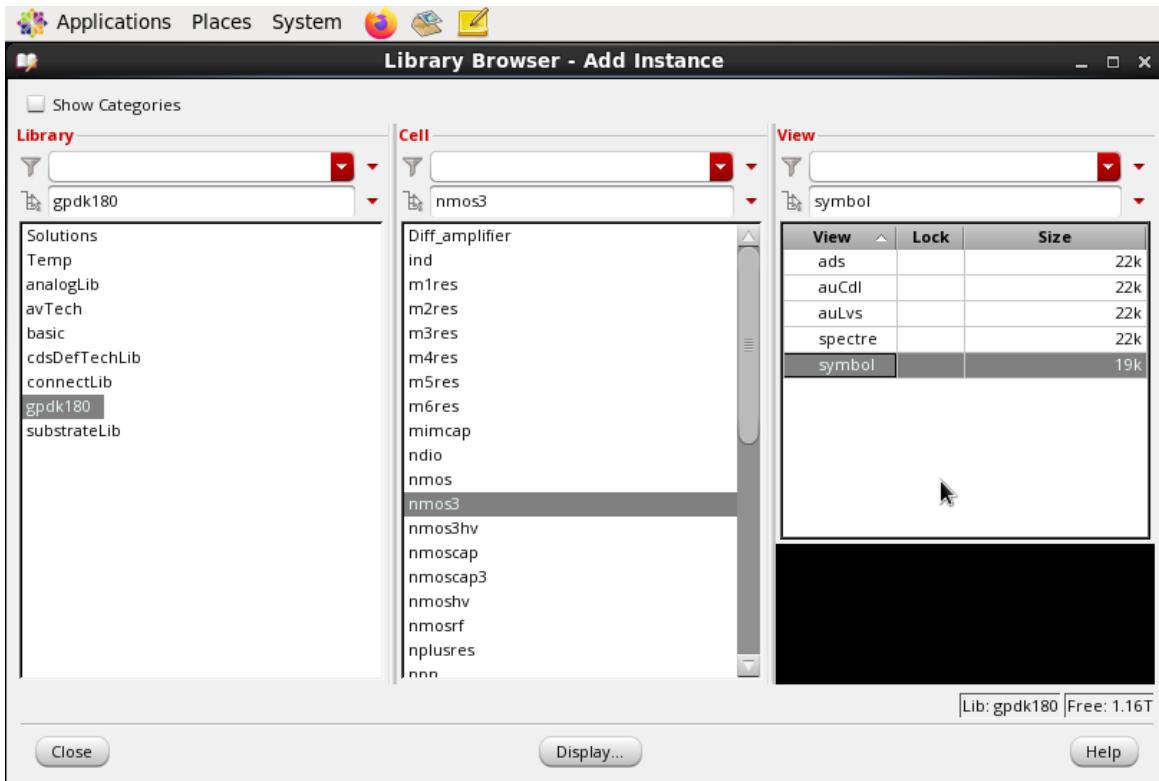
**Step 1:** Click Create→Instance from the toolbar menu (Figure 10).



**Figure 10. Instance Creation**

**Step 2:** For creating NMOS and PMOS symbols, choose gpdk180 in the library, and for other components like power supply, ground, etc. choose analogLib in the library.

**Step 3:** For selecting the NMOS symbol, select gpdk180 in the library, nmos3 in the cell column, and symbol in the view column (Figure 11).



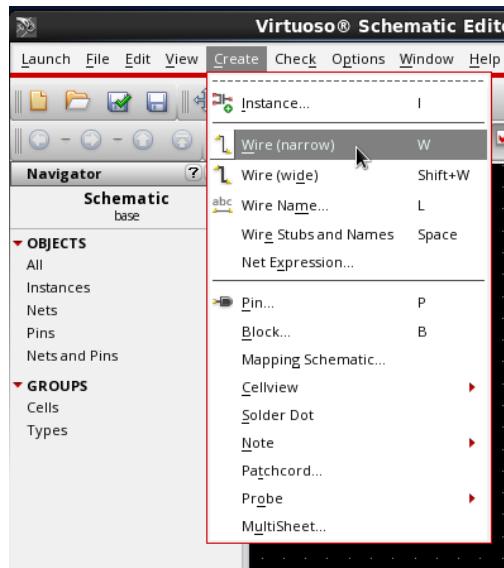
**Figure 11. NMOS Symbol Creation**

**Step 4:** Hover the mouse pointer over the schematic editor and place the NMOS.

**Step 5:** For selecting the input sources (vpulse, vdc), select analogLib in the library, vdc/vpulse in the cell column, and spectre in the view column.

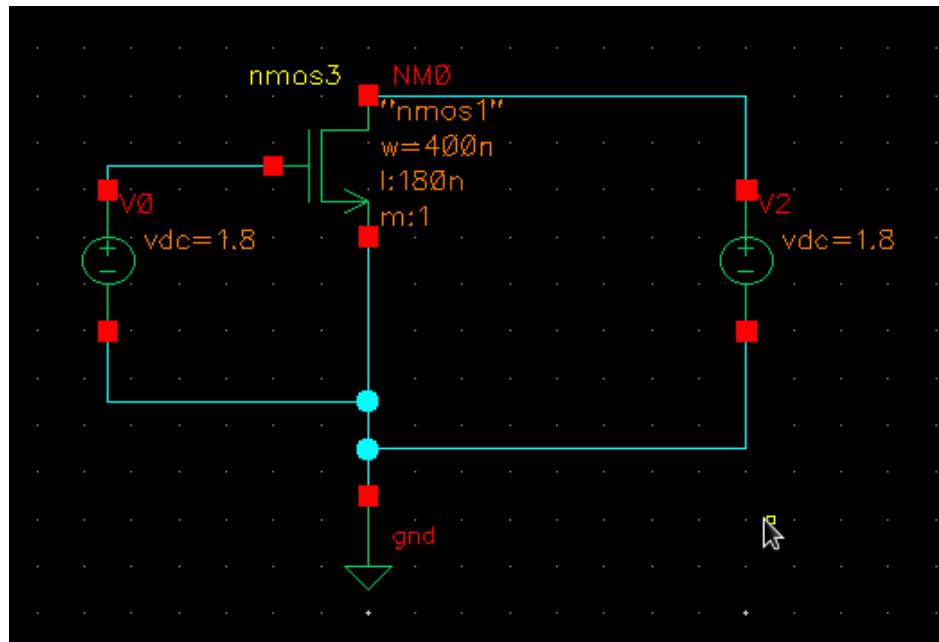
**Step 6:** Place the remaining components required for building the schematic.

**Step 7:** Use a narrow wire for connecting the components (Figure 12).



**Figure 12. Wire Creation**

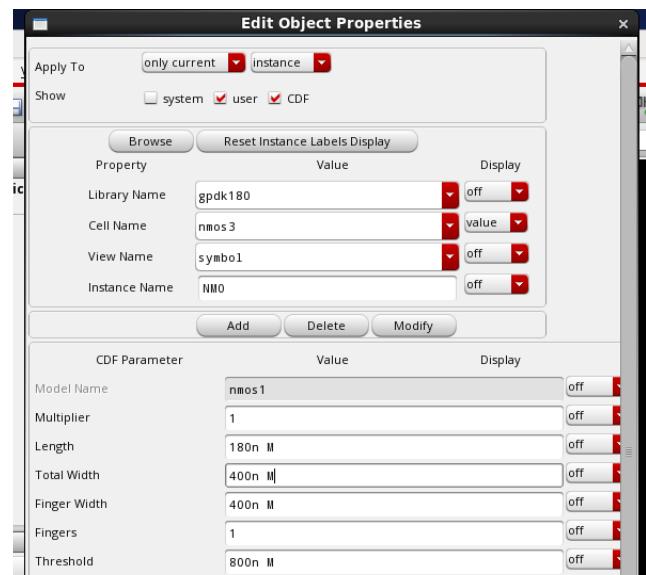
**Step 8:** Complete the remaining circuit connections (Figure 13).



**Figure 13. NMOS DC Analysis Circuit**

**Step 9:** Click on the NMOS symbol and press Q for displaying its properties.

**Step 10:** In the properties dialog box, change NMOS width to 400nm and click OK (Figure 14).



**Figure 14.** NMOS Properties Dialog Box

**Step 11:** Similarly for the voltage sources, define their voltage values by clicking on these sources, pressing Q, and providing 1.8 V in DC voltage value.

**Step 12:** Click Check and Save (Figure 15). Ensure that there are no errors and warnings.

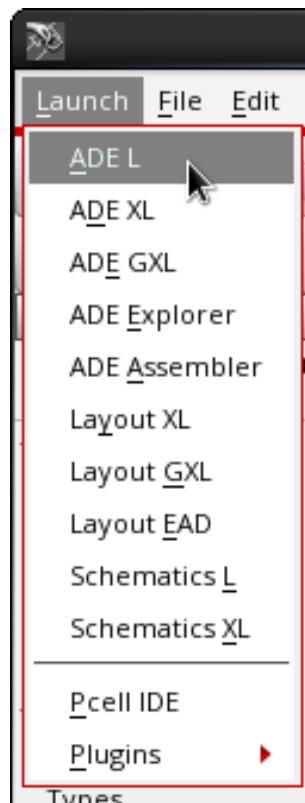


**Figure 15.** Check and Save Option

### **3. Running Spectre Simulation (DC Analysis)**

#### **Launching ADE**

**Step 1:** Once the schematic is constructed, we need to simulate them. Click Launch→ADE L (Figure 16).



**Figure 16. ADE Launch**

#### **Choosing Analysis**

**Step 1:** Initially, the DC analysis is performed. Click Analysis→Choose.

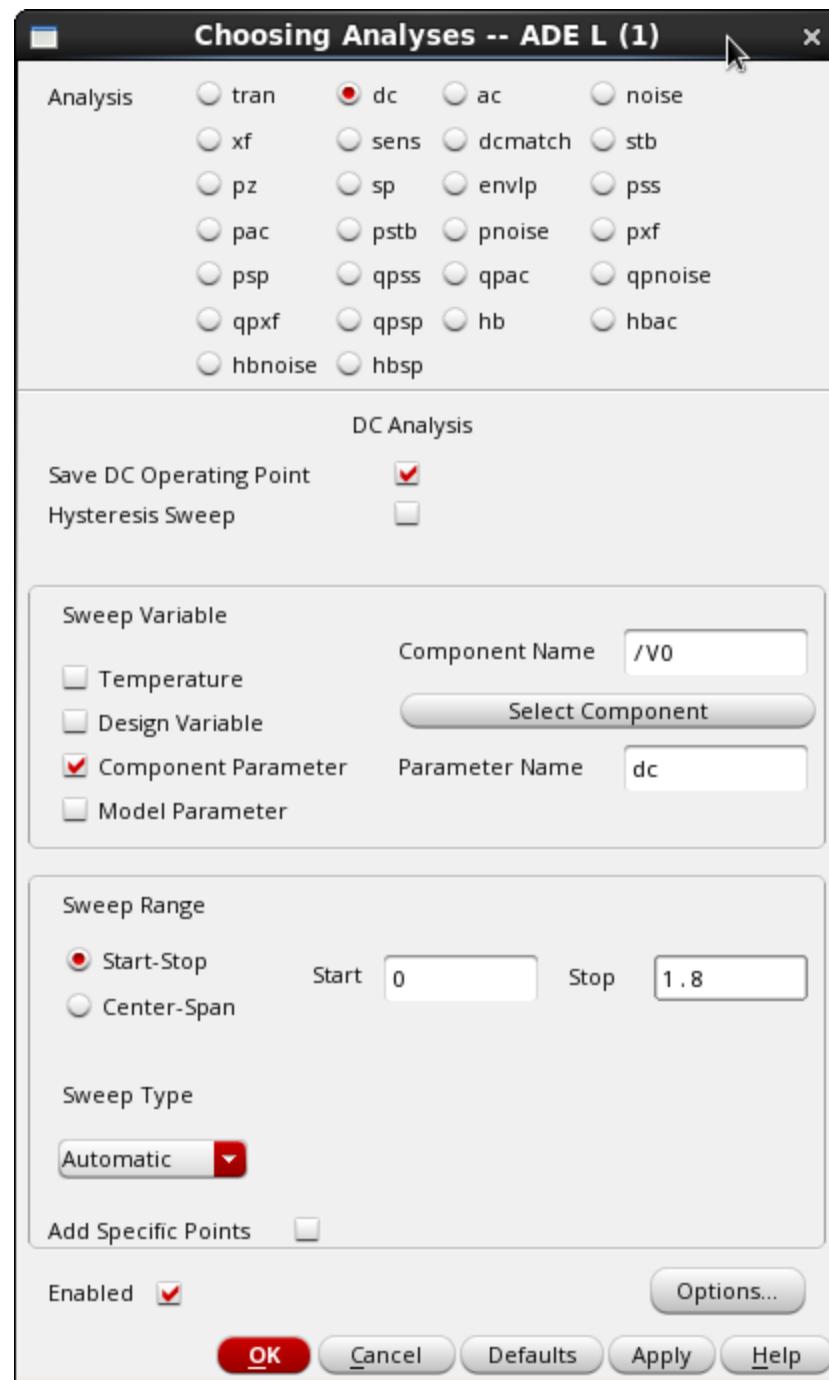
**Step 2:** In the Analysis dialog box, choose dc. Select the Save DC Operating Point.

**Step 3:** Under Sweep Variable, select Component Parameter.

**Step 4:** Click Select Component and click V<sub>GS</sub> voltage source in the schematic.

**Step 5:** Select DC voltage and click OK.

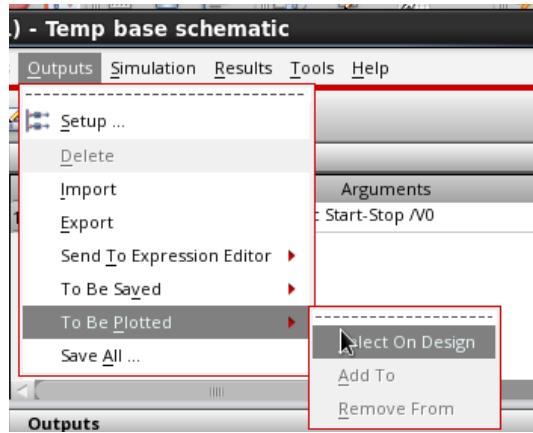
**Step 6:** In the sweep range, make the start value 0 and the stop value 1.8 and click OK (Figure 17).



**Figure 17. DC Analysis Settings**

### Plotting Signals

**Step 1:** After setting up the analysis, for plotting the output, click Output→To Be Plotted→Select On Design (Figure 18).



**Figure 18. Output Signals**

**Step 2:** From the schematic, choose the drain terminal of the transistor.

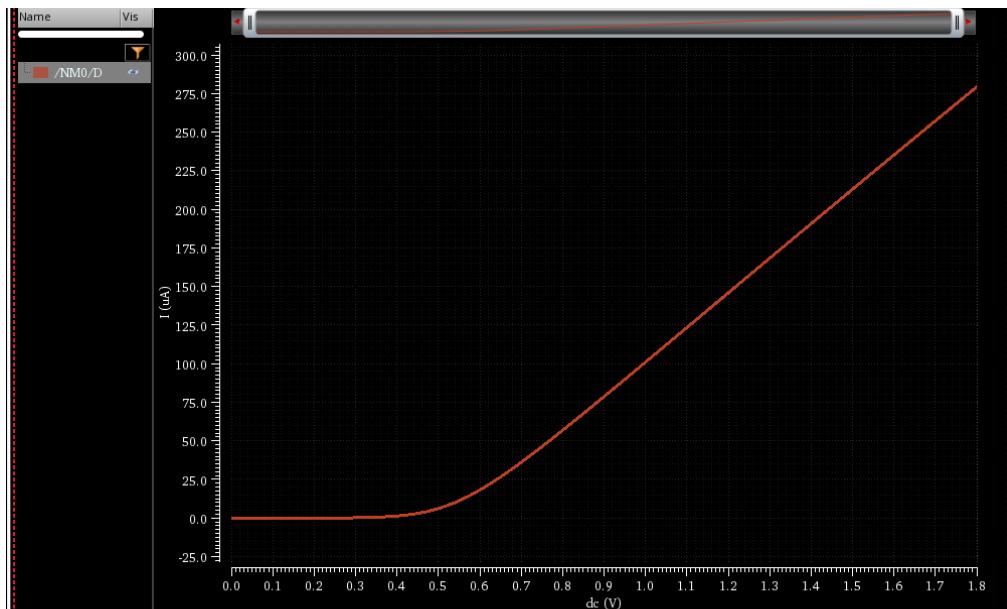
#### Running Simulation

**Step 1:** Click the Netlist and Run (Figure 19).



**Figure 19. Run Button**

**Step 2:** Upon successful simulation, we will get the following graph (Figure 20).



**Figure 20. Output Graph V<sub>GS</sub> vs I<sub>D</sub>**

## 4. Running Spectre Simulation (Transient Analysis)

### Altering Inputs

**Step 1:** For performing a transient simulation, the input must be vpulse instead of vdc.

### Choosing Analysis

**Step 1:** Click Launch→ADE L. Click Analysis→Choose.

**Step 2:** Click Analysis→Choose. In the Analysis dialog box, choose transient.

**Step 3:** Provide any value for stop time w.r.t the input signal period and click OK.

### Plotting Signals

**Step 1:** After setting up the analysis, for plotting the output, click Output→To Be Plotted→Select On Design.

**Step 2:** From the schematic, choose both the input and output nets of the inverter.

### Running Simulation

**Step 1:** Click the Netlist and Run

**Step 2:** Upon successful simulation, we will get the following graph (Figure 21).

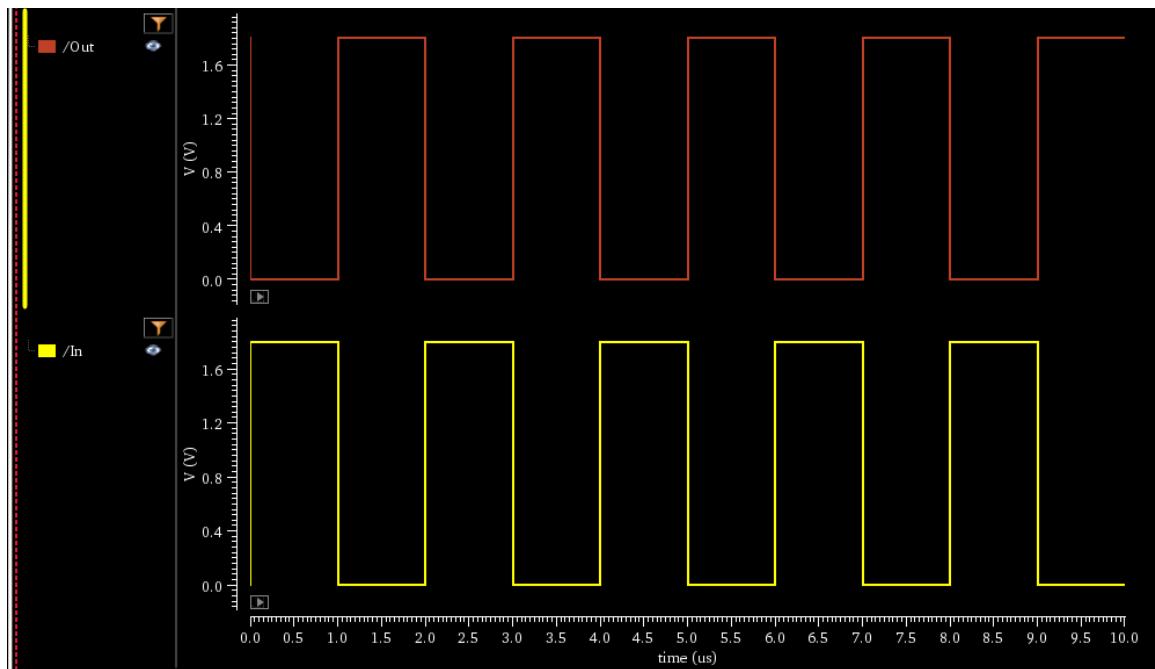


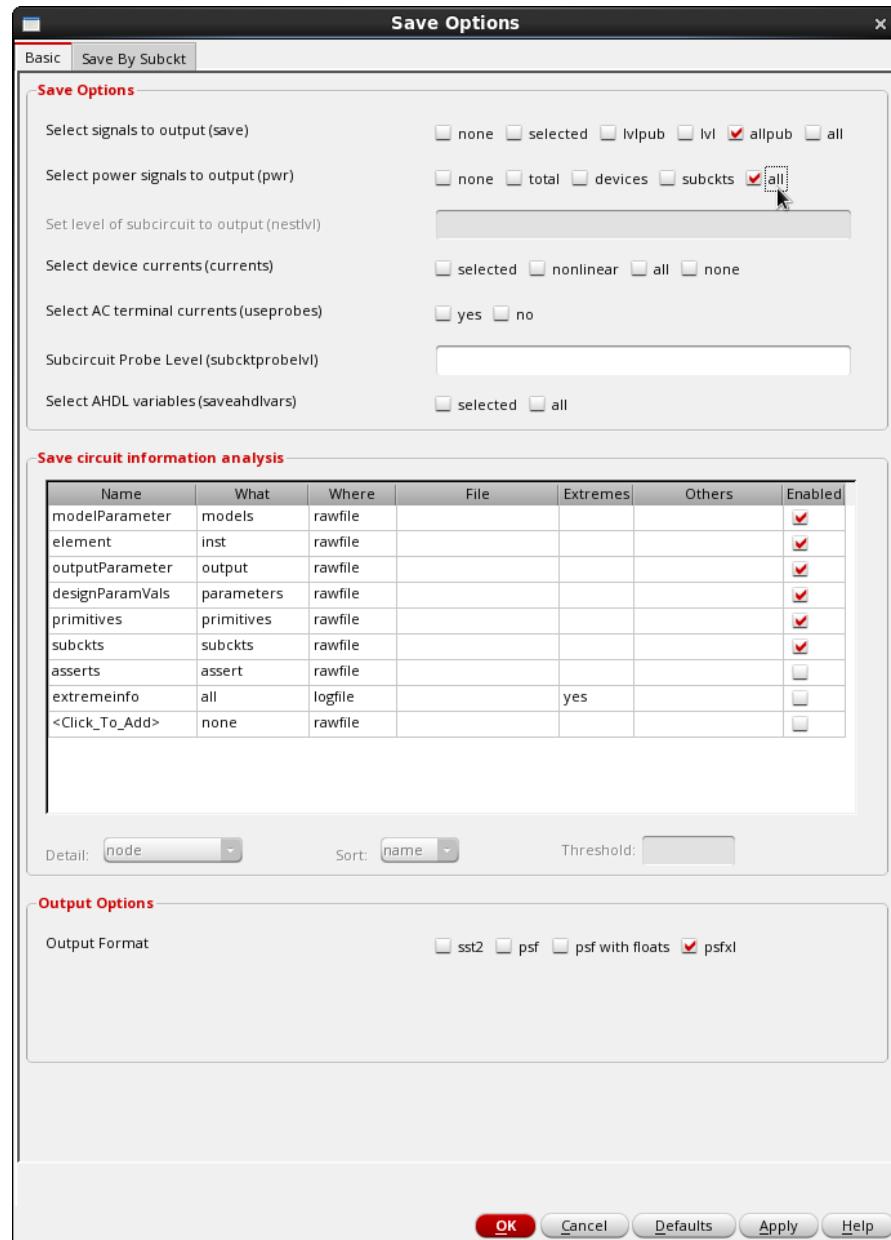
Figure 21. Output Graph for Inverter

## 5. Power Measurement

**Step 1:** Once the simulation is done and the outputs are verified, the average power dissipation can be measured.

**Step 2:** After setting the analysis, click Outputs→Save All.

**Step 3:** In the Save Options dialog box, tick the “all” button in Select power signals to output (pwr) (Figure 22) and click OK.

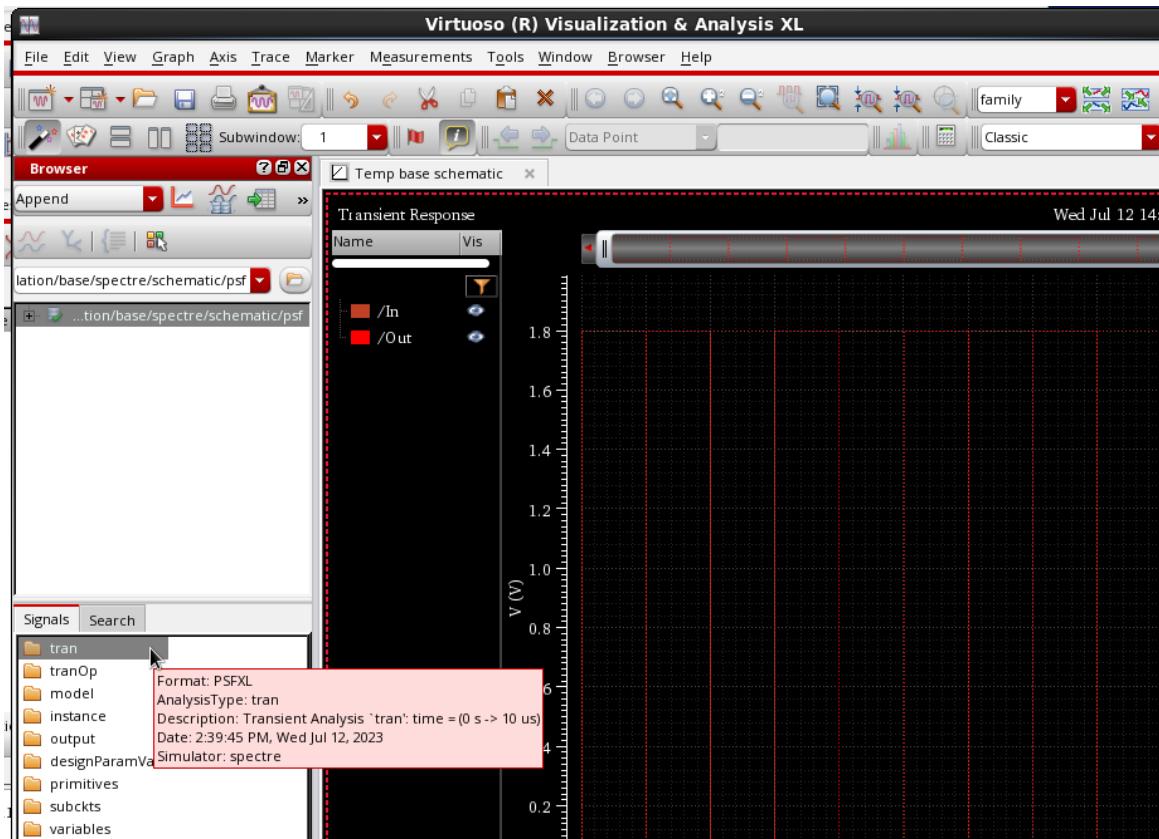


**Figure 22. Saving Power Signals**

**Step 4:** Run the simulation and obtain the waveform.

**Step 5:** Click Tools→Results Browser from the ADE window.

**Step 6:** Now check the Signals window in the waveform window and find the “tran” signal (Figure 23).

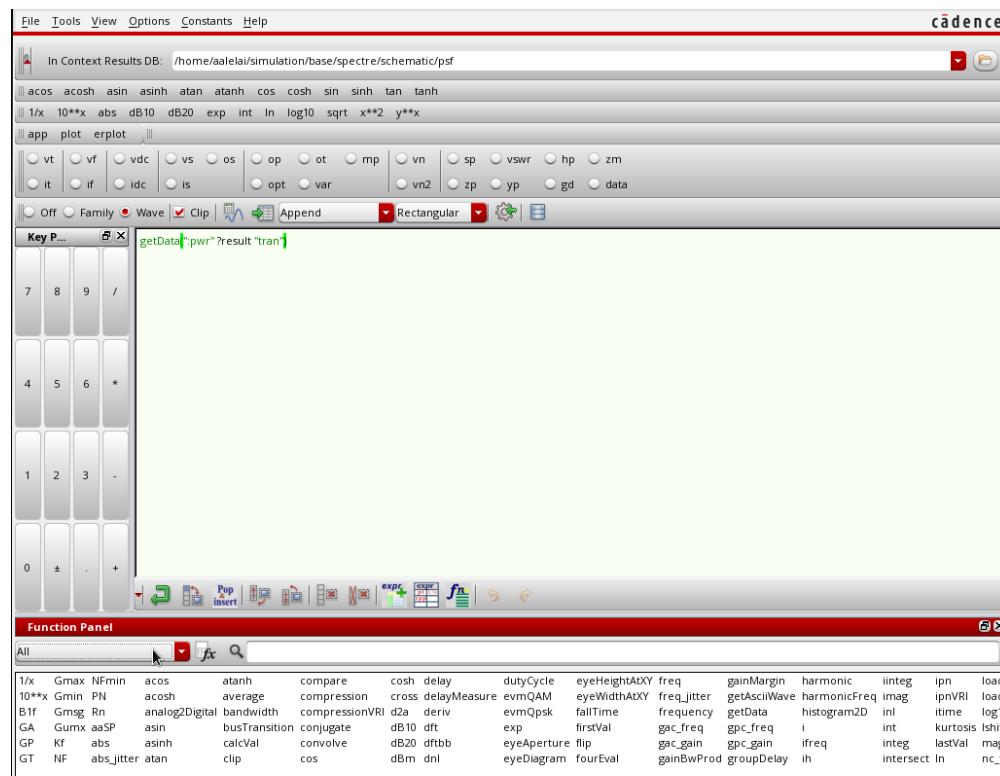


**Figure 23. Signals Window**

**Step 7:** Double-click the tran folder and find the “:pwr” signal.

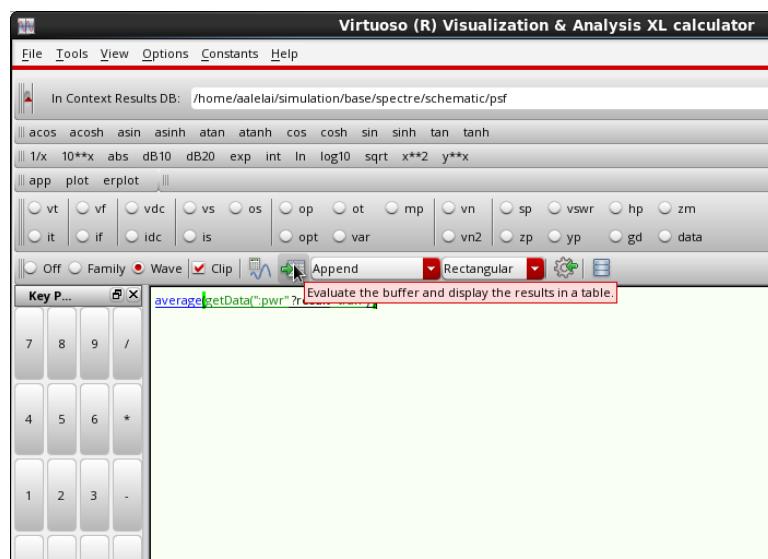
**Step 8:** Right-click on :pwr and select the Calculator option, which opens the calculator tool.

**Step 9:** Select “All” from the function panel and choose “average” from the list and click OK (Figure 24).



**Figure 24. Function Panel in Calculator**

**Step 10:** Click the “Evaluate the buffer” option to display the average power (Figure 25).

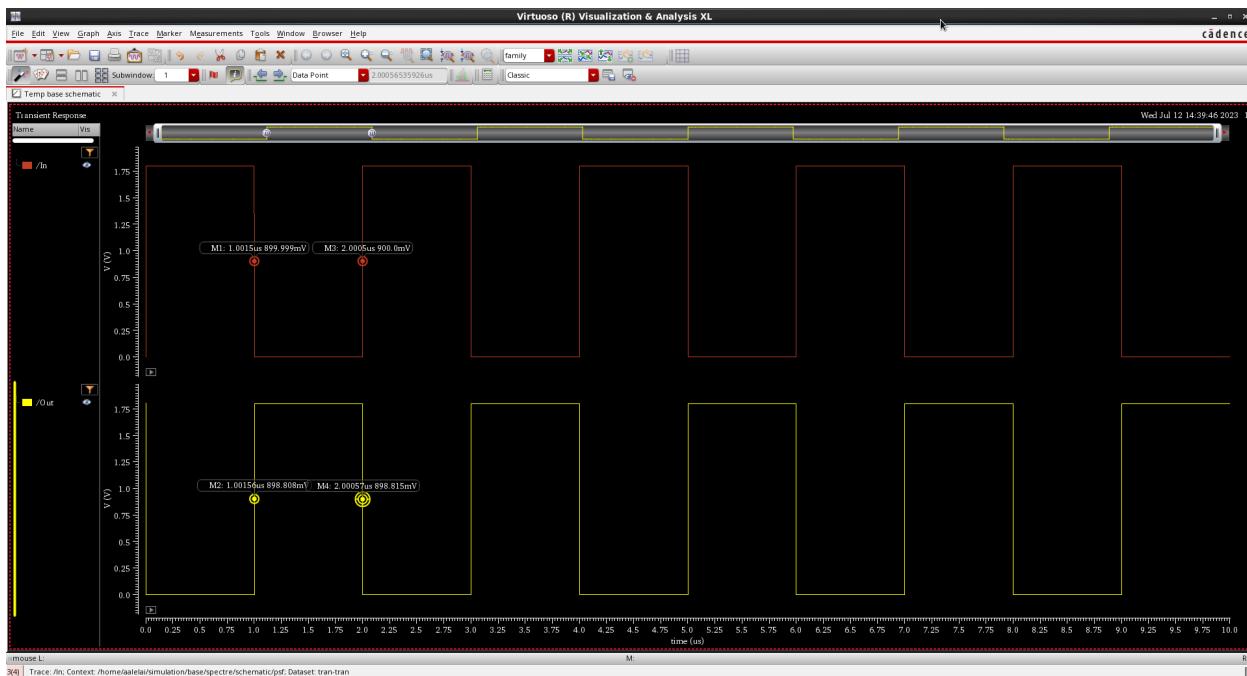


**Figure 25. Buffer Evaluation**

## 6. Delay Measurement

**Step 1:** Repeat steps 1 to 5 in the power measurement procedure.

**Step 2:** Delay is the average of tphl and tplh. For calculating tphl and tplh, mark the 50% of both input and output waveform at rising and falling transitions. For placing a marker, hover the mouse pointer over that value in the waveform and press “m”. (Figure 26).



**Figure 26. Delay Measurement**

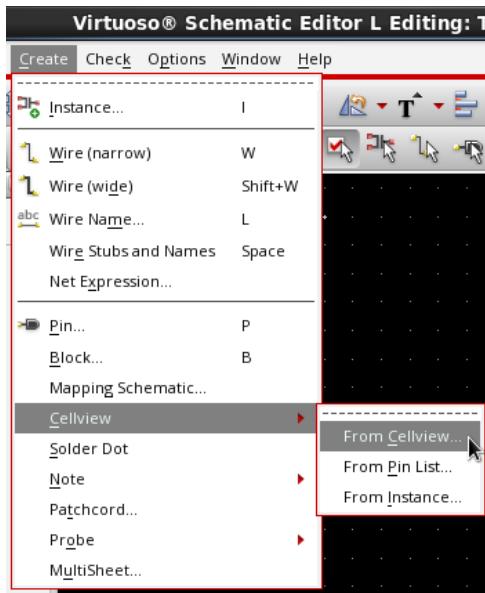
## 7. Symbol Creation

**Step 1:** Remove all the power sources such as vdc, vpulse from the schematic.

**Step 2:** Click Check and Save

**Step 3:** Click Create→Cellview→From Cellview

**Step 4:** By default, the library and cell name will be mapped correctly. If not, select the correct library and cell in which the schematic is saved and click OK (Figure 27).



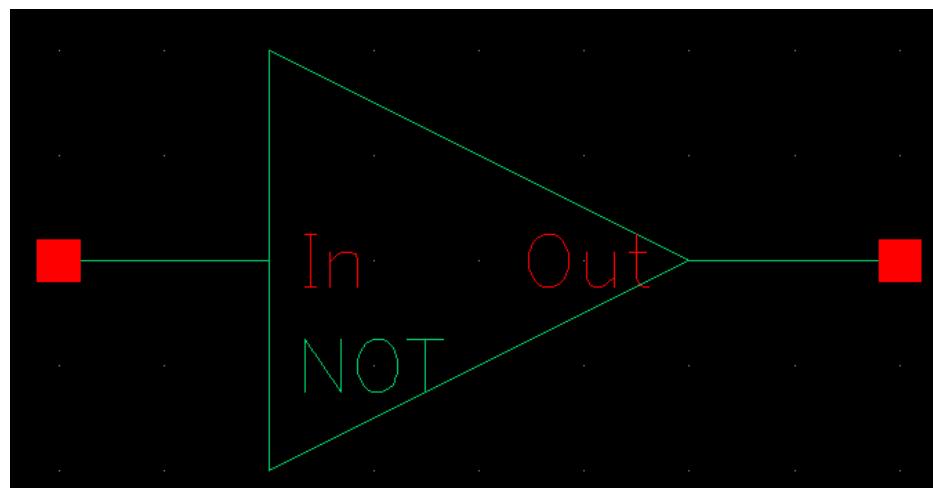
**Figure 27. Symbol Creation**

**Step 5:** Label the pins and click OK (Figure 28).



**Figure 28. Symbol Properties**

**Step 6:** The created symbol window will open, where you can rename the part name and also redraw the shape of the symbol if required (Figure 29).



**Figure 29. Inverter Symbol**

**Step 7:** Click Check and Save

## **8. Case Study - NMOS and PMOS DC Characteristics**

For explaining the entire process flow from drawing a schematic to plotting the outputs, we will take the following experiment as a case study.

- 8.1 For an NMOS, study the variation of  $I_D$  with  $V_{GS}$  by keeping  $V_{DS}$  constant. Find the value of  $V_T$  from this characteristic.
- 8.2 Repeat (8.1) for at least three values of  $V_{DS}$ .
- 8.3 Keeping  $V_{GS}$  constant, study the variation of  $I_D$  with  $V_{DS}$ .
- 8.4 Repeat (8.3) for 5 different values of  $V_{GS}$ .
- 8.5 Keeping  $V_{GS} \geq V_T$ , study the variation of  $I_D$  with the width of the transistor (at least 5 different values for width).
- 8.6 Repeat (8.1) – (8.5) for PMOS transistor.

### 8.1 NMOS - $I_D$ vs $V_{GS}$

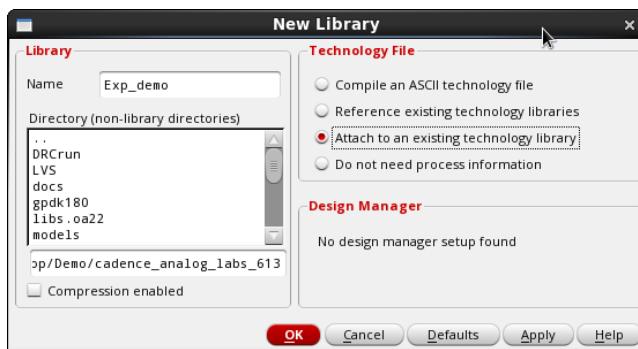
**Step 1:** Refer to Section 1 for logging into the server and setting up the Cadence environment.

**Step 2:** Right-click on the `cadence_analog_labs_613` folder and select Open in Terminal.

**Step 3:** In the terminal window, type the following command “`virtuoso &`”

**Step 4:** From the virtuoso log window, create a new library by clicking File→New→Library.

**Step 5:** We have created a library named “**Exp\_demo**”. Under Technology File, choose Attach to an existing technology library (Figure 30) and click OK.

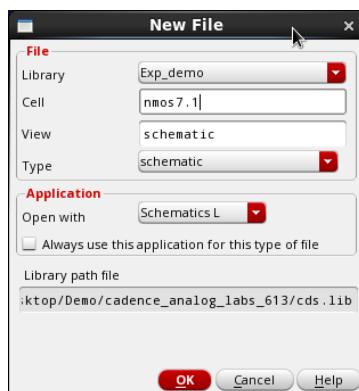


**Figure 30. New Library (**Exp\_demo**) Creation**

**Step 6:** In the next dialog box, select `gpdk180` and click OK.

**Step 7:** For creating a new cellview “**nmos7.1**”, from the log window, Open File→New→Cellview.

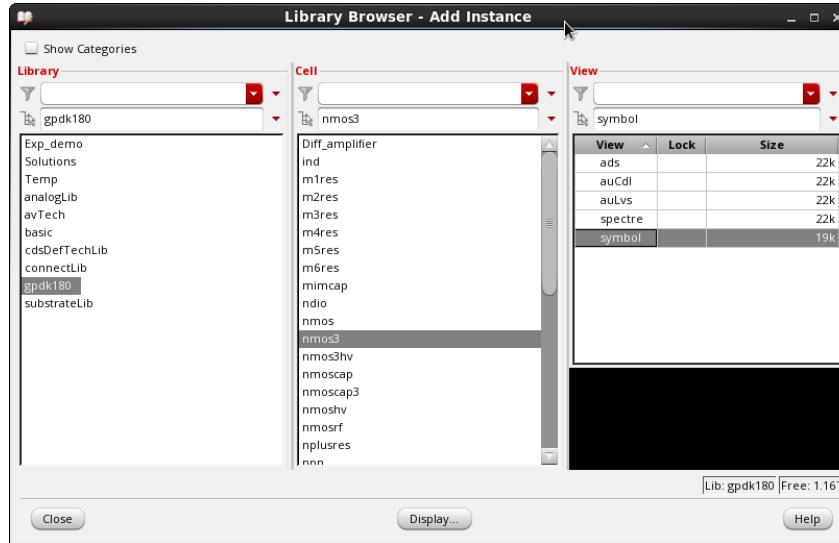
**Step 8:** In the New File dialog box, select the library, which you created earlier and provide any cellview name (Figure 31), and click OK.



**Figure 31. New Cellview (**nmos7.1**) Creation**

**Step 9:** In the schematic window, Click Create→Instance from the toolbar menu.

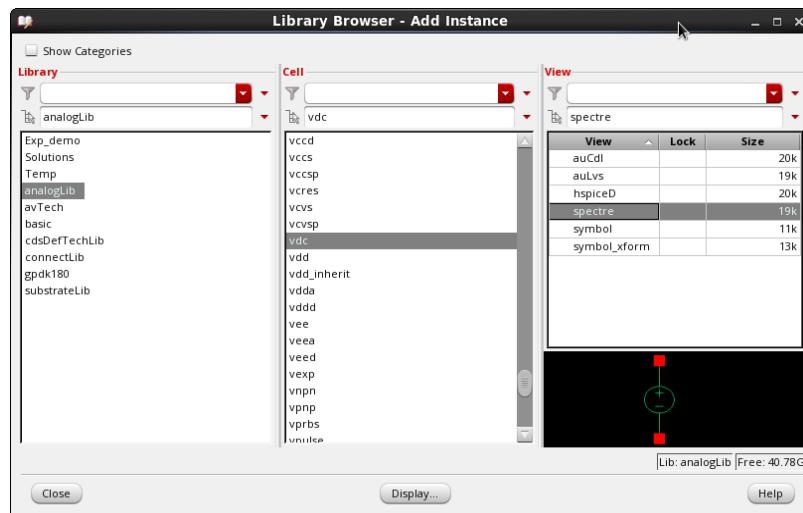
**Step 10:** For selecting the NMOS symbol, select gpdk180 in the library, nmos3 in the cell column, and symbol in the view column (Figure 32).



**Figure 32. NMOS Symbol Selection**

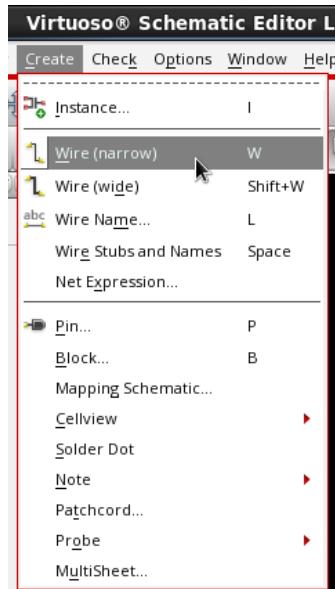
**Step 11:** Hover the mouse pointer over the schematic editor and place the NMOS.

**Step 12:** For selecting the input source vdc and ground terminal gnd, select analogLib in the library, vdc/gnd in the cell column, and spectre in the view column for vdc and symbol in the view column of gnd (Figure 33).



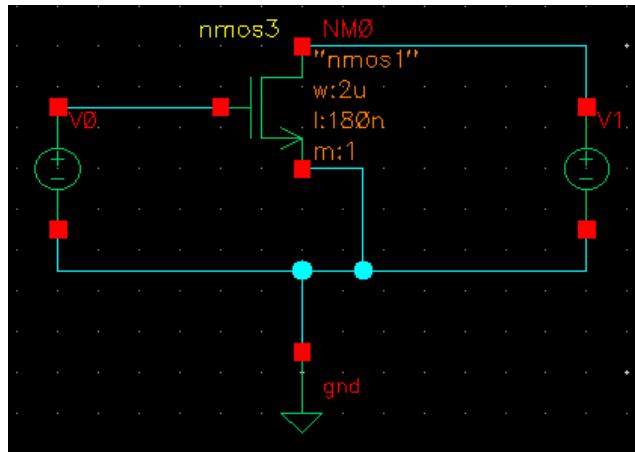
**Figure 33. VDC Symbol Selection**

**Step 13:** Use a narrow wire for connecting the components (Figure 34).



**Figure 34.** Wire Selection

**Step 14:** Complete the remaining circuit connections (Figure 35).



**Figure 35.** NMOS Final Circuit

**Step 15:** Click on the NMOS symbol and press Q for displaying its properties.

**Step 16:** In the properties dialog box, change NMOS width to 400 nm.

**Step 17:** Similarly for the voltage sources  $V_{GS}$  and  $V_{DS}$ , define their voltage values by clicking on these sources, pressing Q, and providing 1.8 in DC voltage value.

**Step 18:** Click Check and Save and ensure that there are no errors and warnings.

**Step 19:** Once the schematic is constructed, simulate them by clicking Launch→ADE L.

**Step 20:** In the ADE window, Click Analysis→Choose.

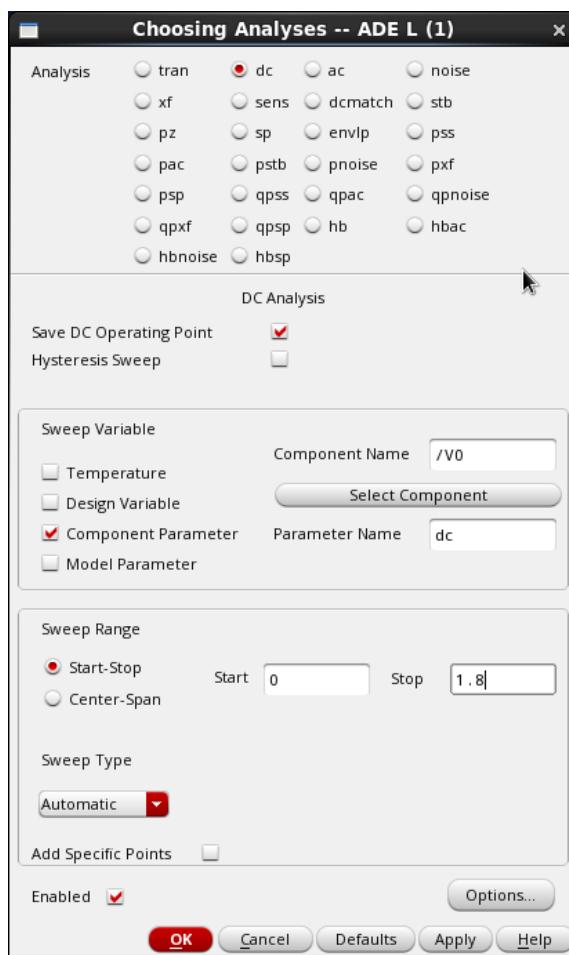
**Step 21:** In the Analysis dialog box, choose dc. Select the Save DC Operating Point.

**Step 22:** Under Sweep Variable, select Component Parameter.

**Step 23:** Click Select Component and click  $V_{GS}$  voltage source in the schematic.

**Step 24:** Select DC voltage and click OK.

**Step 25:** In the sweep range, make the start value 0 and the stop value 1.8 and click OK (Figure 36).



**Figure 36. DC Analysis Settings**

**Step 26:** After setting up the analysis, click Output→To Be Plotted→Select On Design to plot the output.

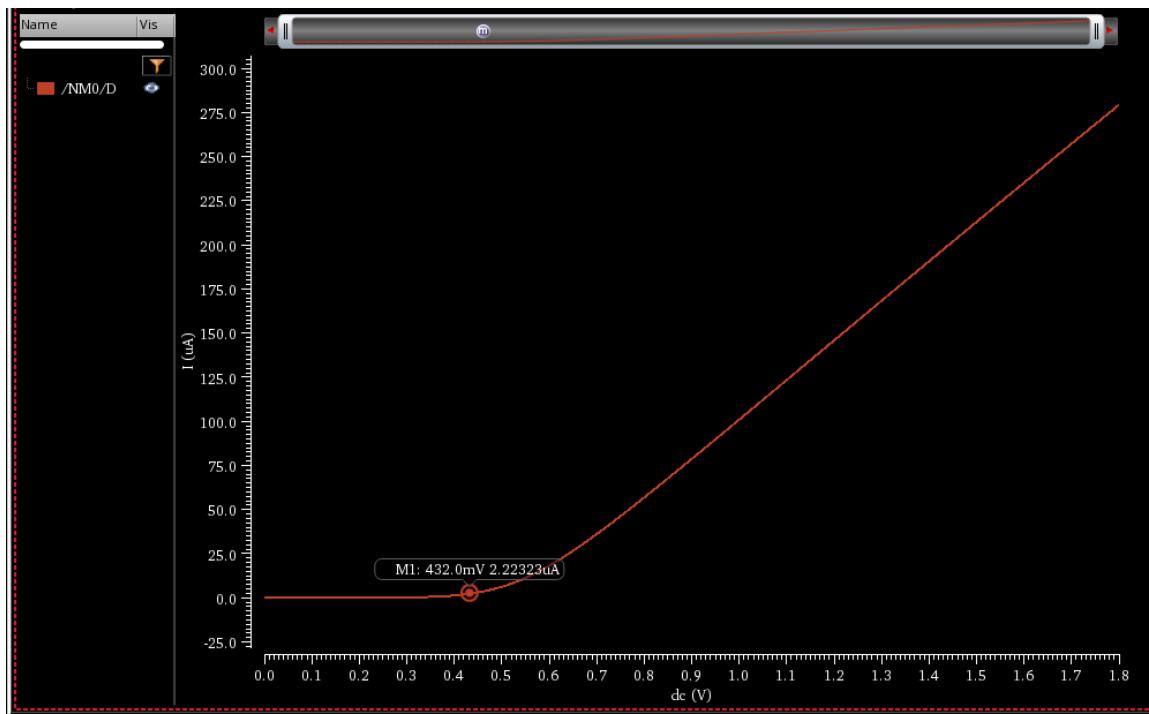
**Step 27:** From the schematic, choose the drain terminal of the transistor.

**Step 28:** In the ADE window, click the Netlist and Run (Figure 37).



**Figure 37. Run Simulation Button**

**Step 29:** Upon successful simulation, the following graph will be obtained (Figure 38).



**Figure 38. NMOS V<sub>GS</sub> vs I<sub>D</sub> Graph**

**Step 30:** For finding V<sub>T</sub>, place the mouse over the graph over the point where the current starts to increase from zero and use a marker (press m) to find that voltage.

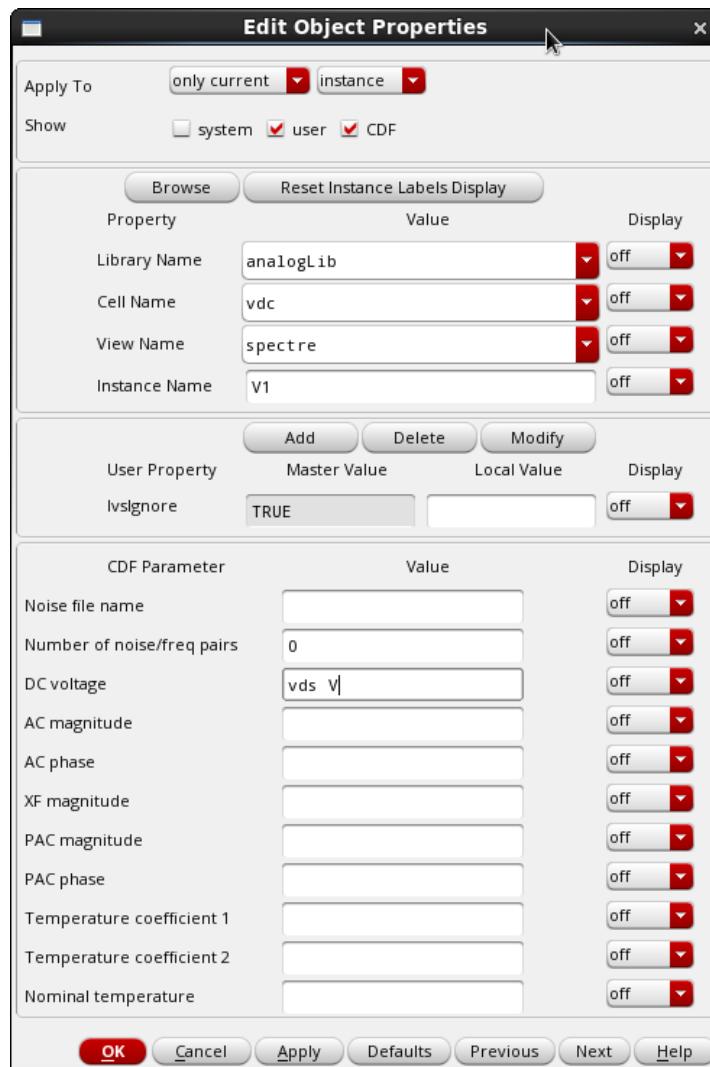
**Step 31:** By inferring the graph in Figure 38, V<sub>T</sub> is found to be 0.43 V.

## 8.2 NMOS $V_{GS}$ vs $I_D$ for variable $V_{DS}$

**Step 1:** In the same library (Exp\_demo), create a new cellview “**nmos7.2**”.

**Step 2:** Reconstruct the same circuit from 8.1 or copy the entire circuit from the previous schematic by following steps 9 to 17 in section 8.1.

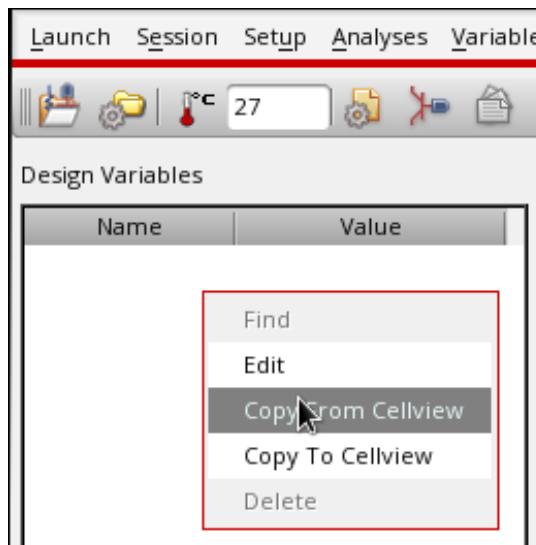
**Step 3:** Instead of giving  $V_{DS}$  as 1.8 V, keep the DC Voltage of  $V_{DS}$  as vds (Figure 39).



**Figure 39.  $V_{DS}$  as variable**

**Step 4:** Follow steps 18 to 27 in section 8.1.

**Step 5:** Inside the ADE window, find the Design Variables tab, right-click on it, and select Copy From Cellview (Figure 40).



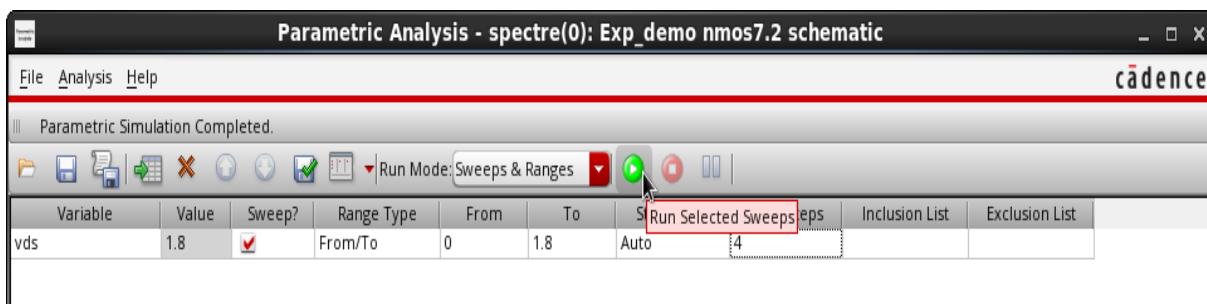
**Figure 40. Design Variables Tab**

**Step 6:** The variable vds will automatically occur in the Design Variables tab and type the vds value as 1.8.

**Step 7:** In the ADE window, click Tools→Parametric Analysis.

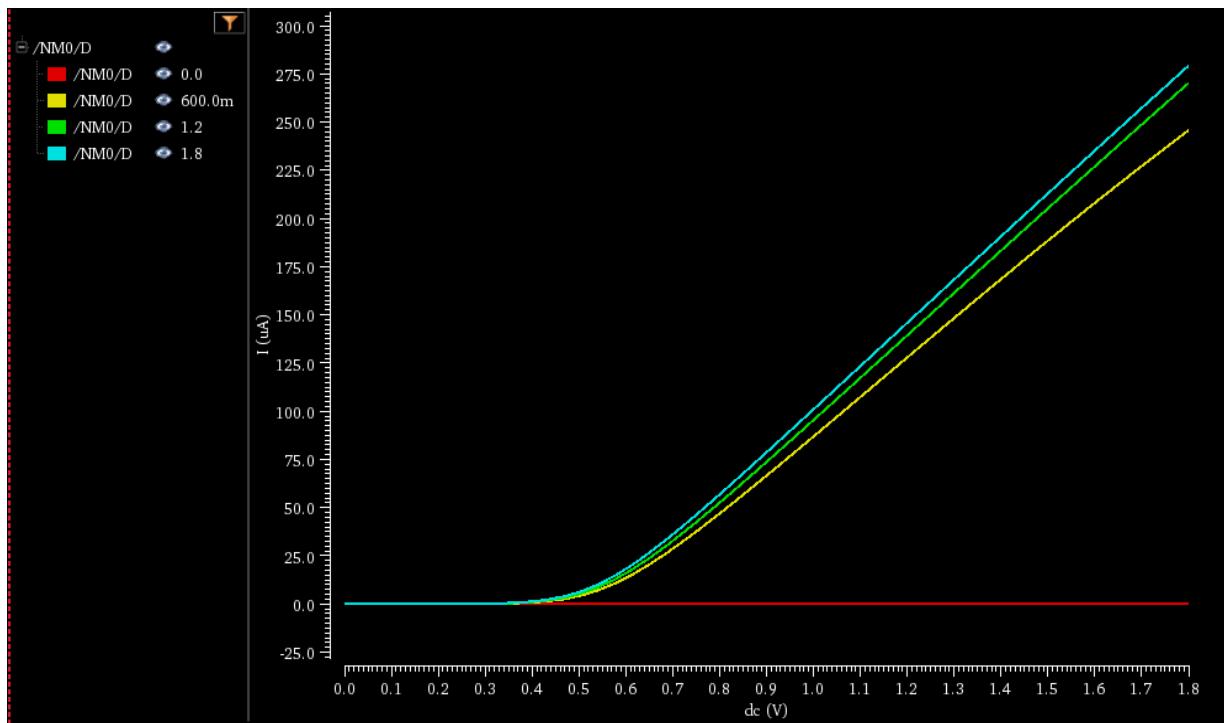
**Step 8:** In the Parametric Analysis window, in the Add Variables column, select vds, give the From and To values as 0 and 1.8 and Total Steps as 4.

**Step 9:** Click Run Selected Sweeps (Figure 41).



**Figure 41. Parametric Analysis Settings**

**Step 10:** Upon successful execution, the following graph will be obtained (Figure 42).



**Figure 42. NMOS  $V_{GS}$  vs  $I_D$  Graph for variable  $V_{DS}$**

### 8.3 NMOS $V_{DS}$ vs $I_D$

**Step 1:** In the same library (Exp\_demo), create a new cellview “**nmos7.3**”.

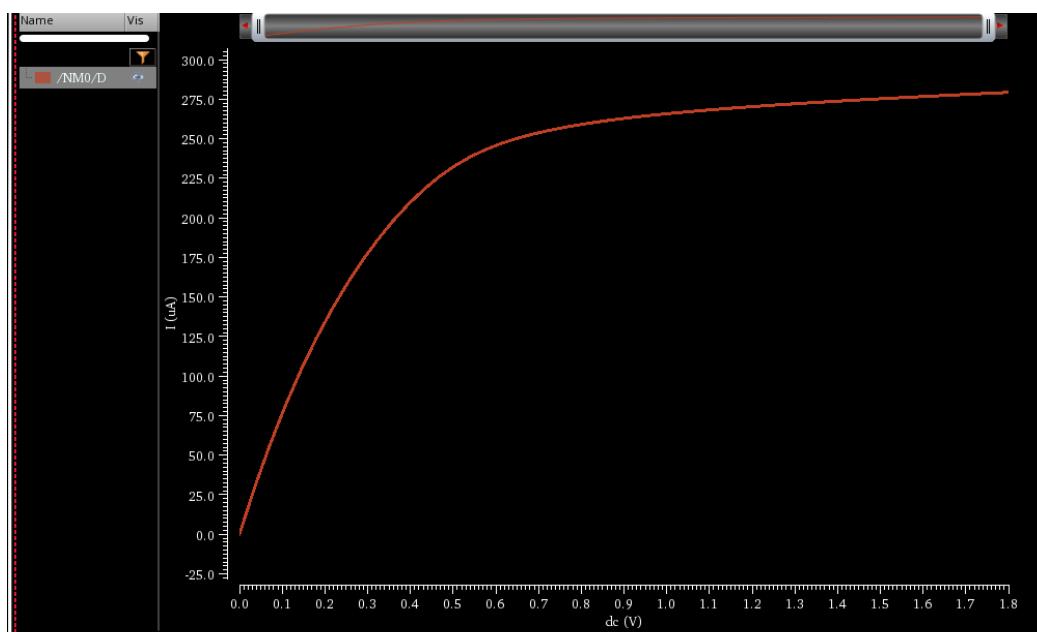
**Step 2:** Reconstruct the same circuit from 8.1 or copy the entire circuit from the previous schematic.

**Step 3:** Follow steps 9 to 22 in section 8.1.

**Step 4:** Instead of selecting  $V_{GS}$  under Select Component, now select  $V_{DS}$ .

**Step 5:** Follow steps 24 to 28 in section 8.1.

**Step 6:** Upon successful simulation, the following graph will be obtained (Figure 43).



**Figure 43. NMOS  $V_{DS}$  vs  $I_D$  Graph**

#### 8.4 NMOS $V_{DS}$ vs $I_D$ for variable $V_{GS}$

**Step 1:** In the same library (Exp\_demo), create a new cellview “**nmos7.4**”.

**Step 2:** Reconstruct the same circuit from 8.1 or copy the entire circuit from the previous schematic by following steps 9 to 17 in section 8.1.

**Step 3:** Instead of giving  $V_{GS}$  as 1.8 V, keep the DC Voltage of  $V_{GS}$  as vgs.

**Step 4:** Follow steps 18 to 22 in section 8.1.

**Step 5:** Instead of selecting  $V_{GS}$  under Select Component, now select  $V_{DS}$ .

**Step 6:** Follow steps 24 to 27 in section 8.1.

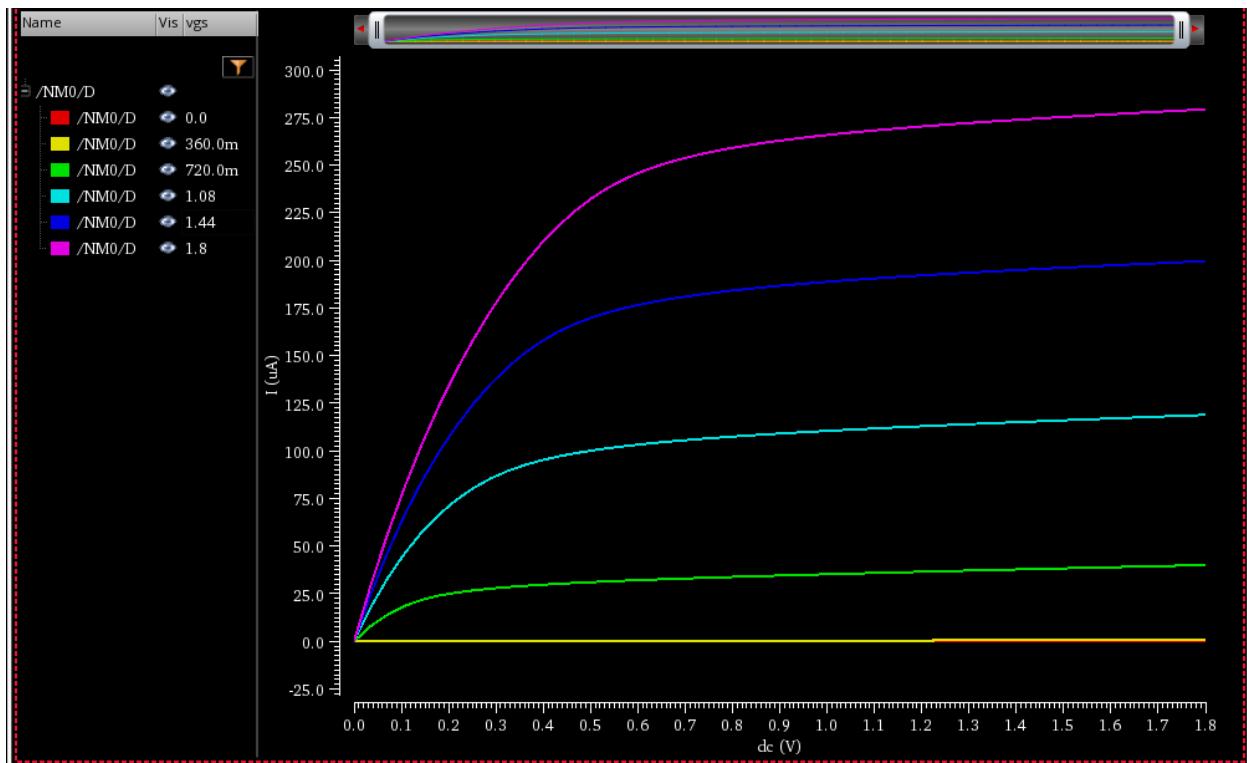
**Step 7:** Inside the ADE window, find the Design Variables tab, right-click on it, and select Copy From Cellview.

**Step 8:** The variable vgs will automatically occur in the Design Variables tab and type the vgs value as 1.8.

**Step 9:** In the ADE window, click Tools→Parametric Analysis.

**Step 10:** In the Parametric Analysis window, in the Add Variables column, select vgs, give the From and To values as 0 and 1.8 and Total Steps as 6.

**Step 11:** Click Run Selected Sweeps and the following graph will be obtained (Figure 44).



**Figure 44. NMOS  $V_{DS}$  vs  $I_D$  Graph for variable  $V_{GS}$**

### 8.5 NMOS Width vs $I_D$

**Step 1:** In the same library (Exp\_demo), create a new cellview “**nmos7.5**”.

**Step 2:** Reconstruct the same circuit from 8.1 or copy the entire circuit from the previous schematic.

**Step 3:** Follow steps 9 to 15 in section 8.1.

**Step 4:** Instead of giving the width as 400 nm, keep the width as w.

**Step 5:** Follow steps 17 to 27 in section 8.1

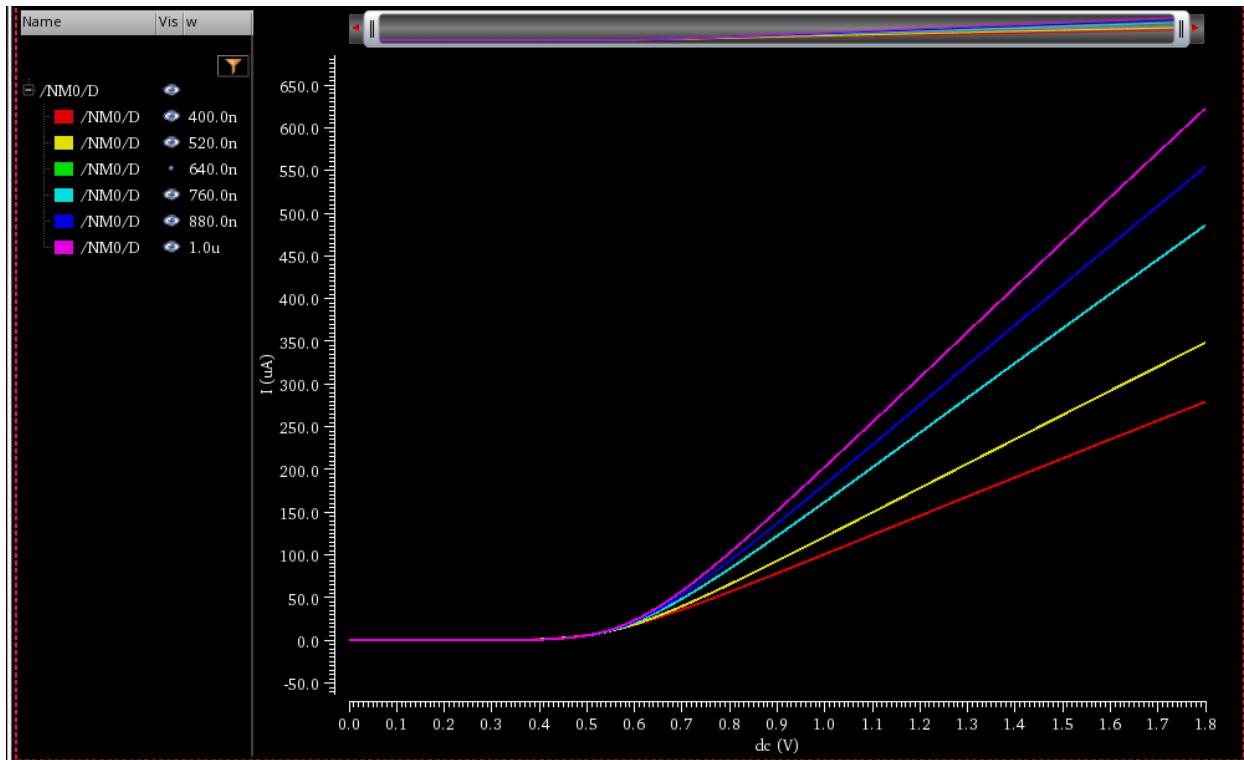
**Step 6:** Inside the ADE window, find the Design Variables tab, right-click on it, and select Copy From Cellview.

**Step 7:** The variable w will automatically occur in the Design Variables tab and type the w value as 1u.

**Step 8:** In the ADE window, click Tools→Parametric Analysis.

**Step 9:** In the Parametric Analysis window, in the Add Variables column, select w, give the From and To values as 400n and 1u and Total Steps as 6.

**Step 10:** Click Run Selected Sweeps and the following graph will be obtained (Figure 45).



**Figure 45. NMOS Width vd  $I_D$**

### 8.6.1 PMOS $V_{GS}$ vs $I_D$

**Step 1:** In the same library (Exp\_demo), create a new cellview “**pmos7.1**”.

**Step 2:** In the schematic window, Click Create→Instance from the toolbar menu.

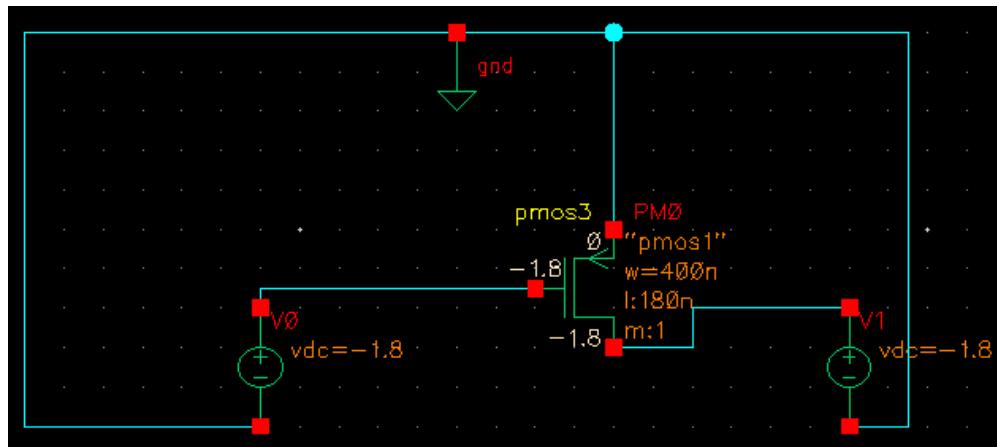
**Step 3:** For selecting the PMOS symbol, select gpdk180 in the library, pmos3 in the cell column, and symbol in the view column.

**Step 4:** Hover the mouse pointer over the schematic editor and place the PMOS.

**Step 5:** For selecting the input source vdc and ground terminal gnd, select analogLib in the library, vdc/gnd in the cell column, and spectre in the view column for vdc and symbol in the view column of gnd.

**Step 6:** Use a narrow wire for connecting the components.

**Step 7:** Complete the remaining circuit connections (Figure 46).



**Figure 46. PMOS Final Circuit**

**Step 8:** Click on the PMOS symbol and press Q for displaying its properties.

**Step 9:** In the properties dialog box, change the PMOS width to 400 nm.

**Step 10:** Similarly for the voltage sources  $V_{GS}$  and  $V_{DS}$ , define their voltage values by clicking on these sources, pressing Q, and providing -1.8 in DC voltage value.

**Step 11:** Click Check and Save and ensure that there are no errors and warnings.

**Step 12:** Once the schematic is constructed, simulate them by clicking Launch→ADE L.

**Step 13:** In the ADE window, Click Analysis→Choose.

**Step 14:** In the Analysis dialog box, choose dc. Select the Save DC Operating Point.

**Step 15:** Under Sweep Variable, select Component Parameter.

**Step 16:** Click Select Component and click  $V_{GS}$  voltage source in the schematic.

**Step 17:** Select DC voltage and click OK.

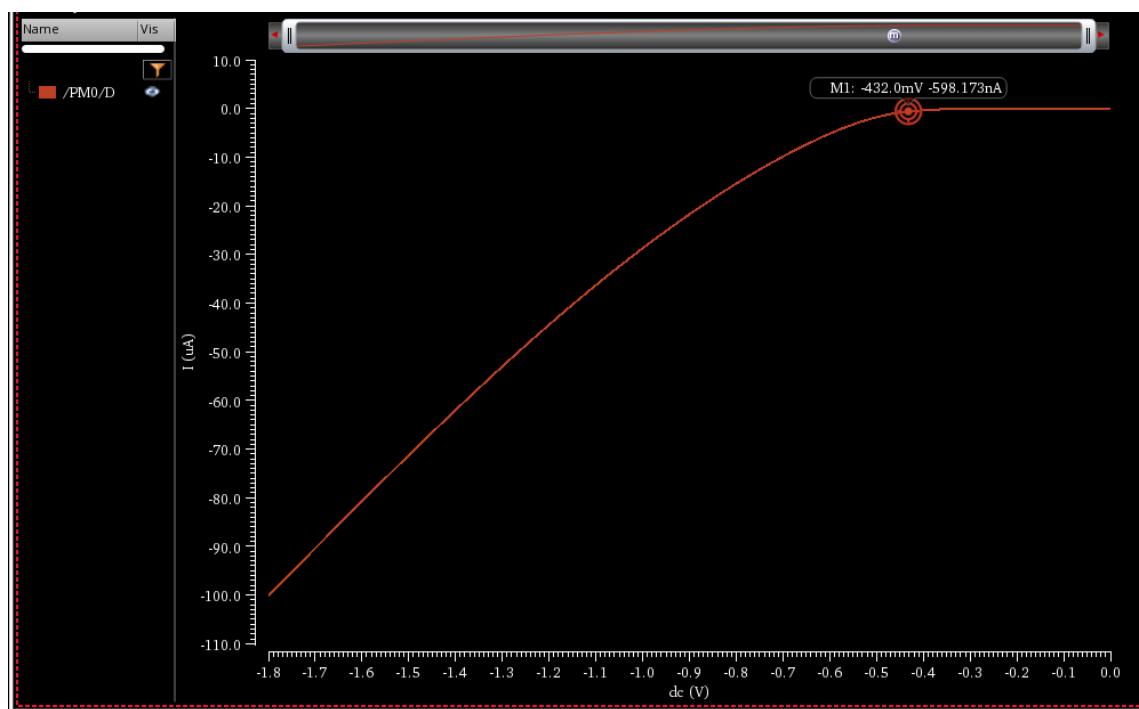
**Step 18:** In the sweep range, make the start value -1.8 and the stop value 0 and click OK.

**Step 19:** After setting up the analysis, click Output→To Be Plotted→Select On Design to plot the output.

**Step 20:** From the schematic, choose the drain terminal of the transistor.

**Step 21:** In the ADE window, click the Netlist and Run.

**Step 22:** Upon successful simulation, the following graph will be obtained (Figure 47).



**Figure 47. PMOS  $V_{GS}$  vs  $I_D$**

**Step 23:** For finding  $V_T$ , place the mouse over the graph over the point where the current starts to decrease from zero and use a marker (press m) to find that voltage.

Step 31: By inferring the graph in Figure 47,  $V_T$  is found to be -0.43 V.

### 8.6.2 PMOS $V_{GS}$ vs $I_D$ for variable $V_{DS}$

**Step 1:** In the same library (Exp\_demo), create a new cellview “**pmos7.2**”.

**Step 2:** Reconstruct the same circuit from 8.1 or copy the entire circuit from the previous schematic by following steps 2 to 10 in section 8.6.1.

**Step 3:** Instead of giving VDS as -1.8 V, keep the DC Voltage of VDS as vds.

**Step 4:** Follow steps 11 to 20 in section 8.6.1.

**Step 5:** Inside the ADE window, find the Design Variables tab, right-click on it, and select Copy From Cellview.

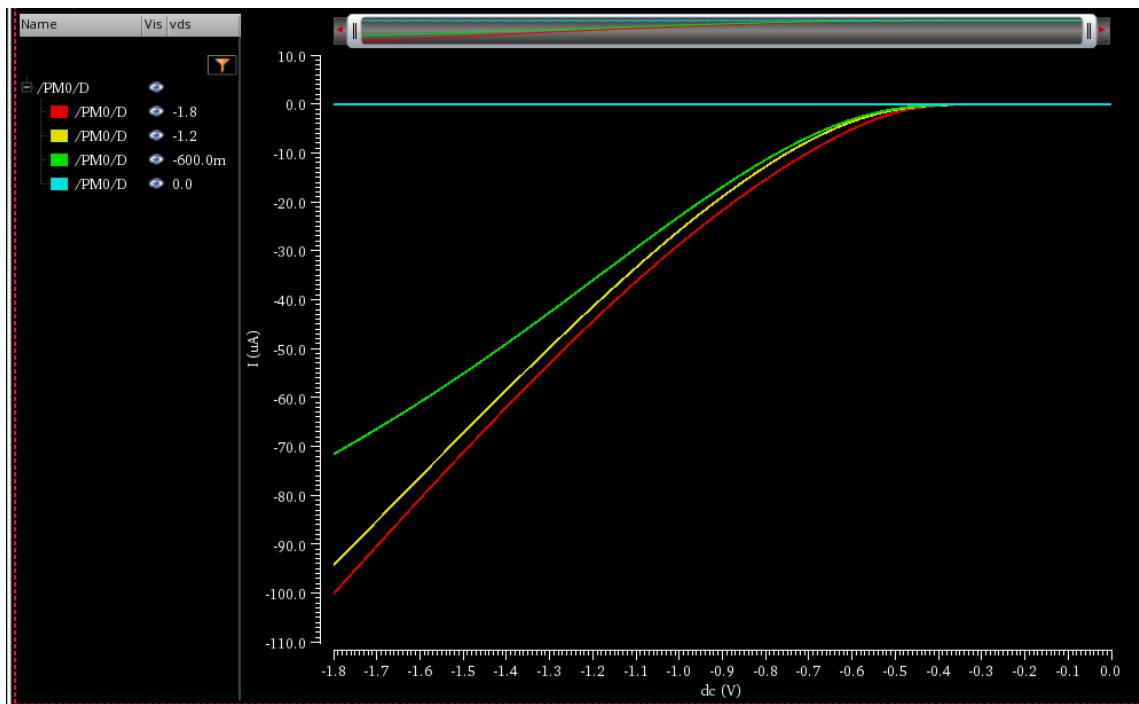
**Step 6:** The variable vds will automatically occur in the Design Variables tab and type the vds value as -1.8.

**Step 7:** In the ADE window, click Tools→Parametric Analysis.

**Step 8:** In the Parametric Analysis window, in the Add Variables column, select vds, give the From and To values as -1.8 and 0 and Total Steps as 4.

**Step 9:** Click Run Selected Sweeps.

**Step 10:** Upon successful execution, the following graph will be obtained (Figure 48).



**Figure 48. PMOS  $V_{GS}$  vs  $I_D$  for variable  $V_{DS}$**

### 8.6.3 PMOS $V_{DS}$ vs $I_D$

**Step 1:** In the same library (Exp\_demo), create a new cellview “**pmos7.3**”.

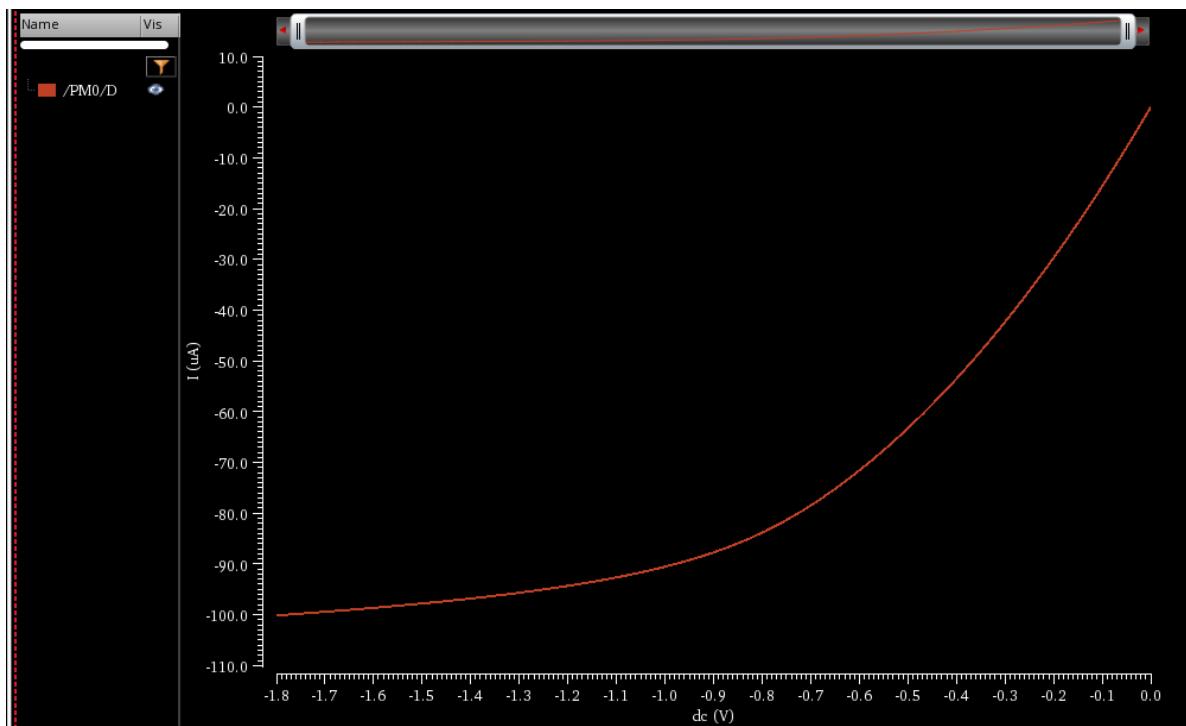
**Step 2:** Reconstruct the same circuit from 8.6.1 or copy the entire circuit from the previous schematic.

**Step 3:** Follow steps 2 to 15 in section 8.6.1.

**Step 4:** Instead of selecting  $V_{GS}$  under Select Component, now select  $V_{DS}$ .

**Step 5:** Follow steps 17 to 21 in section 8.6.1.

**Step 6:** Upon successful simulation, the following graph will be obtained (Figure 49).



**Figure 49. PMOS  $V_{DS}$  vs  $I_D$**

### 8.6.4 PMOS $V_{DS}$ vs $I_D$ for variable $V_{GS}$

**Step 1:** In the same library (Exp\_demo), create a new cellview “**pmos7.4**”.

**Step 2:** Reconstruct the same circuit from 8.6.1 or copy the entire circuit from the previous schematic by following steps 2 to 10 in section 8.6.1.

**Step 3:** Instead of giving  $V_{GS}$  as 1.8 V, keep the DC Voltage of  $V_{GS}$  as  $vgs$ .

**Step 4:** Follow steps 11 to 15 in section 8.6.1.

**Step 5:** Instead of selecting  $V_{GS}$  under Select Component, now select  $V_{DS}$ .

**Step 6:** Follow steps 17 to 20 in section 8.6.1.

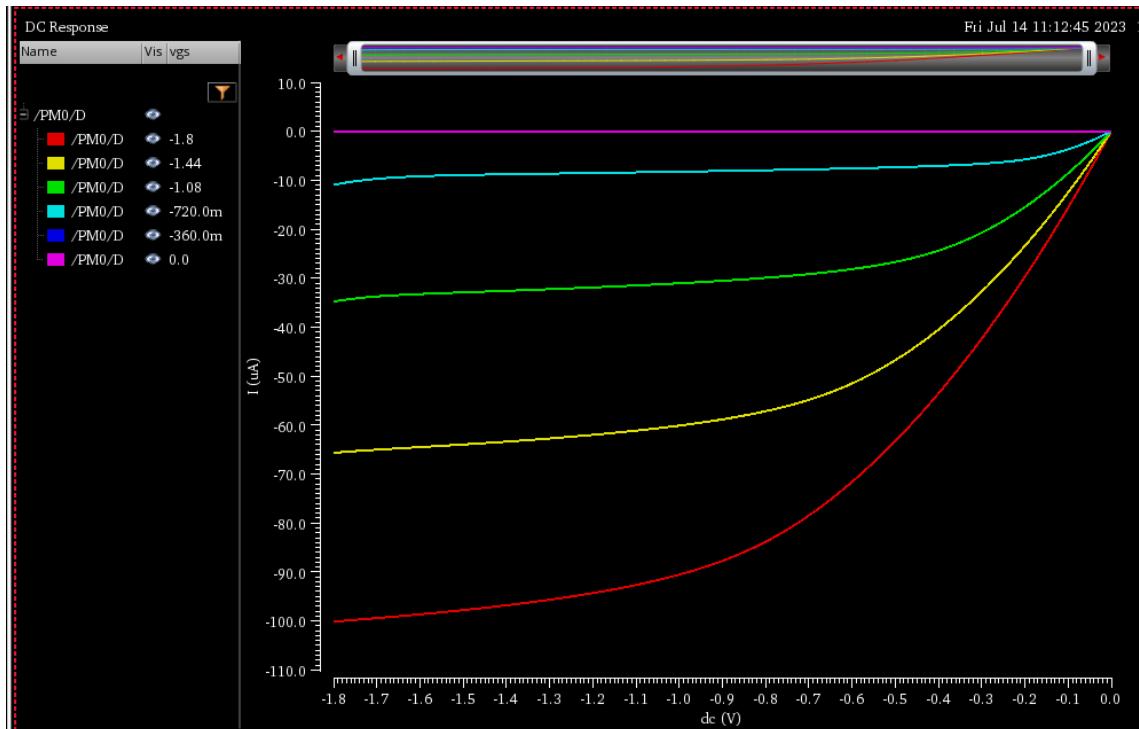
**Step 7:** Inside the ADE window, find the Design Variables tab, right-click on it, and select Copy From Cellview.

**Step 8:** The variable  $vgs$  will automatically occur in the Design Variables tab and type the  $vgs$  value as -1.8.

**Step 9:** In the ADE window, click Tools→Parametric Analysis.

**Step 10:** In the Parametric Analysis window, in the Add Variables column, select  $vgs$ , give the From and To values as -1.8 and 0, and Total Steps as 6.

**Step 11:** Click Run Selected Sweeps (Figure 50).



**Figure 50. PMOS  $V_{DS}$  vs  $I_D$  for variable  $V_{GS}$**

### 8.6.5 PMOS Width vs $I_D$

**Step 1:** In the same library (Exp\_demo), create a new cellview “**pmos7.5**”.

**Step 2:** Reconstruct the same circuit from 8.6.1 or copy the entire circuit from the previous schematic.

**Step 3:** Follow steps 2 to 8 in section 8.6.1.

**Step 4:** Instead of giving the width as 400 nm, keep the width as w.

**Step 5:** Follow steps 10 to 20 in section 8.6.1

**Step 6:** Inside the ADE window, find the Design Variables tab, right-click on it, and select Copy From Cellview.

**Step 7:** The variable w will automatically occur in the Design Variables tab and type the w value as 1u.

**Step 8:** In the ADE window, click Tools→Parametric Analysis.

**Step 9:** In the Parametric Analysis window, in the Add Variables column, select w, give the From and To values as 400n and 1u and Total Steps as 6.

**Step 10:** Click Run Selected Sweeps and the following graph will be obtained (Figure 51).

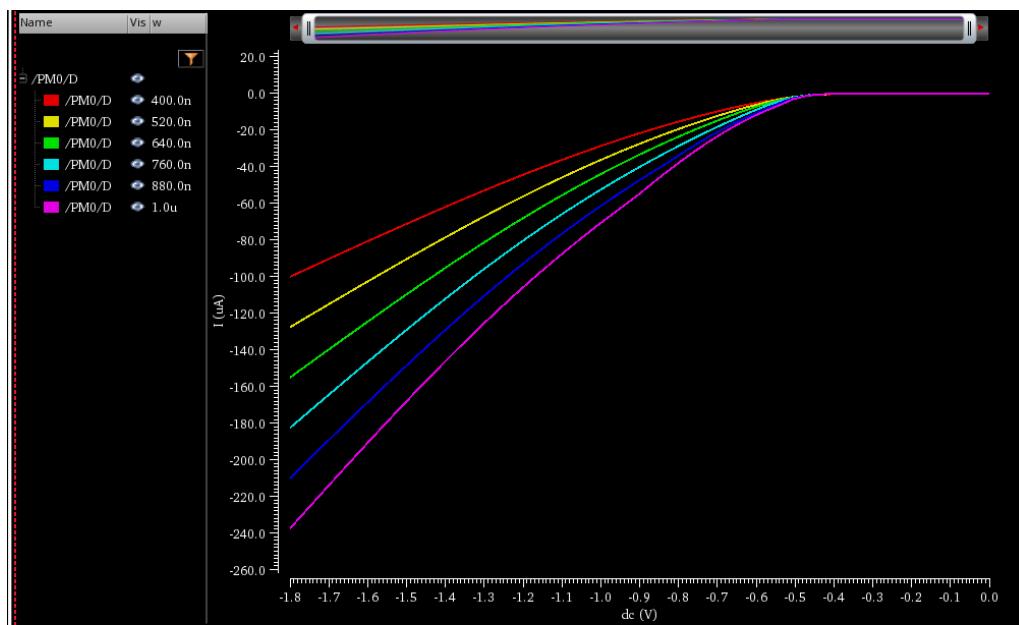
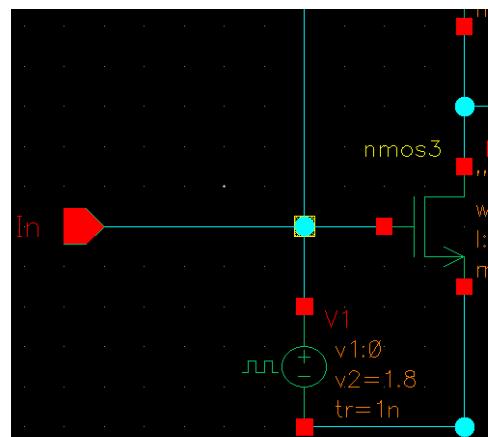


Figure 51. PMOS Width vs  $I_D$

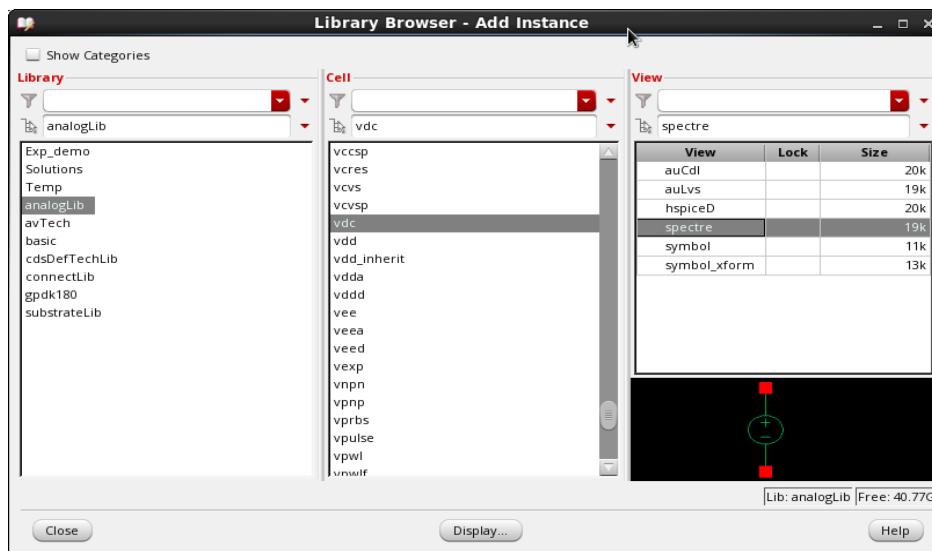
## 9. Important Notes

- Check the Virtuoso log window for checking the error and warning messages.
- Always maintain the NMOS width as 400 nm, unless specified.
- Double-click on the graph lines for changing their properties.
- Solder dot on cross-over warning: Make sure that there are not more than three wire connections at a single point (Figure 52).



**Figure 52. Solder Dot on Cross Over Warning**

- For selecting the input sources (vpulse, vdc), select analogLib in the library, vdc/vpulse in the cell column, and spectre in the view column (Figure 53).



**Figure 53. vds/vpulse Selection**

- For creating a common power supply refer to Figure 54. Once the following circuit is created, then the V<sub>dd</sub> symbol can be used (Figure 55).

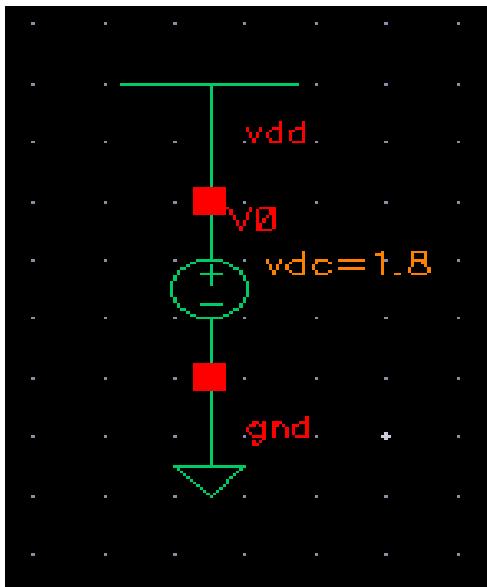


Figure 54. Vdd Creation

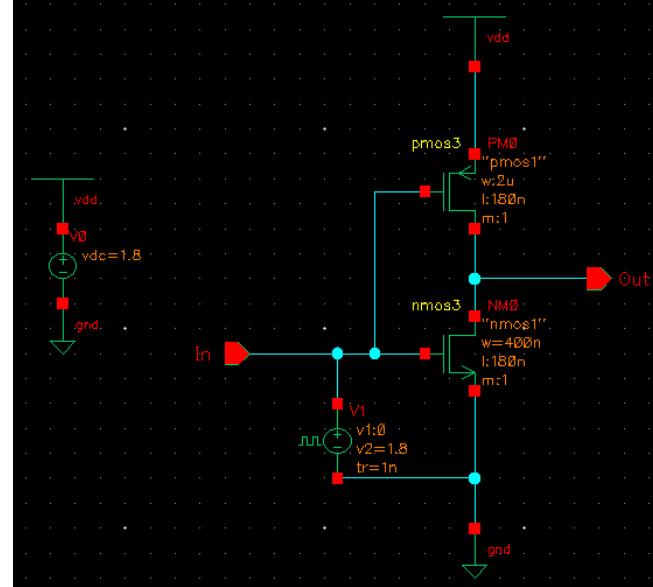


Figure 55. Vdd Symbol used in circuit

- The inputs and outputs can be labeled using pins. For creating a pin, click Create Pin and provide the pin name, and pin direction, and click OK (Figure 56).

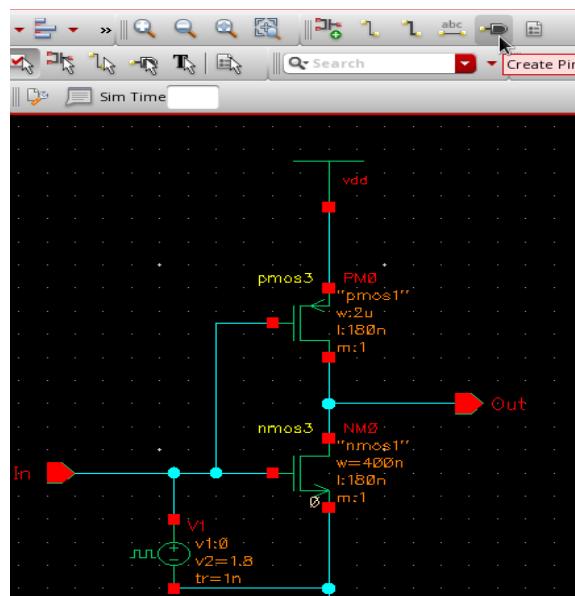
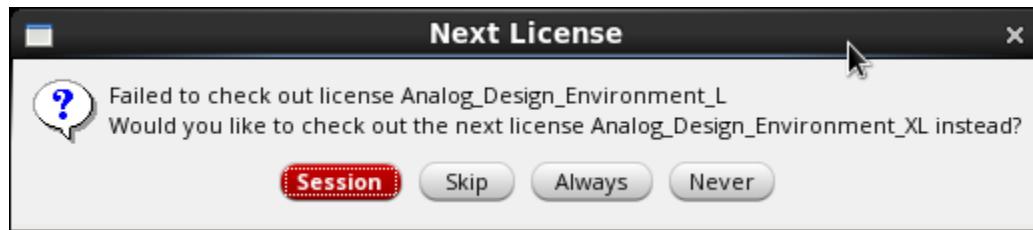


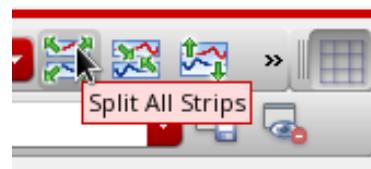
Figure 56. Pin Creation - In and Out are the pins

- When the Next License dialog box appears, click “Session” (Figure 57).



**Figure 57. Next License warning**

- If more than one plots overlap each other on the graph window, use the “Split All Strips” option to view them separately (Figure 58).



**Figure 58. Graph Plot Splitting**

- Steps to close Virtuoso: First close the schematics, ADE, and output windows. Then in the virtuoso log window, click File→Exit. This process will exit the Cadence Virtuoso. Then close the terminal window.
- Steps to log out of the server: Click the top right corner of the screen where the username is displayed and select Quit. Then click Log Out. Do not directly close the server.