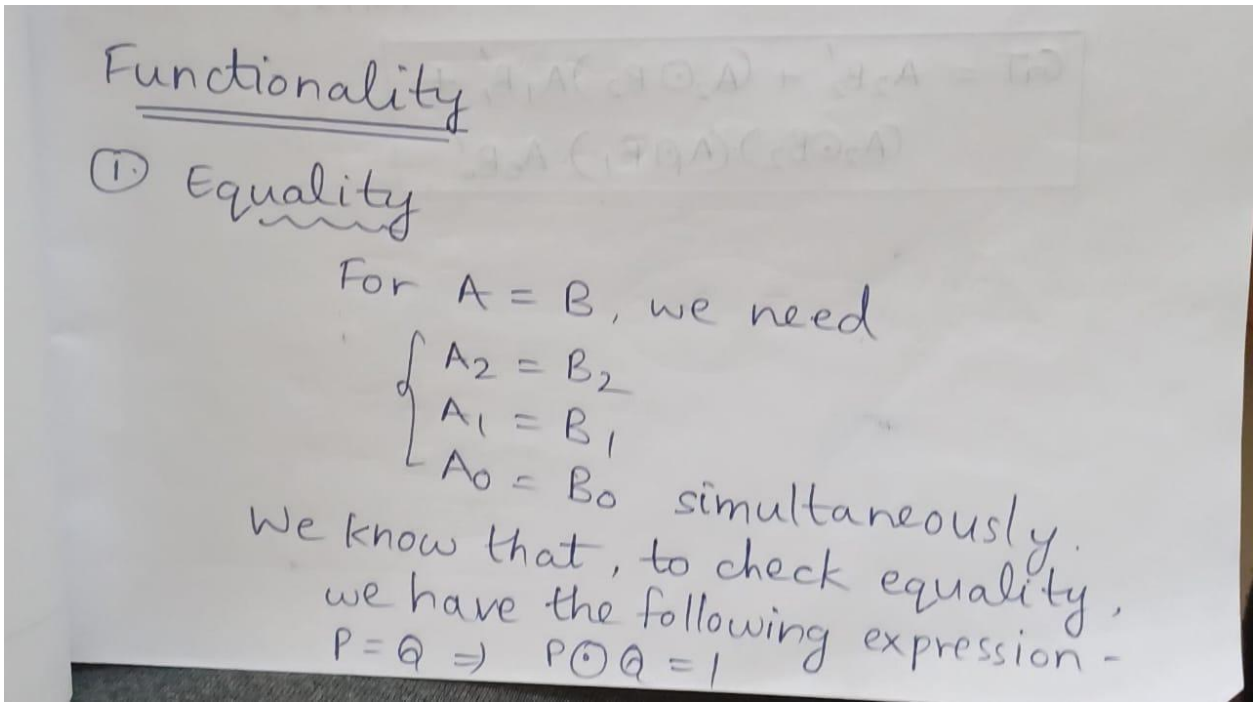
VLSI LAB Exercise-4 3-bit Magnitude Comparator

Group Number: 2

Group Members:
Thathapudi Sanjeev Paul Joel - 2020AAPS0120H
Aditya Anirudh - 2020AAPS0373H

Design Workout:



$\Rightarrow EQ = (A_2 \odot B_2) \cdot (A_1 \odot B_1) \cdot (A_0 \odot B_0)$

② Less Than:

For $A < B$

(i.) $A_2 < B_2$

$$C_1 = A_2' B_2$$

(ii.) $A_2 = B_2$, $A_1 < B_1$

$$C_2 = (A_2 \odot B_2) A_1' B_1$$

(iii.) $A_2 = B_2$; $A_1 = B_1$, $A_0 < B_0$

$$C_3 = (A_2 \odot B_2) \cdot (A_1 \odot B_1) A_0' B_0$$

$\Rightarrow LT = C_1 + C_2 + C_3$

$\Rightarrow$

$$\boxed{LT = A_2' B_2 + (A_2 \odot B_2) A_1' B_1 + (A_2 \odot B_2)(A_1 \odot B_1) A_0' B_0}$$

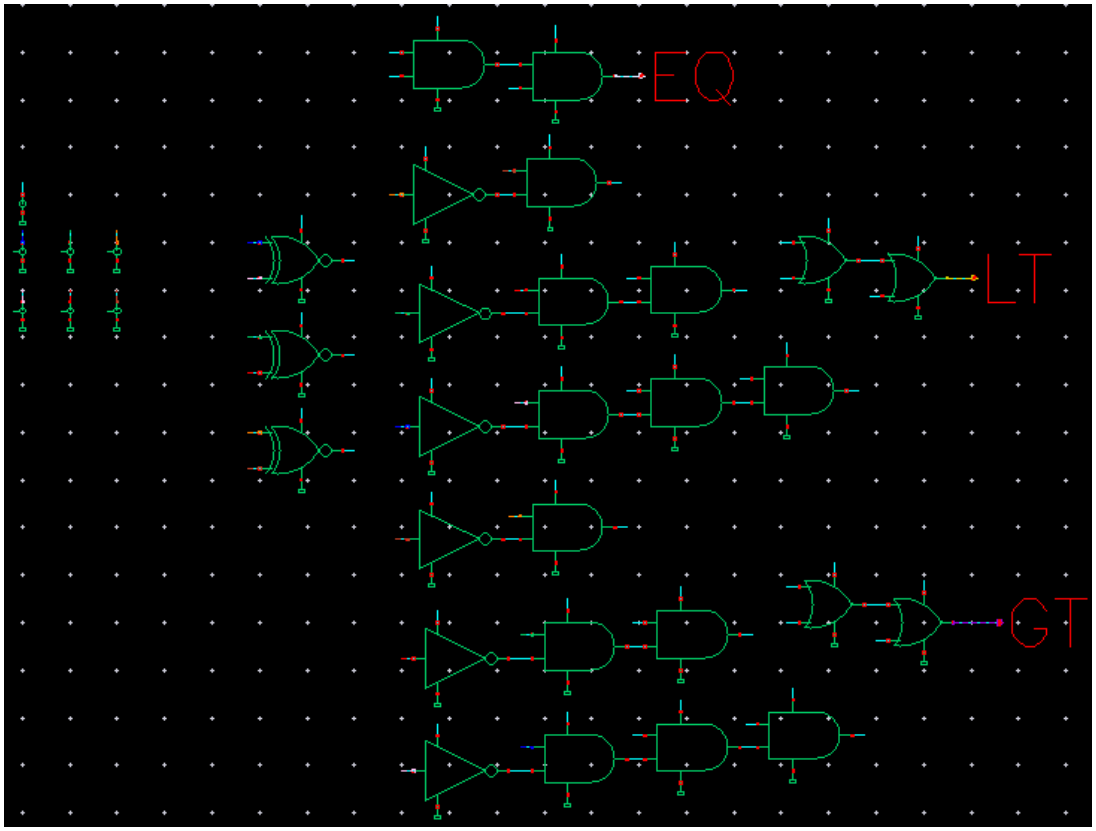
③ Greater Than

Similar to less, the following expression can be obtained -

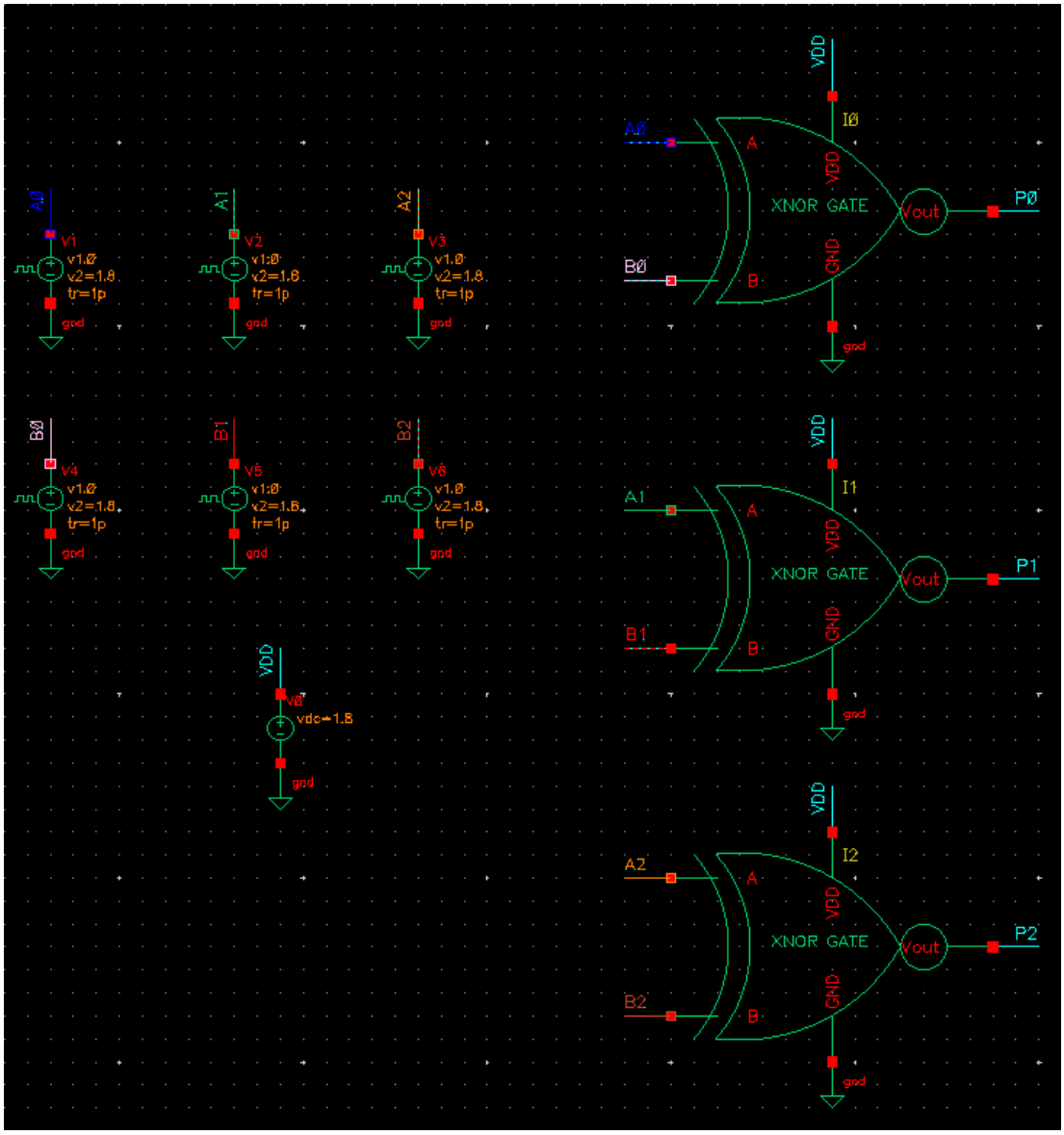
$$\boxed{GT = A_2 B_2' + (A_2 \odot B_2) A_1 B_1' + (A_2 \odot B_2) \cdot (A \odot B_1) \cdot A_0 B_0'}$$

Schematics:

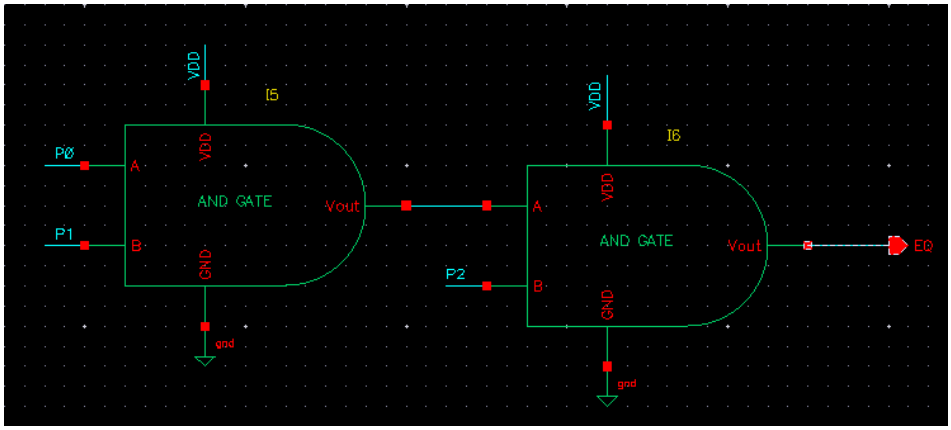
Main schematic:-



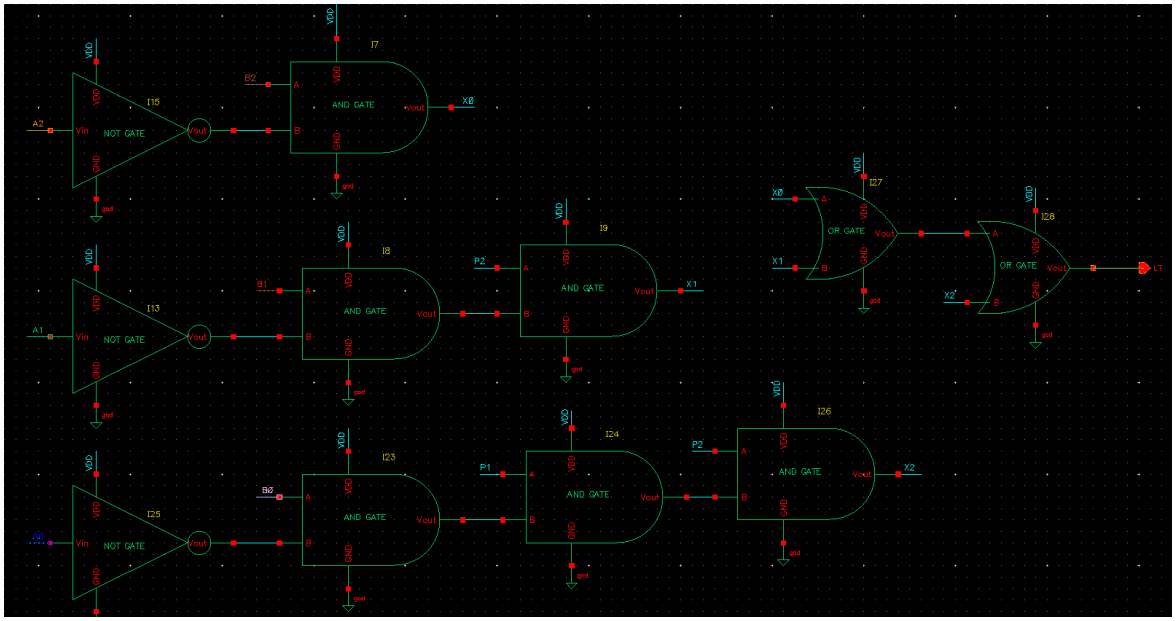
Excitation schematic:-



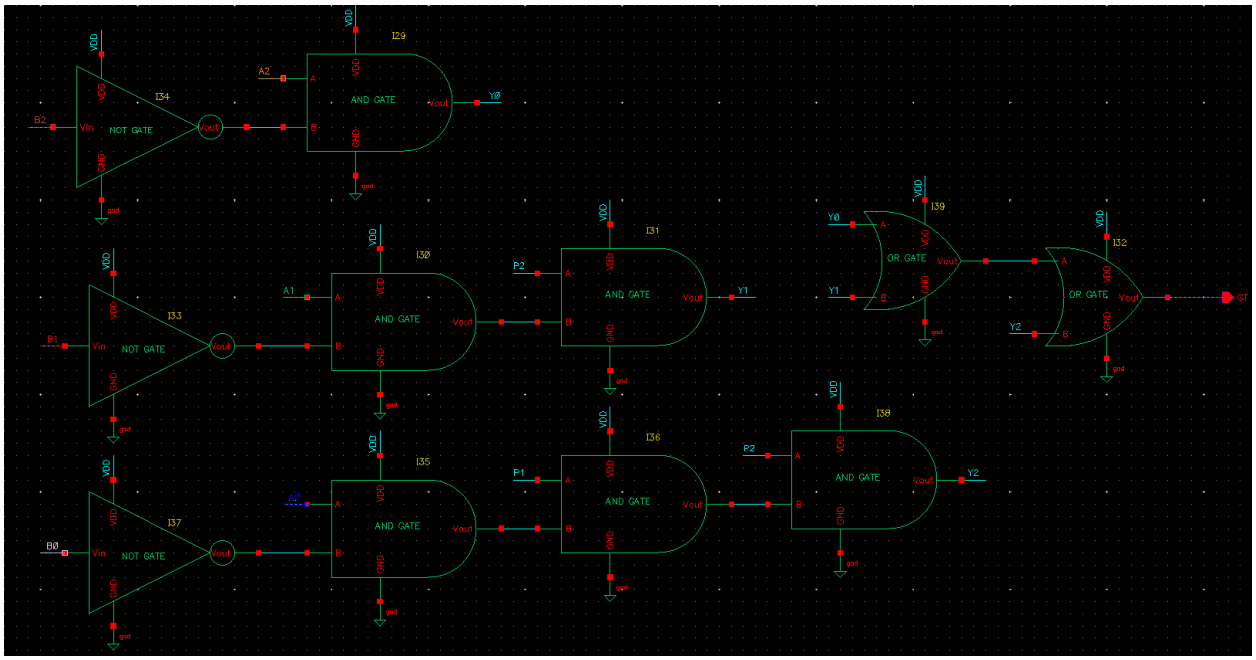
Schematic for *Equality* logic:-



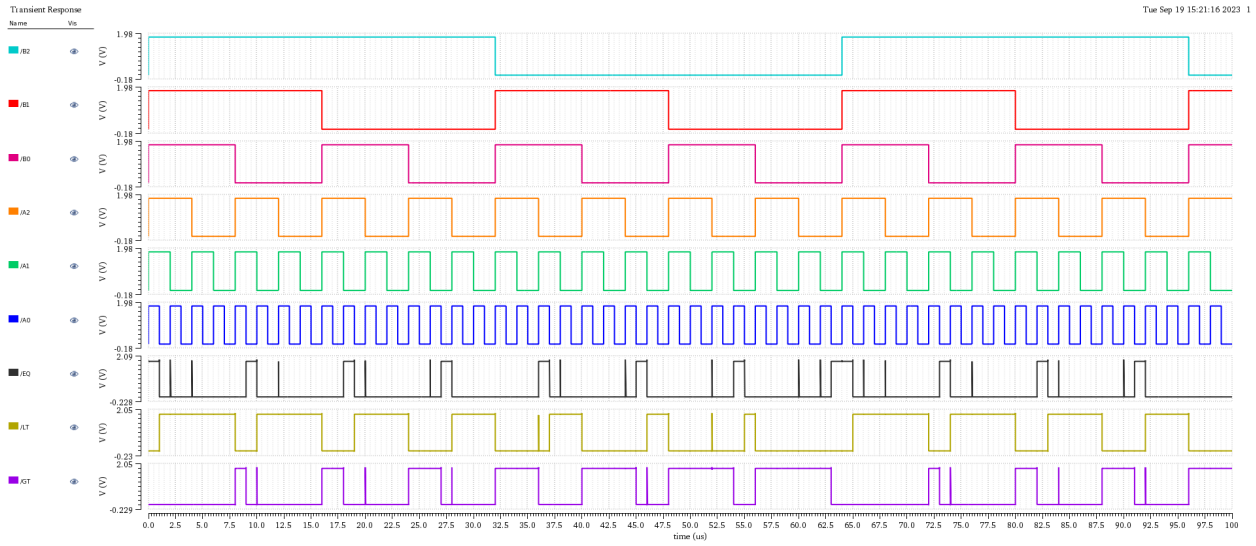
Schematic for *Less Than* logic:-



Schematic for *Greater Than* logic:-



Waveforms:



Conclusion:

In this exercise first we **derived the logic function using the behavioral description** of the 3-bit magnitude comparator and then used the derived logic function to implement the logic operation in Cadence Virtuoso using logic gates. Then, we simulated the circuit using suitable pulse waveforms for each input to obtain the results.