VLSI LAB Experiment-4 CMOS LOGIC GATES

Group Number: 2

Group Members:
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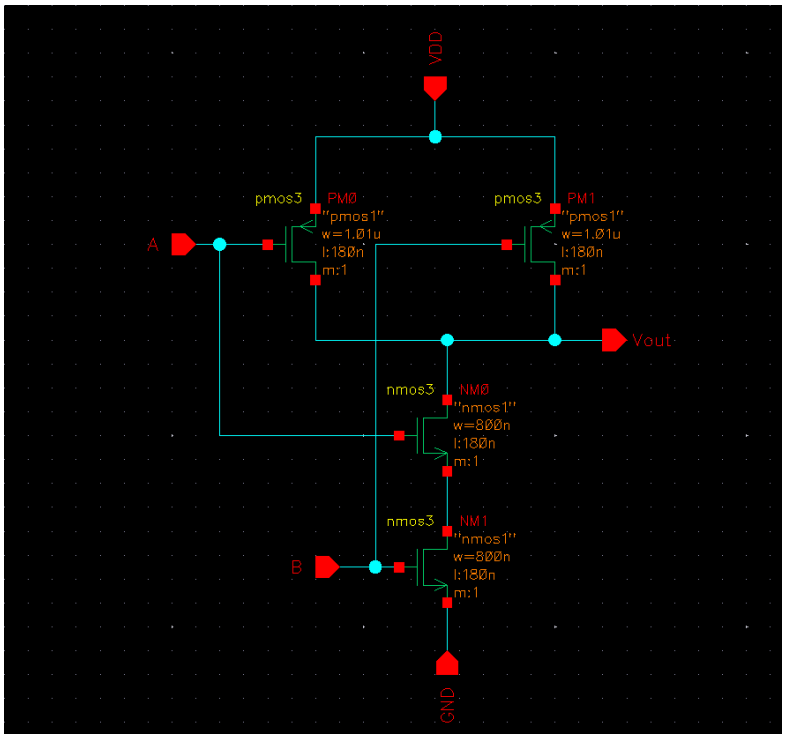
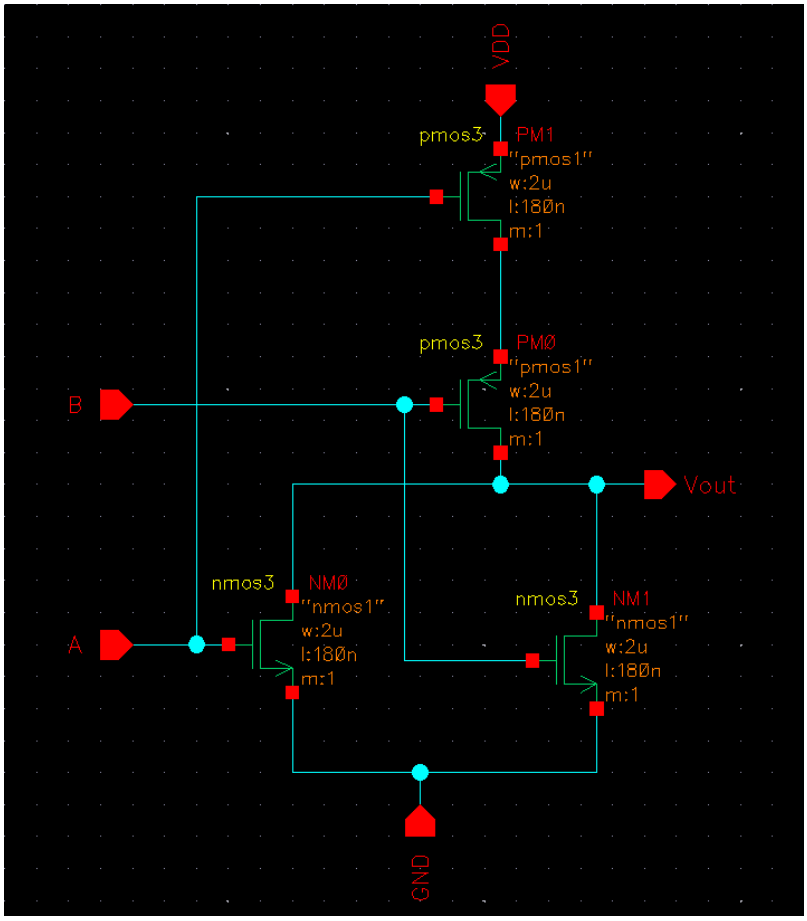
Aditya Anirudh - 2020AAPS0373H

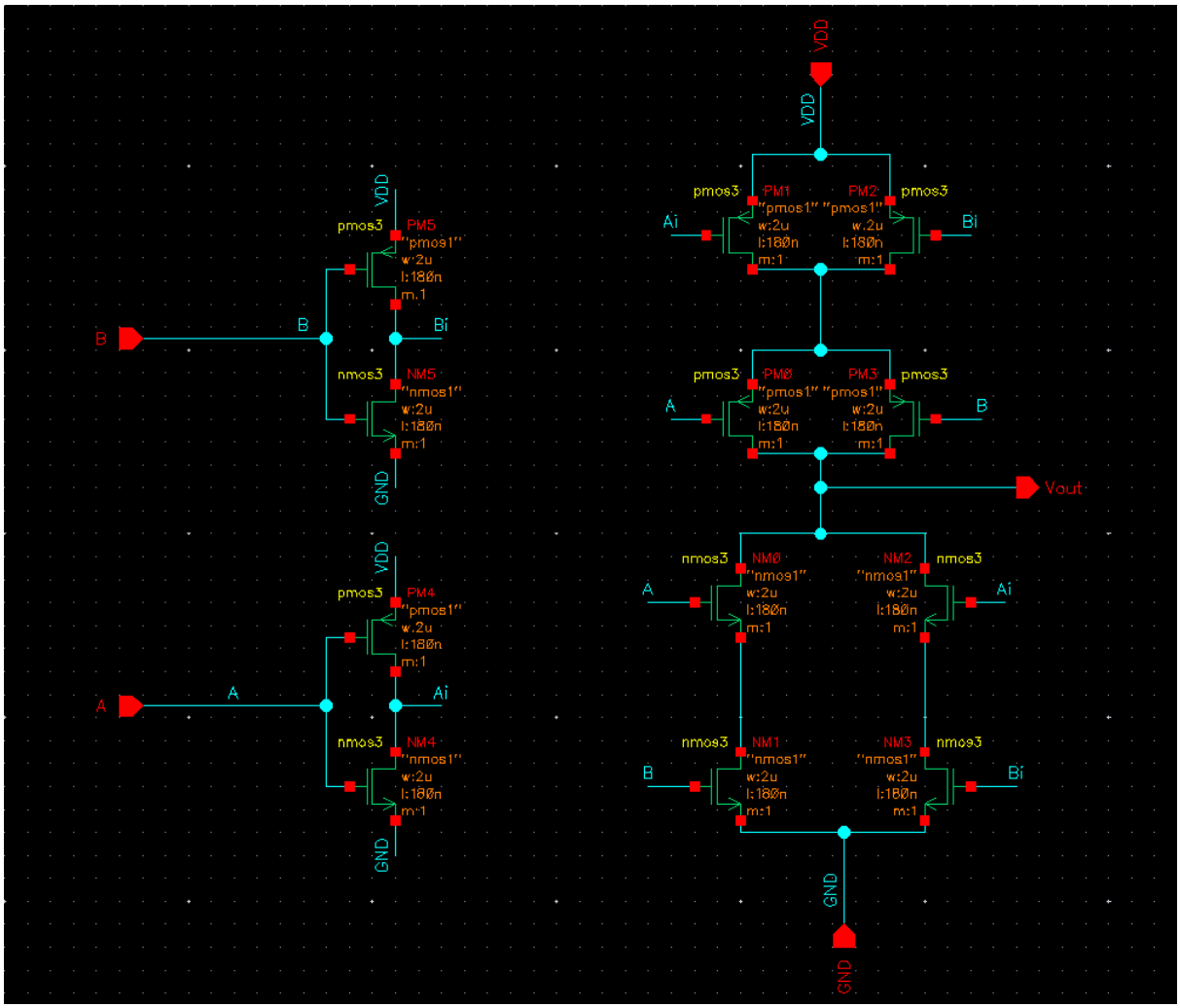
Schematic view of Gates:
NAND GATE -



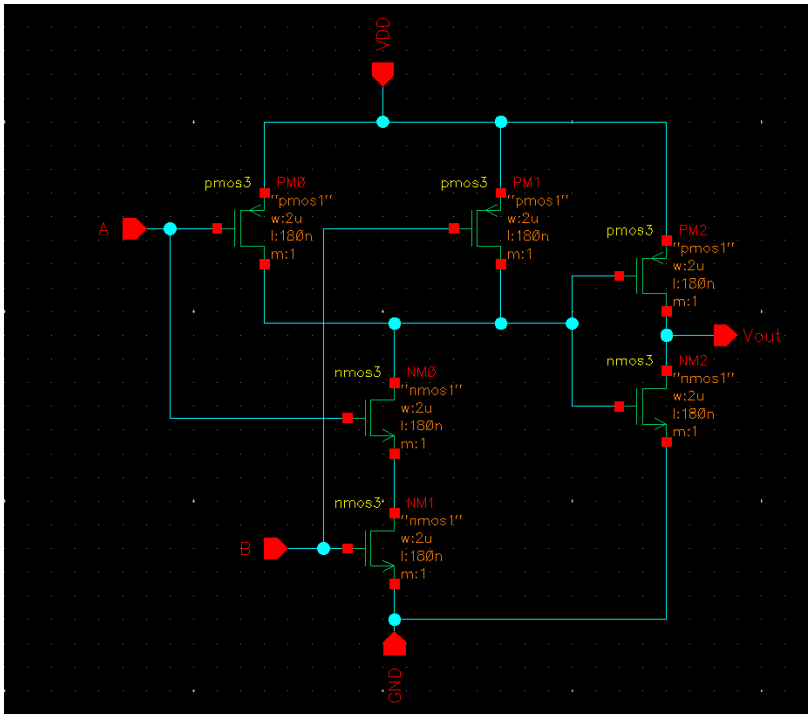
NOR GATE -


VDD
pmos3
PM1
"pmos1"
w:2u
l:180n
m:1
pmos3
PMØ
"pmos1"
w:2u
l:180n
m:1
B
Vout
nmos3
NMØ
"nmos1"
w:2u
l:180n
m:1
nmos3
NM1
"nmos1"
w:2u
l:180n
m:1
A
GND

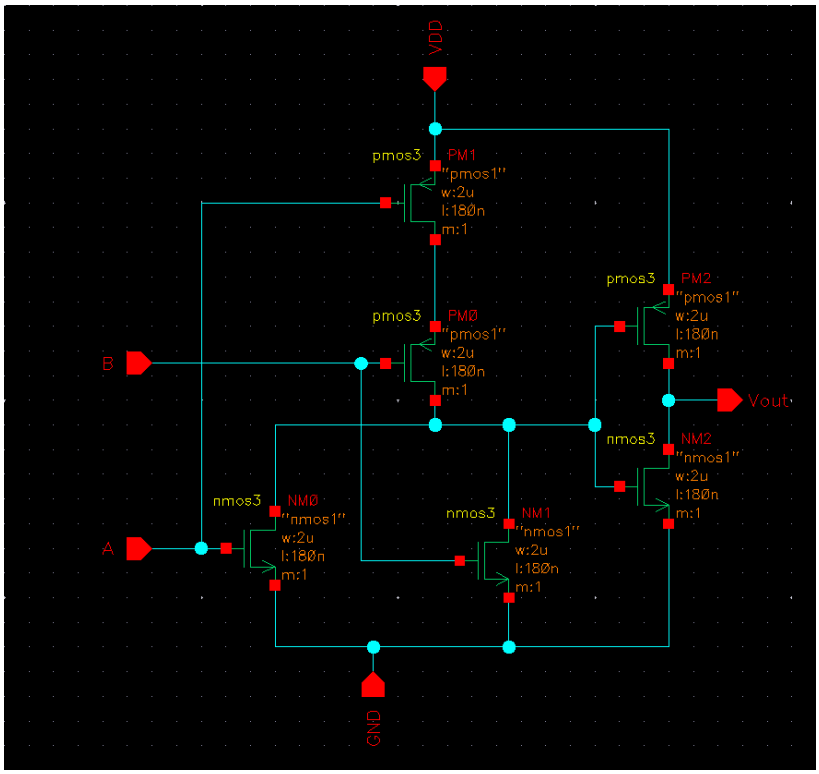
XOR GATE -


VDD
pmos3
PM5
"pmos1"
w:2u
l:180n
m:1
B
Bi
nmos3
NM5
GND
A
Ai
PM4
NM4
PM1
PM2
Ai
Bi
PM0
PM3
Vout
NM0
NM2
NM1
NM3
GND

AND GATE -



OR GATE -



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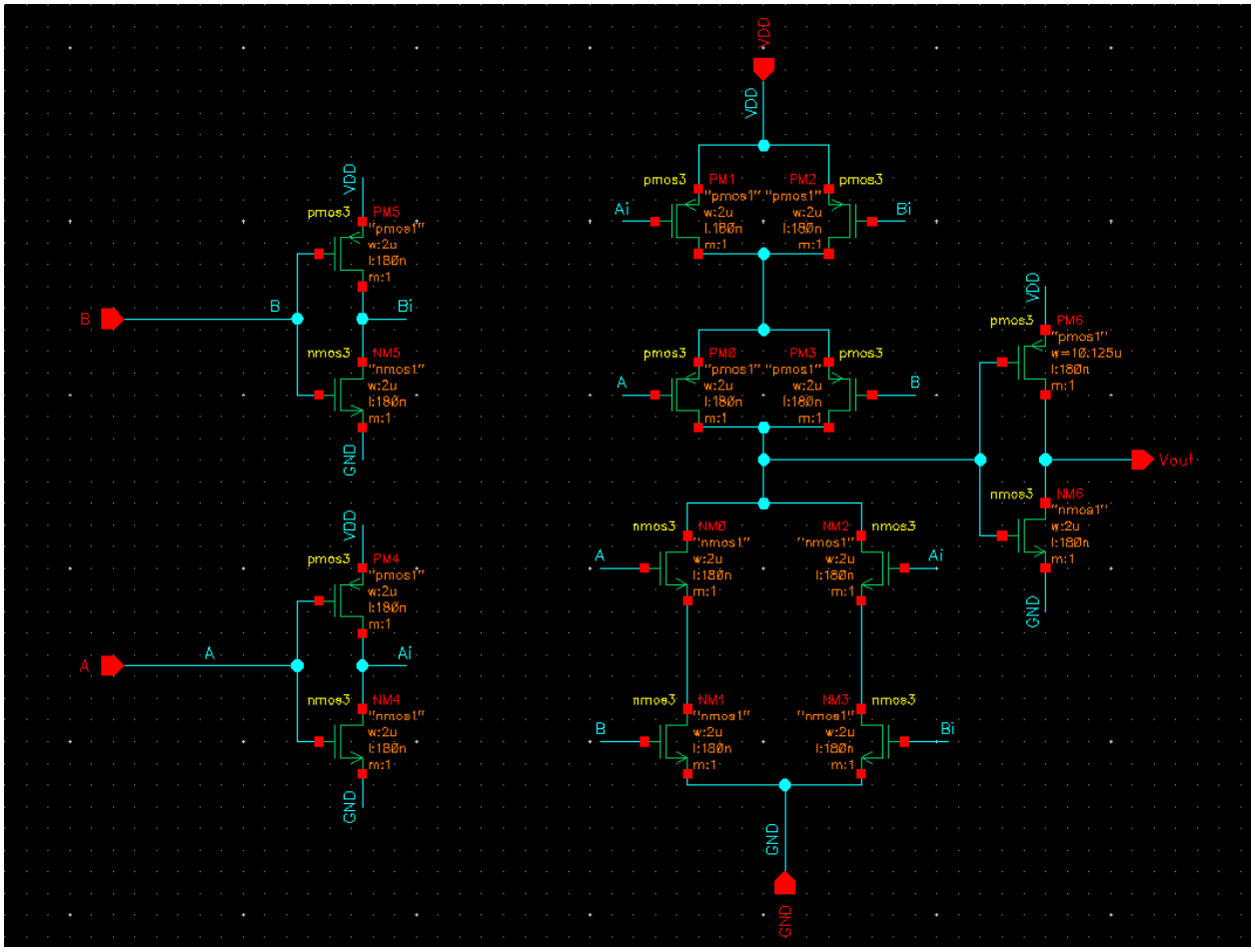
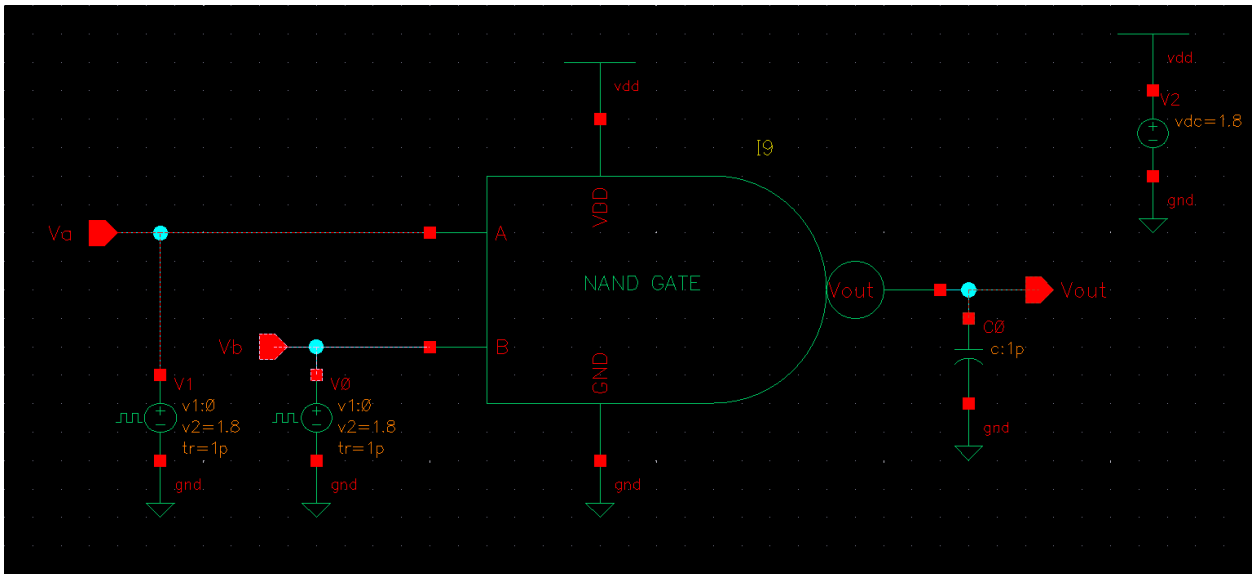


Circuit Schematics:

NAND GATE -



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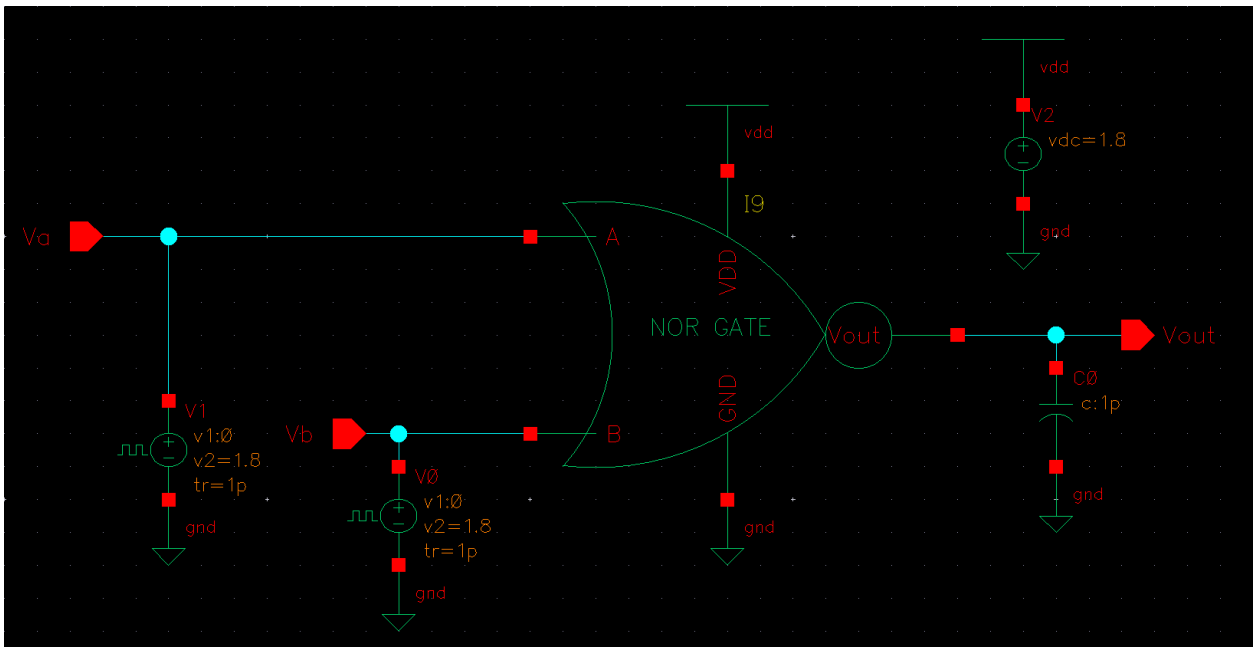

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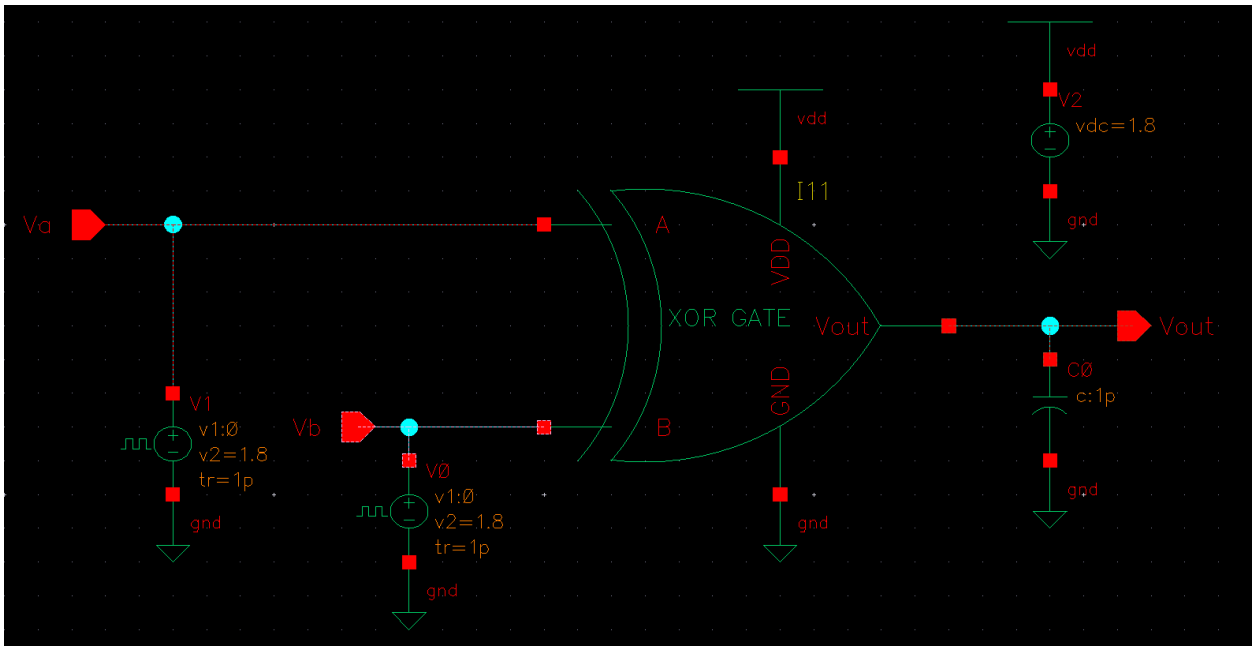

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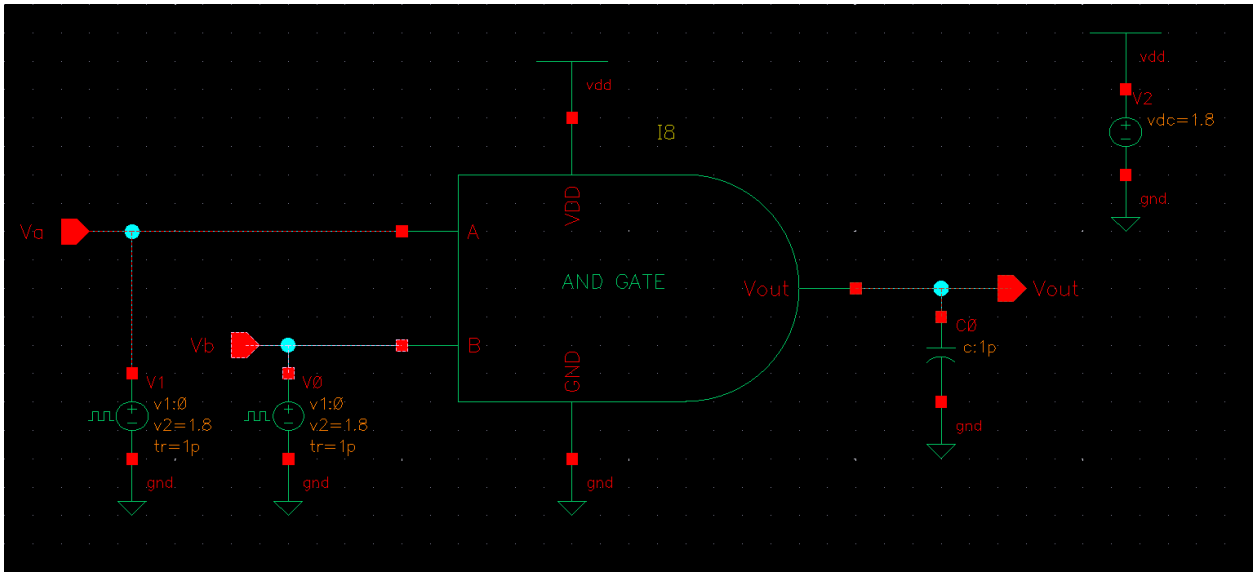

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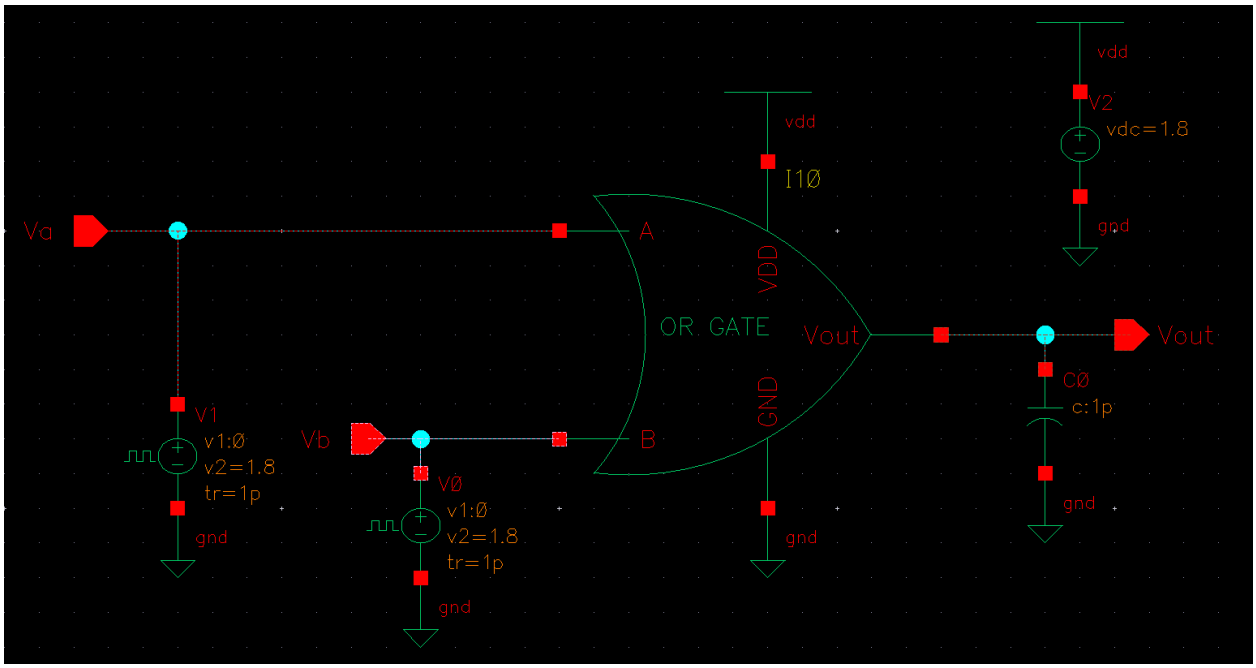

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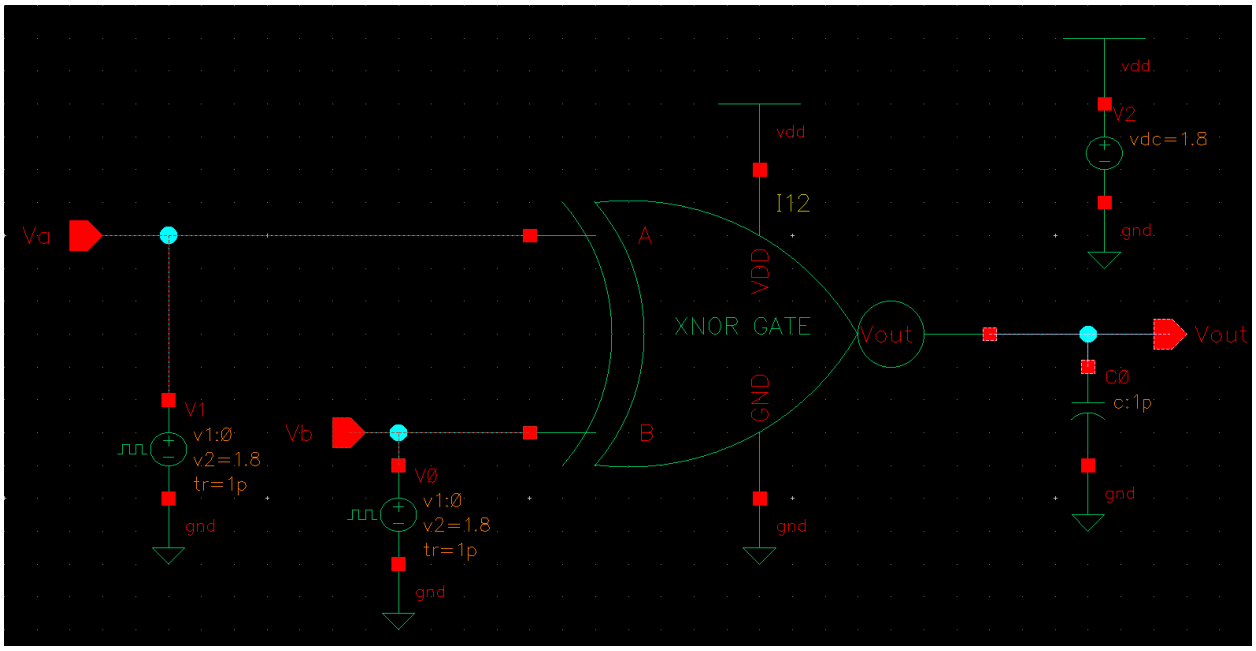
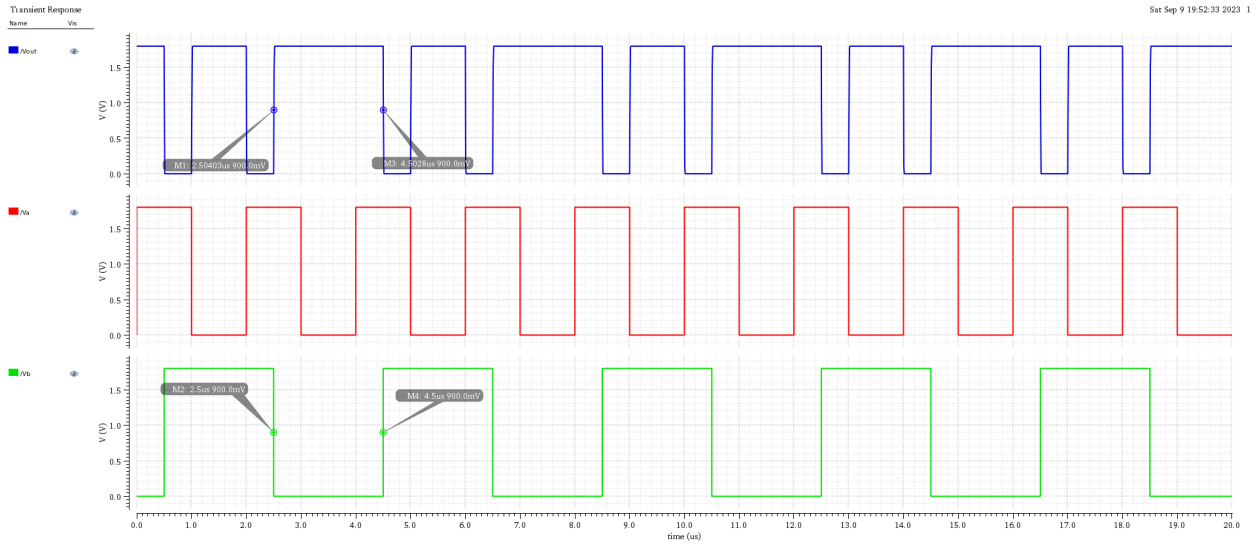


Waveforms:

NAND GATE -



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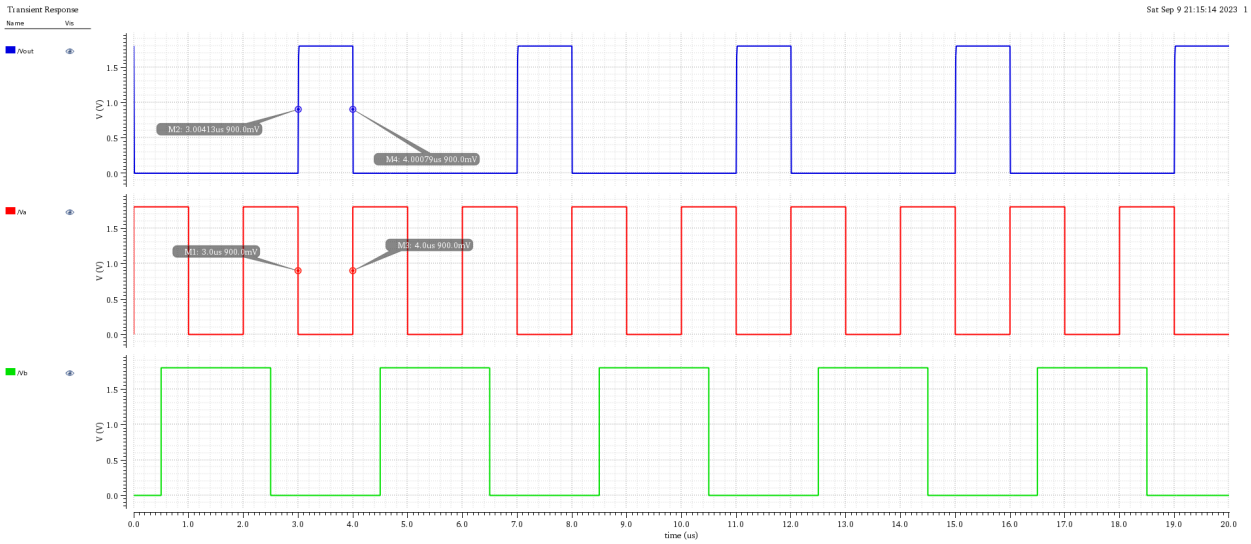

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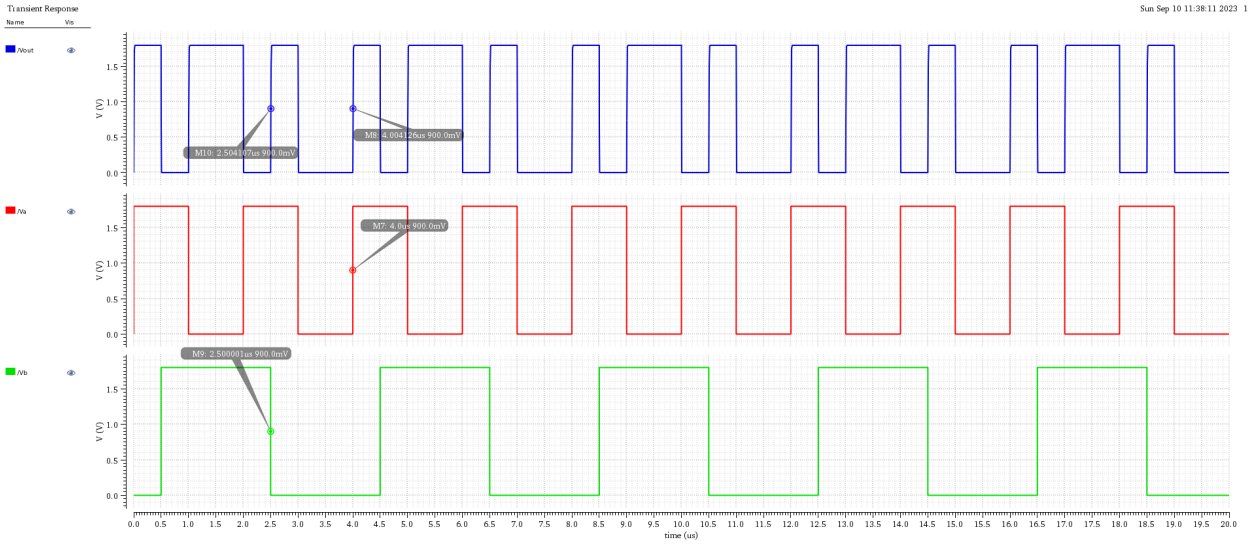

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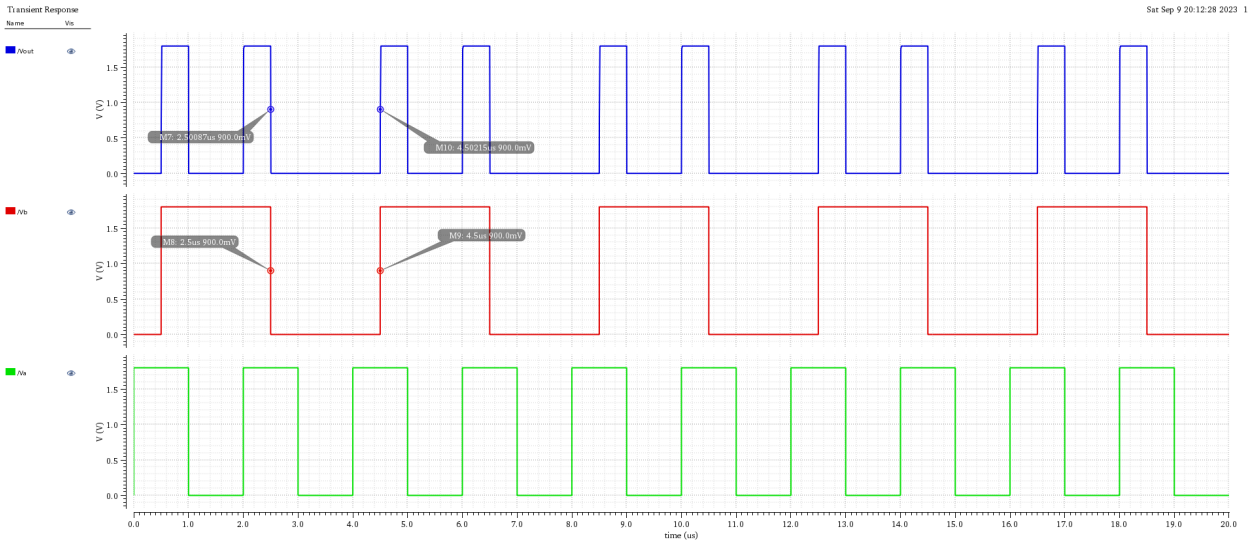

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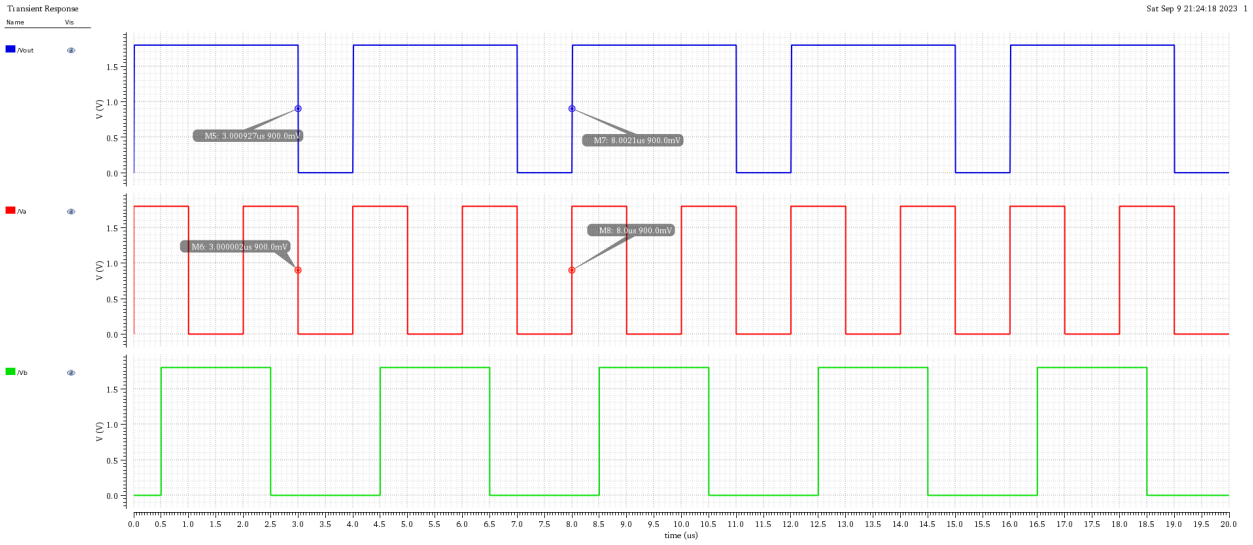

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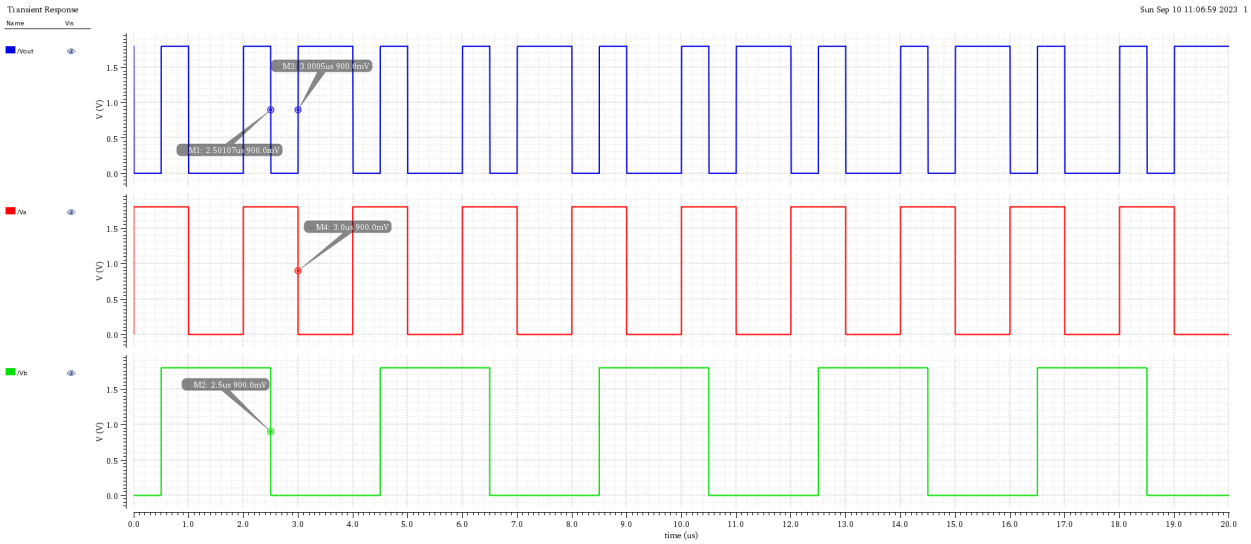
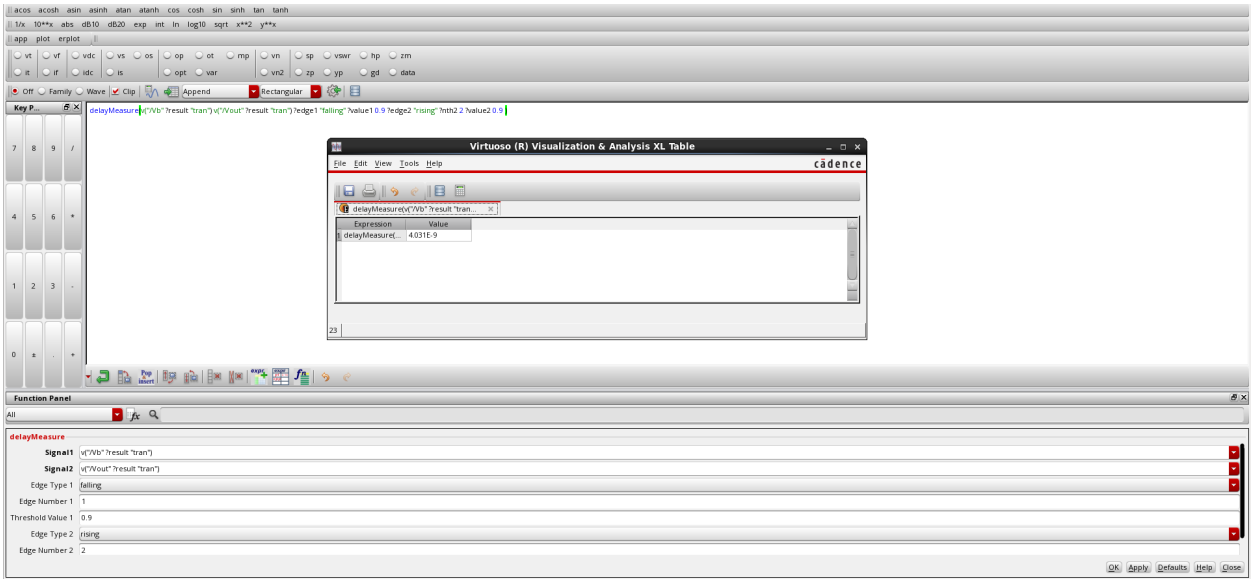


Observations:

NAND GATE -



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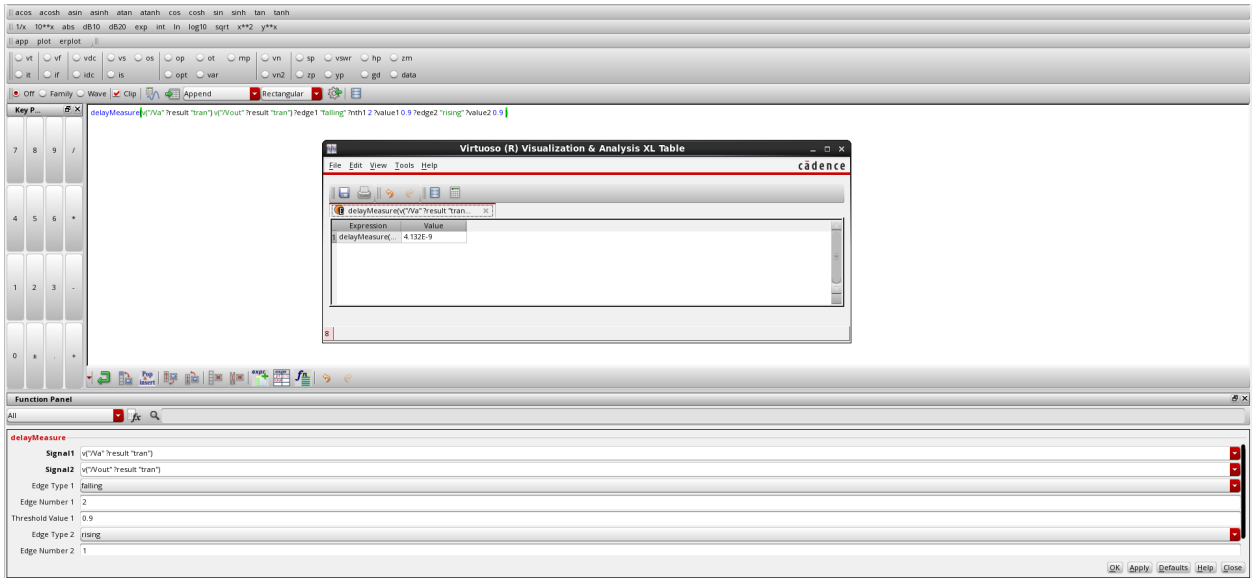

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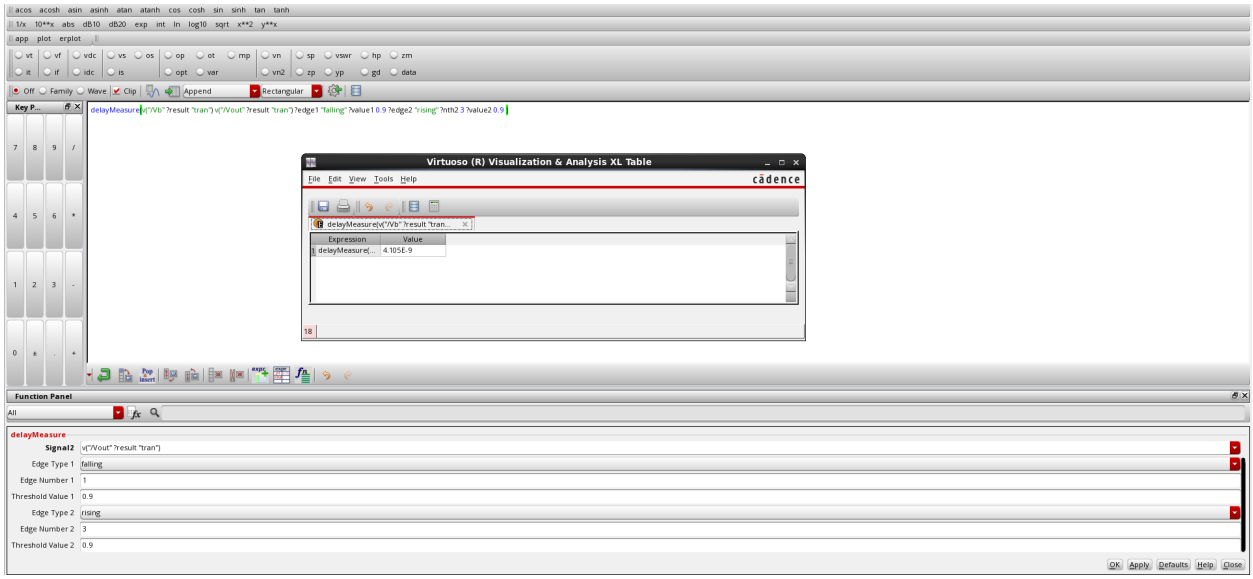

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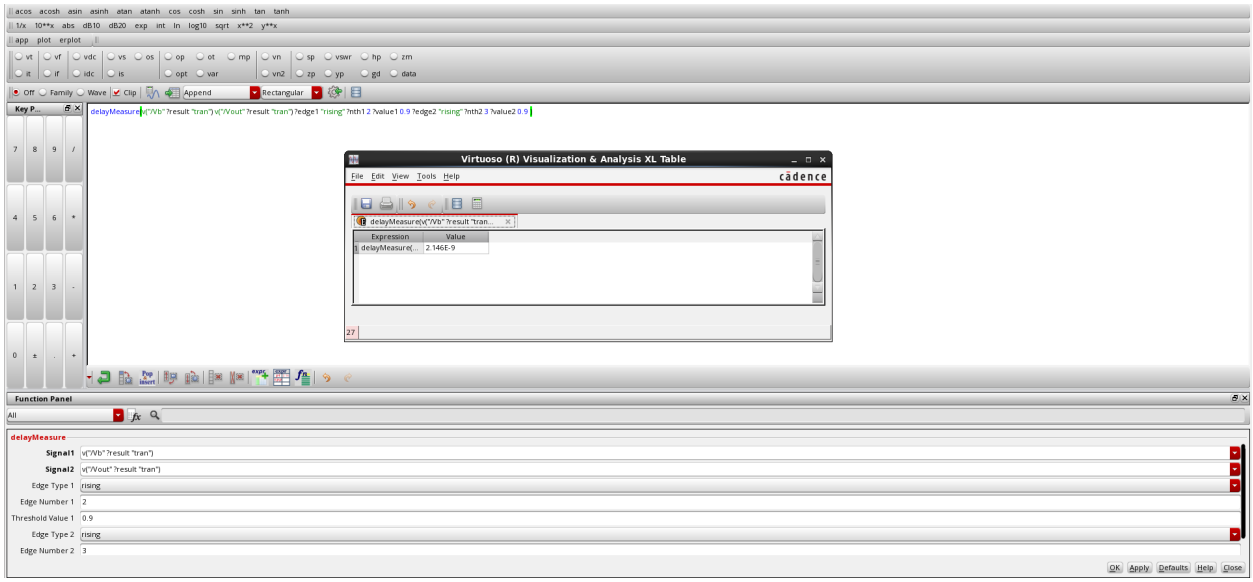

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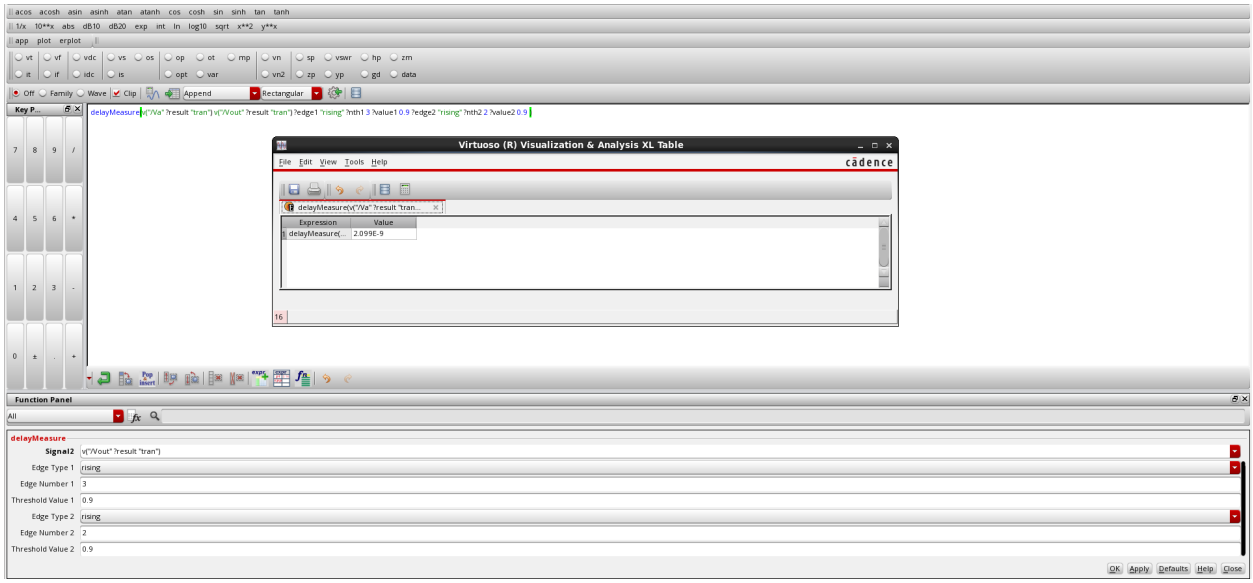

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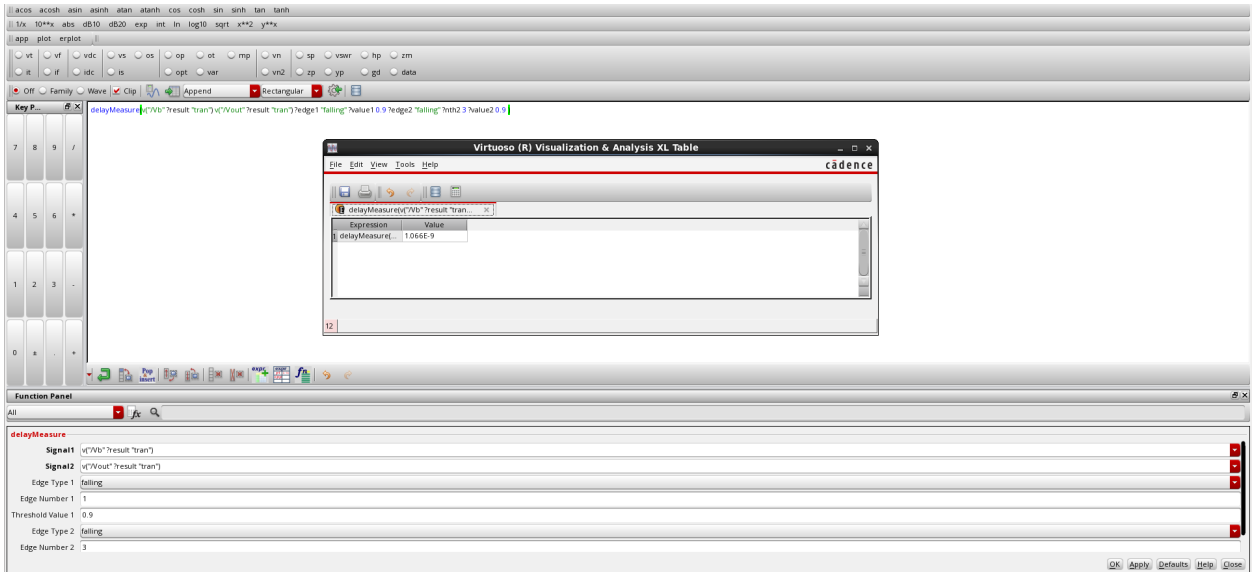

Metrics Measured:

Here $W_p = W_n = 2$ µm, and $\mu_n/\mu_p \approx 5$. So, the resistance offered by the PMOS transistor is higher than that of the NMOS transistor by nearly 5 times ⇒ the delay in **charging up the load capacitor** (LOW to HIGH) is more than the **delay in discharging it** (HIGH to LOW).

t_{worst} (NAND) = 4.013 ns
t_{worst} (NOR) = 4.132 ns
t_{worst} (XOR) = 4.105 ns

t_{worst} (AND) = 2.146 ns
t_{worst} (OR) = 2.099 ns
t_{worst} (XNOR) = 1.066 ns

Inferences:

1. The **delay of NOT of a particular gate** (say the pair AND & NAND gates) is **lesser than** the **delay of the gate on its own**. This is because the net resistance of the RC network decreases as the inverter and gate transistor resistances may have been placed in parallel combination.

2. The **critical path for the worst case delay**, for NAND gate as an example, is nothing but the **combination which leads to the highest resistance in the RC network** (here only one of the

PMOS transistors being ON).

A	B	OUT	Resistance
0	0	1	$R_p/2$
0	1	1	R_p
1	0	1	R_p
1	1	0	$2R_n$

So the delay will be maximum for a transition of (1, 1) to (0, 1) or (1, 1) to (1, 0).

3. The worst case delay of the NOR gate is the highest because the **resistance of the RC network in the LOW to HIGH transition equals to a value of $2R_p$** which is larger than only R_p in the case of NAND gate, etc.

Conclusion:

In this experiment, we learnt how to construct the CMOS Logic Gates using transistors and then convert them into custom symbols for usage in the circuit schematics. We also learnt how to find the critical path for evaluating the worst case delay in a given transistor network, and found out the worst case delays of all the gates built using the Calculator Tool in Cadence Virtuoso.