

VLSI LAB Experiment-2 CMOS INVERTER

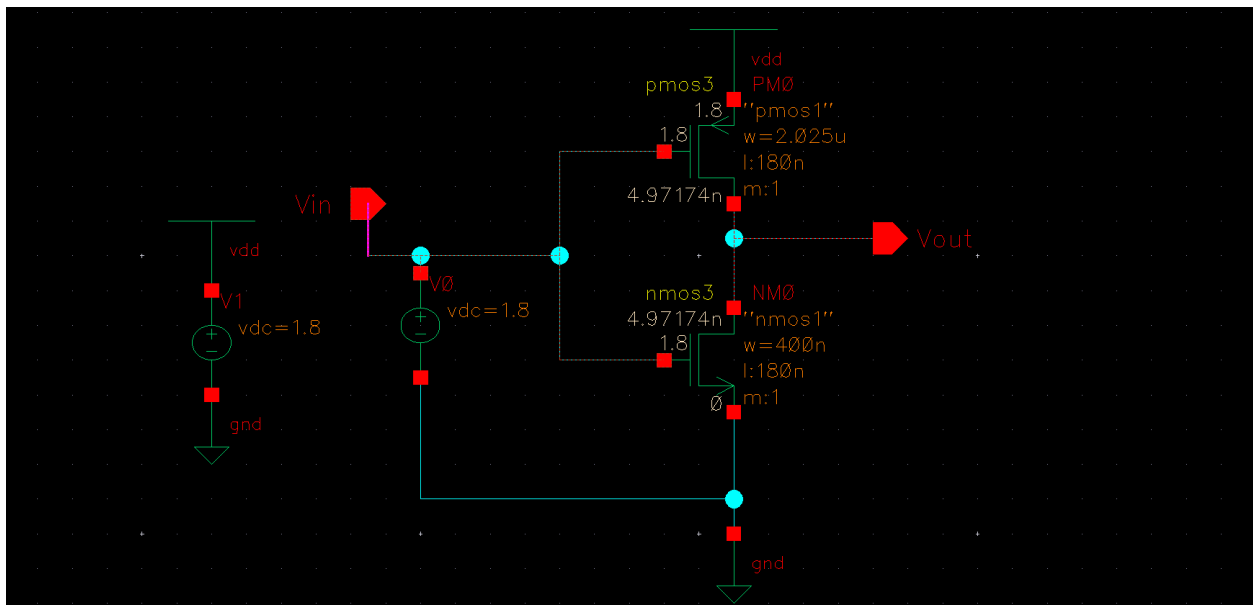
Group Number: 2

Group Members:

Thathapudi Sanjeev Paul Joel - 2020AAPS0120H

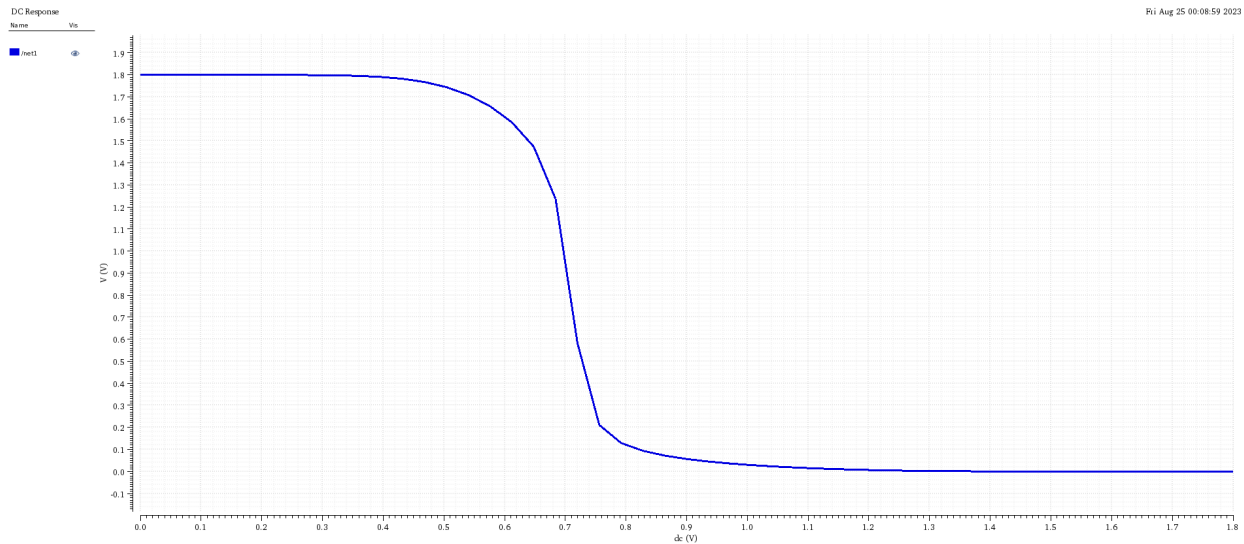
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Schematics:



Waveforms:

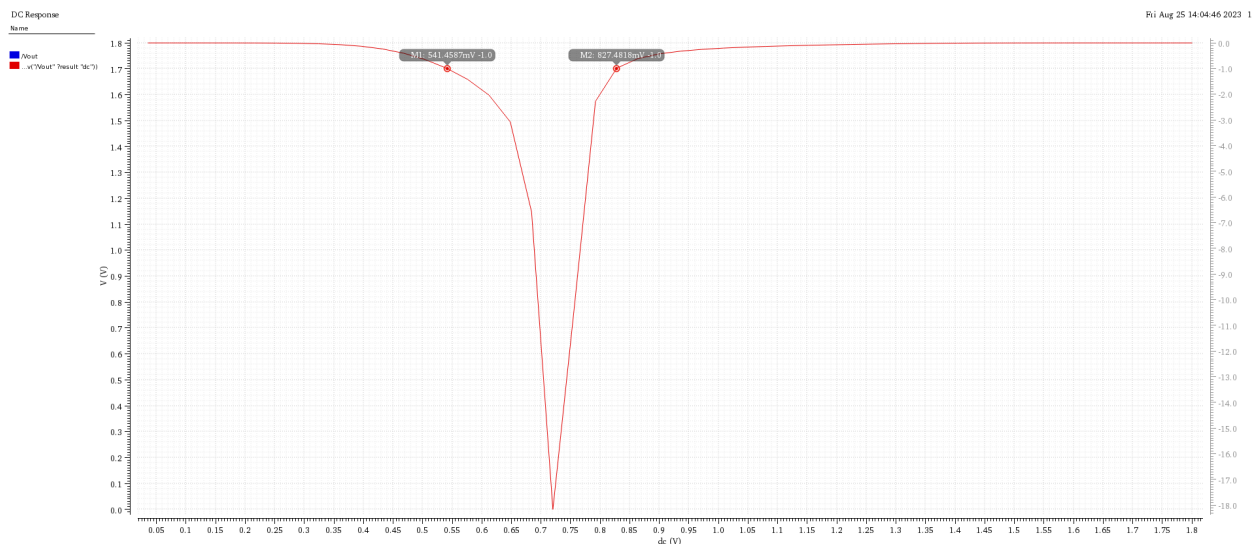
1) Plot of V_{out} vs V_{in} :



Initially when V_{in} is LOW, the PMOS transistor is ON and operating in the linear region while NMOS is OFF. As we increase V_{in} , NMOS is switched ON but since V_{out} , which is the drain potential of NMOS, is still HIGH, NMOS kicks into saturation.

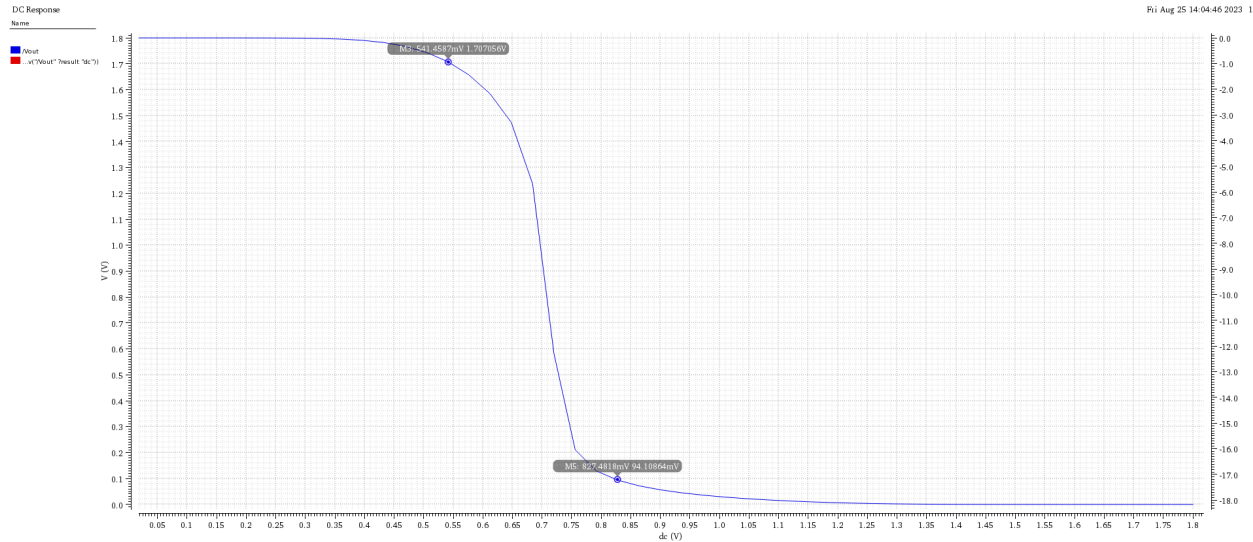
Then as we still increase V_{in} , there comes a point where both the transistors are in saturation (switching threshold). After this the behavior of the two transistors is the exact reverse of the behavior before the switching threshold.

2) Plot of dV_{out}/dV_{in} vs V_{in} :



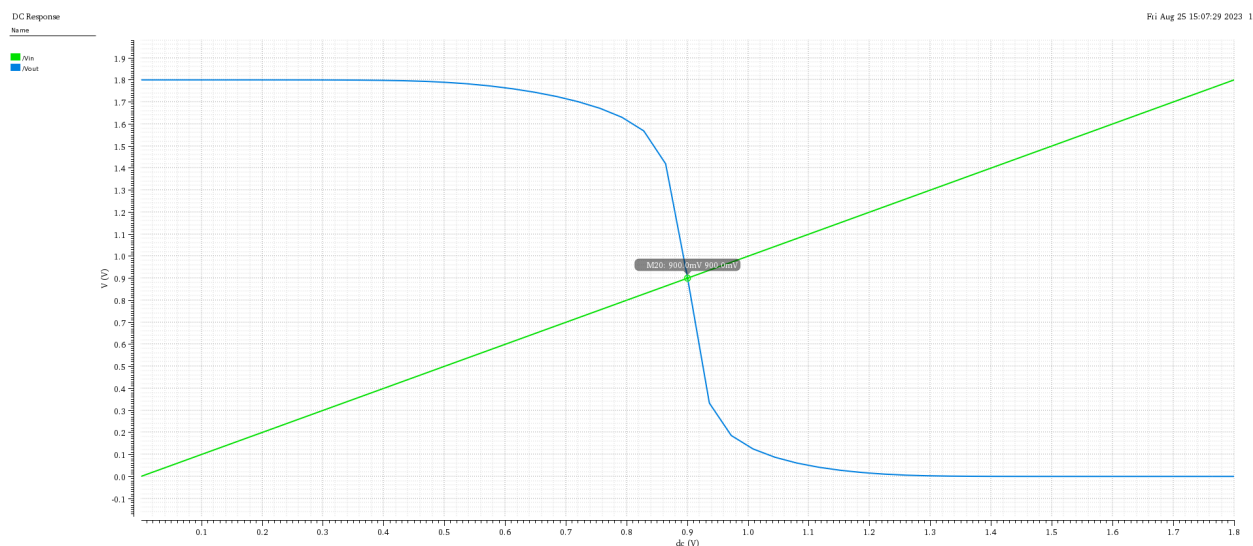
The derivative dV_{out}/dV_{in} is minimum (maximum negative) in the transition region where the plot of V_{out} vs V_{in} is the steepest.

4) Calculating the values V_{IL} , V_{IH} , V_{OH} , V_{OL} :



We can obtain the points of V_{IL} and V_{IH} from the graph by taking the derivative of the plot and plotting against the input. Then, we can map the points with derivative = -1 on the original plot to get the ordered pairs, (V_{IL}, V_{OH}) & (V_{IH}, V_{OL}) .

5) Plot of ideal switching characteristics, $V_m = V_{DD}/2$:



The switching threshold is defined as the point of intersection of the VTC with the line $V_{in} = V_{out}$. To get a symmetric switching threshold, we varied the PMOS widths by trial and error to obtain the desired solution.

Metrics Measured:

$$V_M = 712.09 \text{ mV}$$

$$V_{IL} = 541.4587 \text{ mV}$$

$$V_{OL} = 94.10864 \text{ mV}$$

$$NM_H = 0.87957 \text{ V}$$

$$V_{IH} = 827.4818 \text{ mV}$$

$$V_{OH} = 1.707056 \text{ V}$$

$$NM_L = 0.44735 \text{ V}$$

$$W_p/W_n = 5.0625 \text{ (For symmetrical transfer characteristics)}$$

Conclusion:

In this experiment we learnt how to design a CMOS inverter in Cadence. Also, we learnt how to calculate the different design metrics such as V_{IL} , V_{IH} , V_{OH} , V_{OL} , etc. from the plot.

Finally, we were able to obtain a symmetric switching threshold, that is, the range of input voltages for which the output is HIGH is equal to that when it is LOW.