VLSI LAB Experiment-7 JK Flip Flop design using Static CMOS, Pass Transistor, & Transmission Gate Logic Styles

Group Number: 2

Group Members:
Thathapudi Sanjeev Paul Joel - 2020AAPS0120H
Aditya Anirudh - 2020AAPS0373H

Design Workout:

29/09/23 | Lab-7 | JK Flip Flop using Static CMOS, PTL & TGL.

① Excitation Table

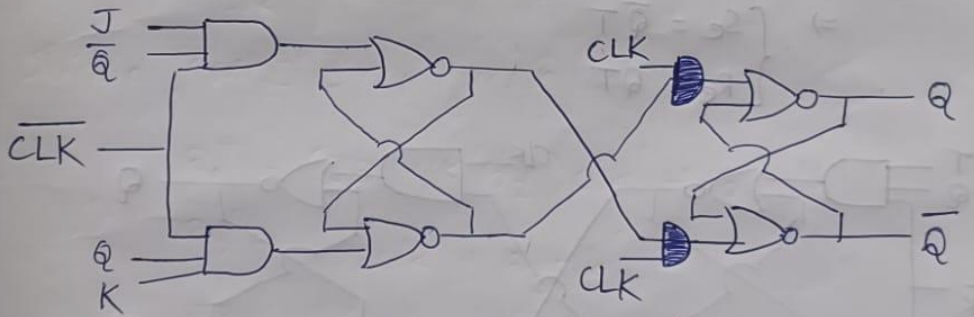
Q	J	K	Q^+	Se	Re
0	0	0	0	0	X
0	0	1	0	0	X
0	1	0	1	1	0
0	1	1	1	1	0
1	0	0	1	X	0
1	0	1	0	0	1
1	1	0	1	X	0
1	1	1	0	0	1

Q \ JK	00	01	11	10
0	0	0	1	1
1	X	0	0	X

$Q^+ = J\bar{Q}$

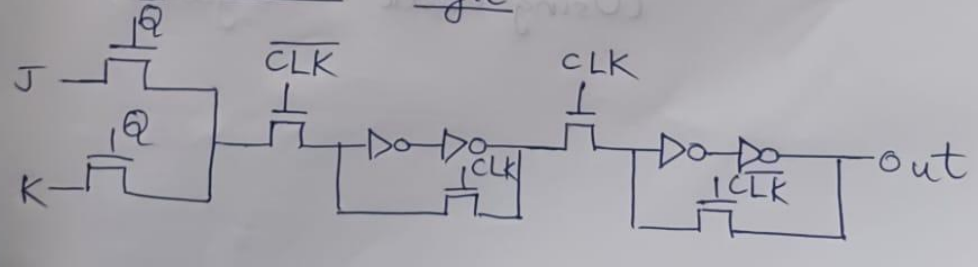
Q \ JK	00	01	11	10
0	X	X	0	0
1	0	1	1	0

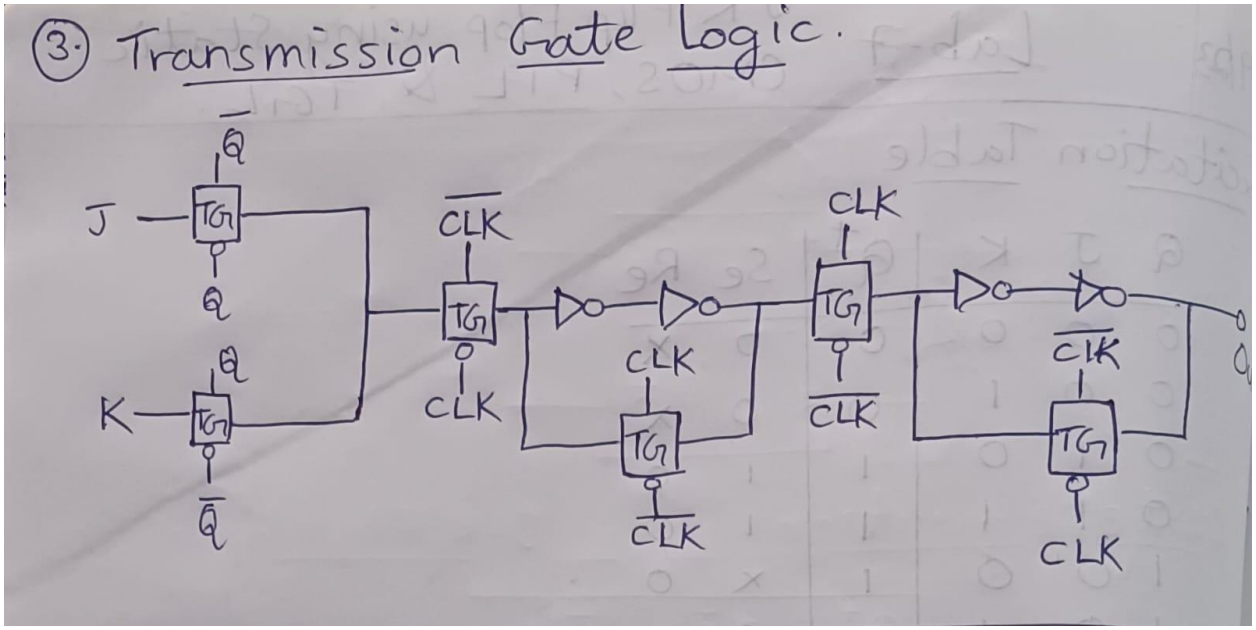
$Q^+ = KQ$



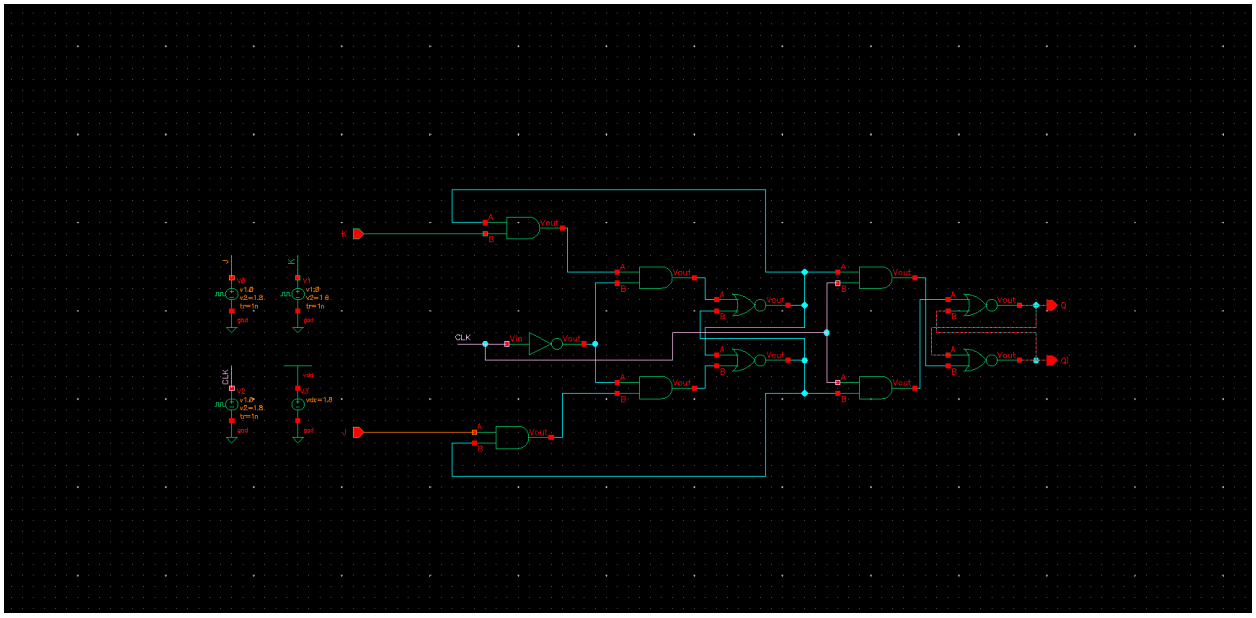
+ve-edge triggered J-K Flip flop (Using static CMOS gates.)

② Pass Transistor logic





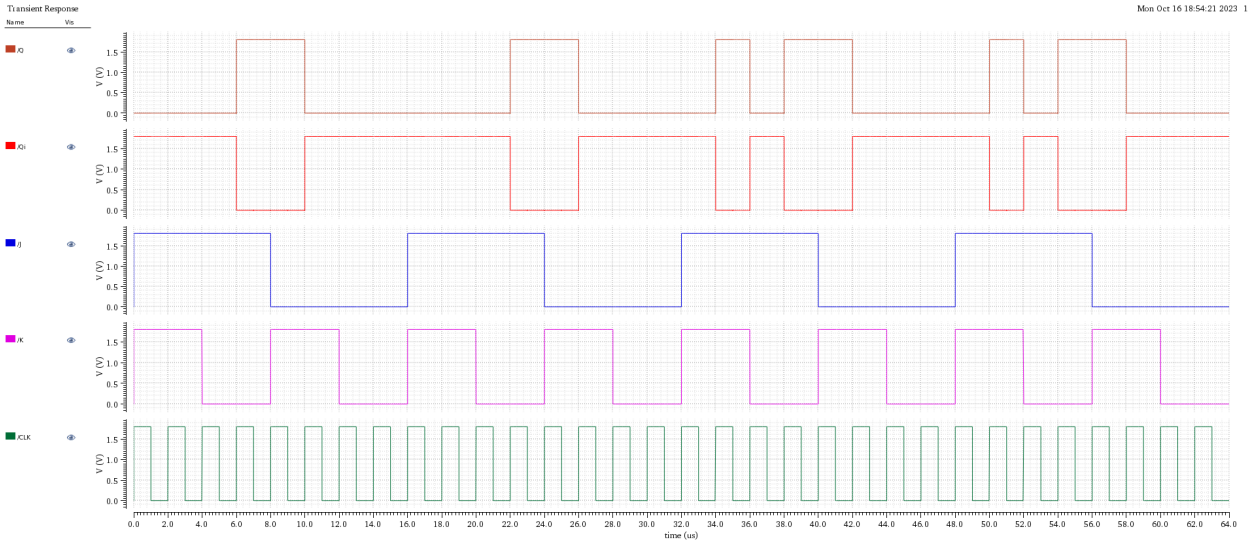
Schematic:



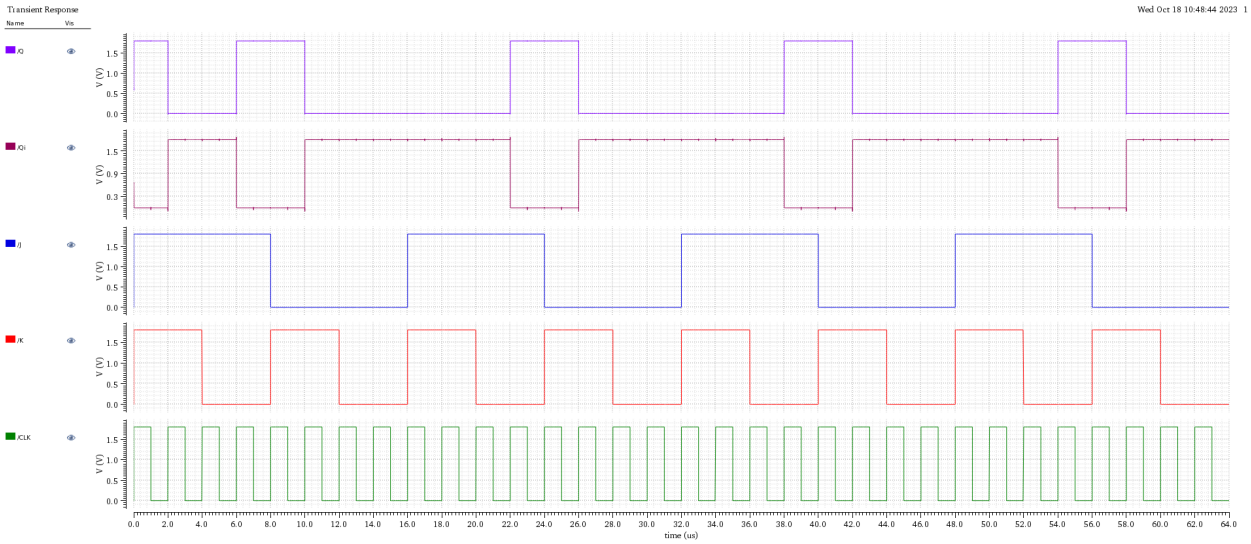
Waveforms:

JK Flip Flop using CMOS:

JK Flip Flop using PTL:



JK Flip Flop using TGL:



Metrics Measured:

1. JK Flip Flop using Static CMOS:
   $t_{clk\text{-}Q(LH)}$ = 374.4 ps
   $t_{clk\text{-}Q(HL)}$ = 300.6 ps
   Power dissipation = 121.8 µW

2. JK Flip Flop using Pass Transistors:
   $t_{clk\text{-}Q(LH)}$ = 782.3 ps
   $t_{clk\text{-}Q(HL)}$ = 63.72 ps
   Power dissipation = 87.56 µW

3. JK Flip Flop using Transmission Gates:
   $t_{clk\text{-}Q(LH)}$ = 270.8 ps
   $t_{clk\text{-}Q(HL)}$ = 770.1 ps
   Power dissipation = 50.32 µW

Inferences:

1. The clocked-Q delay in the case of pass transistor logic is very low for a high-to-low transition as compared to the other logic styles.
2. Level Restorers had to be used to deal with the logic degradation problem while designing the Flip Flop using Pass Transistors.

3. No of transistors:
   PTL < TGL < Static CMOS logic
4. The power dissipation is the largest in Static CMOS approach because the gates directly draw the power from the V_{DD} rails.

Conclusion:

In this experiment, we designed a **JK-flip flop** using **master-slave configuration of latches** in the *Static CMOS*, *Pass Transistor*, and *Transmission Gate Logic styles*. We then compared their performances with respect to the metrics like **clocked-Q delay** and **power dissipation**.