VLSI LAB Exercise-5 8:1 MUX using Pass Transistors and level restoring circuit

Group Number: 2

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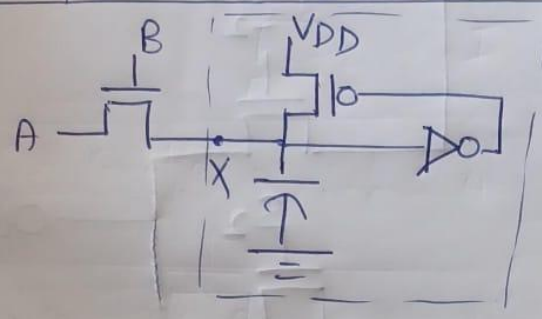
Design Workout:

25/09/23 | Exe-5 | 8:1 MUX & Level Restorer



Level Restorers are used in

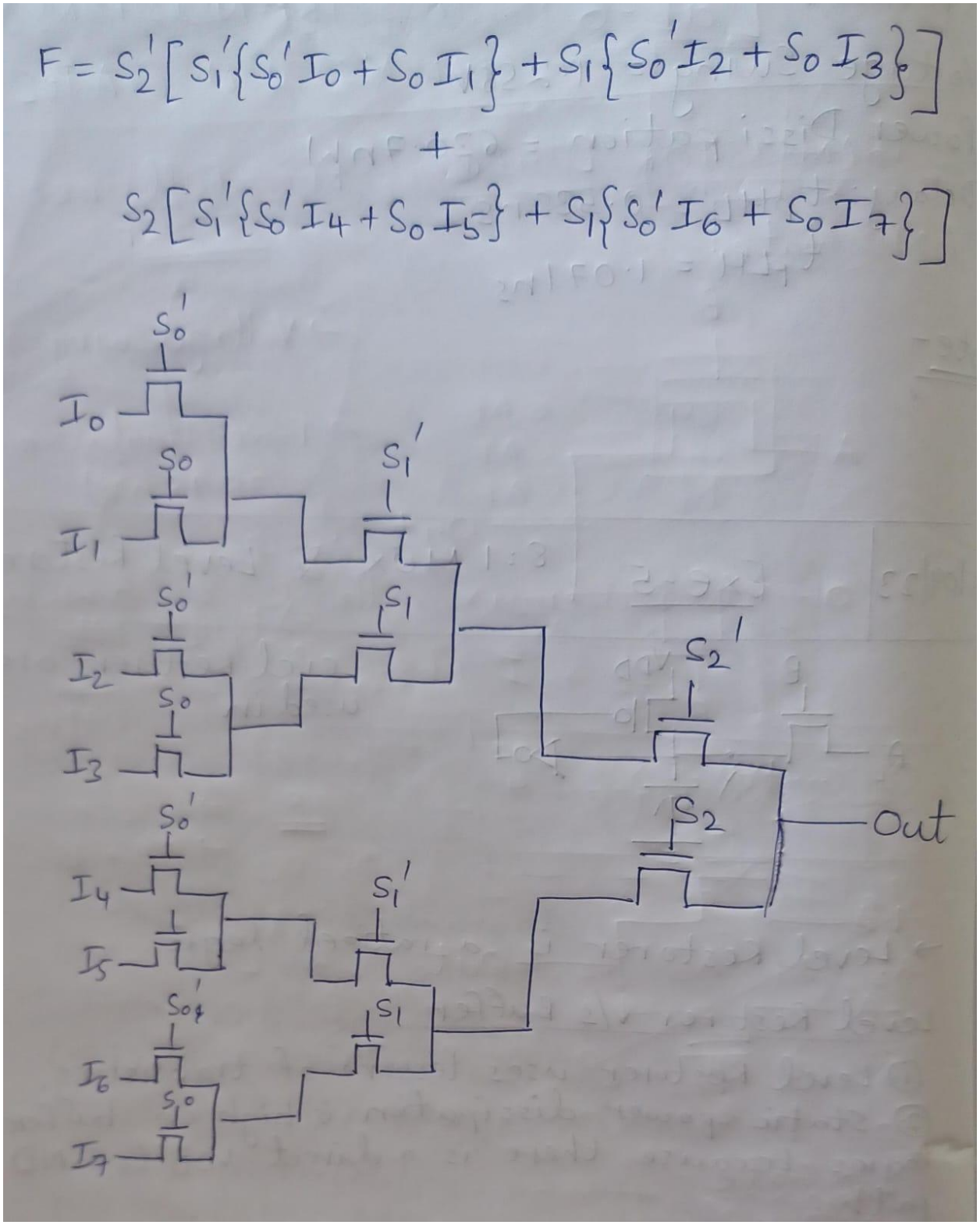
→ Level Restorer is a ratioed logic.

Level Restorer v/s Buffer

① Level Restorer uses lesser no. of transistors.
② Static power dissipation is high in buffered logics because there is a direct VDD to GND path.
③ Delay is lower in level restorer.
④ Even then buffers are used because it's quite difficult to size the transistors in level restorers.

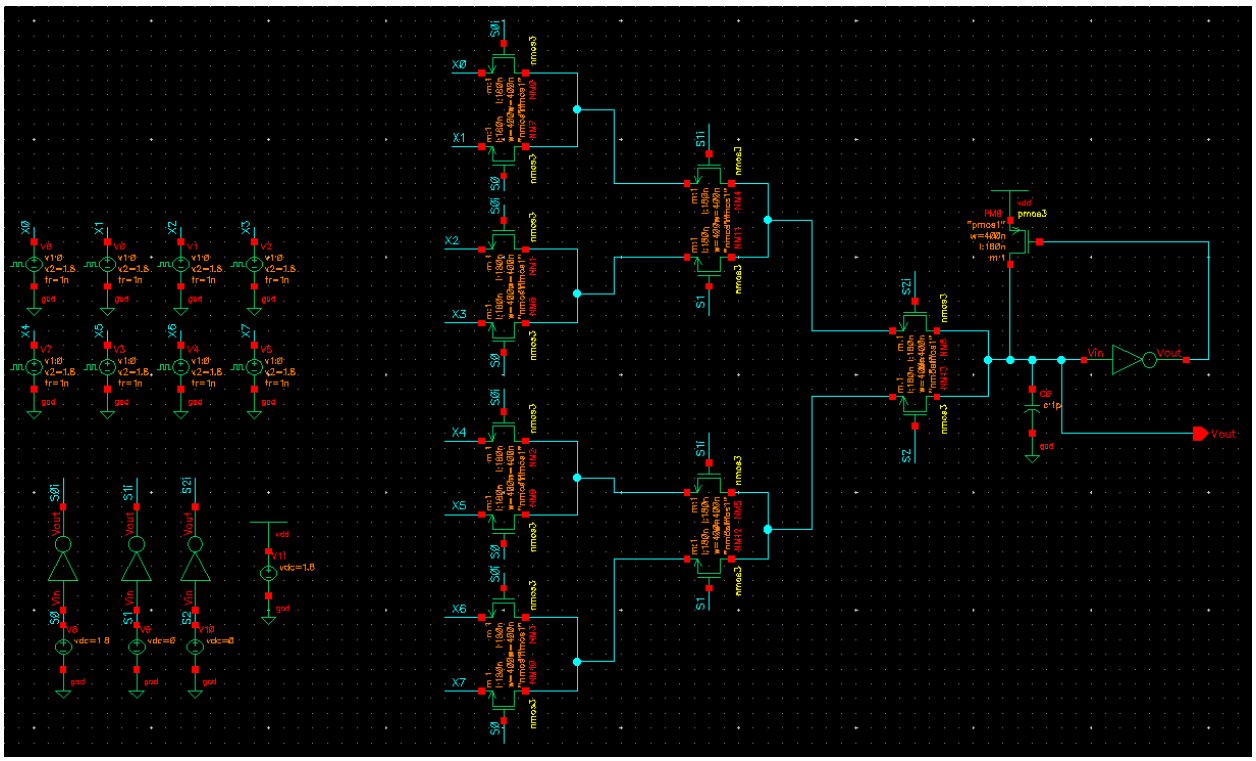
$F = S_2'S_1'S_0'I_0 + S_2'S_1'S_0 I_1 +$
- - — —

$$F = S_2'\left[S_1'\{S_0' I_0 + S_0 I_1\} + S_1\{S_0' I_2 + S_0 I_3\}\right] + S_2\left[S_1'\{S_0' I_4 + S_0 I_5\} + S_1\{S_0' I_6 + S_0 I_7\}\right]$$

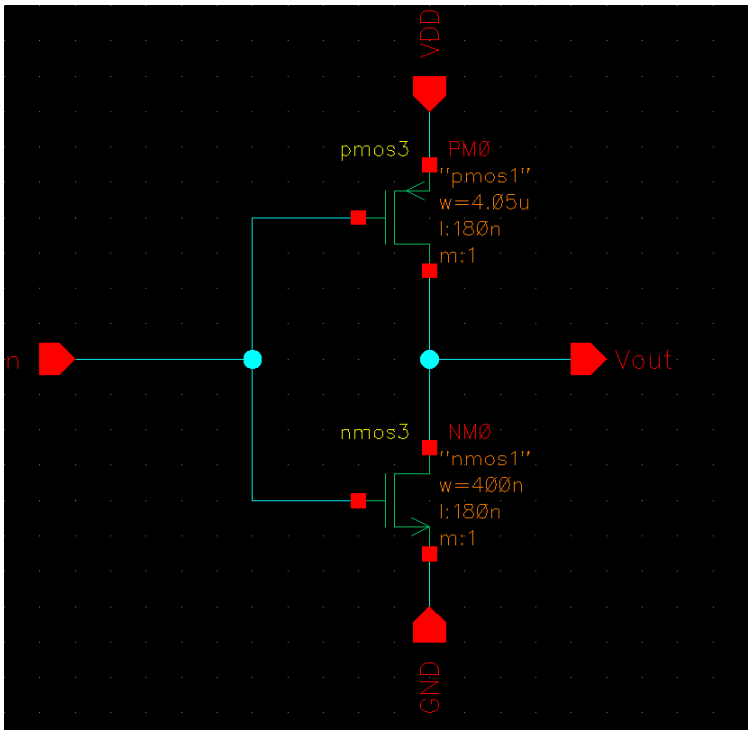


Schematics:

8:1 MUX Schematic:-



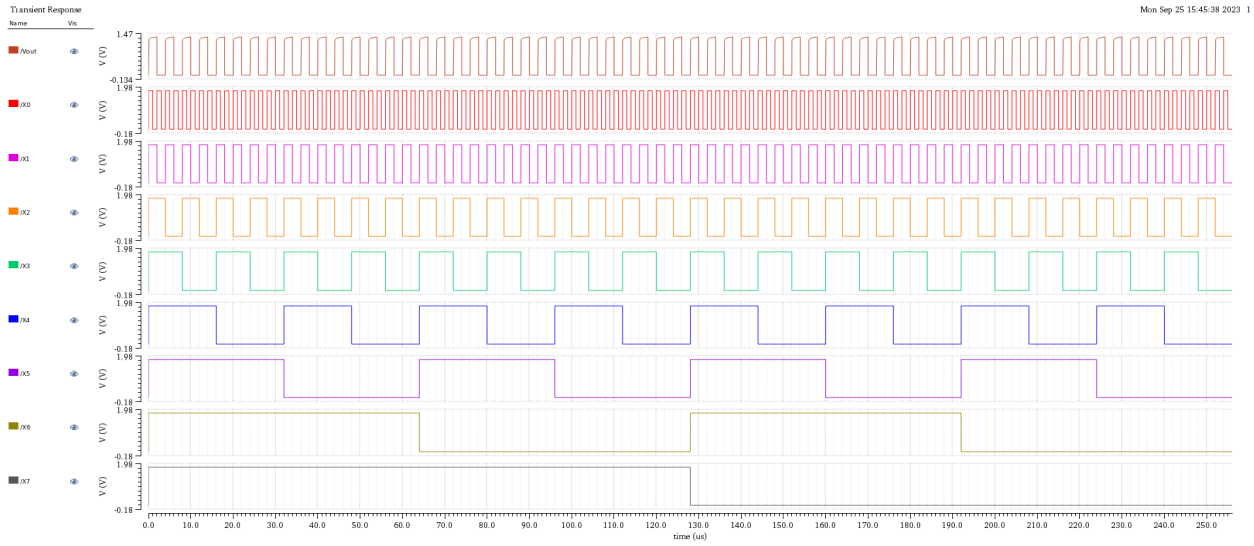
Inverter Modification:-



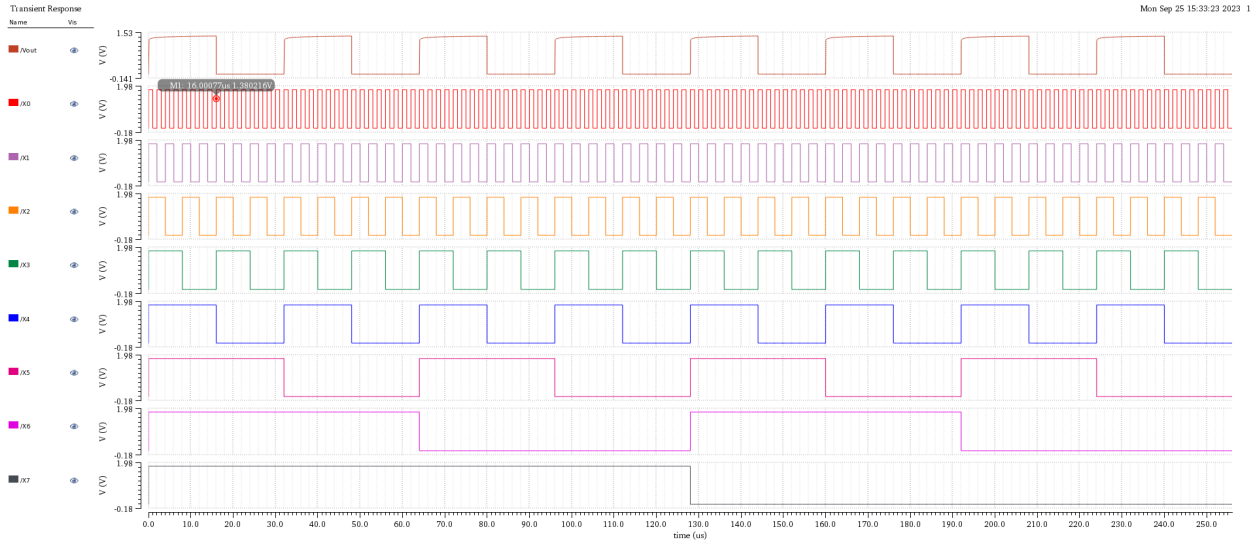
Waveforms:

Before using a level restorer:-

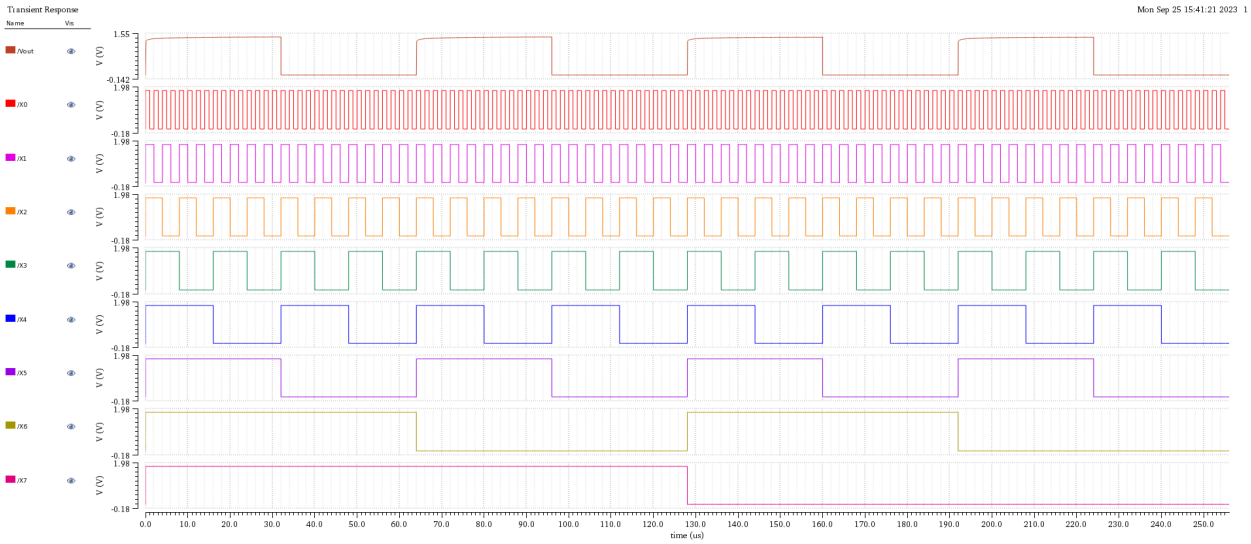
For $S_2S_1S_0 = I_1$:



For $S_2S_1S_0 = I_4$:

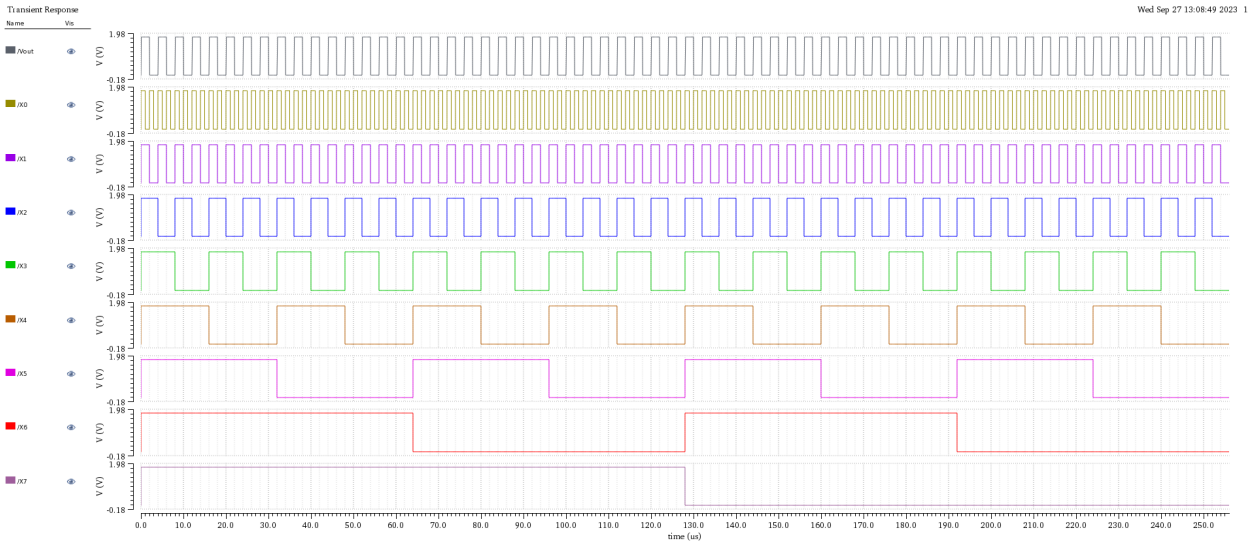


For $S_2S_1S_0 = I_5$:

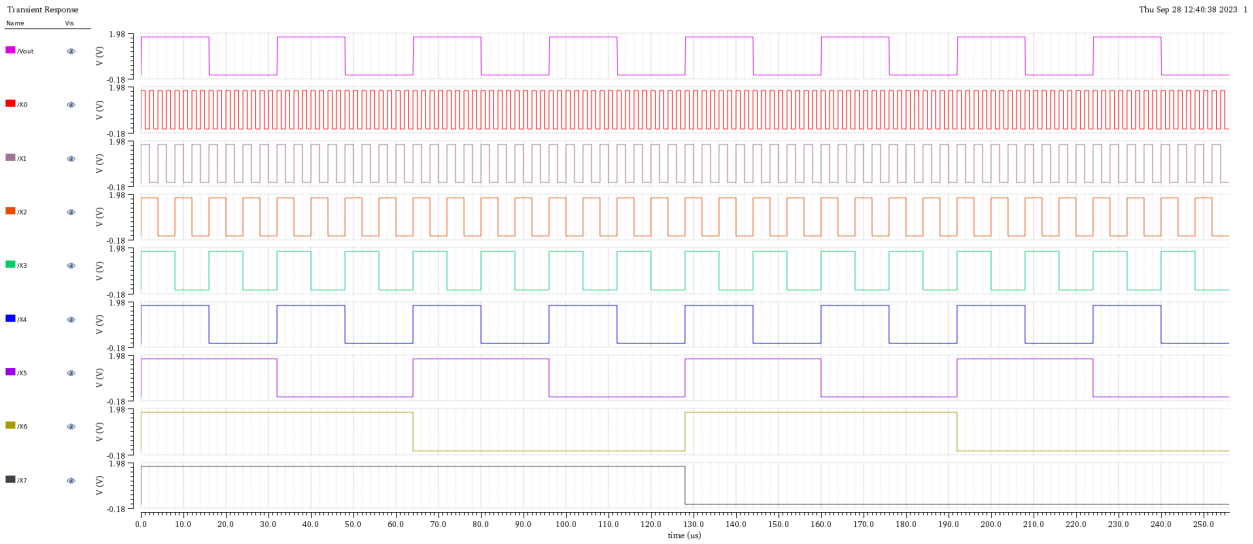


After using a level restorer:-

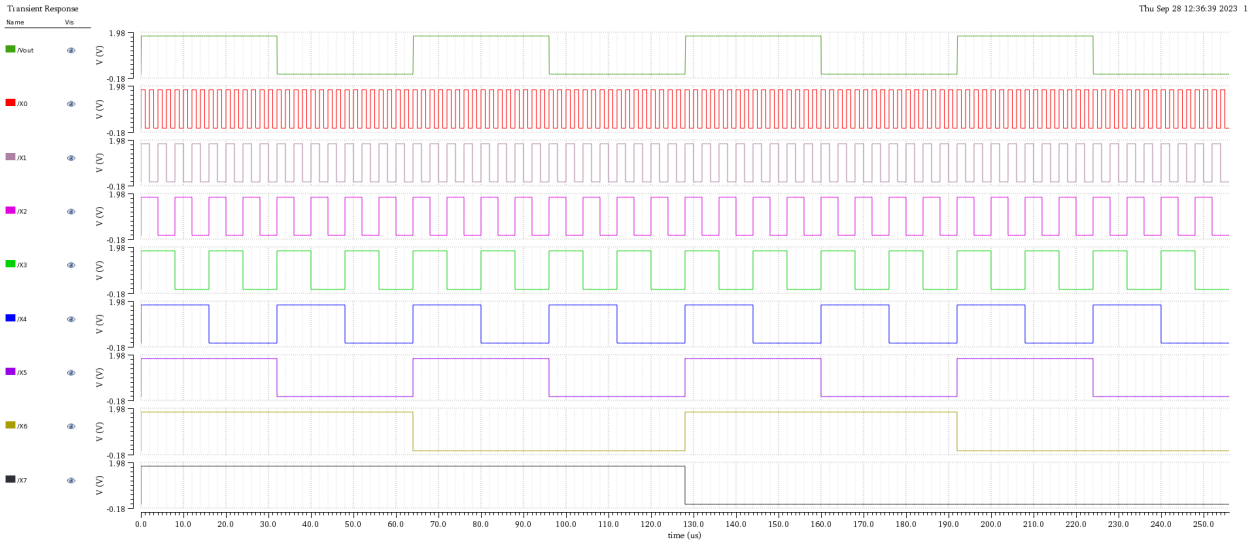
For $S_2S_1S_0 = I_1$:



For $S_2S_1S_0 = I_4$:



For $S_2S_1S_0 = I_5$:



<u>Metrics Measured</u>:

All the analysis below has been done by fixing NMOS width of the inverter, and varying the PMOS width of the level restorer and inverter present in level restorer.

1. $W_{P\text{-level restorer}}$ = 400 nm, $W_{P\text{-inverter}}$ = 400 nm:
   t_{pHL} = 12.16 ns
   t_{pLH} = 12.2 ns

Power dissipation = 182.2 nW

2. $W_{P\text{-level restorer}}$ = 400 nm, $W_{P\text{-inverter}}$ = 2.025 µm:
   t_{pHL} = 11.44 ns
   t_{pLH} = 20.32 ns
   Power dissipation = 205.6 nW

3. $W_{P\text{-level restorer}}$ = 800 nm, $W_{P\text{-inverter}}$ = 4.675 µm:
   t_{pHL} = 1.359 ns
   t_{pLH} = 21.16 ns
   Power dissipation = 13.17 µW

Inferences:

1. To make the circuit perform a rail-to-rail swing, we need to size the level restorer components: PMOS transistor and inverter appropriately. Fixing the width of the NMOS transistor (here at 400 nm) in the inverter, we can alter the values of PMOS transistors to get the desired voltage swing. **Notably, the PMOS in the inverter should be able to pull up the input to the other PMOS transistor as quickly as possible so it has to be sized larger than the PMOS performing the level restoration. This is to ensure that the latter PMOS gets switched OFF as quickly as possible.**

2. By fixing the width of the level restorer PMOS, if we try to **improve the high-to-low transitional delay** of the circuit, **by increasing the inverter's PMOS width**, we would pay for **increased delay for the low-to-high transition** and **increased power dissipation**. This is **because** of the **decreased relative pull-down strength of NMOS in the inverter** and **increase in the net average current** in the circuit respectively.

3. If we **increase the width of the level restorer PMOS** and **sufficiently size the PMOS of inverter for proper level restoration**, then the **high-to-low transitional delay is improved drastically due to a high rise in the current delivered by level restorer PMOS**. However, we **penalize** the circuit by the **increased delay in the low-to-high transition** and **drastic rise in the power dissipated as the average current consumed by the circuit increases**.

Conclusion:
In this exercise, we first designed an 8:1 MUX using only pass transistors. Later, on observing that the circuit **does not have a complete rail-to-rail swing**, we inserted a **level restoring circuit** consisting of an inverter and a PMOS transistor in the feedback path to **restore the level of the waveforms generated**. Finally, we observed that by including the level restorer, although we have gained a complete rail-to-rail voltage swing, as a tradeoff, we have **added chip area (more transistors)**, **increased delay** and **power dissipation**.