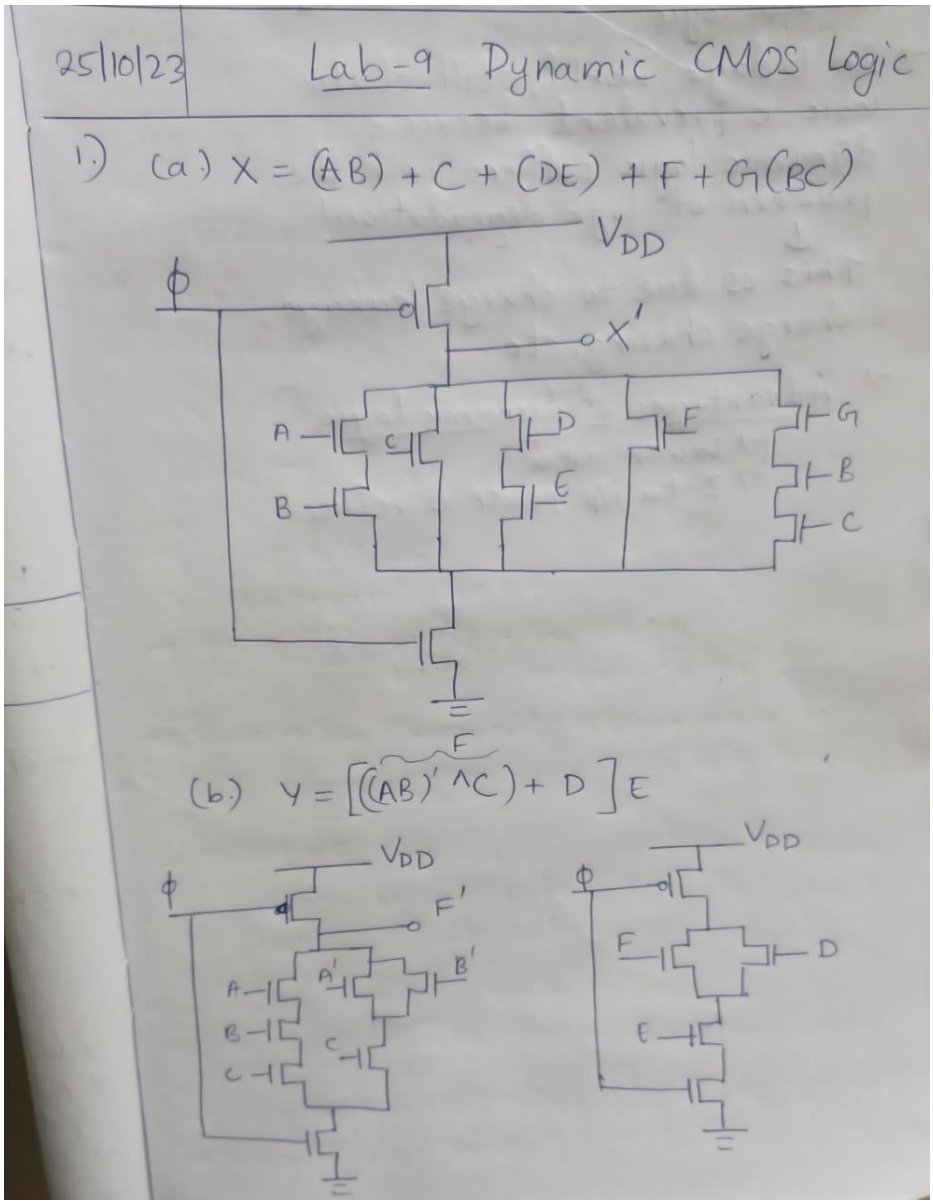
VLSI LAB Experiment-9 Dynamic Logic

Group Number: 2

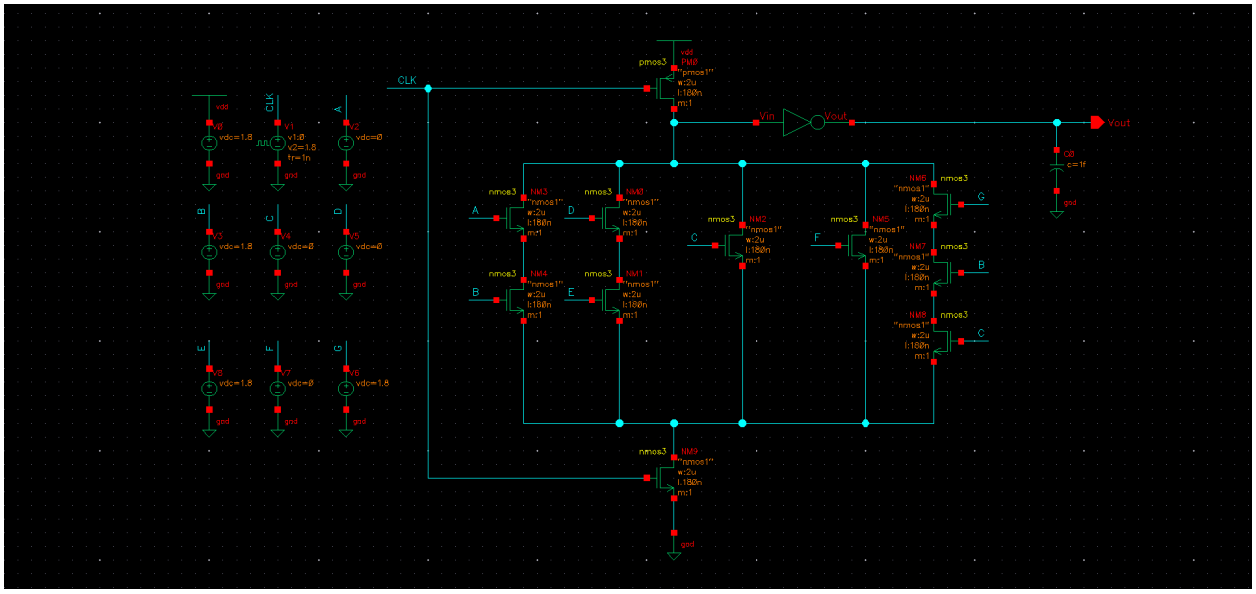
Group Members:
Thathapudi Sanjeev Paul Joel - 2020AAPS0120H
Aditya Anirudh - 2020AAPS0373H

Design Workout:

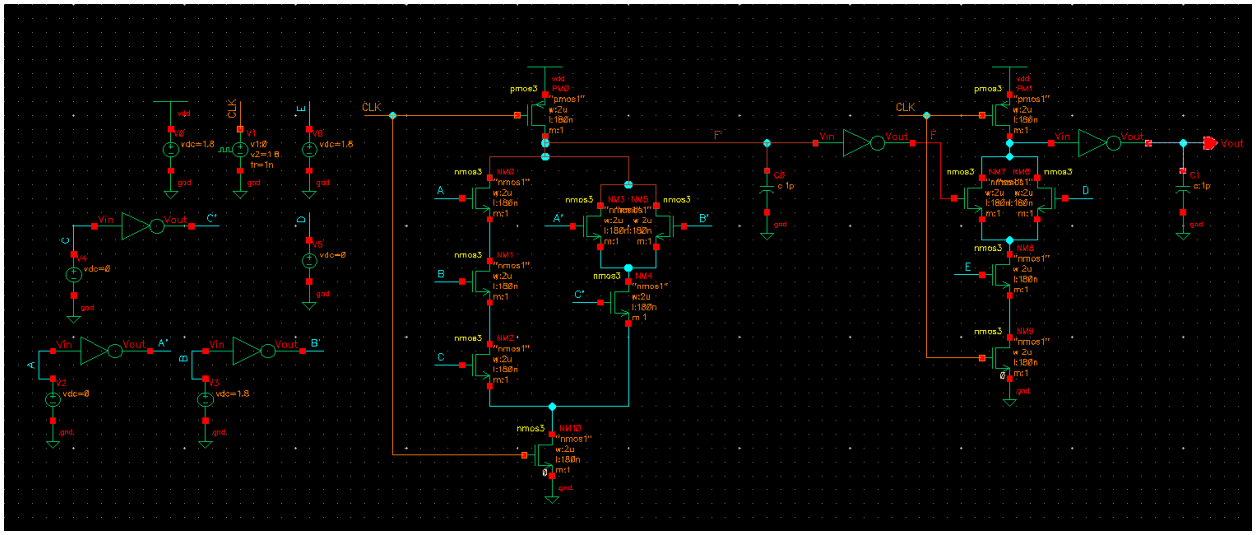


Schematic:

Circuit - 1:-



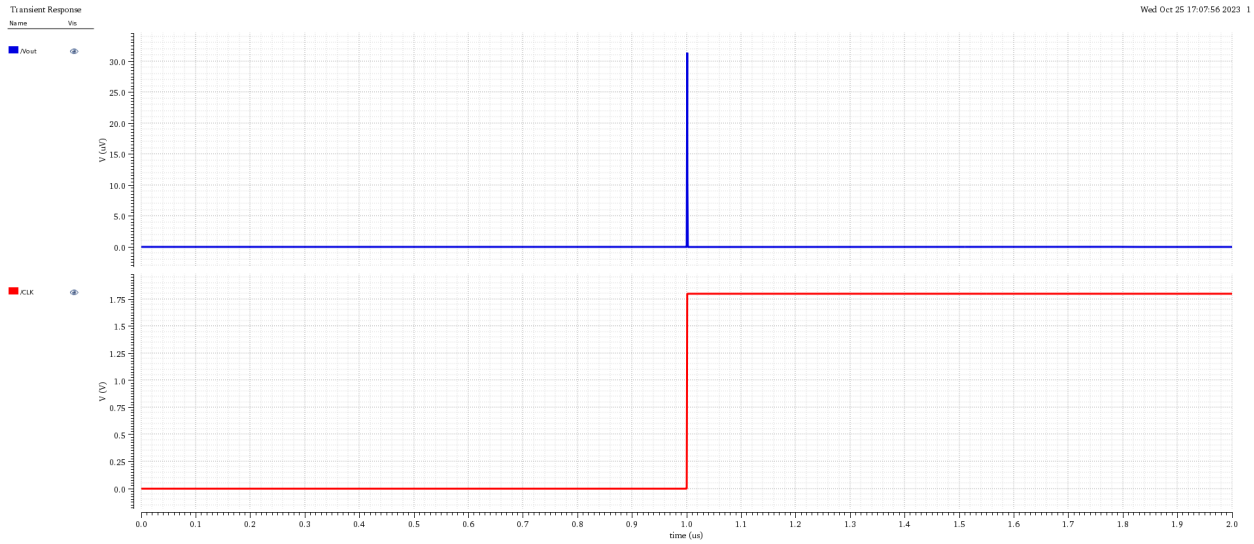
Circuit - 2:-



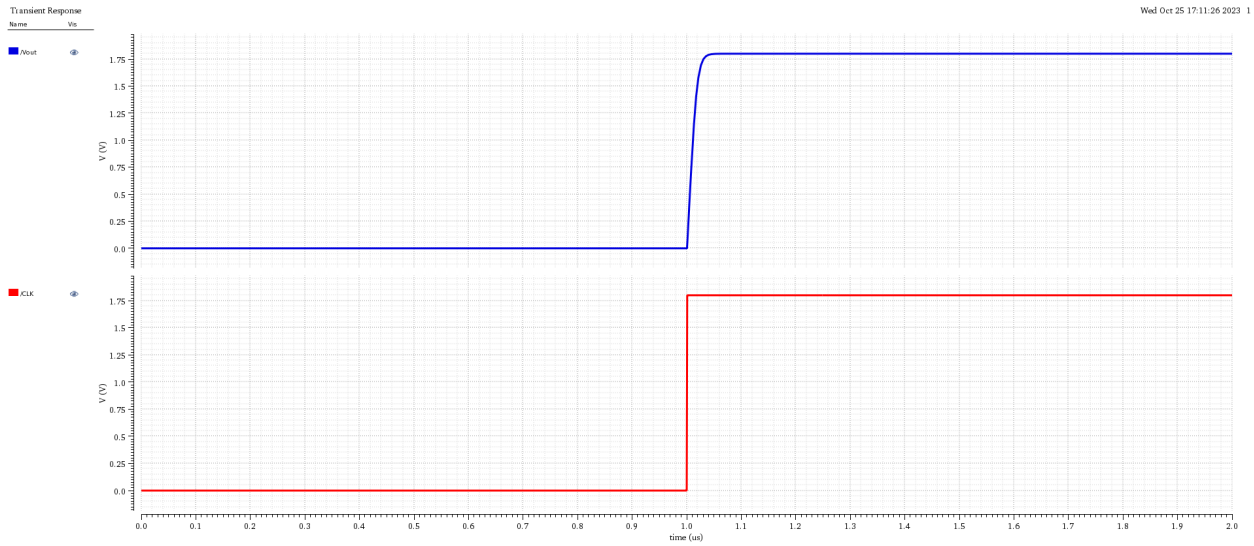
Waveforms:

Circuit - 1:-

Input: A = 0, B = 1, C = 0, D = 0, E = 1, F = 0, G = 1

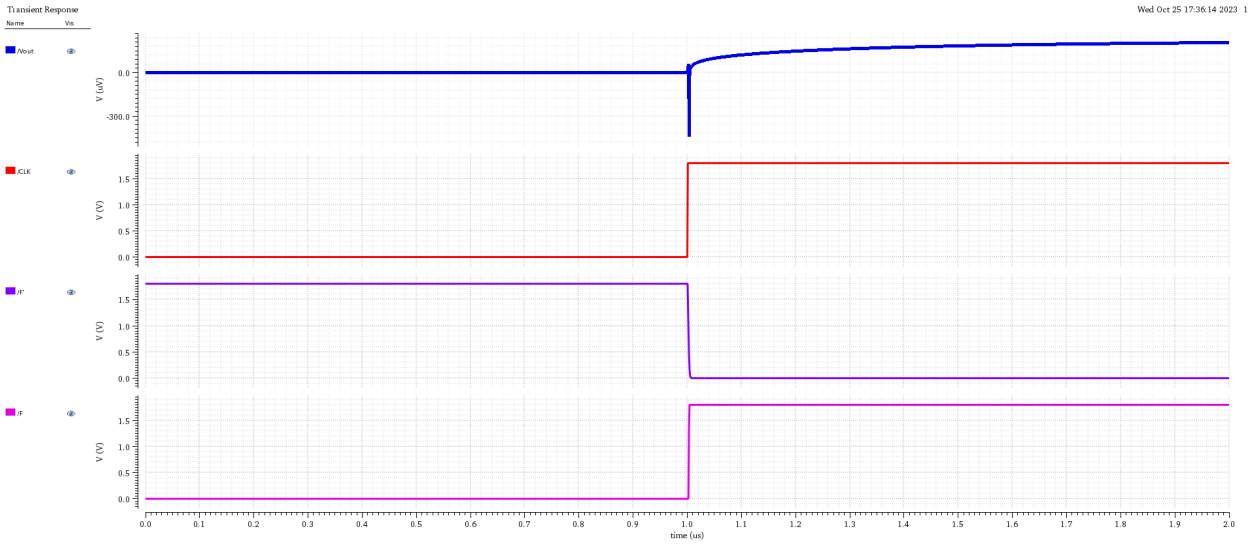


Input: A = 0, B = 1, C = 0, D = 0, E = 1, F = 1, G = 1



Circuit - 2:-

Input: A = 0, B = 1, C = 0, D = 0, E = 0



Input: A = 0, B = 1, C = 0, D = 0, E = 1

Input: A = 0, B = 1, C = 1, D = 0, E = 1

Inferences:

1. In the second excitation sequence provided to circuit-1, the output response equals ‘1’ after the evaluation phase as F = 1.
2. For circuit-2, the excitations covering three possible cases are given:
   a. Stage-1 is evaluated while stage-2 is not.
   b. Both the stages are evaluated.
   c. Both the stages are not evaluated.
3. We can see in the third excitation sequence to circuit-2 that the output response is oscillatory (in μV). This may be due to charge/discharge through the capacitor.

Conclusion:

In this experiment, we learnt how to implement the combinational logic circuits using the **dynamic logic style**. For the first circuit, we used a simple dynamic style with an **NMOS logic block**, while for the second circuit, we implemented it using **Domino logic** i.e., **cascading two NMOS logic stages in series**.