Exercise 1

1. Design a CMOS inverter whose $\mu_n C_{ox}$ = 350 $\mu A/V^2$, $\mu_p C_{ox}$ = 70 $\mu A/V^2$ and midpoint voltage (V_{th}) is 0.8 V. Also determine the noise margin values. (Use threshold voltage values obtained from experiment 1)
2. Compare the noise margin obtained in (1) to that of the noise margin of a symmetric CMOS inverter, and comment on your observations.