VLSI LAB Exercise-3 STATIC CMOS LOGIC

Group Number: 2

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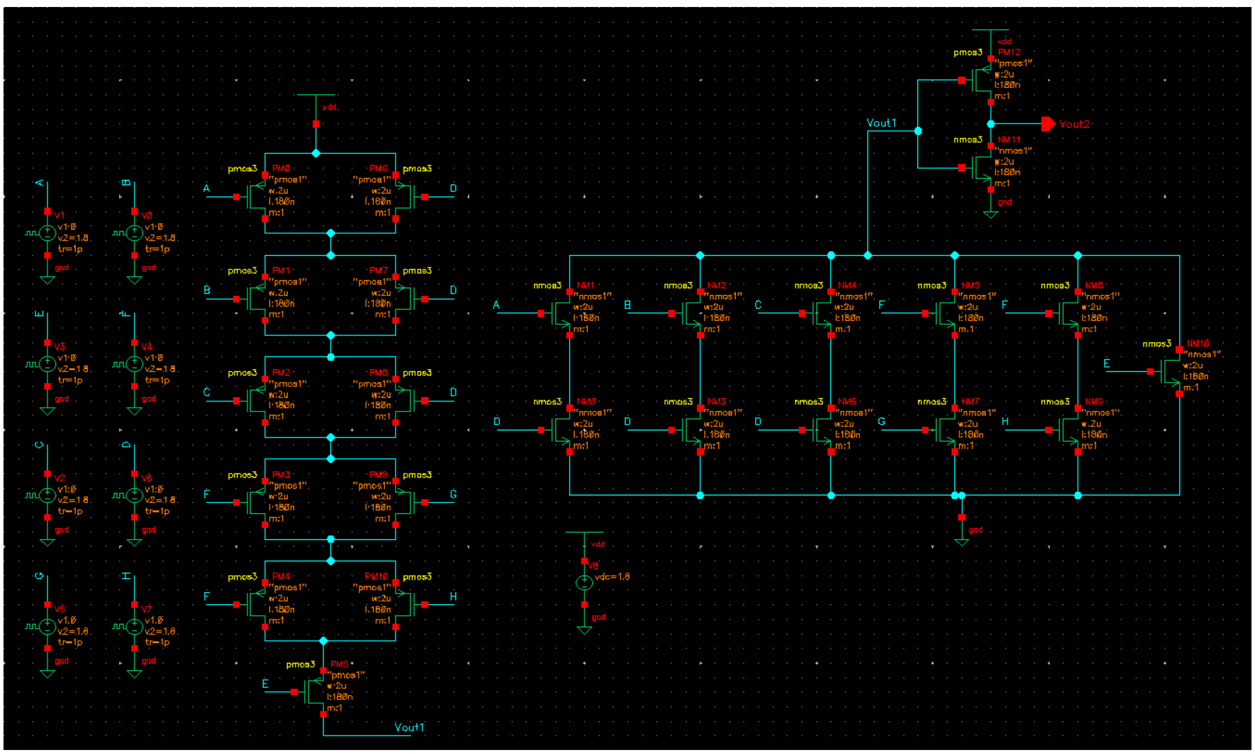
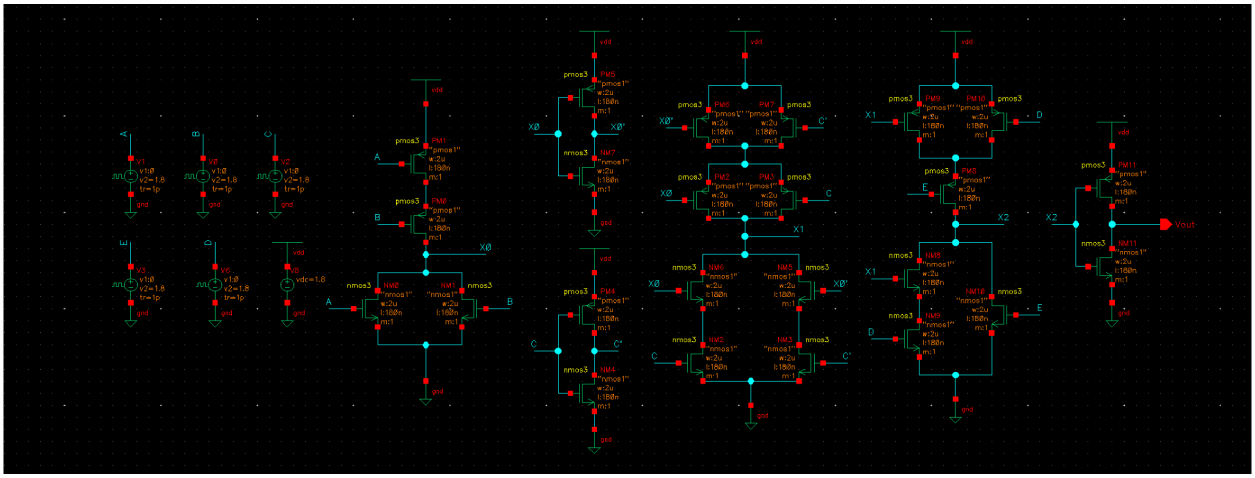
Schematics:

Schematic-1:



Schematic-2:



Design Workout:

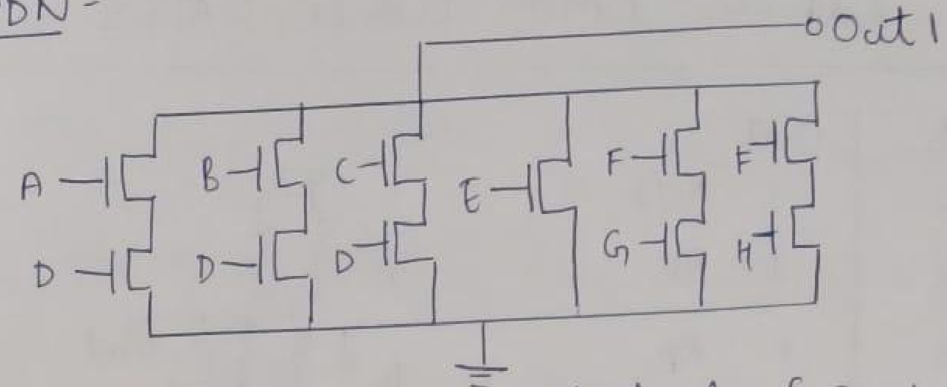
11/09/23 — Exercise - 3 STATIC CMOS CIRCUITS

1) (a) $Y = (A+B+C)D + E + F(G+H)$

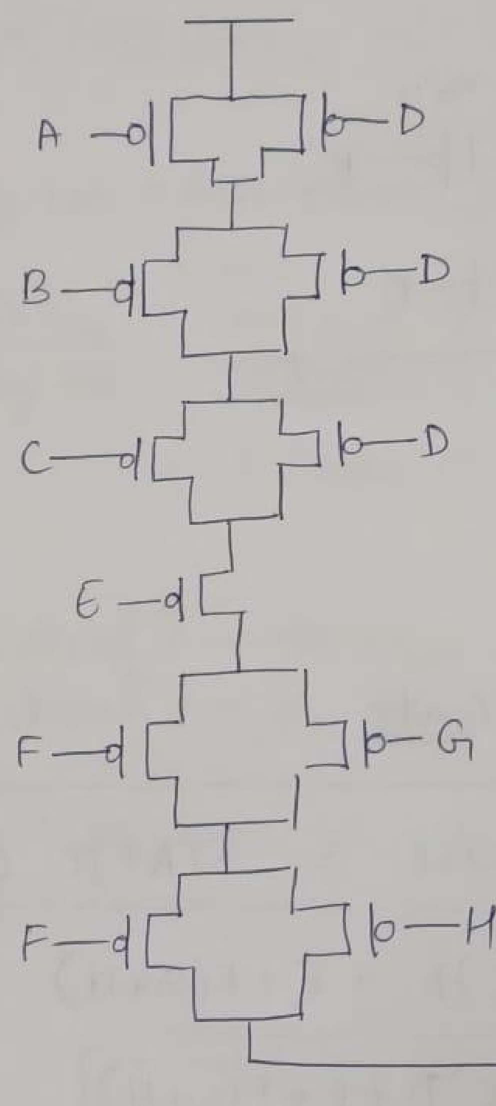
$$\overline{\overline{Y}} = \left[\overline{(A+B+C)D + E + F(G+H)}\right]$$

We can write/design PDN for this function and then pass the result through an inverter to get the final output.

PDN -



The PUN will be the exact dual of PDN ⇒



"Out 1" drives the input of another inverter to get the final result.

(b) $Z = (\overline{A+B} \wedge C)D + E$

through an inverter to get the final output

$$\overline{(\overline{A+B} \wedge C)D + E}$$

Use NOR logic to implement this function

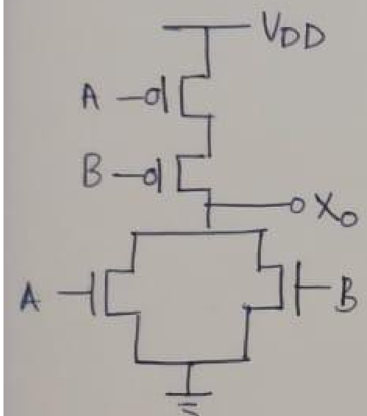
Then use the result & C values to pass them through an XOR logic

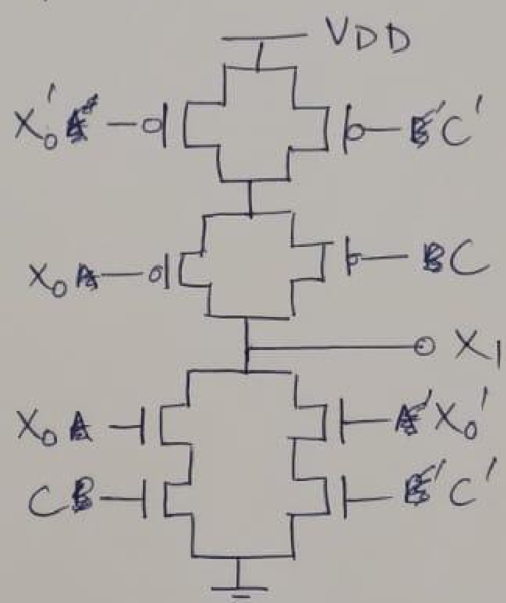
Then finally -

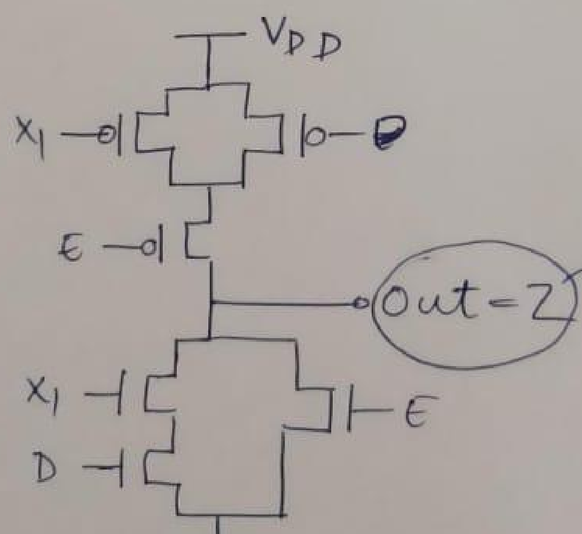
$$\overline{X_1 D + E}$$

Implement this using static CMOS Approach.

where $X_1 = (\overline{A+B} \wedge C)$.



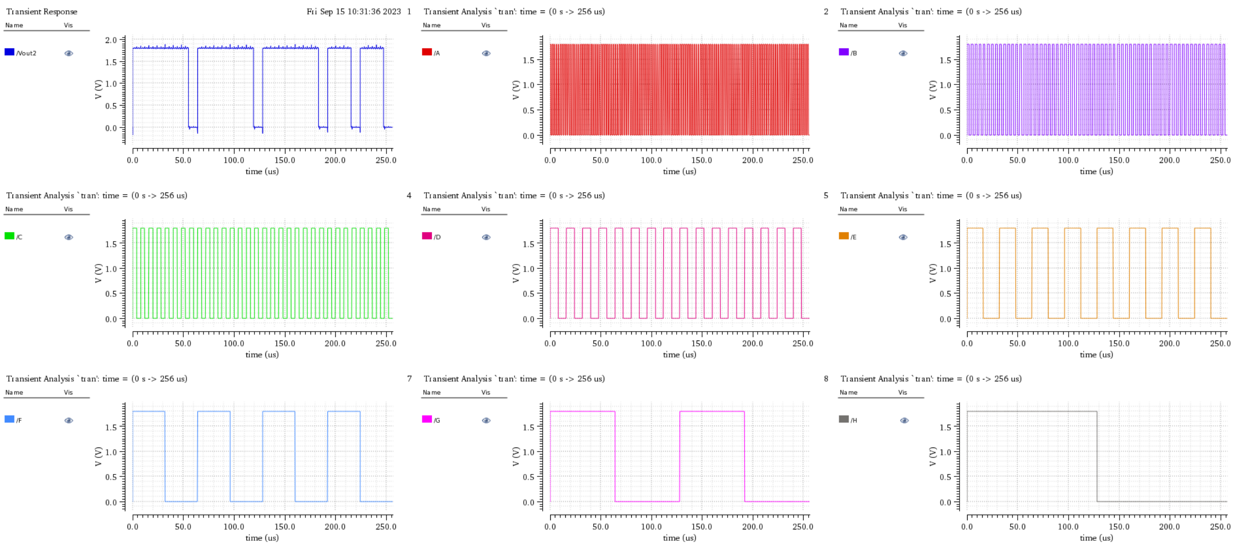


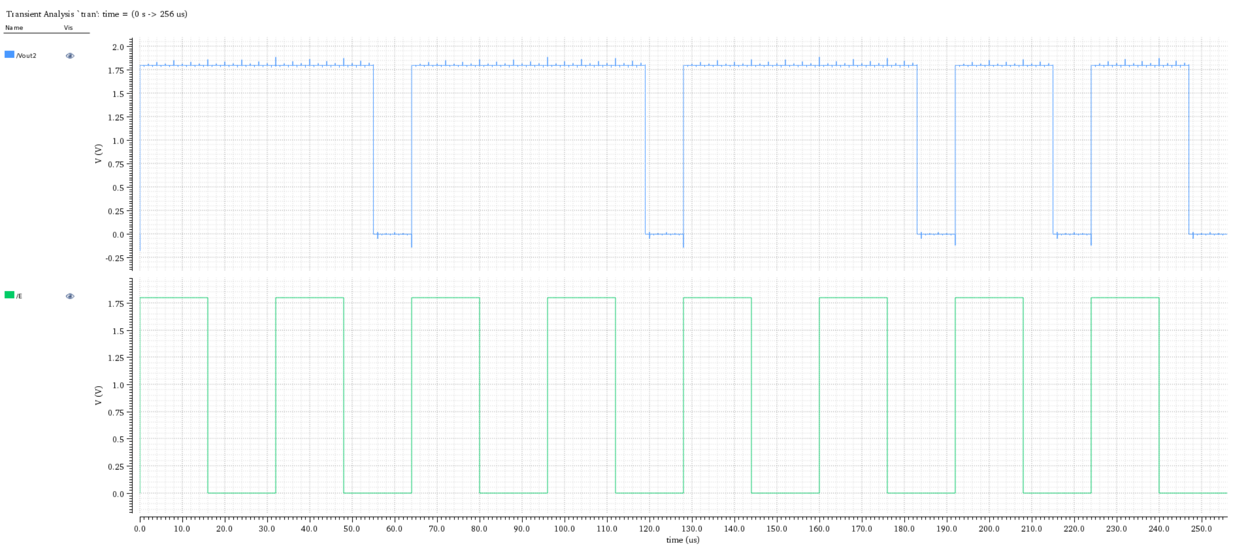


Drives another inverter to get the final result.

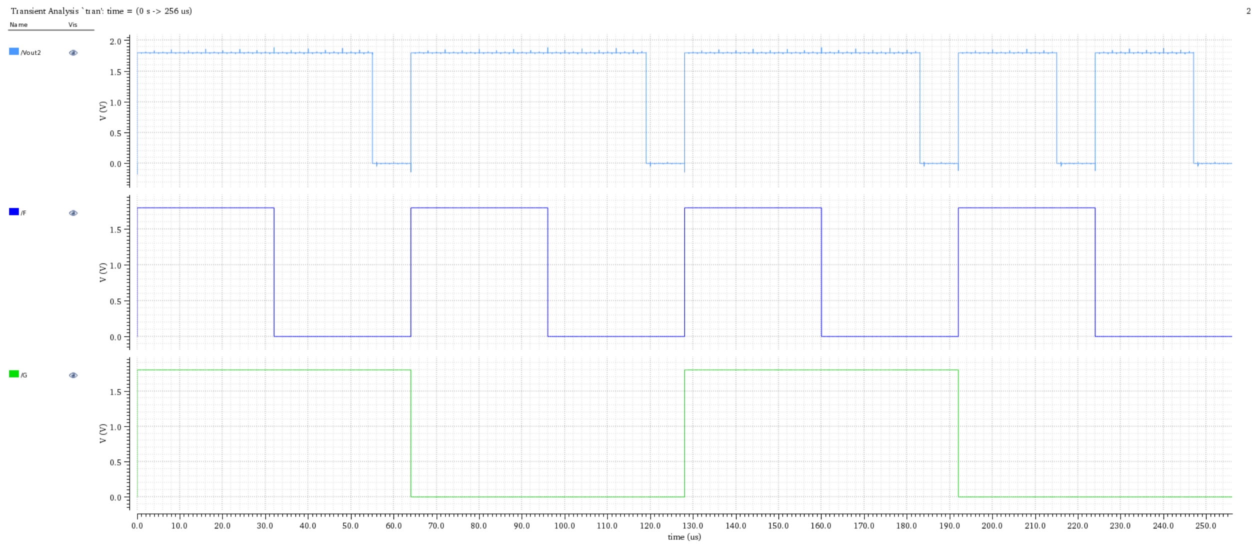
<u>Waveforms</u>:

Schematic-1:

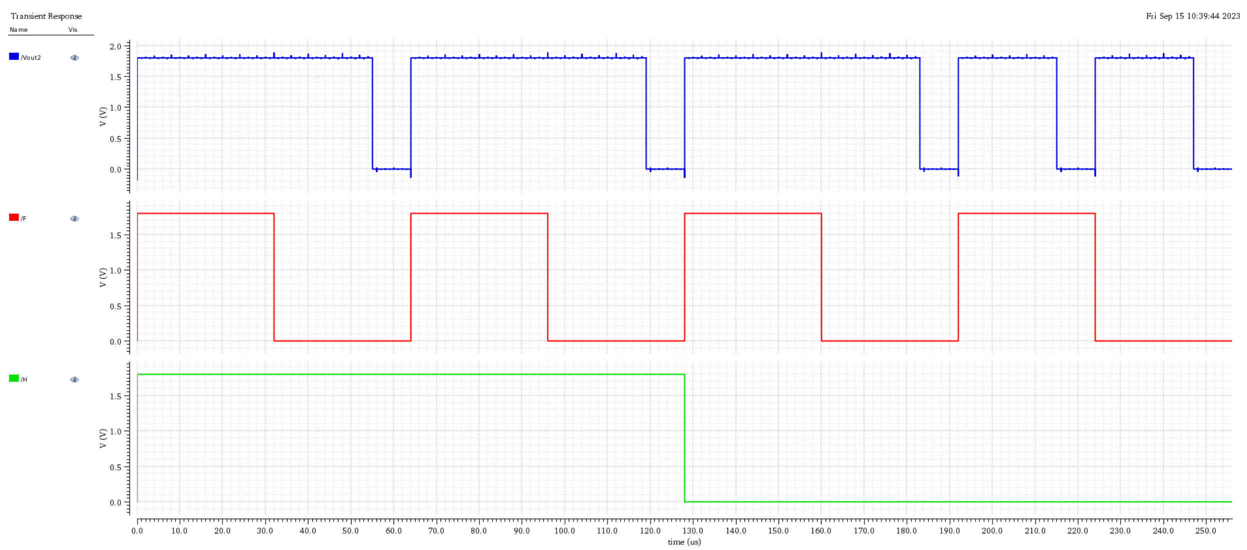




When E = HIGH, Vout2 = HIGH as expected!

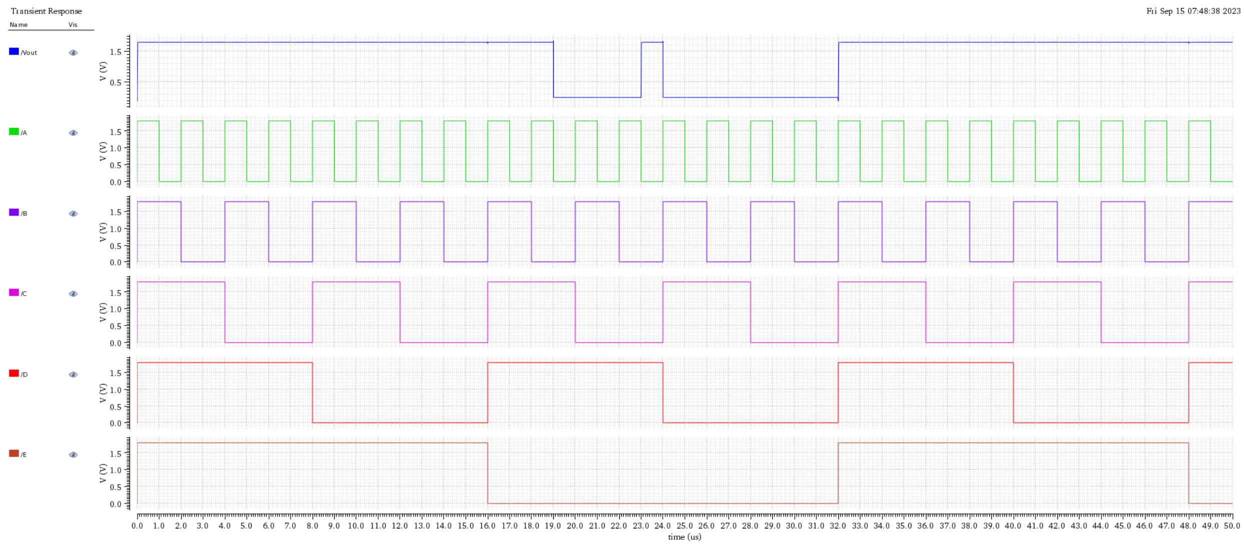


When (F & G) = HIGH, Vout2 = HIGH as expected!



When (F & H) = HIGH, Vout2 = HIGH as expected!

Schematic-2:



- When E = HIGH, Vout = HIGH as expected!
- If we find out the response of [(A + B)’ ^ C].D, we ‘ll get the range of values of the output “Vout” = HIGH that are not compensated by taking E = HIGH alone.

<u>Conclusion</u>:

In this experiment, we learnt how to design combinational logic circuits using Static CMOS Logic. In particular, we have also looked into the fact that **increasing the fan-in of CMOS circuits** leads to **higher delays** because the **resistance of the RC network increases**. This will not be the case with **cascading two/more sublogic functions** to implement the original function.