VLSI LAB Experiment-4 CMOS INVERTER SWITCHING CHARACTERISTICS

Group Number: 2

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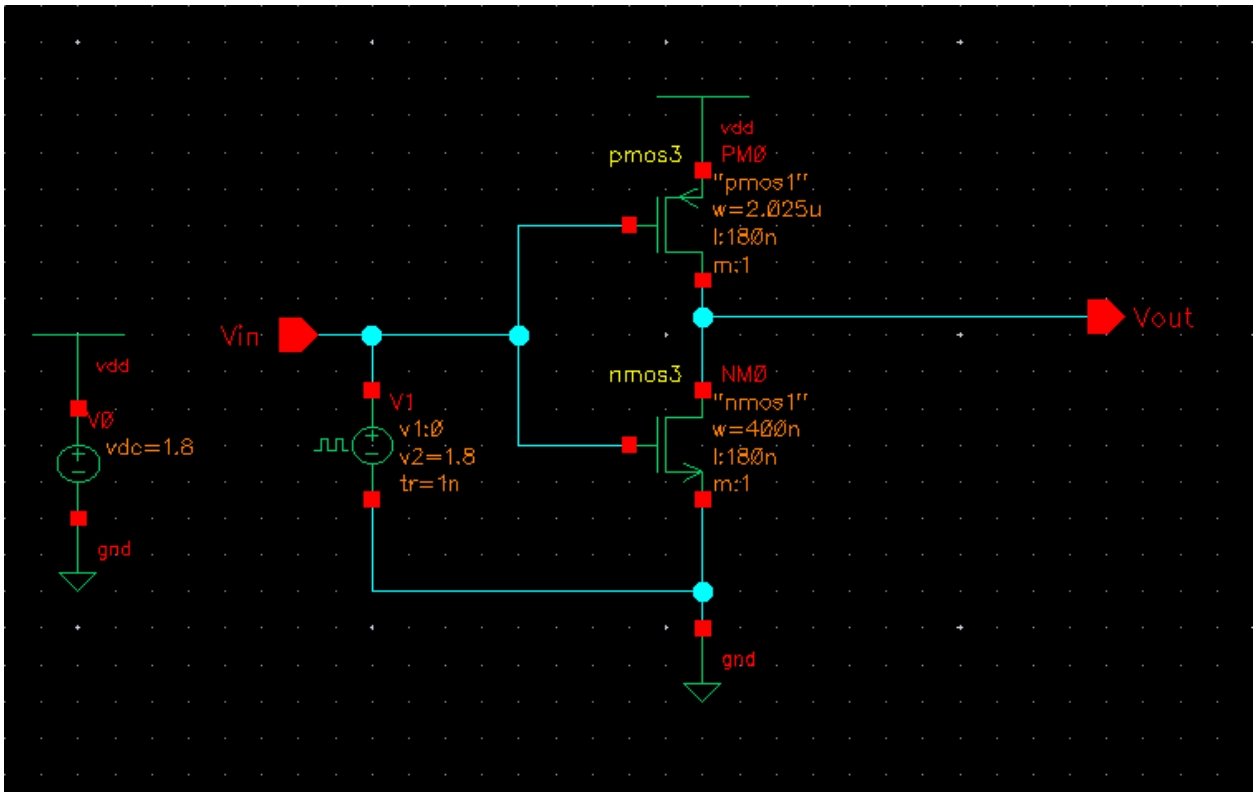
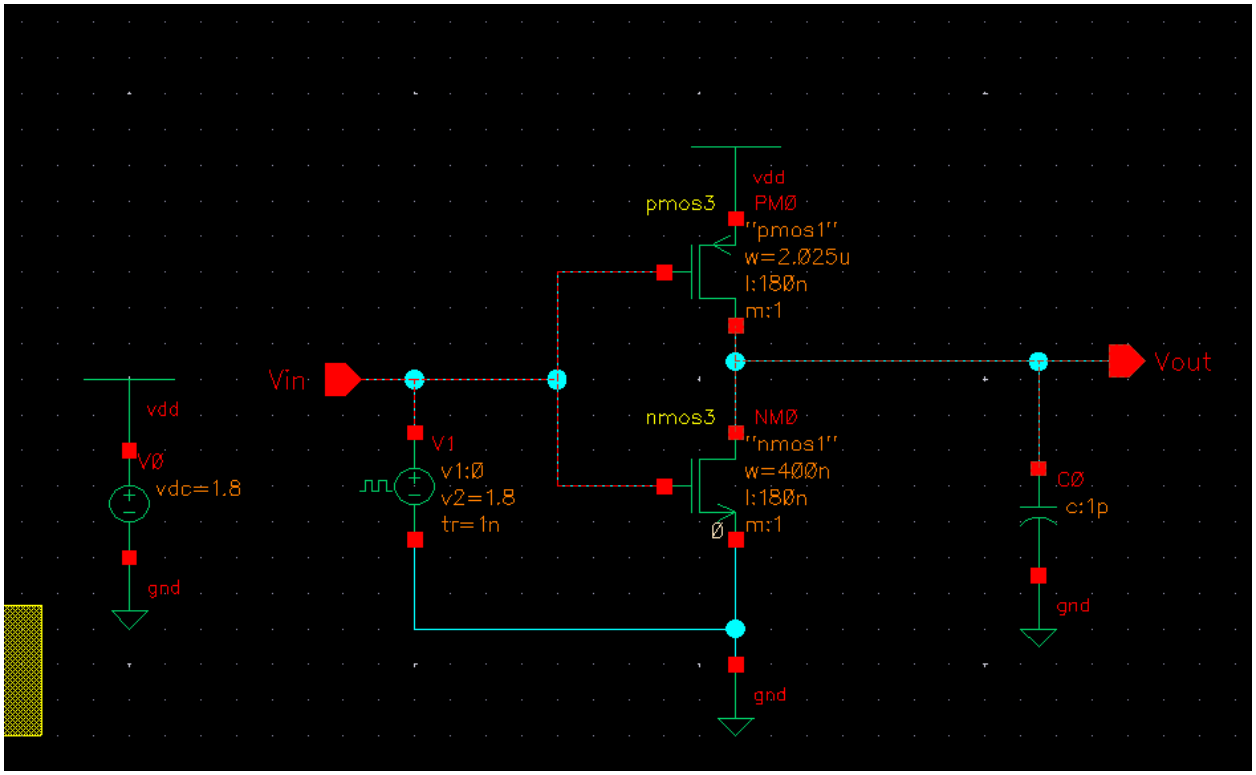
Schematics:
Without load capacitor:

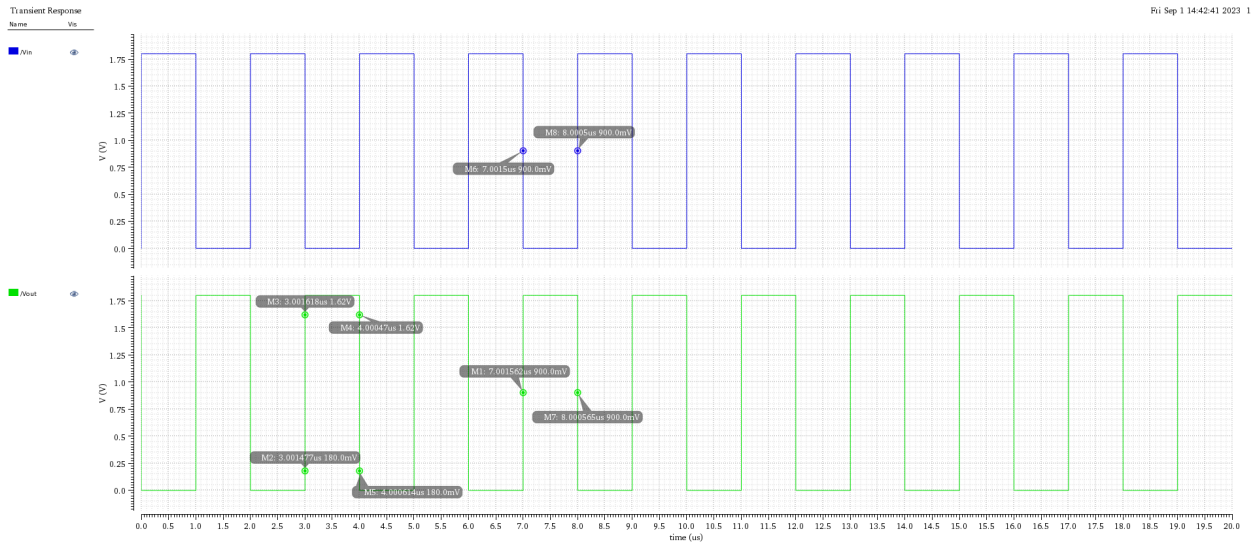


With load capacitor:



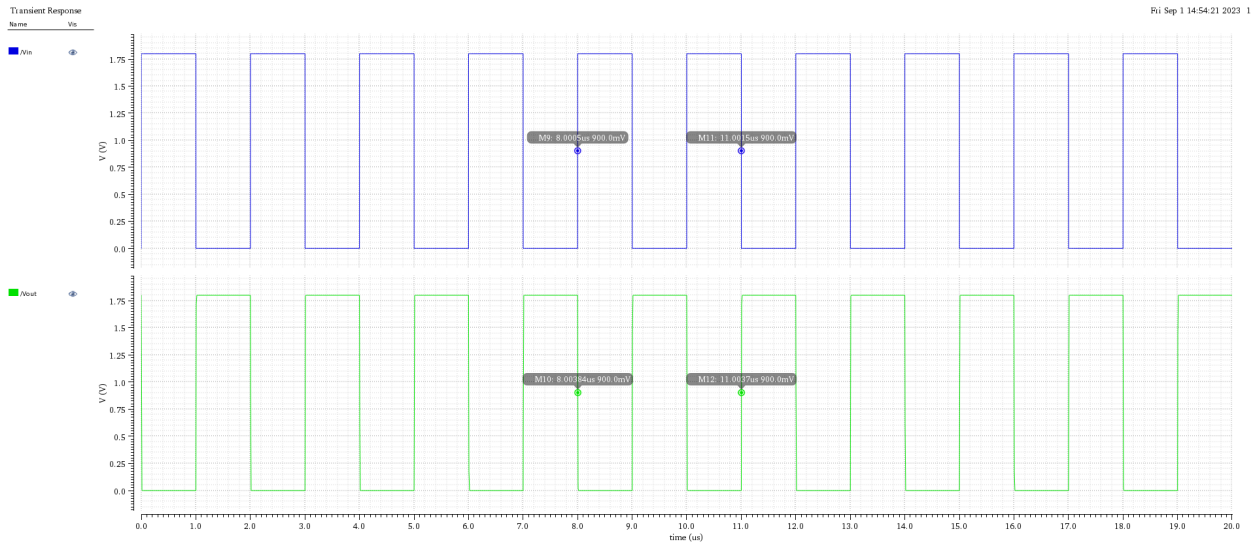
<u>Waveforms</u>:

Without capacitive load:



Without the load capacitance, t_{pHL} and t_{pLH} are similar in value.

With capacitive load:



With the load capacitance, t_{pHL} and t_{pLH} significantly differ in value.

<u>Metrics Measured</u>:
Without capacitive load:
T_{rise} = 0.141 ns
T_{fall} = 0.144 ns
t_{pLH} = 0.062 ns
t_{pHL} = 0.065 ns

With capacitive load:
t_{pLH} = 3.34 ns
t_{pHL} = 2.21 ns
t_{worst} = 3.34 ns
$t_{average}$ = 2.77 ns

In the presence of a load capacitor, the delay of the inverter is increased manyfold. This is because the delay of the inverter is proportional to:

$$\tau_{delay} \propto RC_{load}$$

where R = resistance, C_{load} = load capacitance

Since the biasing resistance of PMOS is greater than that of NMOS (due to higher width), the delay in the output signal for the transition LOW-to-HIGH is greater than the HIGH-to-LOW transition delay.

Conclusion:
This experiment involved analysis of propagation delay, rise and fall times of the transient inverter characteristics and their variation with and without load capacitance.