Lab-1 MOS IV Characteristics

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Current-Voltage Relations in an NMOS Transistor:

In the linear/triode region ($V_{DS} < V_{GS} - V_{TH}$, $V_{GS} >= V_{TH}$),

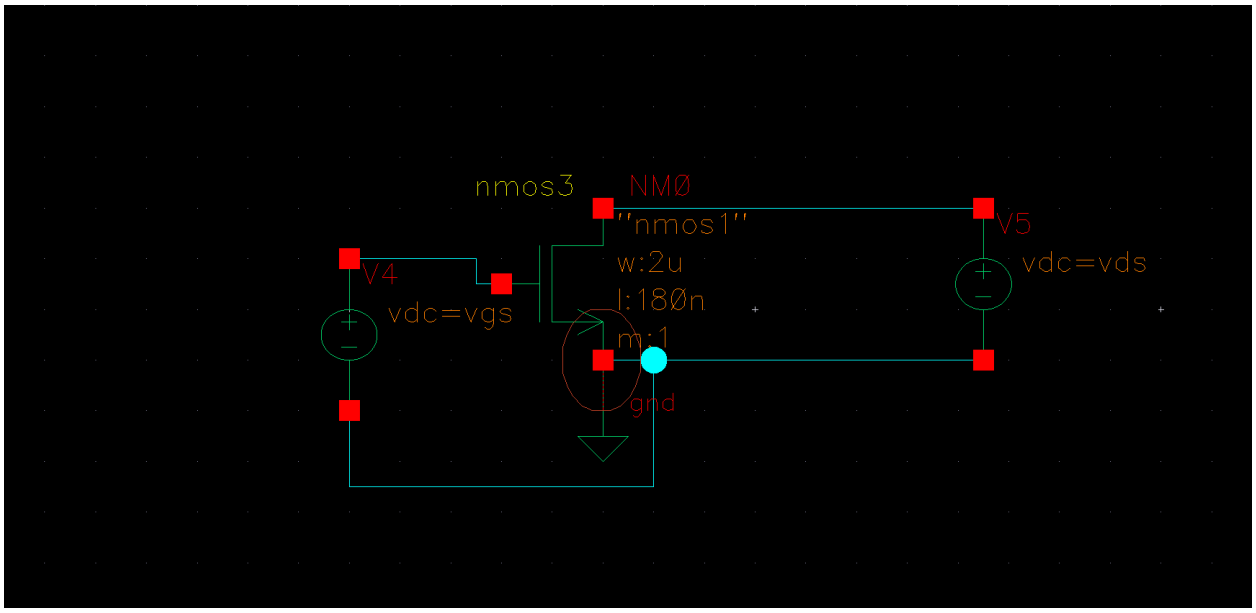
$$I_D = \mu_n C_{ox}(W/L)[(V_{GS} - V_{TH})V_{DS} - V_{DS}^2/2]$$

While in the saturation region ($V_{DS} >= V_{GS} - V_{TH}$, $V_{GS} >= V_{TH}$),

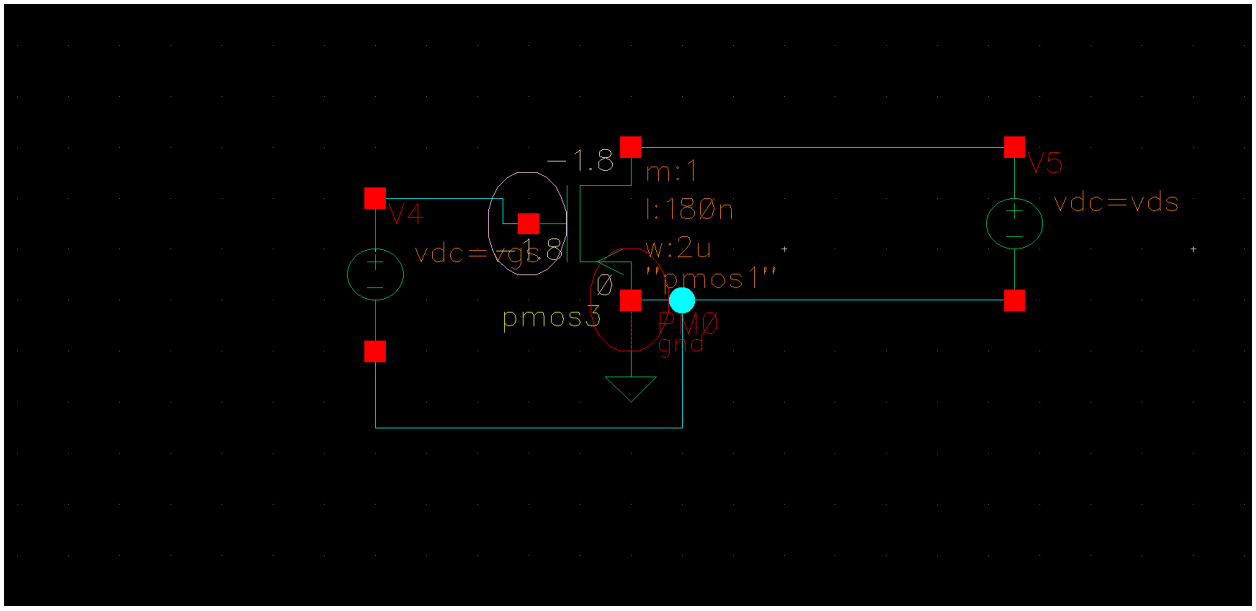
$$I_D = \frac{\mu_n C_{ox}}{2}(W/L)[(V_{GS} - V_{TH})^2]$$

Schematics:

NMOS Voltage Characteristics



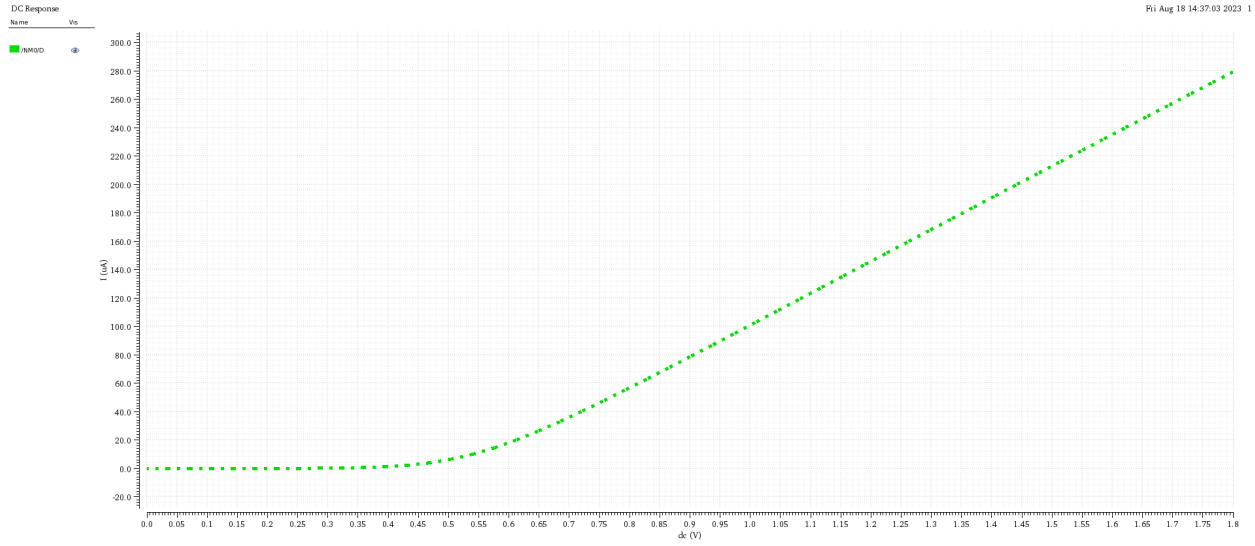
PMOS Voltage Characteristics



Output Waveforms:

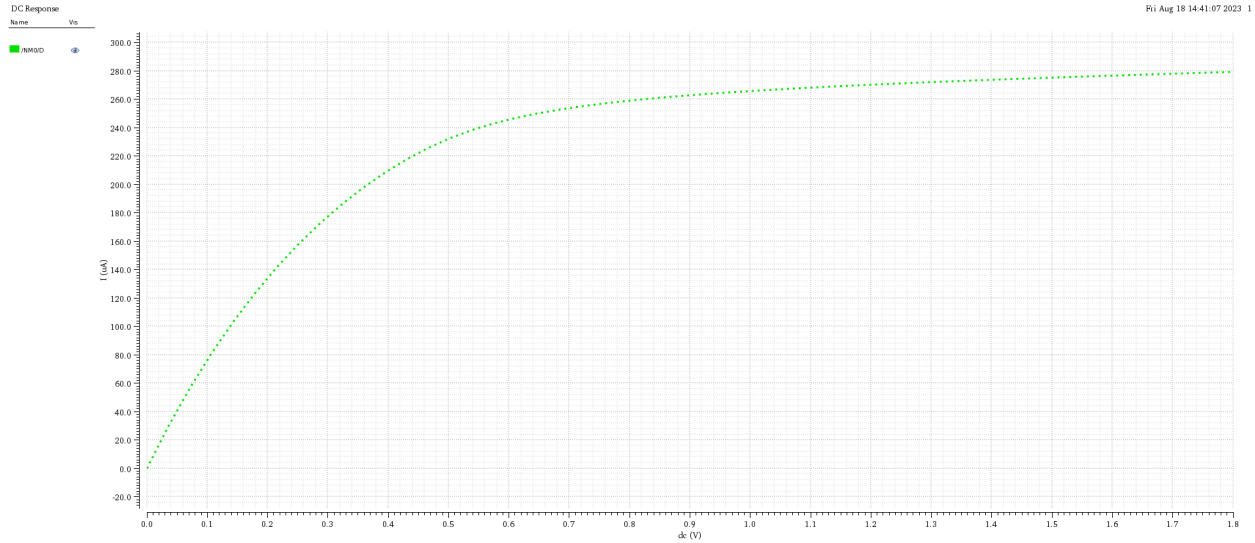
<u>NMOS Voltage Characteristics</u>

1. I_D v/s V_{GS} for fixed V_{DS}



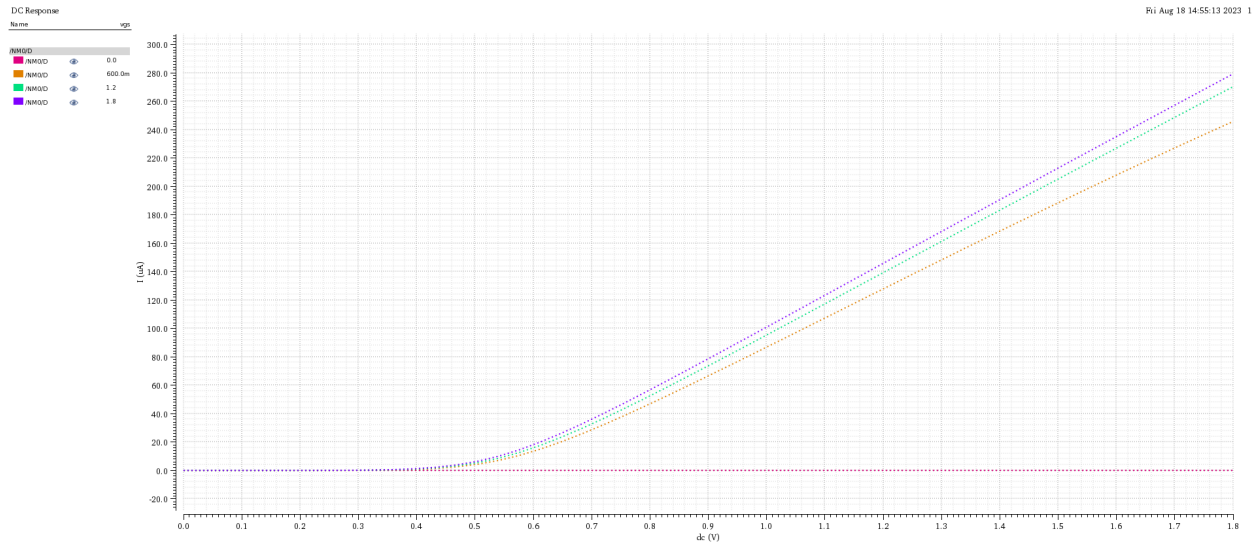
For an enhancement-mode NMOS transistor, the gate voltage applied is responsible for the channel formation. When the gate voltage is greater than the threshold voltage, the channel formation happens and current begins to flow.

2. I_D v/s V_{DS} for fixed V_{GS}



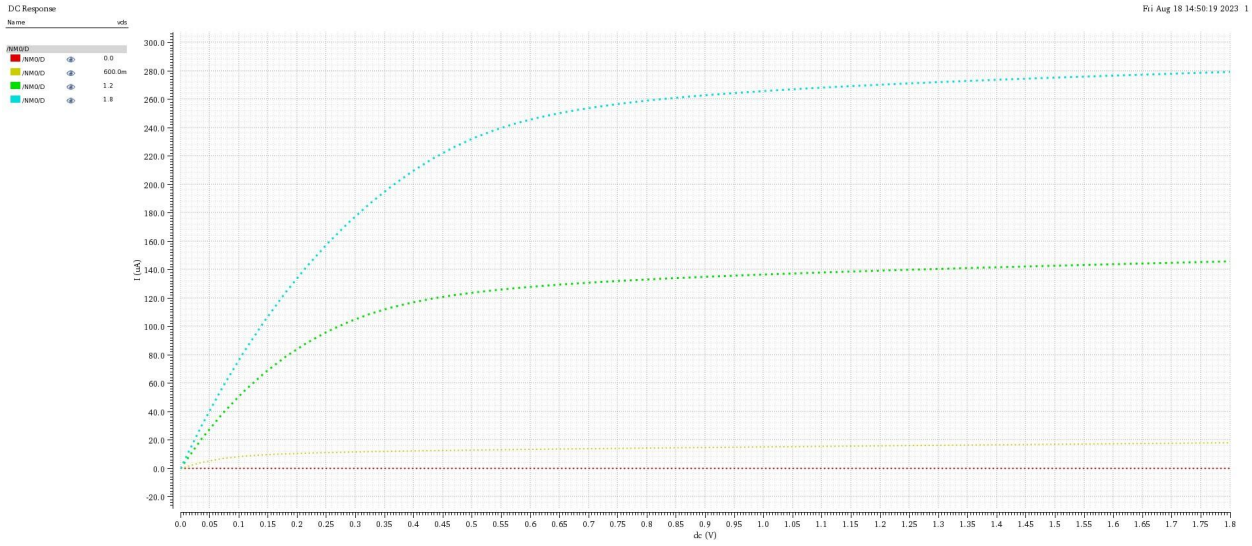
The NMOS device functions in three operating conditions-
I. When the $V_{GS} < V_{TH}$, the device is cut-off as the channel has not formed yet.
II. For $V_{DS} < V_{GS} - V_{TH}$ and $V_{GS} >= V_{TH}$, the device operates in the linear or triode mode where the current varies linearly with the drain voltage.
III. For $V_{DS} >= V_{GS} - V_{TH}$ and $V_{GS} >= V_{TH}$, the device goes into saturation where the drain current becomes constant and does not increase with increase in drain voltage.

3. I_D v/s V_{GS} for varying V_{DS}



The plots follow the characteristics as the plot shown in 1 however for a given V_{GS}, the current increases with greater V_{DS} values.

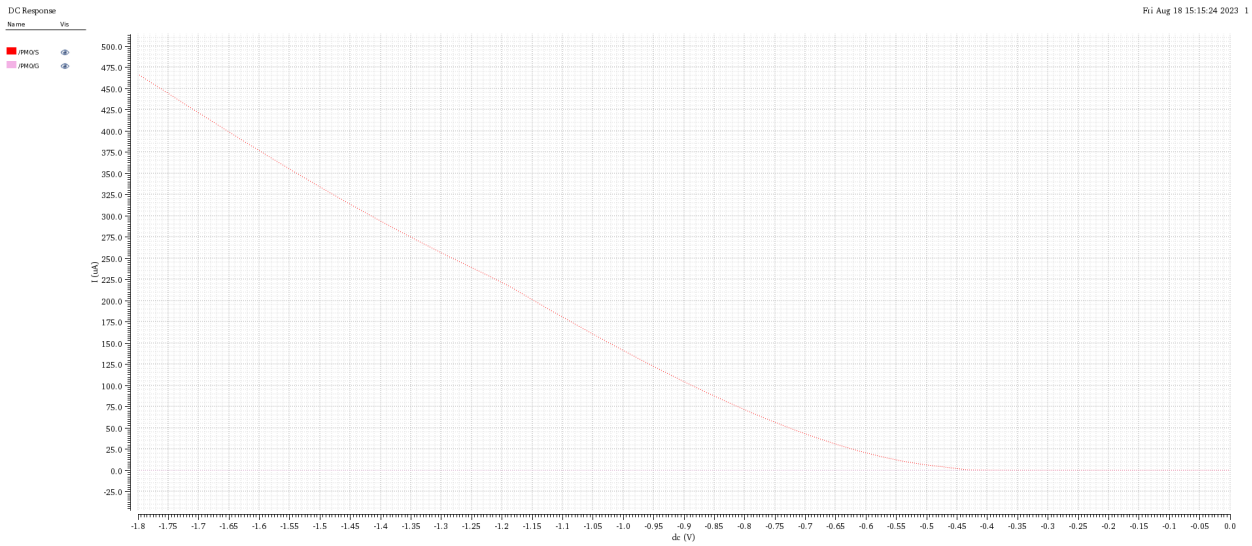
4. I_D v/s V_{DS} for varying V_{GS}



The plots follow the characteristics as the plot shown in 2 however for a given V_{DS}, the current increases with greater V_{GS} values.

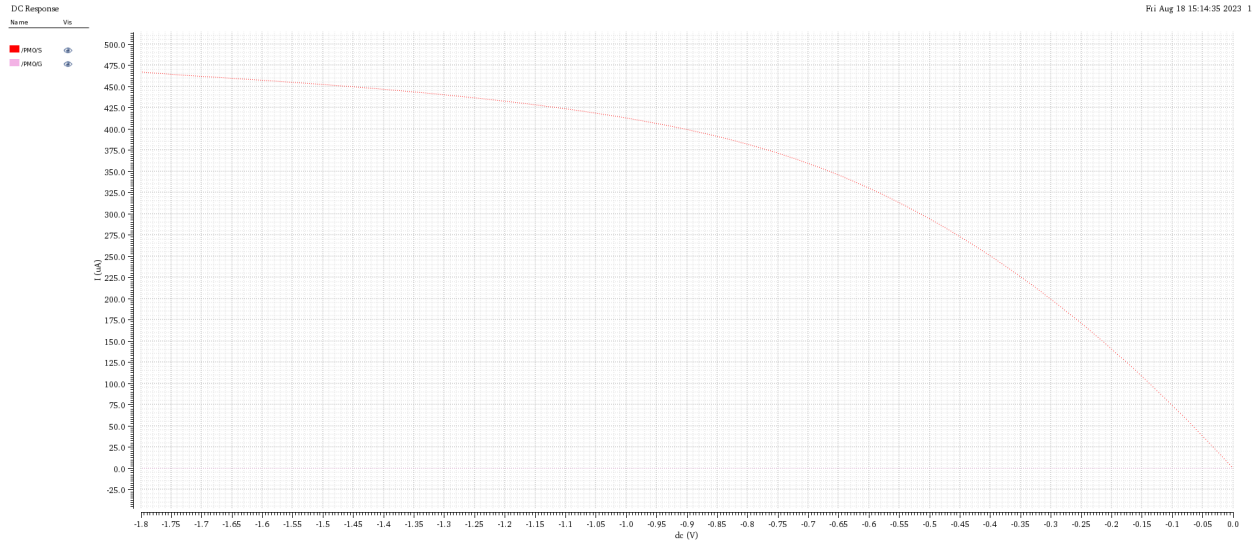
<u>PMOS Voltage Characteristics</u>

1. I_D v/s V_{GS} for fixed V_{DS}



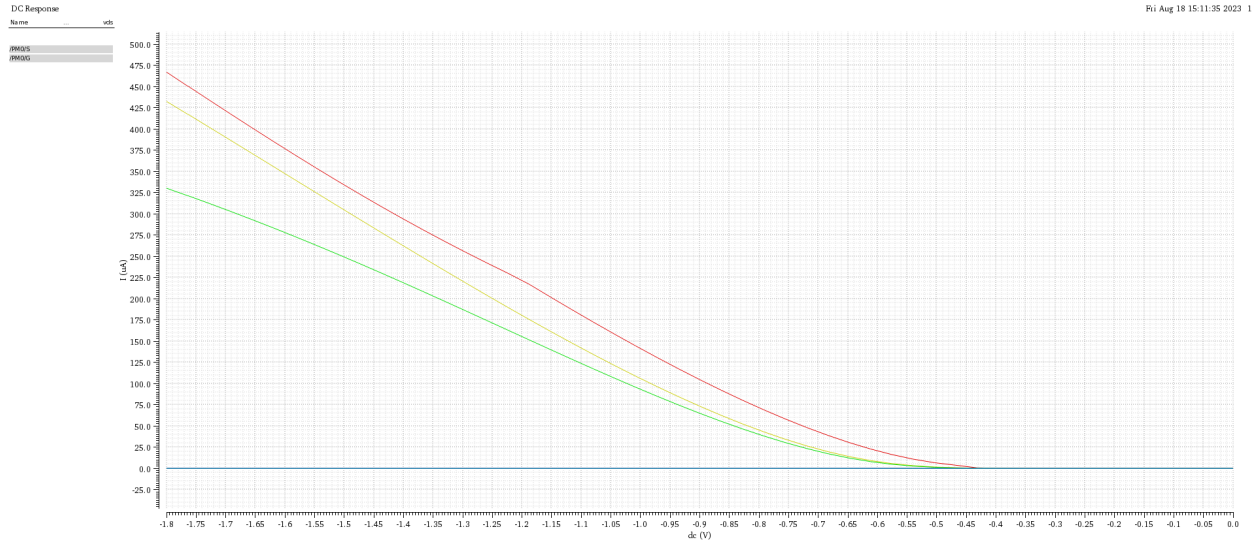
For an enhancement-mode PMOS transistor, the gate voltage applied is responsible for the channel formation. When the gate voltage is less than the threshold voltage (greater in magnitude), the channel formation happens and current begins to flow.

2. I_D v/s V_{DS} for fixed V_{GS}



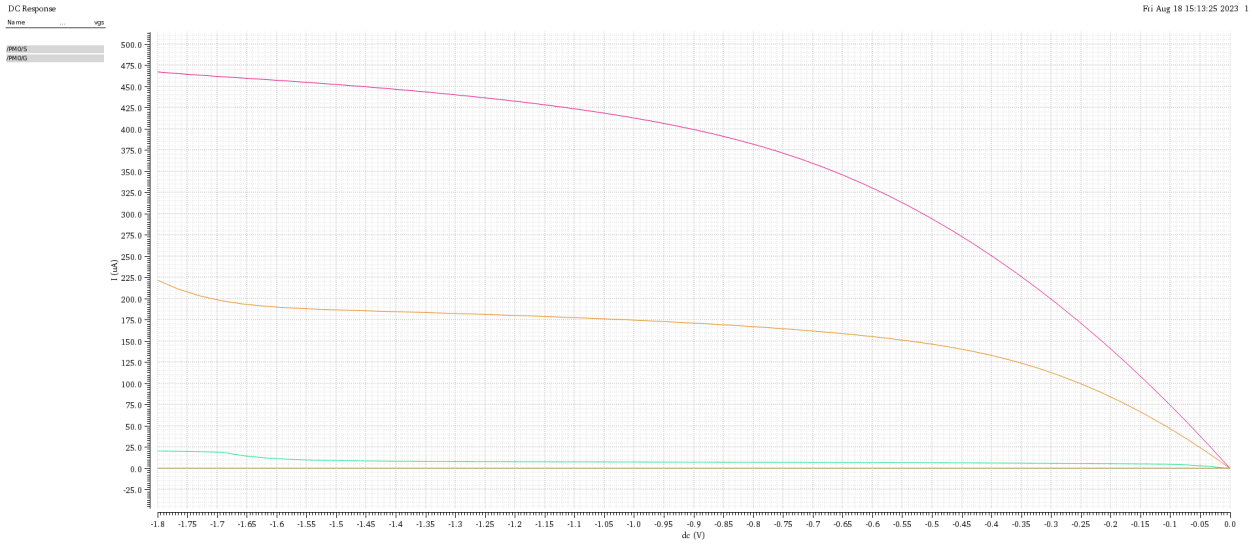
The PMOS device operates in three operating conditions-
I. When the $V_{GS} > V_{TH}$, the device is cut-off as the channel has not formed yet
II. For $V_{DS} > V_{GS} - V_{TH}$ and $V_{GS} <= V_{TH}$, the device operates in the linear or triode mode where the current varies linearly with the drain voltage
III. For $V_{DS} <= V_{GS} - V_{TH}$ and $V_{GS} <= V_{TH}$, the device goes into saturation where the drain current saturates and does not increase with increase in drain voltage

3. I_D v/s V_{GS} for varying V_{DS}



The plots follow the characteristics as the plot shown in 1 however for a given V_{GS}, the current increases with lower V_{DS} values.

4. I_D v/s V_{DS} for varying V_{GS}



The plots follow the characteristics as the plot shown in 2 however for a given V_{DS}, the current increases with lower V_{GS} values.

Metrics Measured:

Threshold Voltage

We can obtain the threshold voltage of the two transistors (NMOS & PMOS) by inspecting the point from which the current flow starts to take place.

$$V_{Tn} = 480 \text{ mV}$$
$$V_{Tp} = -480 \text{ mV}$$

Conclusion:

In this experiment, we learnt how to build a circuit and simulate it in the Cadence software. In particular, we studied the current-voltage relationships in both NMOS & PMOS transistors by building naive biasing networks to excite them.
We also plotted the results for different cases using the Cadence Virtuoso tool and obtained the possible threshold voltage values for each transistor.