

## **Experiment 4**

### **CMOS Static Logic Design**

1. Design a 2-input NAND gate, 2-input NOR gate, 2-input XOR gate, 2-input XNOR gate, 2-input AND gate, and 2-input OR gate using static complementary CMOS logic and create individual symbols of each gate.
2. Calculate the worst-case delay of the logic gates in (1).