VLSI LAB Experiment-6 AND, OR, & XOR Gates using Pass Transistors and Transmission Gates

Group Number: 2

Group Members:
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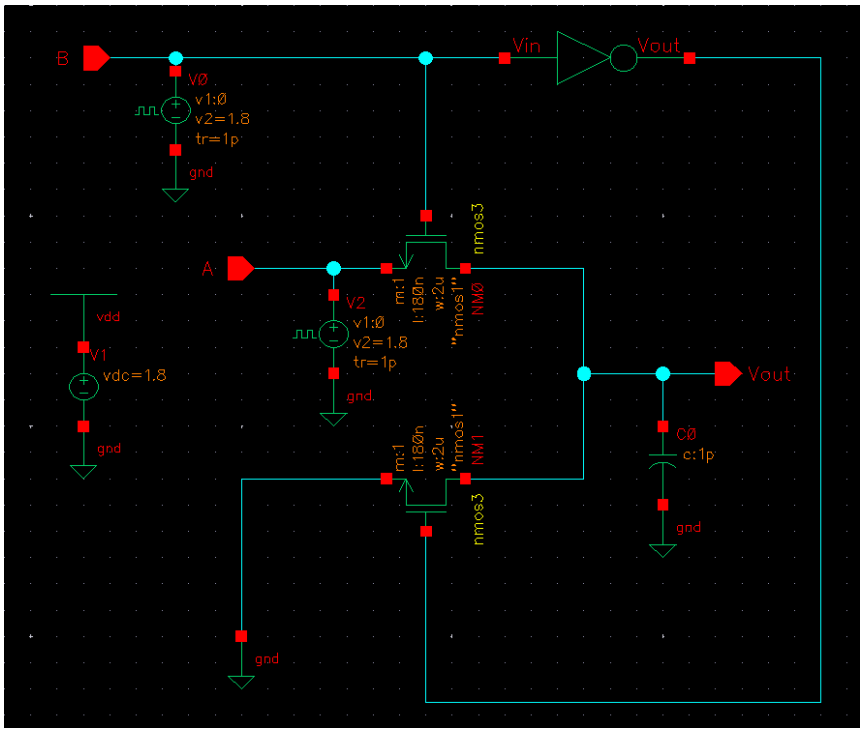
Aditya Anirudh - 2020AAPS0373H

Schematics:
AND GATE using PTL:-



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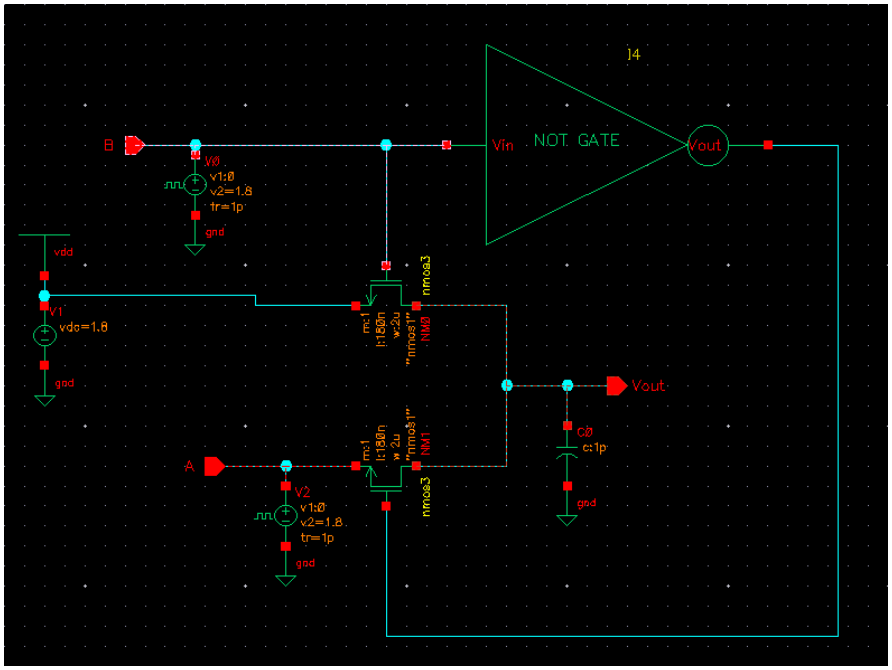

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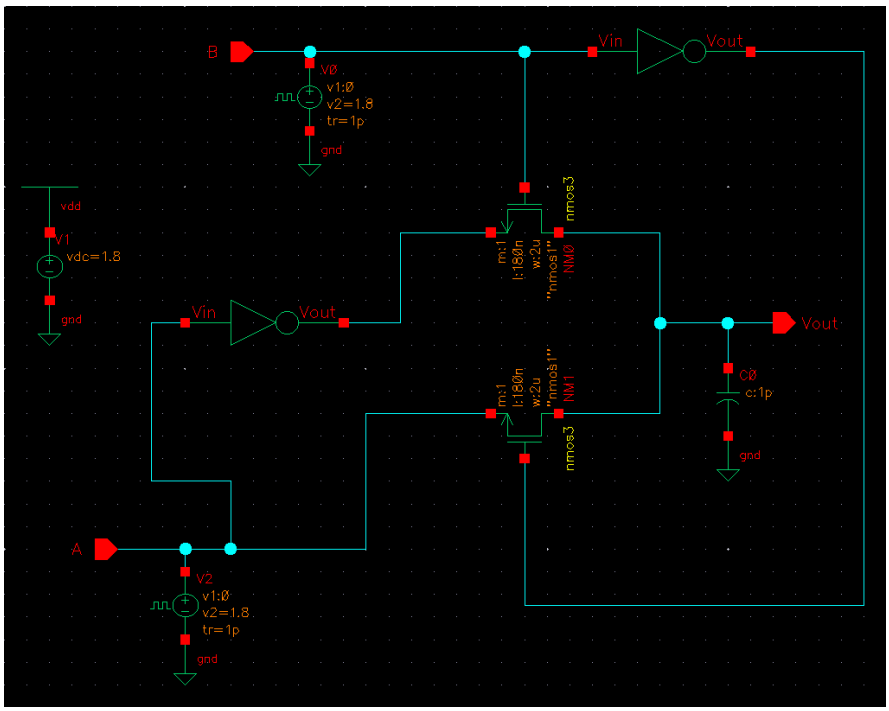
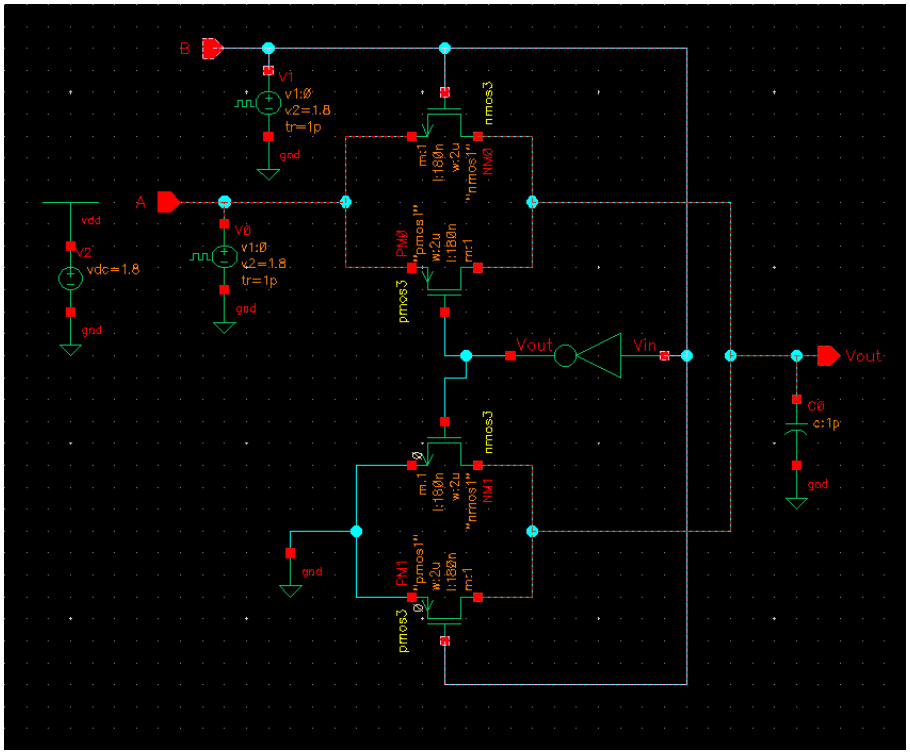


AND GATE using TGL:-



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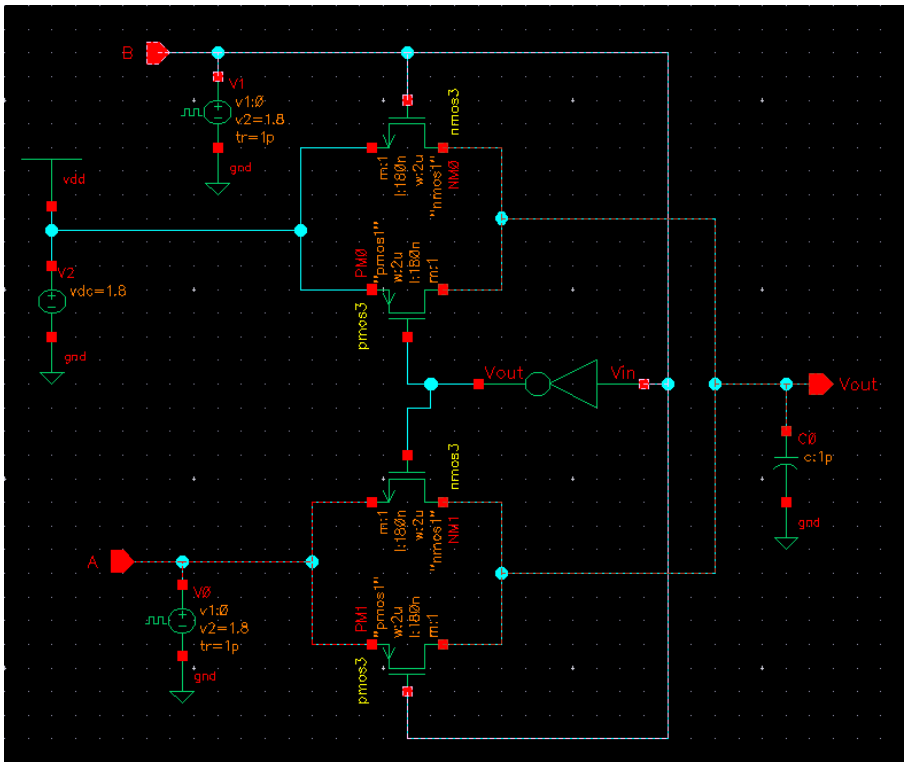

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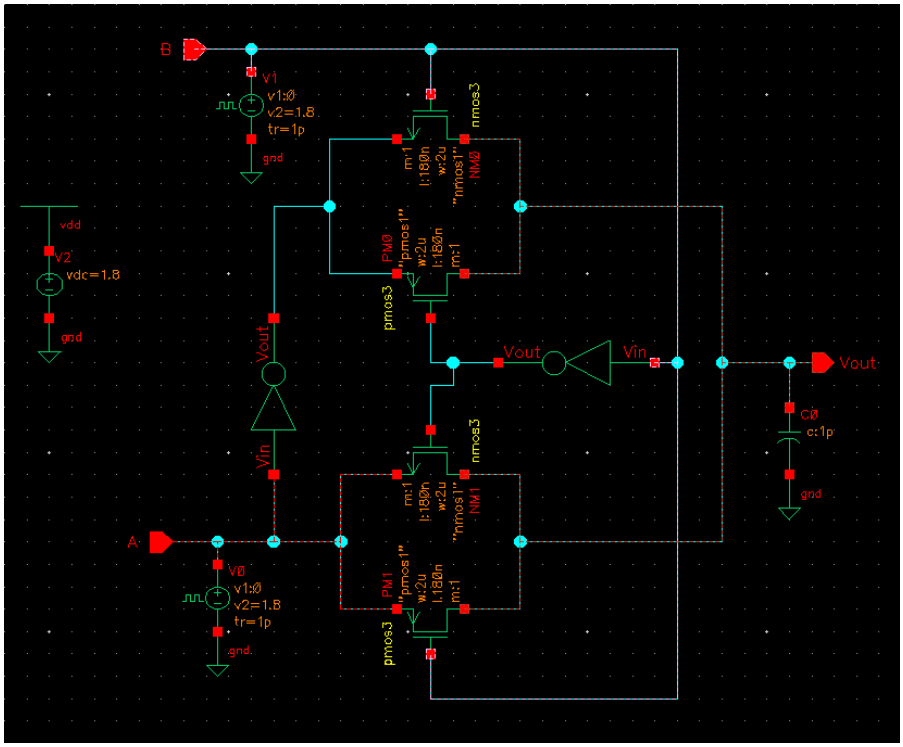
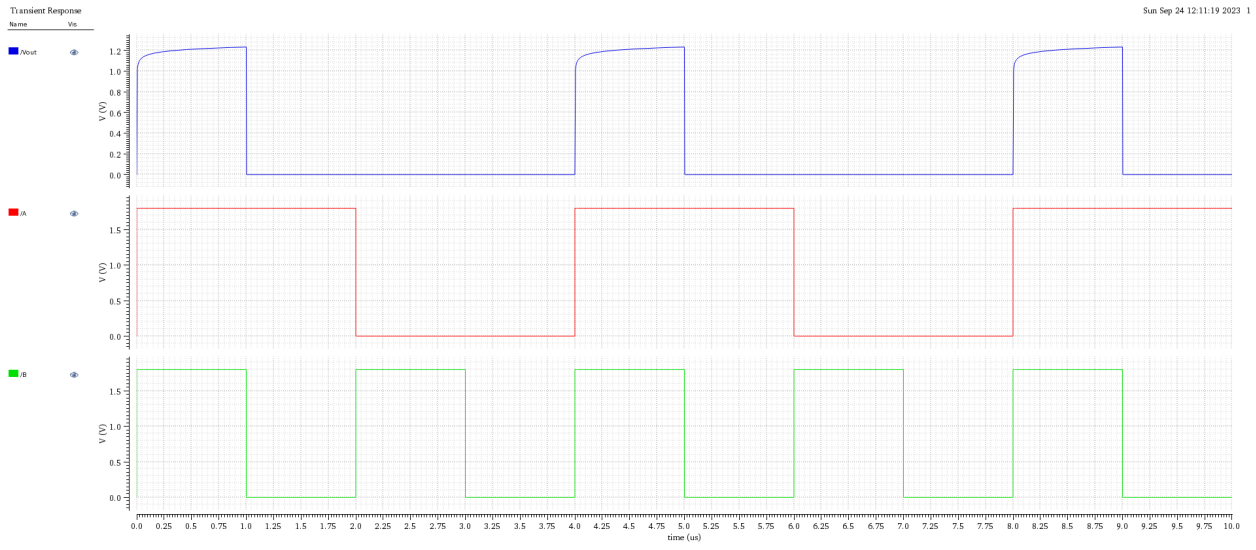


Waveforms:

AND GATE using PTL:-



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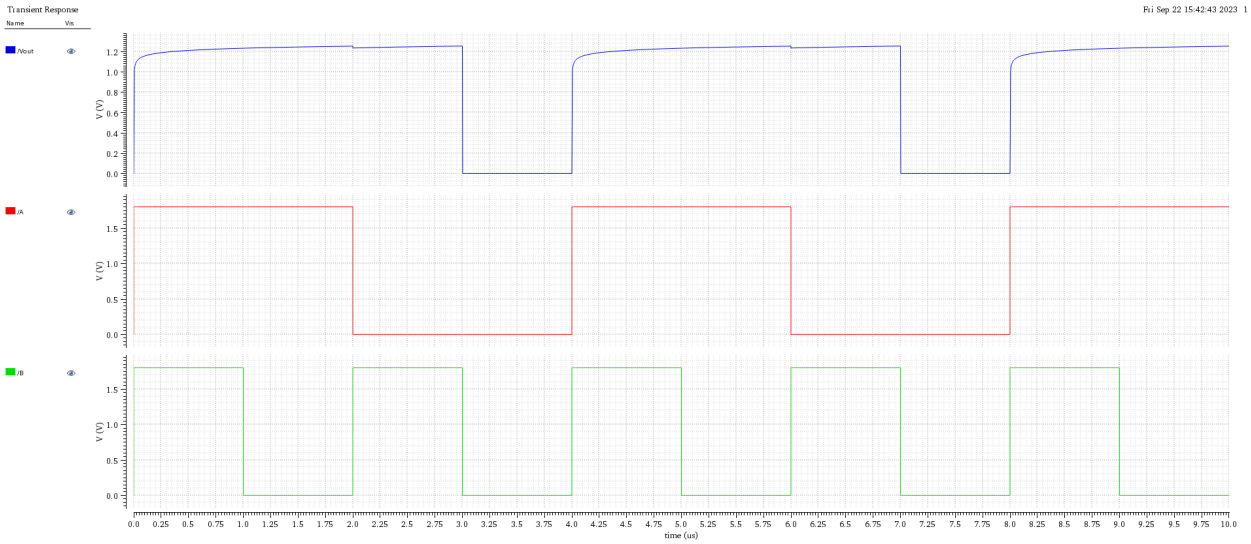

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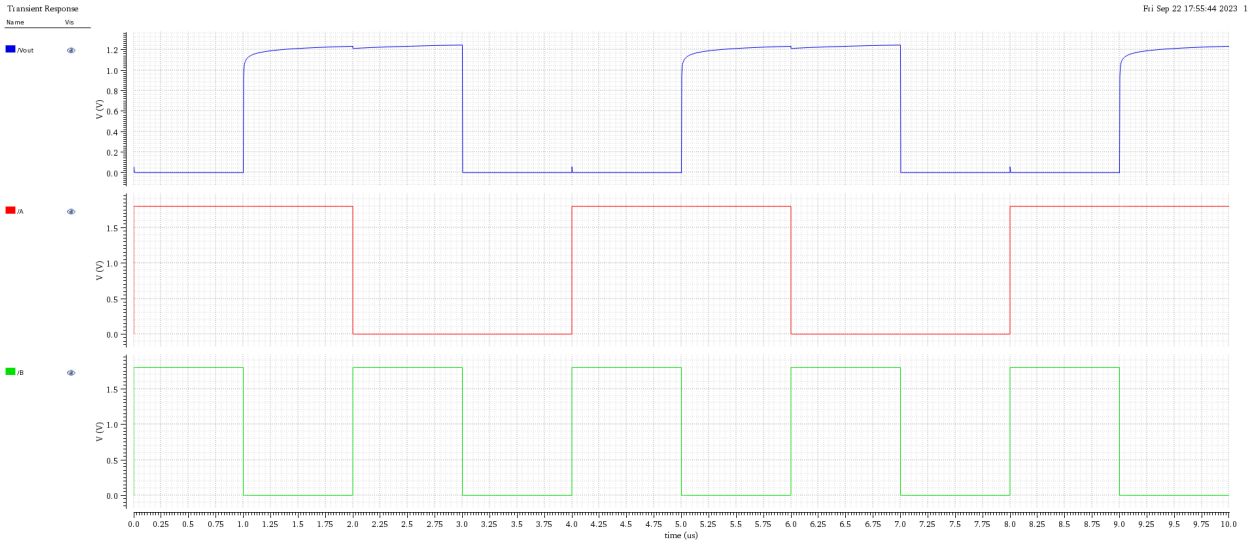

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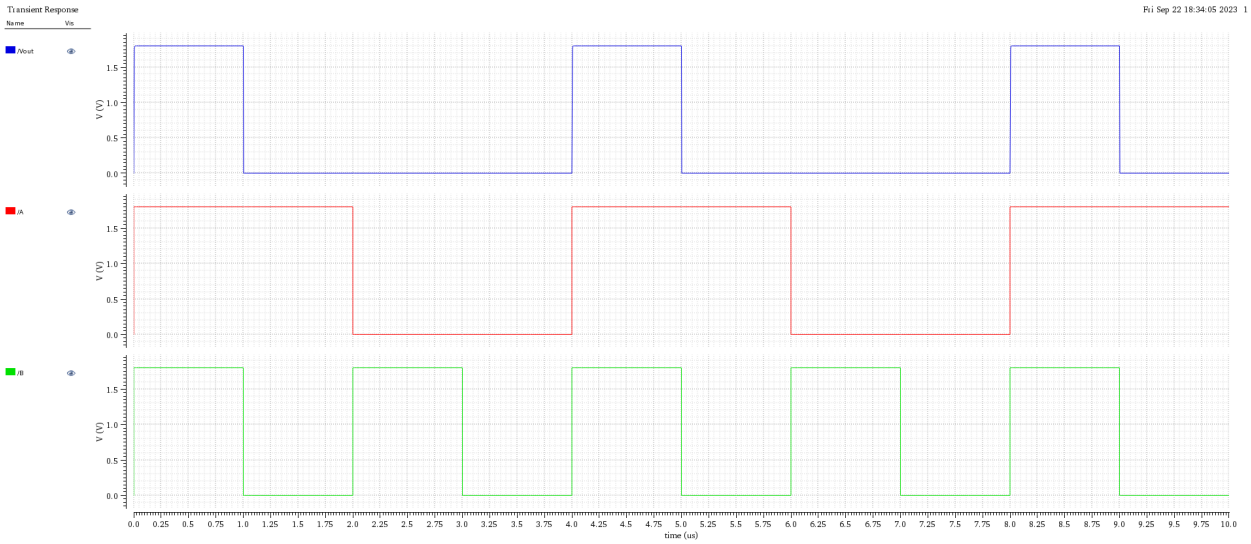

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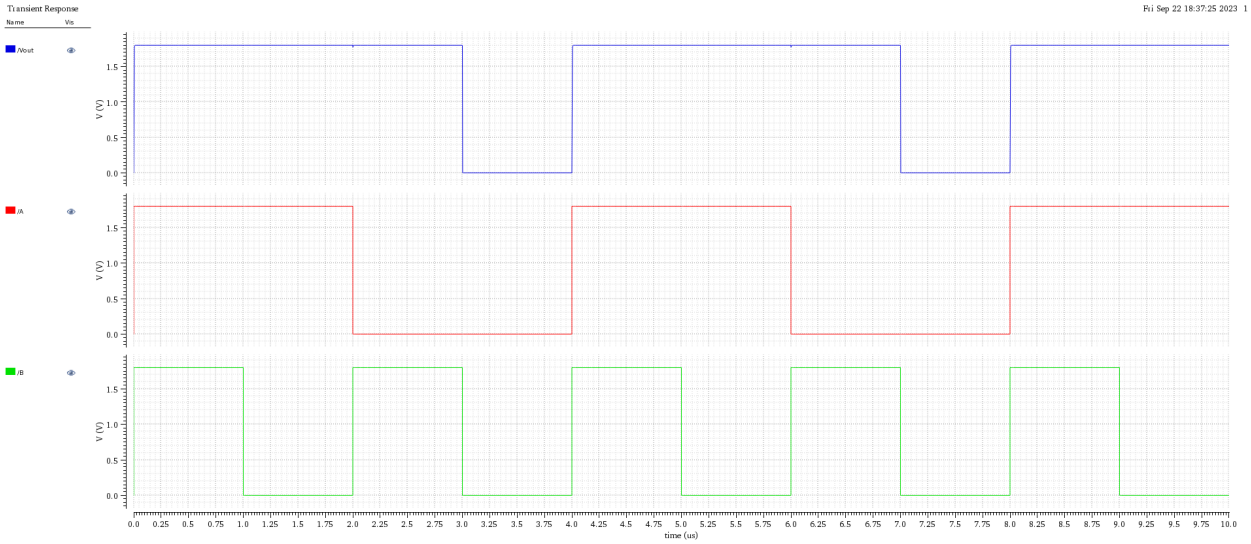

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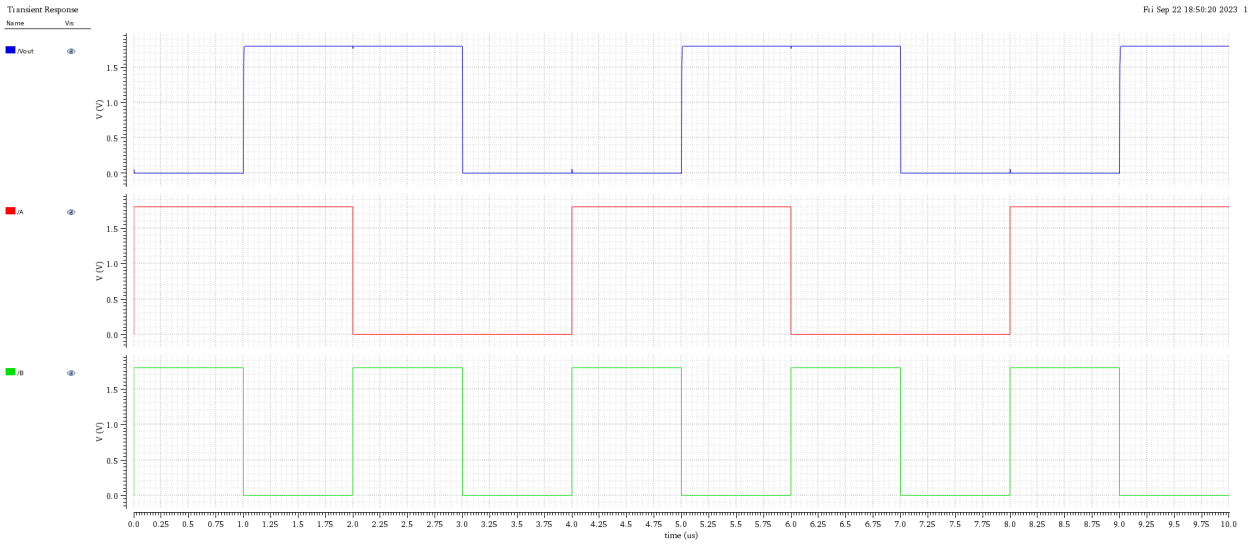
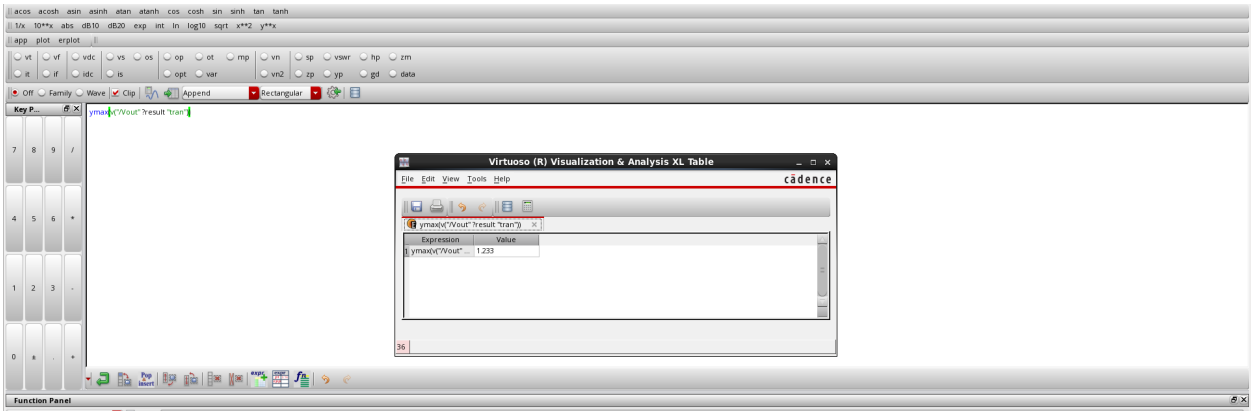


Observations:

Voltage Swing -

AND GATE using PTL:-



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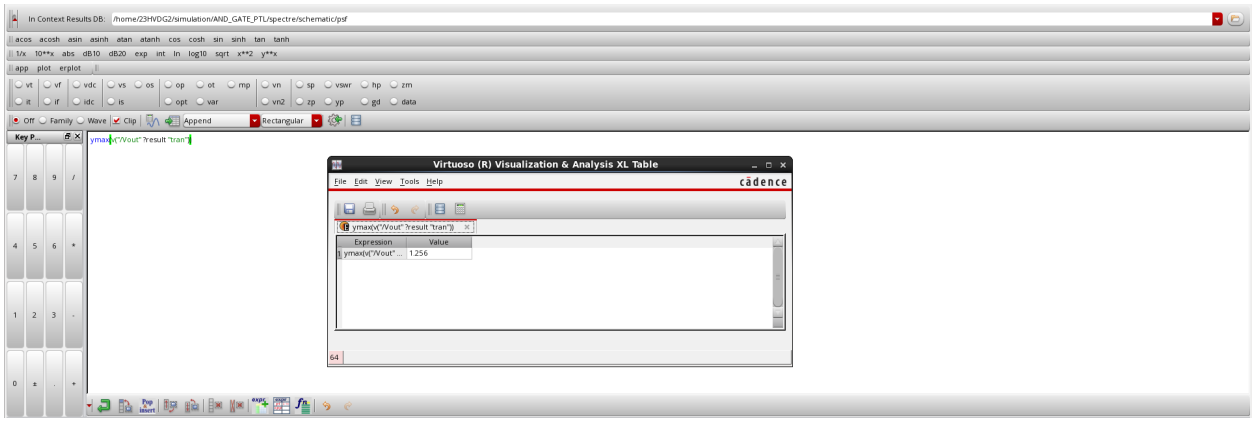

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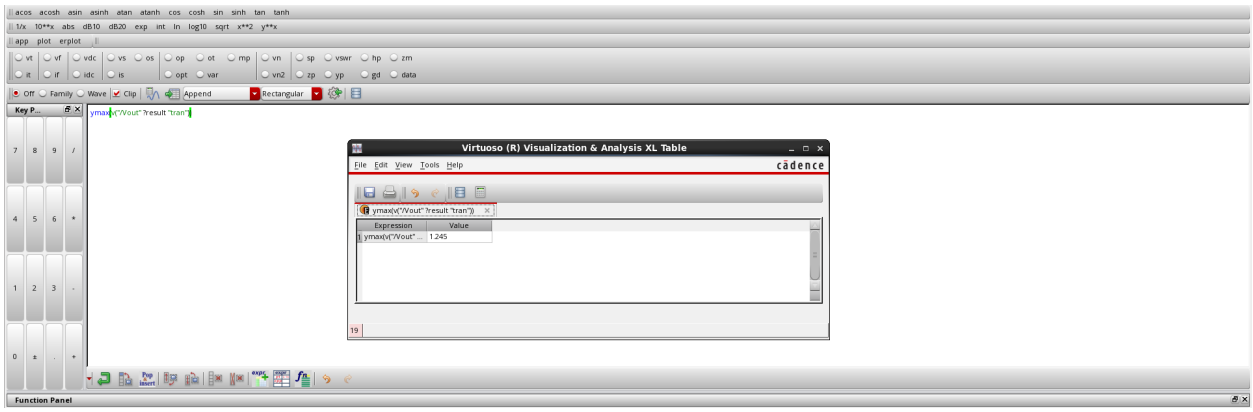

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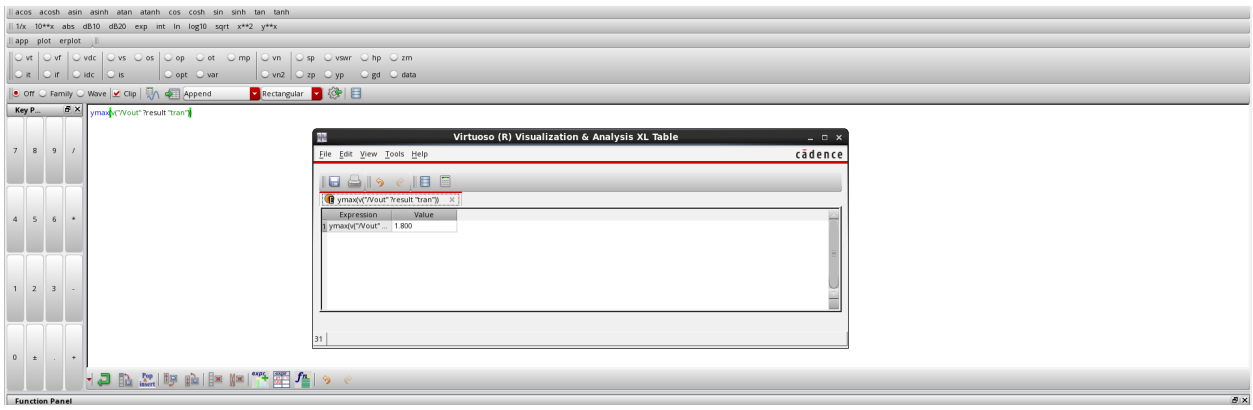

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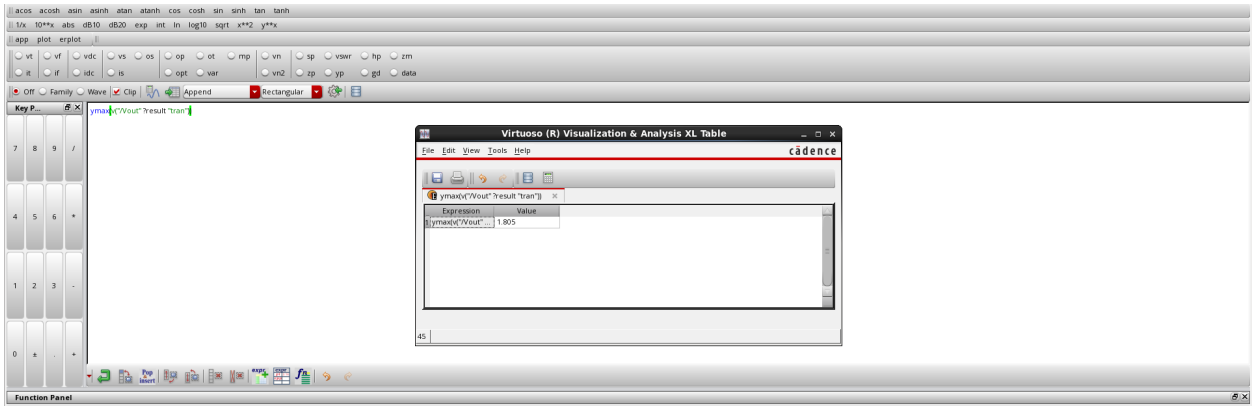

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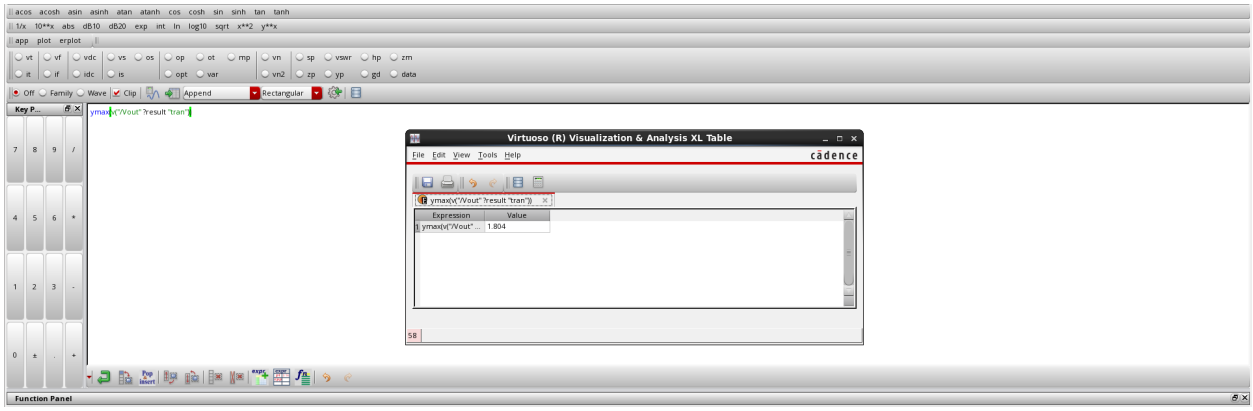
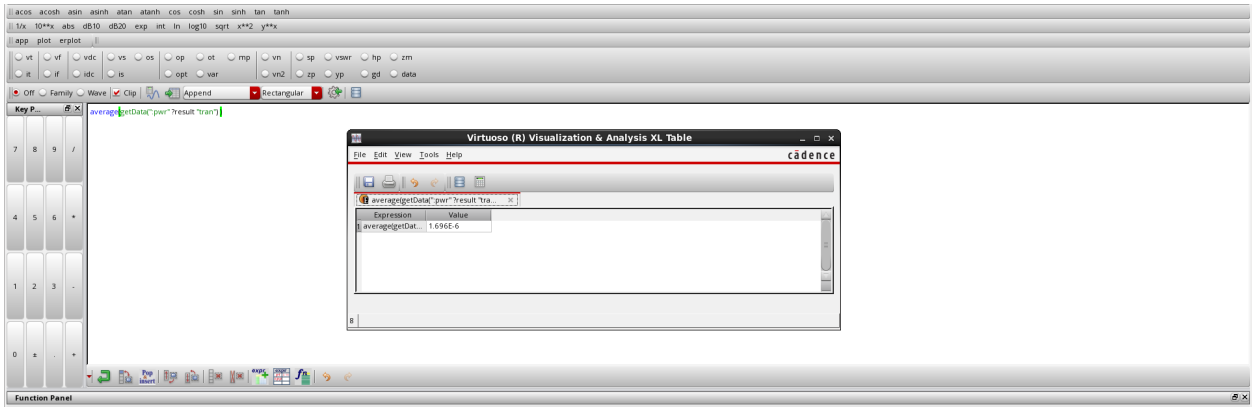


Power dissipation -

AND GATE using CMOS:-



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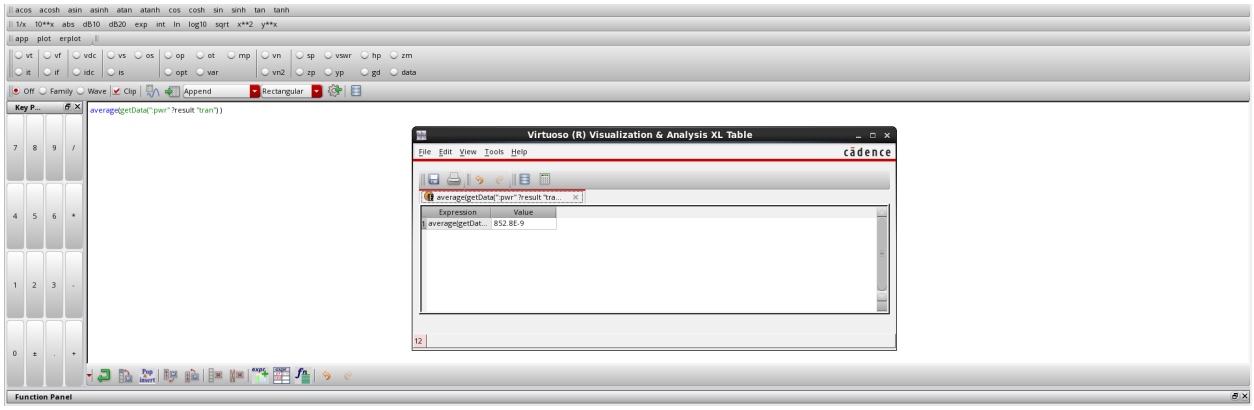

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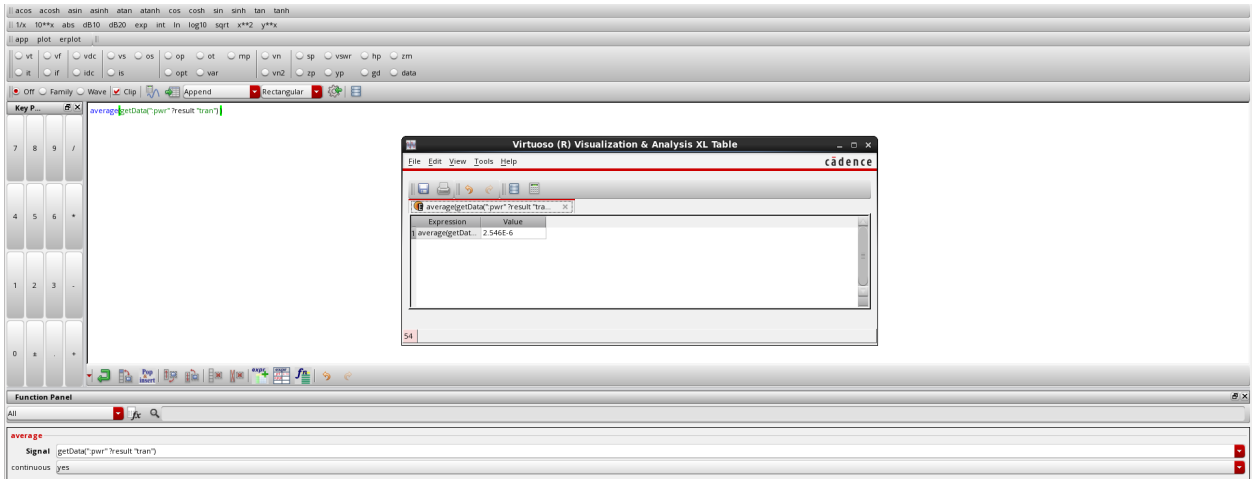

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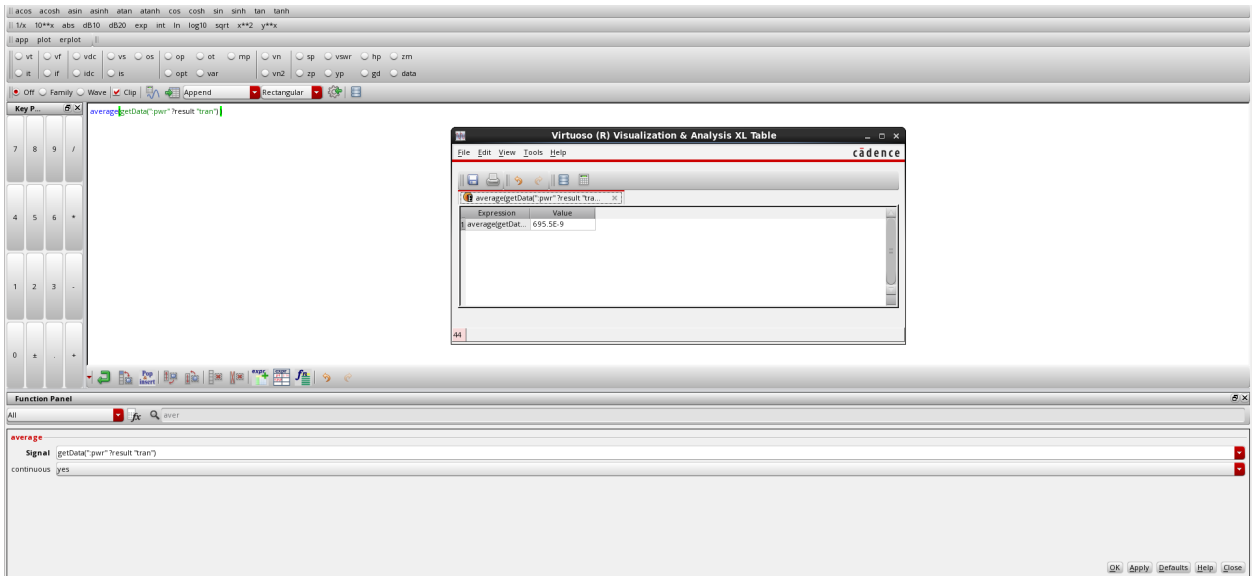

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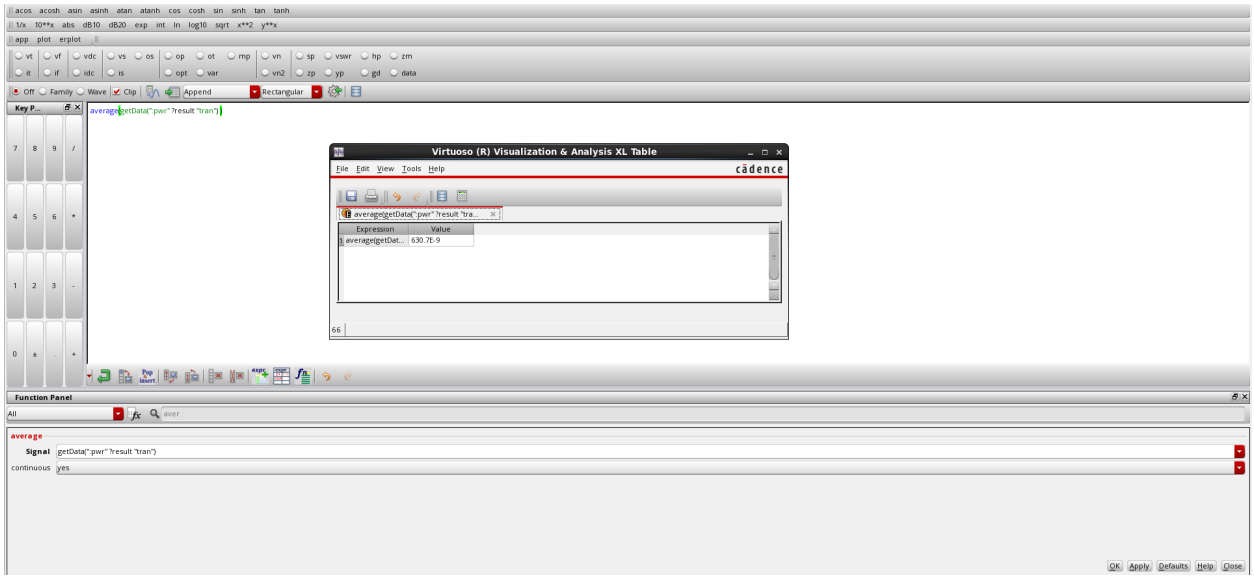

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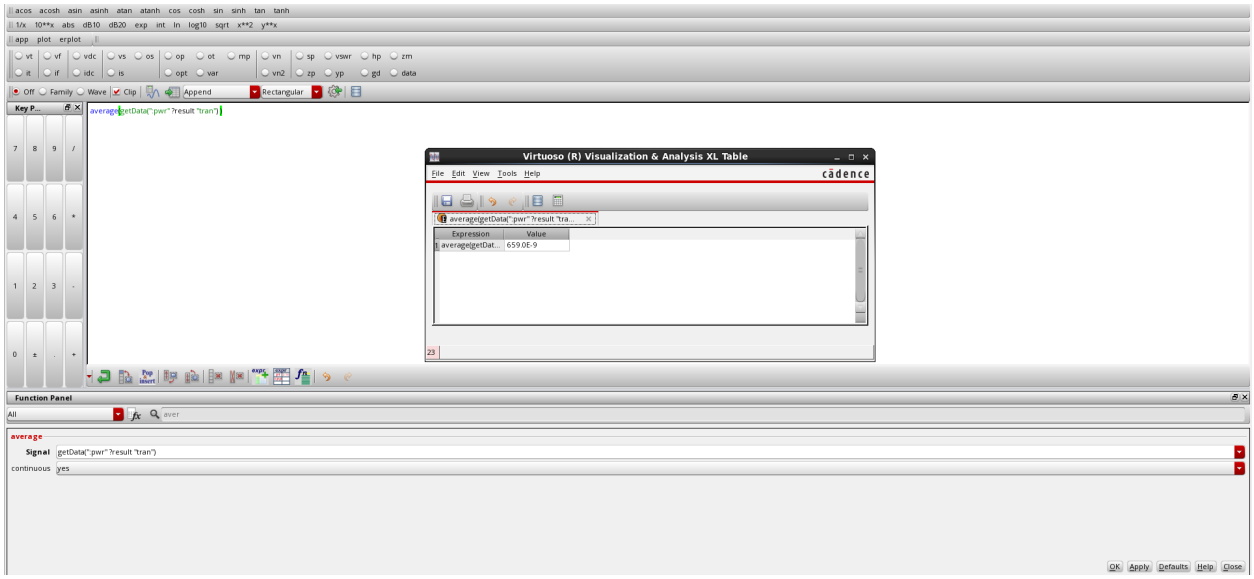

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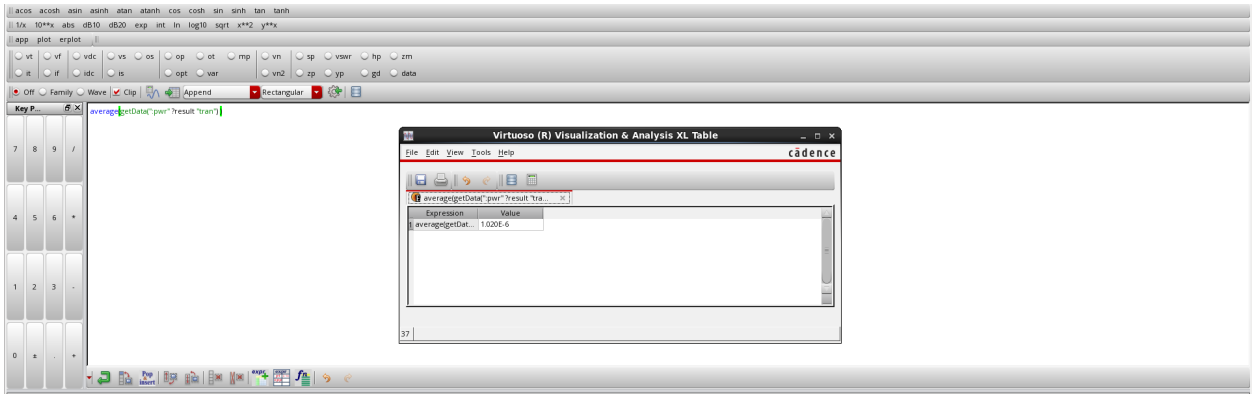

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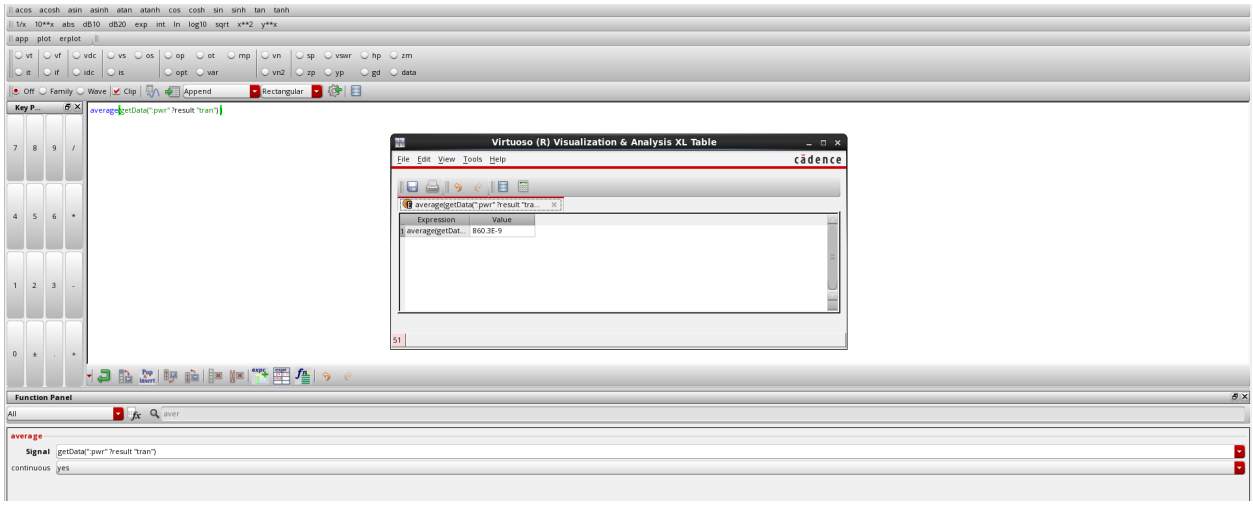

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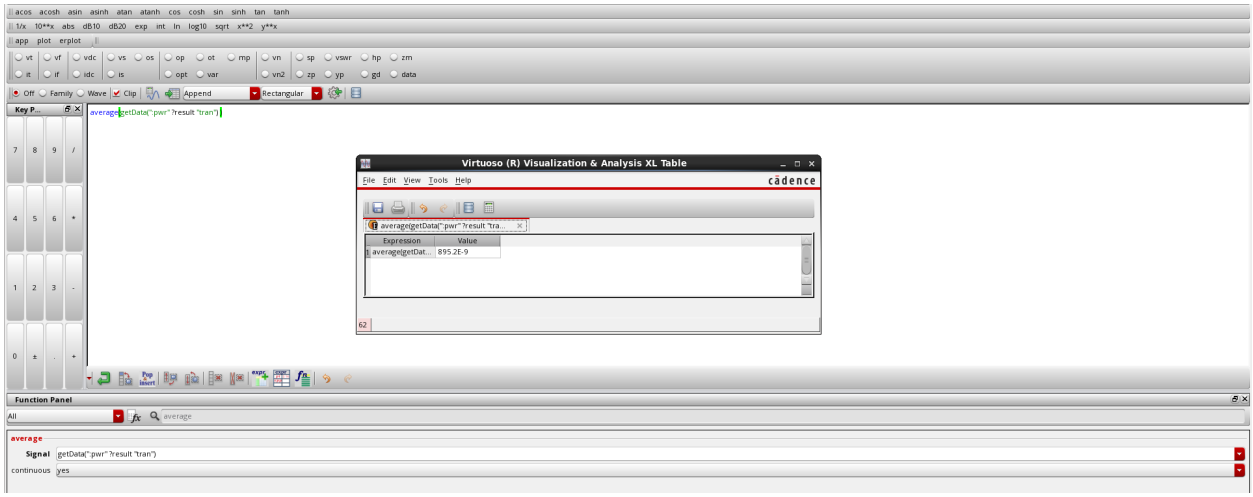
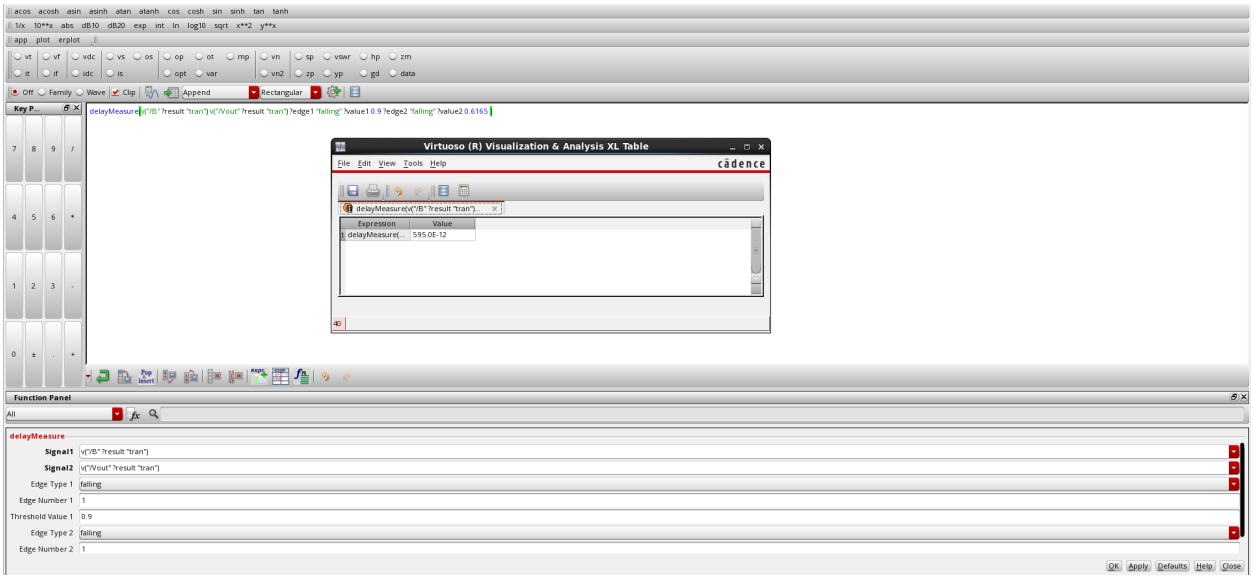


Delay -

AND GATE using PTL:-

t_{pHL}:



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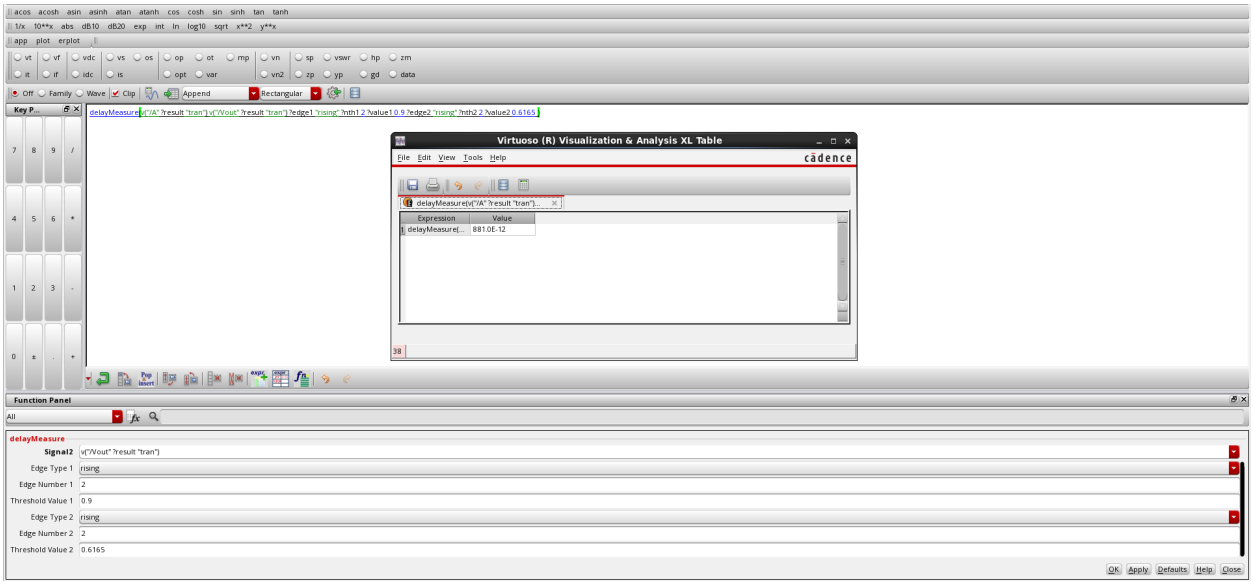
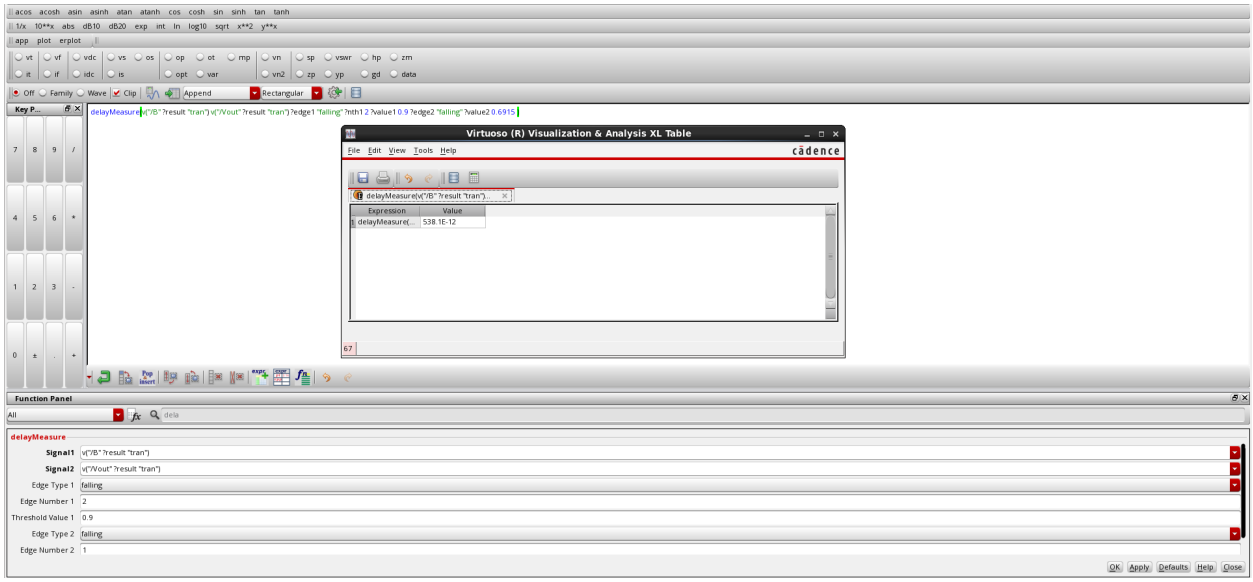


OR GATE using PTL:-

t_{pHL}:



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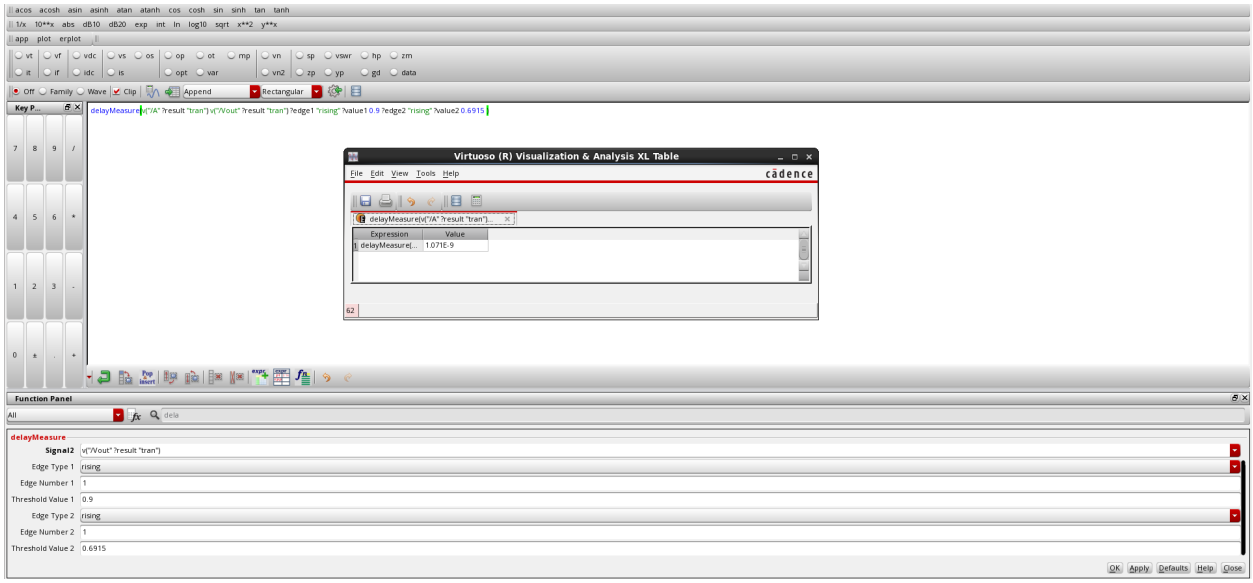
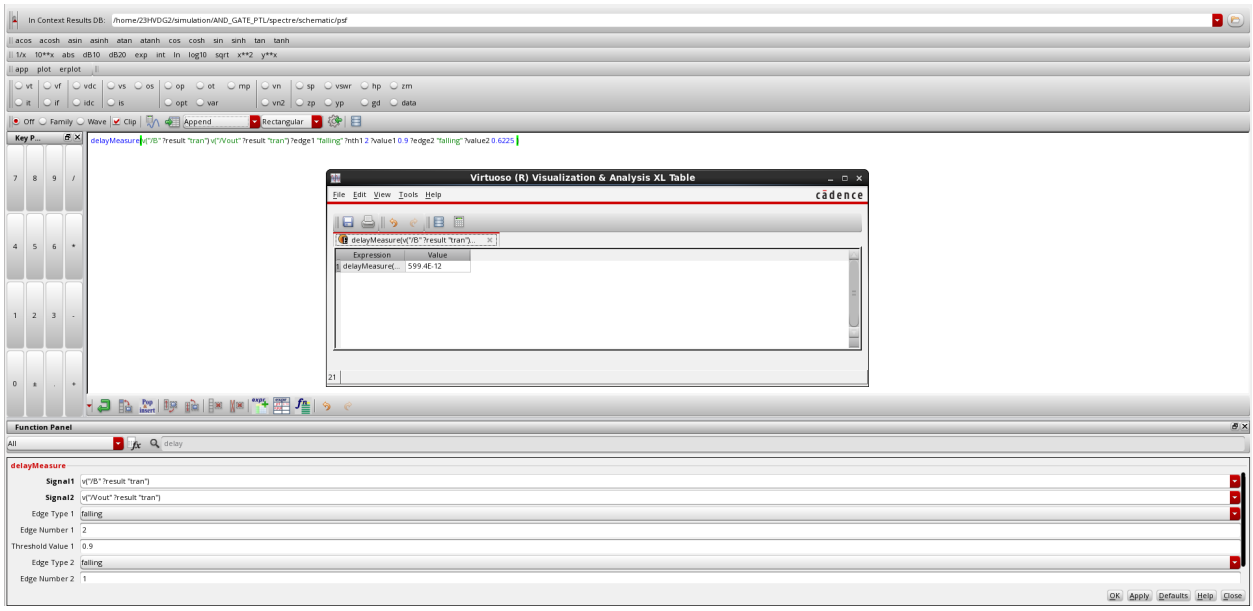


XOR GATE using PTL:-

t_{pHL}:



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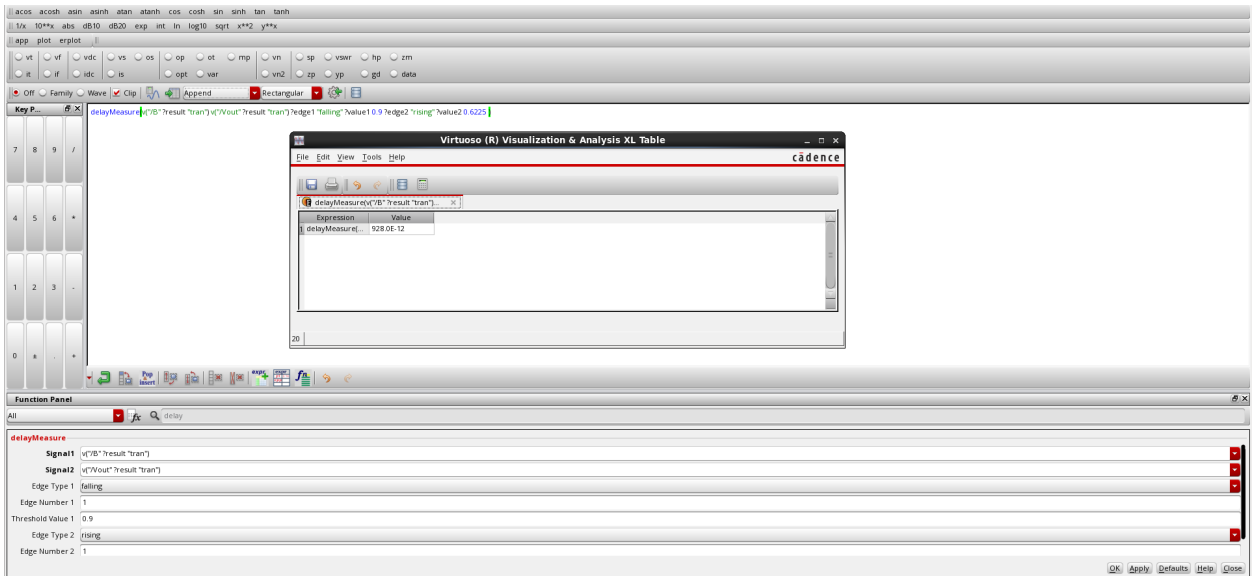
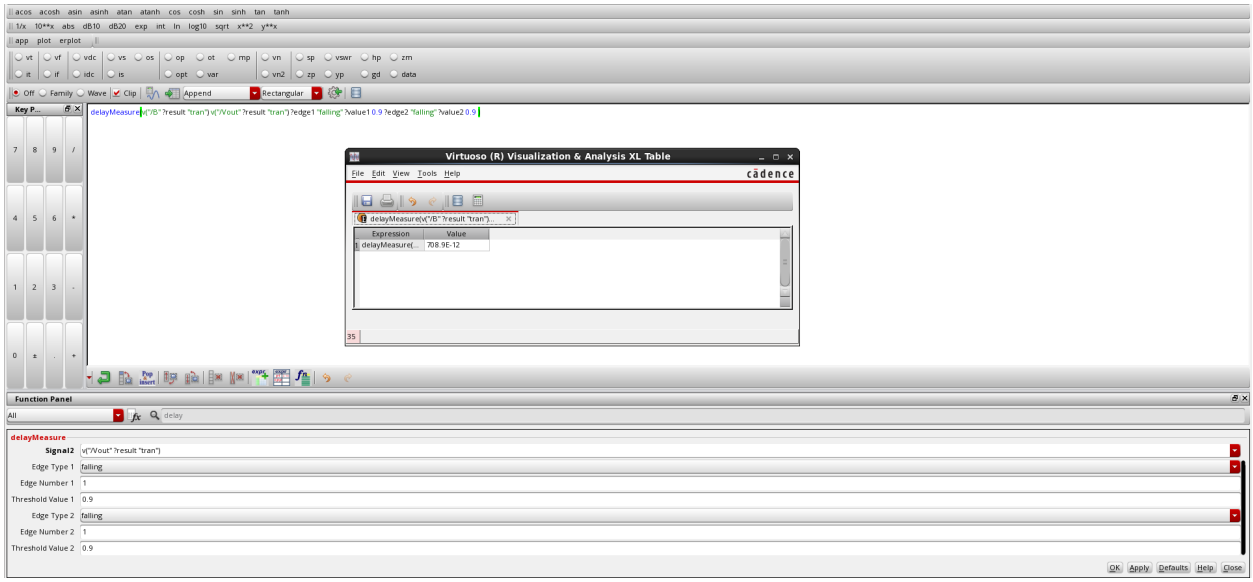


AND GATE using TGL:-

tpHL:



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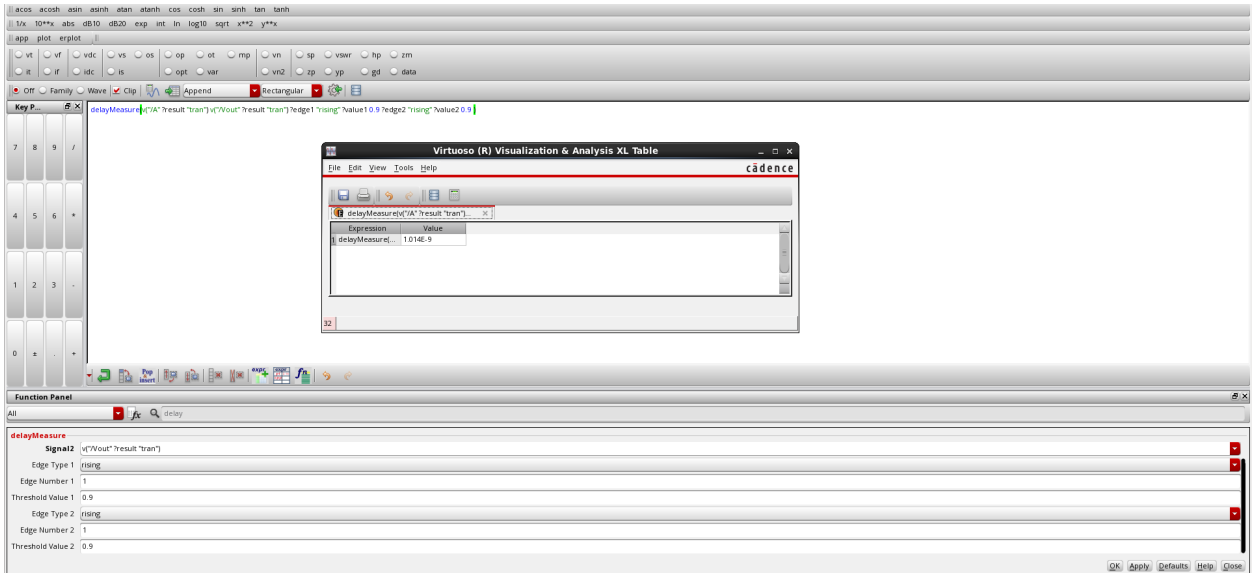

OR GATE using TGL:-

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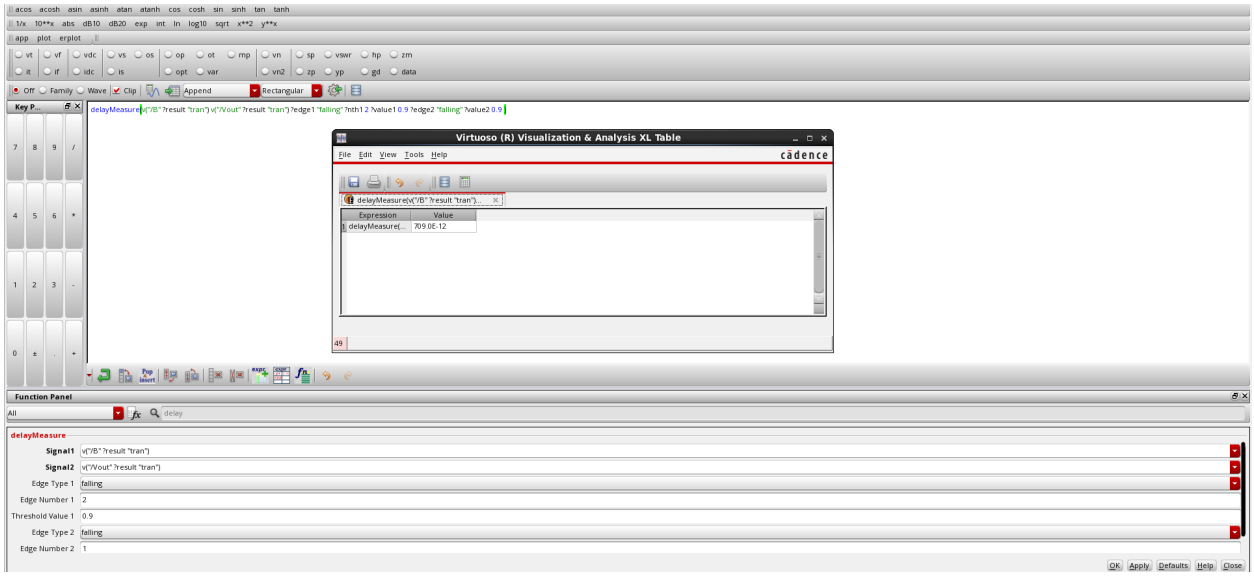

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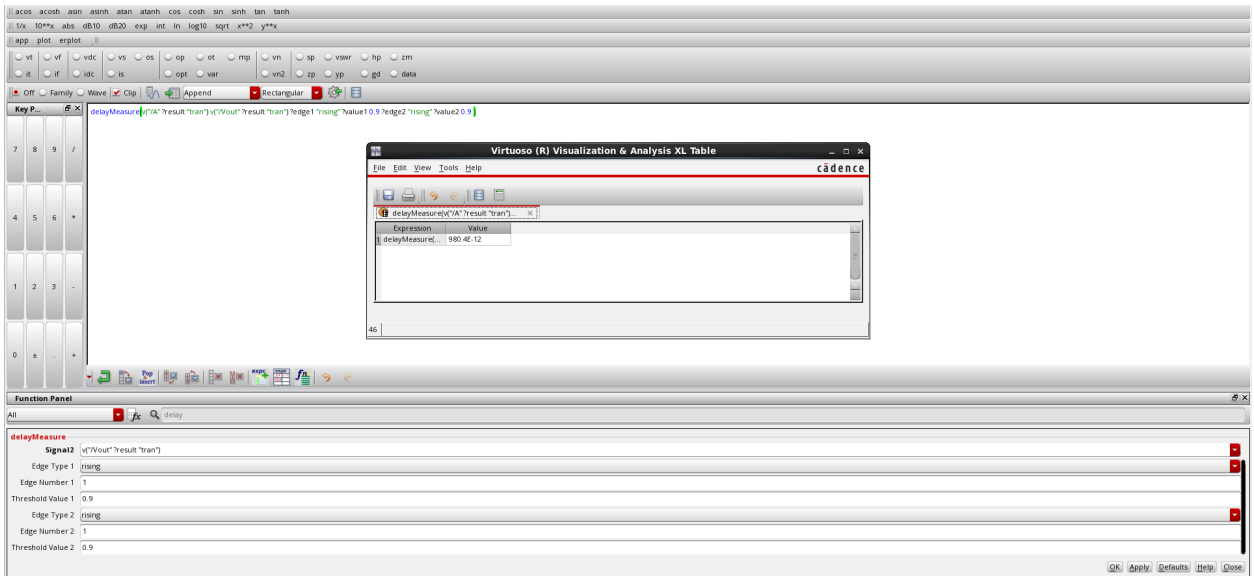

XOR GATE using TGL:-

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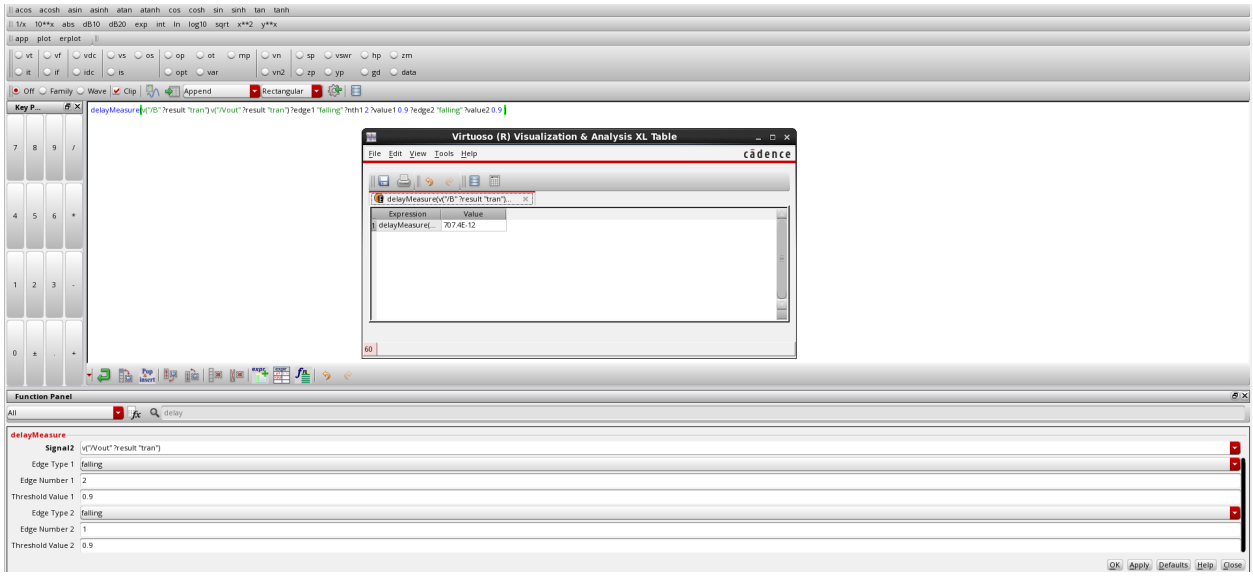
Virtuoso (R) Visualization & Analysis XL Table
File Edit View Tools Help
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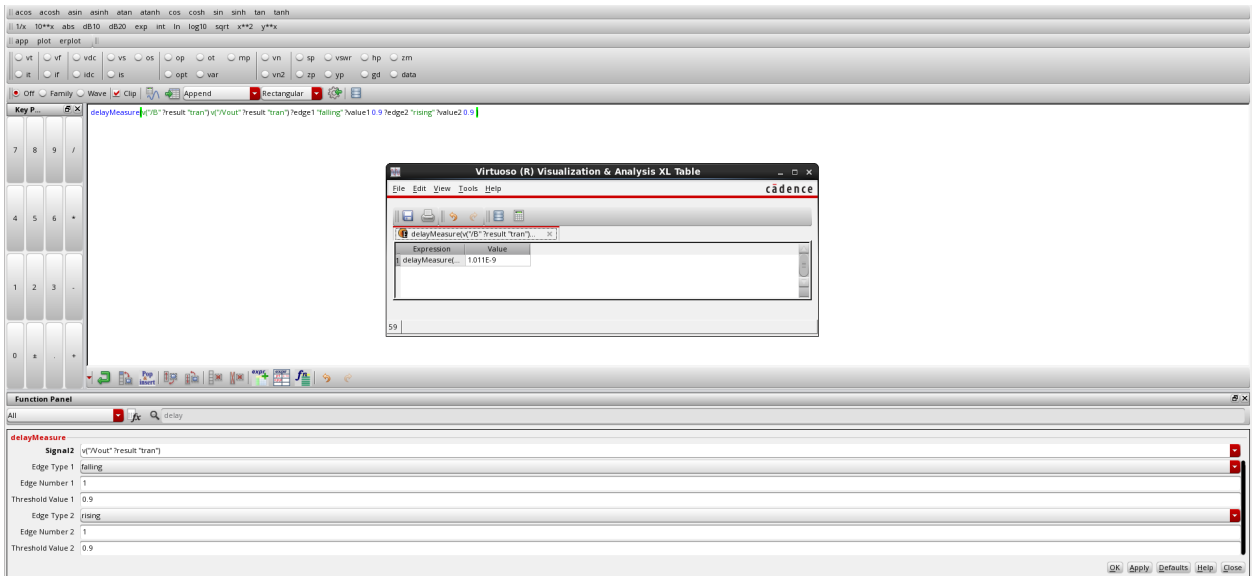
Expression Value
delayMeasure(... 707.4E-12
Function Panel
delayMeasure
Signal2 v("/Vout" ?result "tran")
Edge Type 1 falling
Edge Number 1 2
Threshold Value 1 0.9
Edge Type 2 falling
Edge Number 2 1
Threshold Value 2 0.9
OK Apply Defaults Help Close

t_{pLH}:


Virtuoso (R) Visualization & Analysis XL Table
File Edit View Tools Help
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Expression Value
delayMeasure(... 1.011E-9
Function Panel
delayMeasure
Signal2 v("/Vout" ?result "tran")
Edge Type 1 falling
Edge Number 1 1
Threshold Value 1 0.9
Edge Type 2 rising
Edge Number 2 1
Threshold Value 2 0.9
OK Apply Defaults Help Close

Metrics Measured:

All these metrics are measured for a load capacitance = 1 pF.

GATE	Voltage Swing	Power Dissipated	t_{worst}
AND (CMOS)	1.8 V	1.696 μW	2.146 ns
AND (PTL)	1.233 V	695.5 nW	881 ps
AND (TGL)	1.8 V	1.020 μW	1.014 ns
OR (CMOS)	1.8 V	852.8 nW	2.099 ns
OR (PTL)	1.256 V	630.7 nW	1.071 ns
OR (TGL)	1.805 V	860.3 nW	980.4 ps
XOR (CMOS)	1.8 V	2.546 μW	4.105 ns
XOR (PTL)	1.245 V	659 nW	928 ps
XOR (TGL)	1.804 V	895.2 nW	1.011 ns

Inferences:

1. When the same gate is constructed once using pass transistors and then using transmission gates, the delay involved in transmission gate logic is larger because more transistors are present (as compared to PTL) leading to larger resistance in the RC network. Also, the power dissipation is larger for transmission gate logic style because of similar reasons.

2. Voltage swing in Pass Transistor logic is reduced while in transmission gate style, we still obtain a rail-to-rail swing. This is because in pass transistors we use only NMOS transistors which are weak at passing a 1-logic level. That is, they can pass a

maximum voltage of 'V_{DD} - $V_{T,n}$'. While by connecting NMOS (strong passer of '0') and PMOS (strong passer of '1'), we can get a rail-to-rail swing in transmission gates.

3. The power dissipation and the delay is the largest in CMOS circuits because of the large number of PMOS and NMOS transistors involved in building the logic network.

Conclusion:

In this experiment, we learnt how to design AND, OR, and XOR Gates using Pass Transistor and Transmission GATE Logic Styles. We also learnt how to measure the power dissipation in a circuit using transient analyses in Cadence. Finally, we drew some observations regarding the different design metrics such as power dissipation, delay, voltage swing, etc., in these different logic styles.