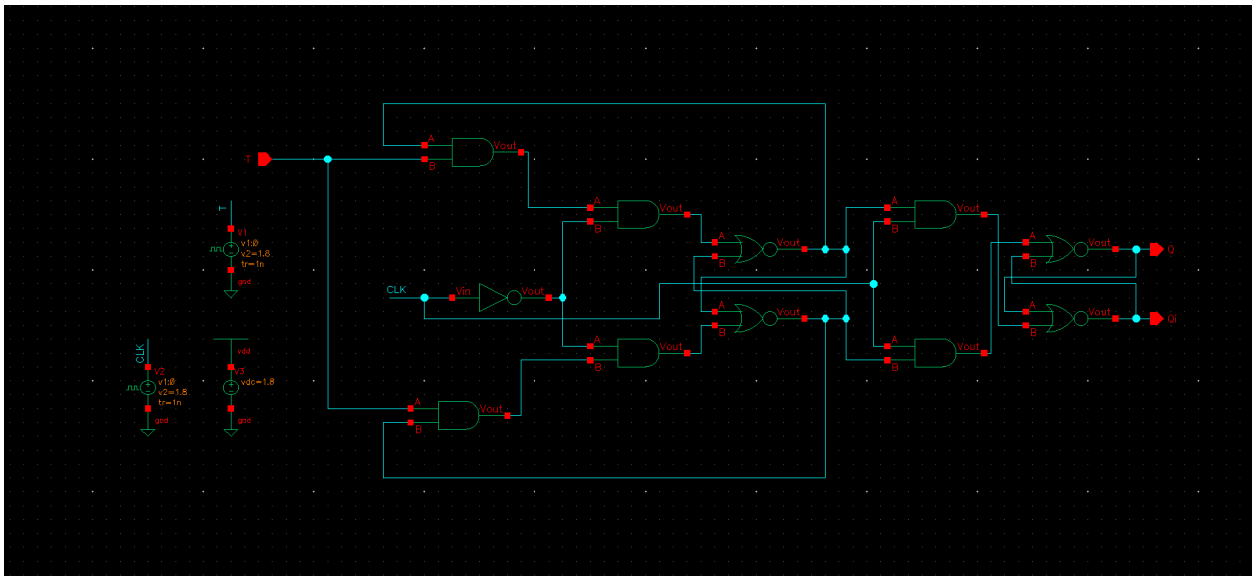
VLSI LAB Exercise-6 T - FlipFlop using Static CMOS Gates

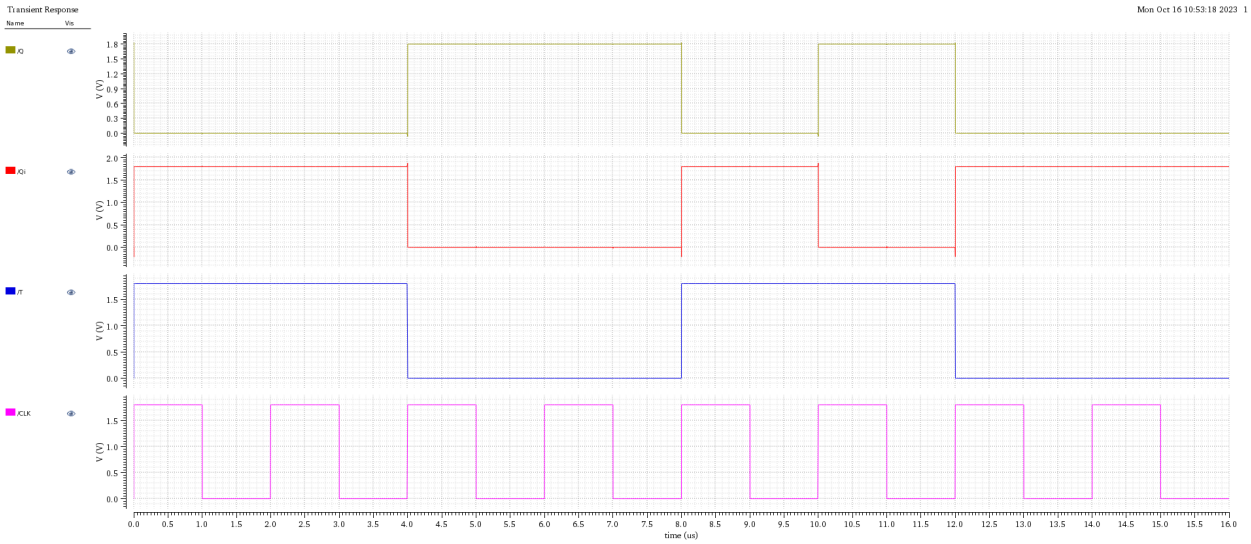
Group Number: 2

Group Members:
Thathapudi Sanjeev Paul Joel - 2020AAPS0120H
Aditya Anirudh - 2020AAPS0373H

Schematics:



Waveforms:



Metrics Measured:

$t_{clk\text{-}Q(LH)}$ = 517.9 ps

$t_{clk\text{-}Q(HL)}$ = 514.6 ps

t_{setup} =

t_{hold} =

Power dissipation = 244 µW

Conclusion:

In this exercise, we designed a T-flip flop using **master-slave configuration of SR-latches** with relevant excitations to the SET and RESET inputs. We also measured the different timing factors like clocked-Q delay, setup time, and hold time.