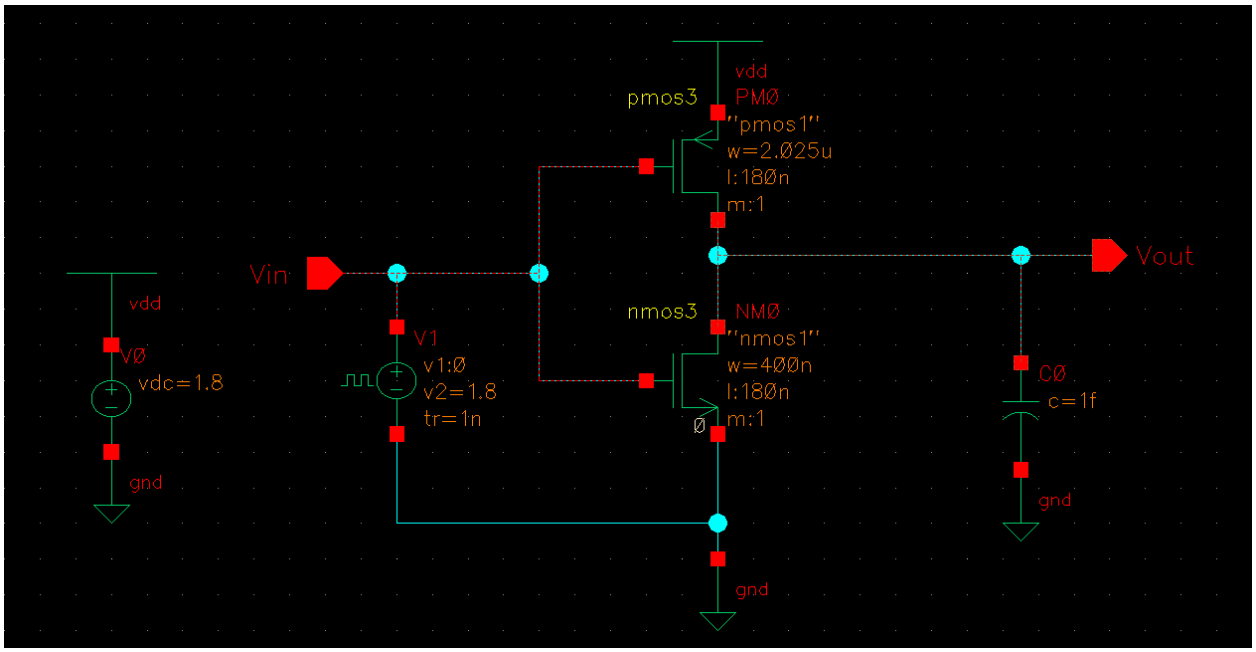
VLSI LAB Exercise-2 CMOS INVERTER SWITCHING CHARACTERISTICS

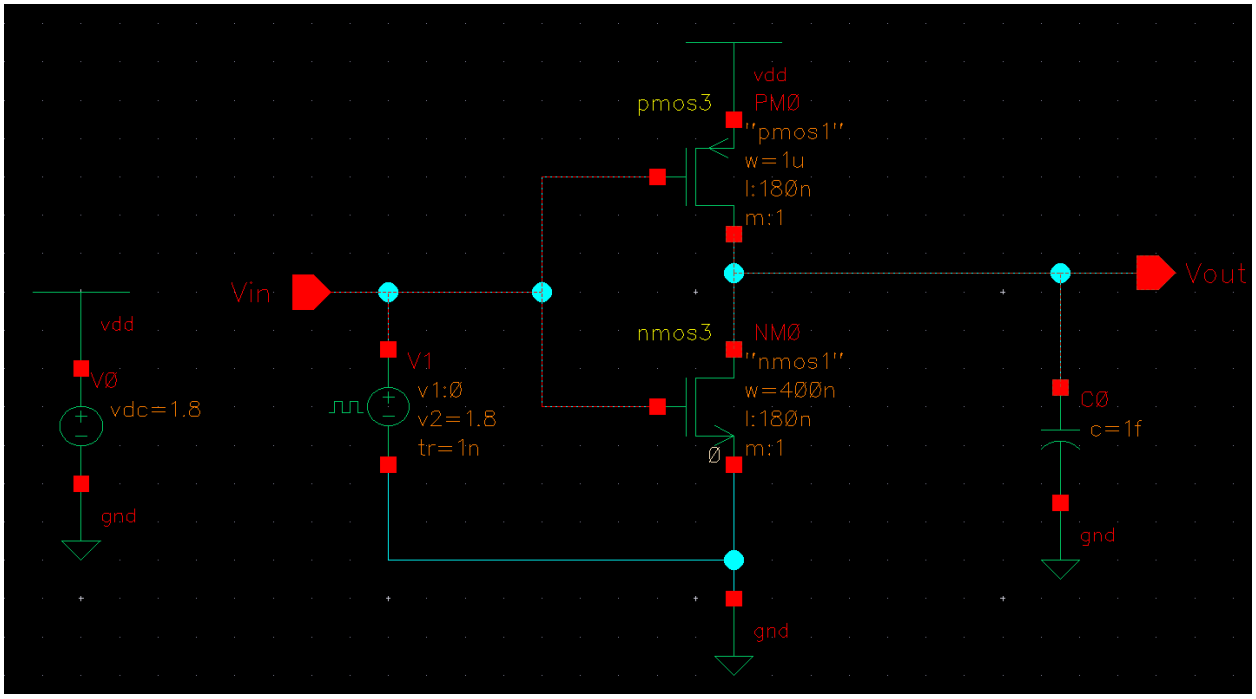
Group Number: 2

Group Members:
Thathapudi Sanjeev Paul Joel - 2020AAPS0120H
Aditya Anirudh - 2020AAPS0373H

Schematics:
Symmetric Inverter:



Inverter with PMOS Width = 1 µm:



Theoretical Calculations:

We used the average current method in evaluating approximate values of low-to-high and high-to-low transition delays as follows:

High-to-Low Transition -

→ Here we're only concerned with the pull-down strength of NMOS. So we write the current equations w.r.t that -

$V_{in} = V_{OH}$, $V_{out} = V_{OH}$ (Saturation) I_{D_1}

$V_{in} = V_{OH}$, $V_{out} = V_{50\%}$ (Linear) I_{D_2}

$$I_{D_1} = \frac{1}{2}\mu_n C_{ox}\left(\frac{W}{L}\right)_n (V_{GS} - V_{T,n})^2$$

$$= \frac{1}{2} \times 350 \times \left(\frac{400}{180}\right) \times (1.8 - 0 - 0.429)^2$$

$$= 730.9715\,\mu A.$$

$$I_{D_2} = \frac{1}{2}\mu_n C_{ox}\left(\frac{W}{L}\right)_n \left((V_{GS} - V_{T,n})V_{DS} - \frac{1}{2}V_{DS}^2\right)$$

$$= 350 \times \left(\frac{400}{180}\right) \times \left((1.8 - 0.429)0.9 - \frac{0.9^2}{2}\right)$$

$$= 644.7\,\mu A$$

$$I_{avg\,HL} = \frac{I_{D1} + I_{D2}}{2} = 687.83575\,\mu A.$$

$$t_{PHL} = \frac{\Delta V \cdot C_L}{I_{avg\,HL}} = \frac{0.9 \times 10^{-15}}{687.83575\,\mu A} \approx 1.31\,ps$$

Low-to-High Transition -

→ Here we're only concerned with the pull-up strength of PMOS. So we write the current equations as follows -

$V_{in} = V_{OL}$, $V_{out} = V_{OL}$ (Saturation) I_{D_1}

$V_{in} = V_{OL}$, $V_{out} = V_{50\%}$ (linear) I_{D_2}

$$I_{D_1} = \frac{1}{2}\mu_p C_{ox}\left(\frac{W}{L}\right)_p (V_{in} - V_{DD} - V_{T,p})^2$$

$$\Rightarrow I_{D1} = \frac{1}{2} \times 5.0625 \times \left(\frac{400}{180}\right) \times (0 - 1.8 + 0.468)^2 \times 70$$

$$= 698.6\ \mu A$$

$$I_{D2} = \mu_p C_{ox} \left(\frac{W}{L}\right)_p \left((V_{GS} - V_{T,p}) V_{DS} - \frac{1}{2} V_{DS}^2\right)$$

$$= 70 \times 5.0625 \times \left(\frac{400}{180}\right) \times \left((0 - 1.8 + 0.468)(-0.9) - \frac{1}{2}(-0.9)^2\right)$$

$$= 625.1175\ \mu A$$

$$\Rightarrow I_{avg.LH} = 661.85875\ \mu A$$

$$\tau_{PLH} = \frac{\Delta V C_L}{I_{avg.LH}} = \frac{0.9 \times 10^{-15}}{661.85875 \times 10^{-6}}$$

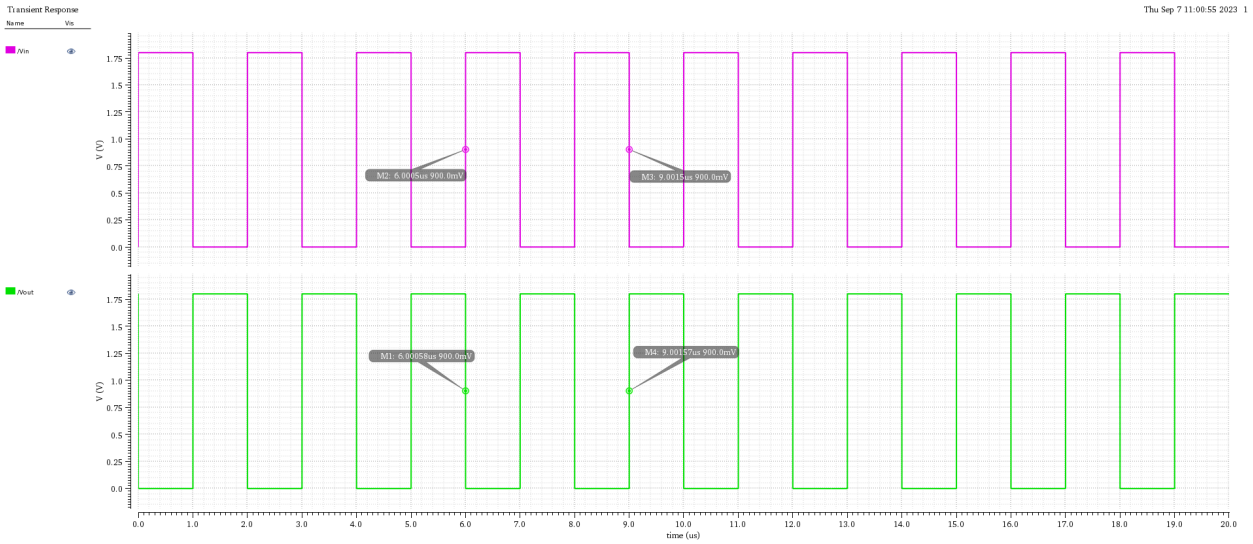
$$= 1.36\ ps$$

$$\begin{cases} \tau_{PHL}(practical) = 75.69\ ps \\ \tau_{PLH}(practical) = 71.25\ ps \end{cases}$$

$$\begin{cases} \tau_{rise} = 151.7\ ps \\ \tau_{fall} = 151.7\ ps \end{cases}$$

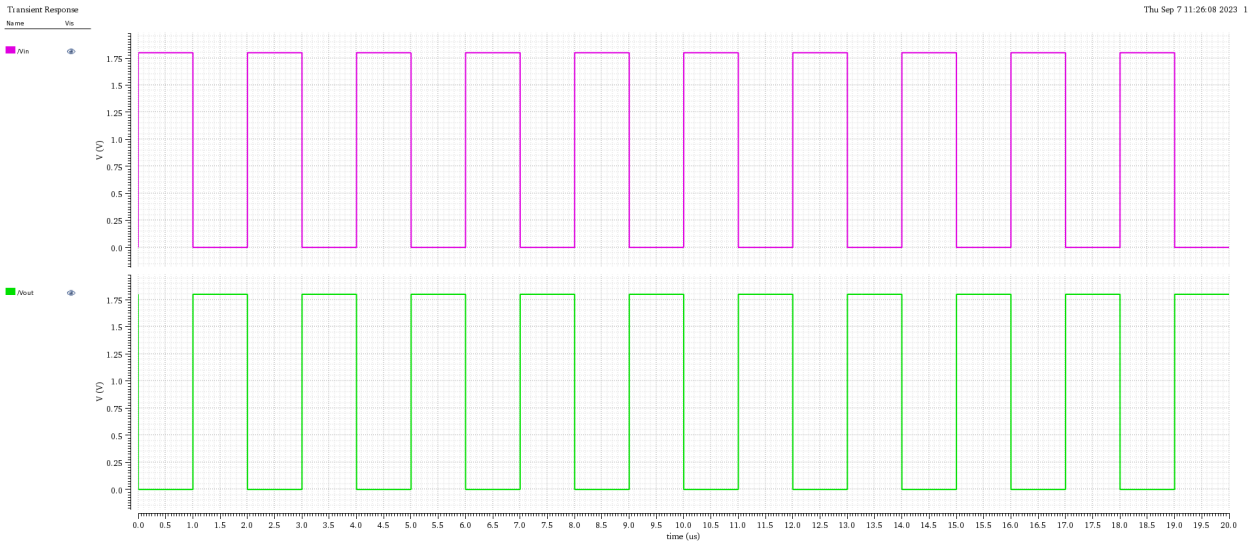
Waveforms:

Symmetric Inverter:



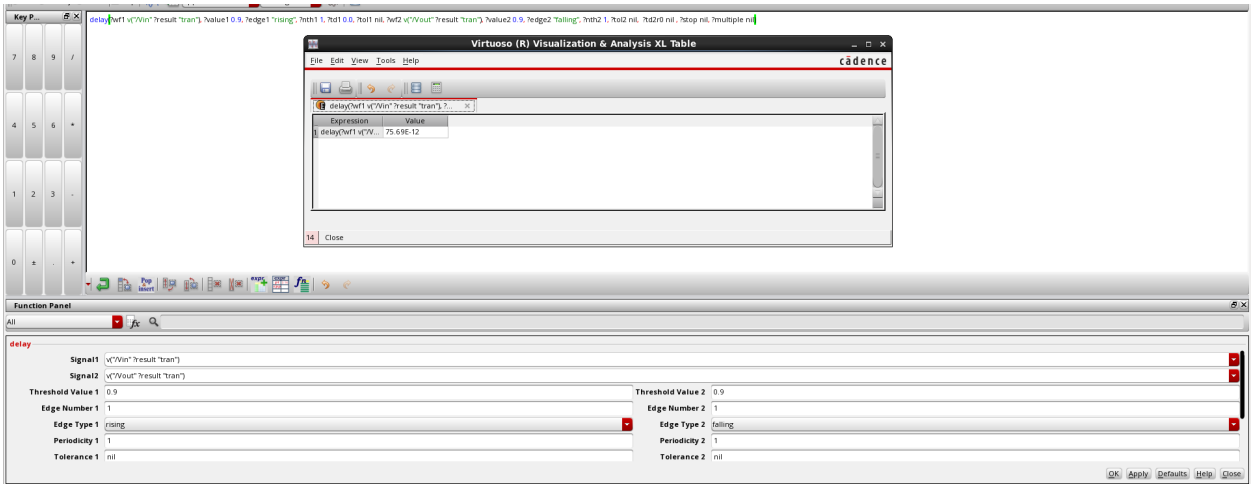
t_{PHL} and t_{PLH} are nearly equal for a symmetrical inverter.

Inverter with PMOS Width = 1 µm:

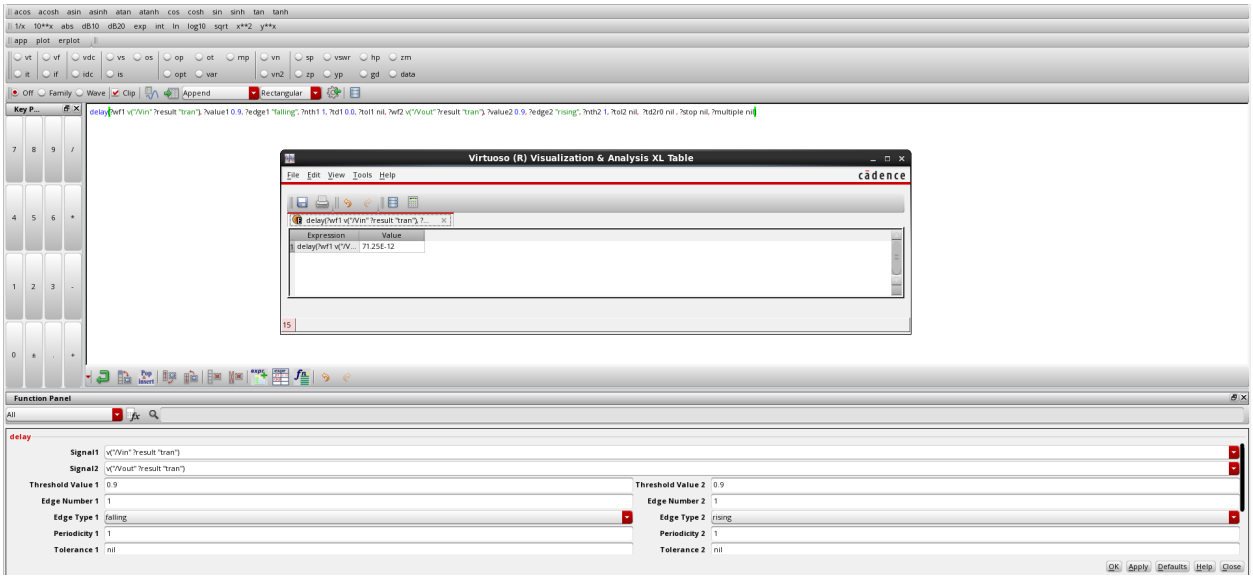


<u>Observations</u>:

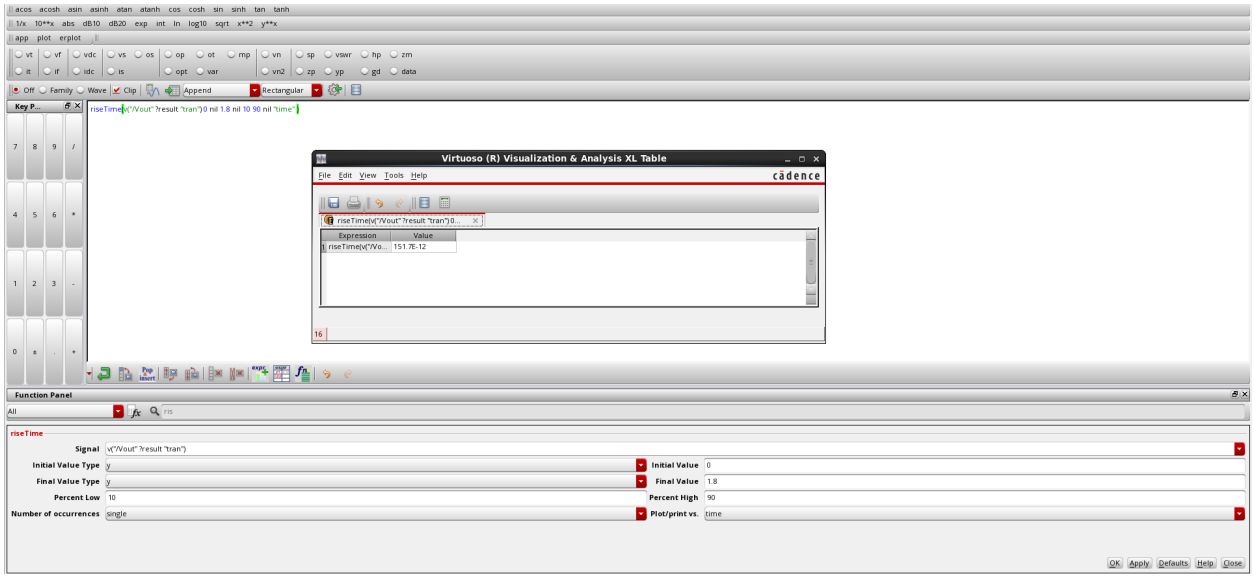
t_{PHL} of symmetrical inverter:



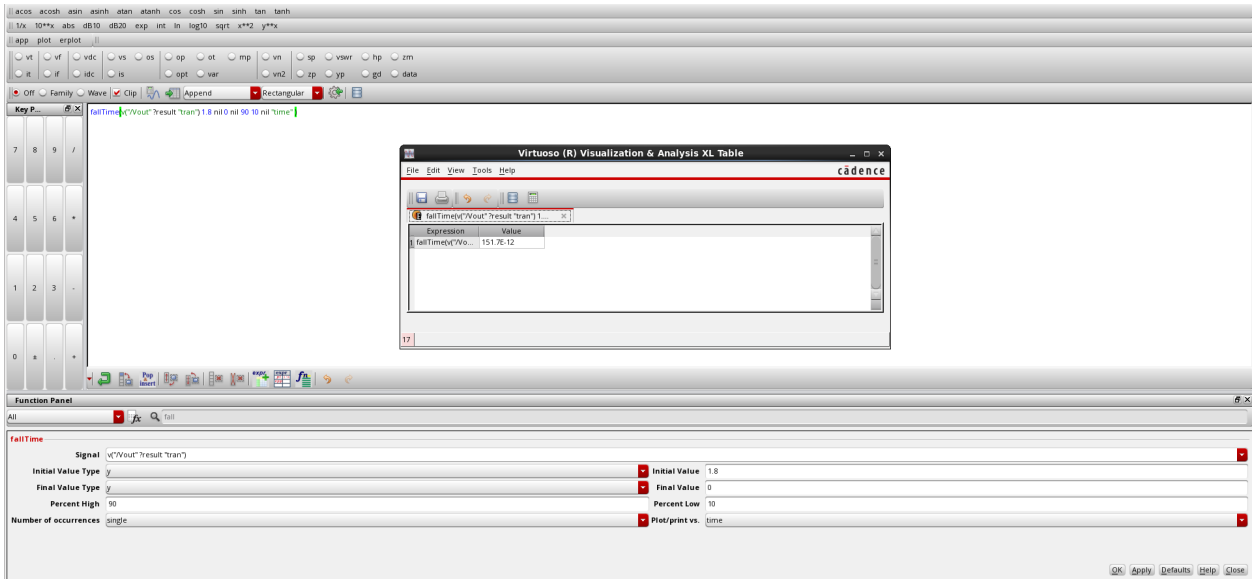
t_{PLH} of symmetrical inverter:



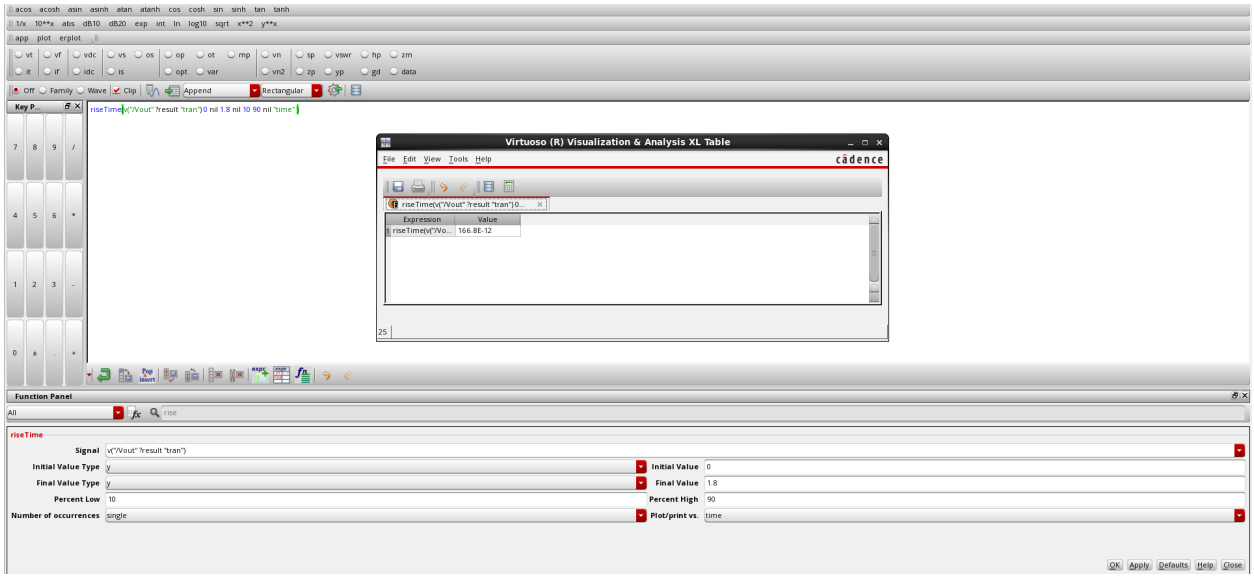
t_{rise} of symmetrical inverter:



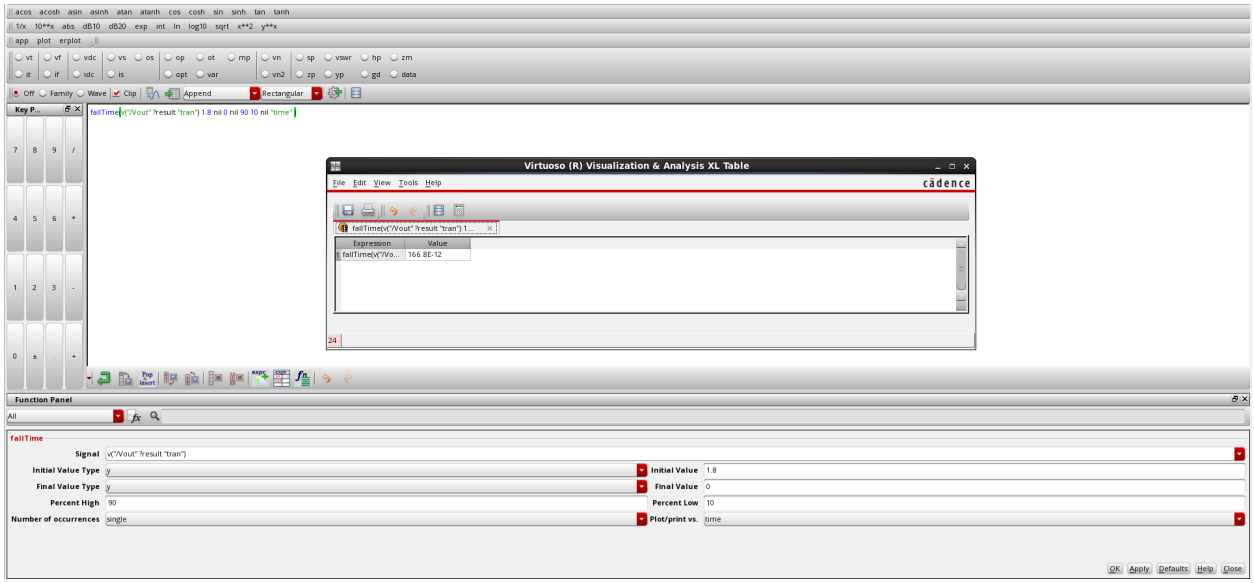
t_{fall} of symmetrical inverter:



t_{rise} of inverter with PMOS width = 1 µm:



t_{fall} of inverter with PMOS width = 1 µm:



<u>Metrics Measured</u>:

Symmetrical Inverter:

t_{PHL} (theoretical) = 1.31 ps

t_{PLH} (theoretical) = 1.36 ps

t_{PHL} (practical) = 75.69 ps

t_{PLH} (practical) = 71.25 ps

$t_{rise} = t_{fall}$ = 151.7 ps

Inverter with PMOS Width = 1 µm:
$t_{rise} = t_{fall} = 166.8$ ps

Inferences:

1. t_{PLH} and t_{PHL} values for theoretical and practical cases differ very much probably because the rise and fall times of the input signal applied is non-zero in value.

2. Also we saw in our previous experiment that the delay values of low-to-high and high-to-low transitions are much higher than in this experiment (of the order of µsec). This is because the load capacitance has changed from 1pF to 1fF.

$$\text{delay} \propto R*C_{load}$$

3. Upon decreasing the width of the PMOS transistor (pull-up transistor) from 2.025 µm to 1 µm, the rise and fall times of the inverter increased. This is because, as the width of PMOS is reduced, the amount of average pull-up current also reduces thus taking more time to charge the load capacitor than before. Hence, the rise time increases.

Conclusion:

In this experiment, we learned how to evaluate the transition delays, rise time, and fall time for a CMOS inverter using the calculator tool in Cadence Virtuoso. We also studied the effect on the rise and fall time values upon modifying the widths of the NMOS and PMOS transistors.