Exercise 2

1. Calculate the propagation delay of a symmetric CMOS inverter using the average capacitor current method. The design specifications of the inverter are as follows; $\mu_n C_{ox}$ = 350 μA/V^2, $\mu_p C_{ox}$ = 70 μA/V^2, and load capacitance is 1fF. (Use threshold voltage values obtained from experiment 1 and PMOS/NMOS width values from experiment 2). Simulate the same on Cadence Virtuoso and comment on your observations. Use the calculator in Virtuoso for measuring the delay.
2. Compare a symmetric CMOS inverter's rise and fall time to that of a CMOS inverter whose PMOS width is 1μm, and comment on your observations. Use the calculator in Virtuoso for measuring rise and fall time.