VLSI LAB Exercise-7 NAND Gate Layout

Group Number: 2

Group Members:
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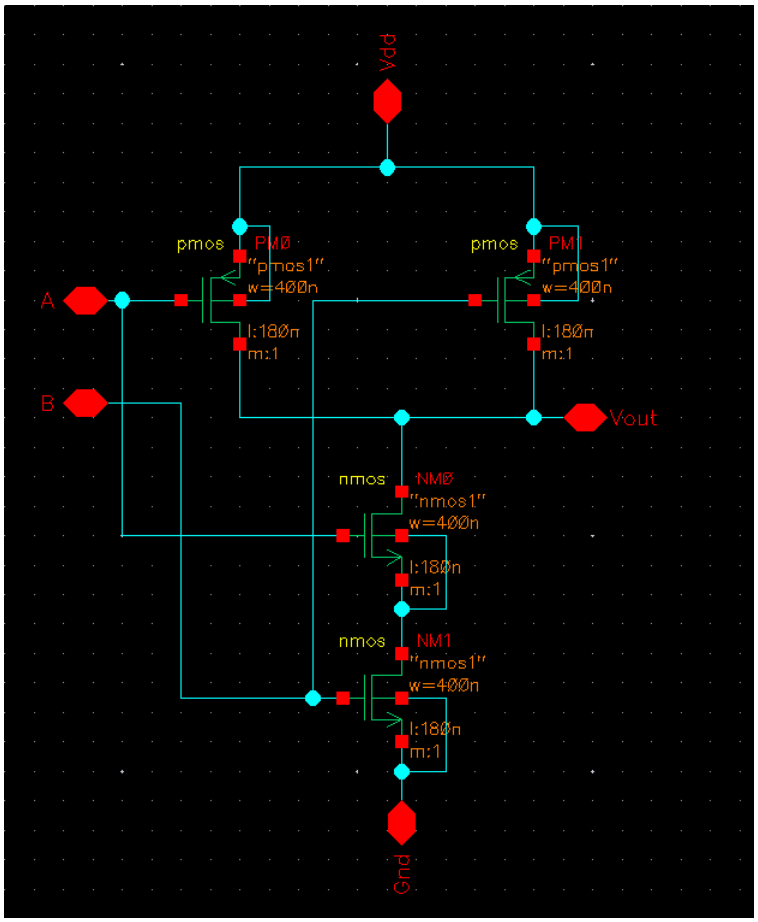
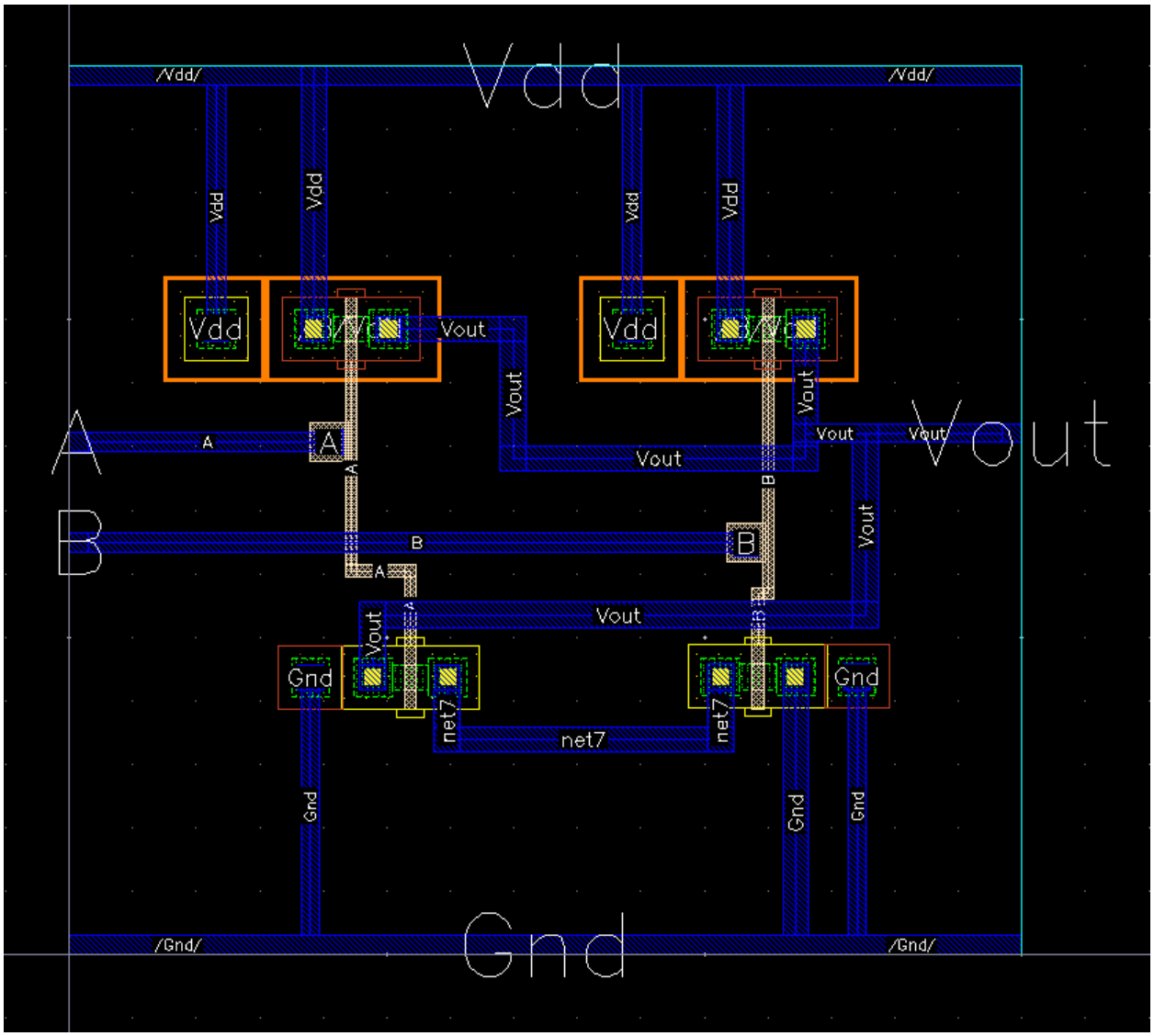
Schematic:

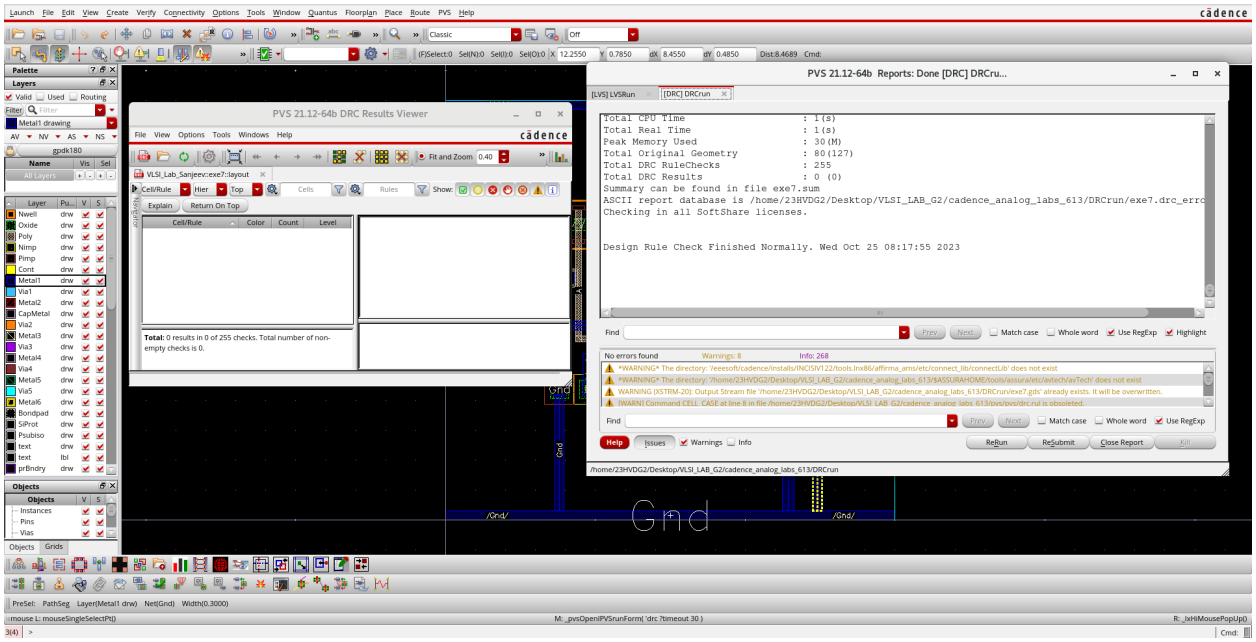


Layout:

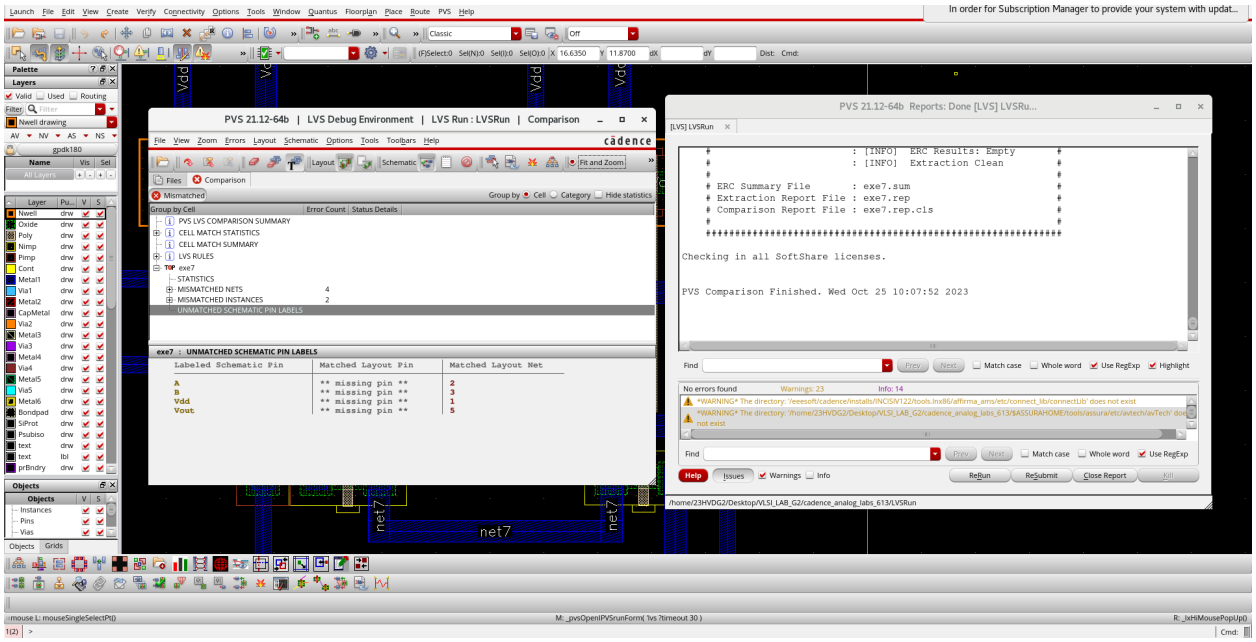


Simulation Results:

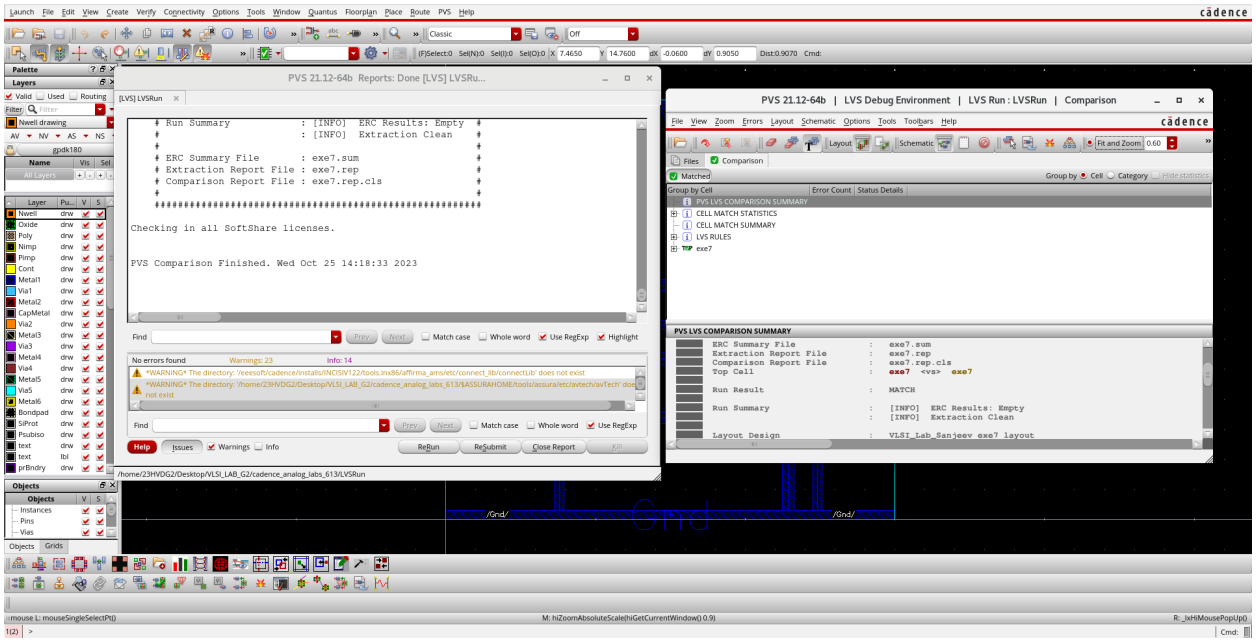
Results obtained for DRC:-



Results obtained for LVS (before pin matching):-



Results obtained for LVS (after pin matching):-



Conclusion:

In this experiment, we learnt how to design the **layout for a CMOS NAND Gate** using Cadence. Then we used the **DRC** and **LVS tools** to check if the layout is behaving correctly or not.