VLSI DESIGN LAB Experiment-3 CMOS INVERTER (Part-2)

Group Number: 2

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Width of PMOS transistor when V_M = 0.8 V:

CMOS INVERTER-2

At the midpoint voltage, $V_{in} = V_{out} = V_M$, and both NMOS and PMOS are in saturation,

$$\Rightarrow I_{DS,n} = I_{DSp}$$

$$\frac{1}{2}\mu_n C_{ox}\left(\frac{W}{L}\right)_n (V_{in} - V_{TO,n})^2 = \frac{1}{2}\mu_p C_{ox}\left(\frac{W}{L}\right)_p (V_{in} - V_{DD} - V_{TO,p})^2$$

$$\Rightarrow \frac{(W/L)_n}{(W/L)_p} = \frac{\mu_p}{\mu_n} \cdot \frac{(V_{in} - V_{DD} - V_{TO,p})^2}{(V_{in} - V_{TO,n})^2}$$

$$\Rightarrow (W/L)_p = \frac{\mu_n}{\mu_p} \cdot \frac{(V_{in} - V_{TO,n})^2}{(V_{in} - V_{DD} - V_{TO,p})^2} \cdot (W/L)_n$$

$\because \frac{\mu_n}{\mu_p} = \frac{\mu_n C_{ox}}{\mu_p C_{ox}} = \frac{350}{70} = 5$, $V_M = 0.8\,V = V_{in}$,

$V_{TO,n} = 0.429\,V$, $V_{TO,p} = -0.468\,V$.

substituting these values, we get -

$$\frac{(W/L)_p}{(W/L)_n} = 5 \cdot \frac{(0.8 - 0.429)^2}{(0.8 - 1.8 + 0.468)^2}$$

$\because L_p = L_n$

$$\Rightarrow \frac{W_p}{W_n} = 2.432$$

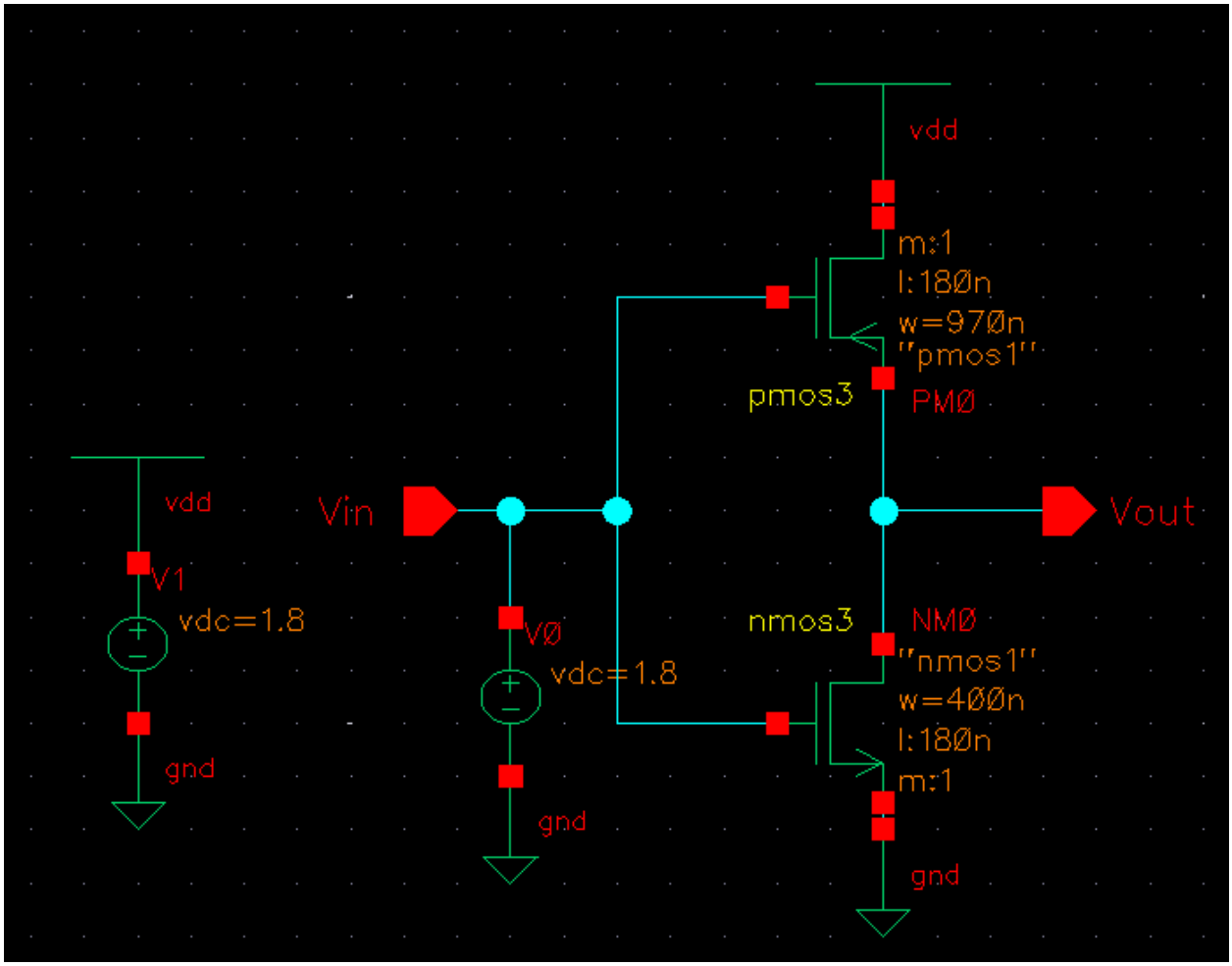
Taking $W_n = 400\,nm$, we get W_p as -

$$W_p = 2.432 * 400 = 972.8 \approx 970\,nm$$

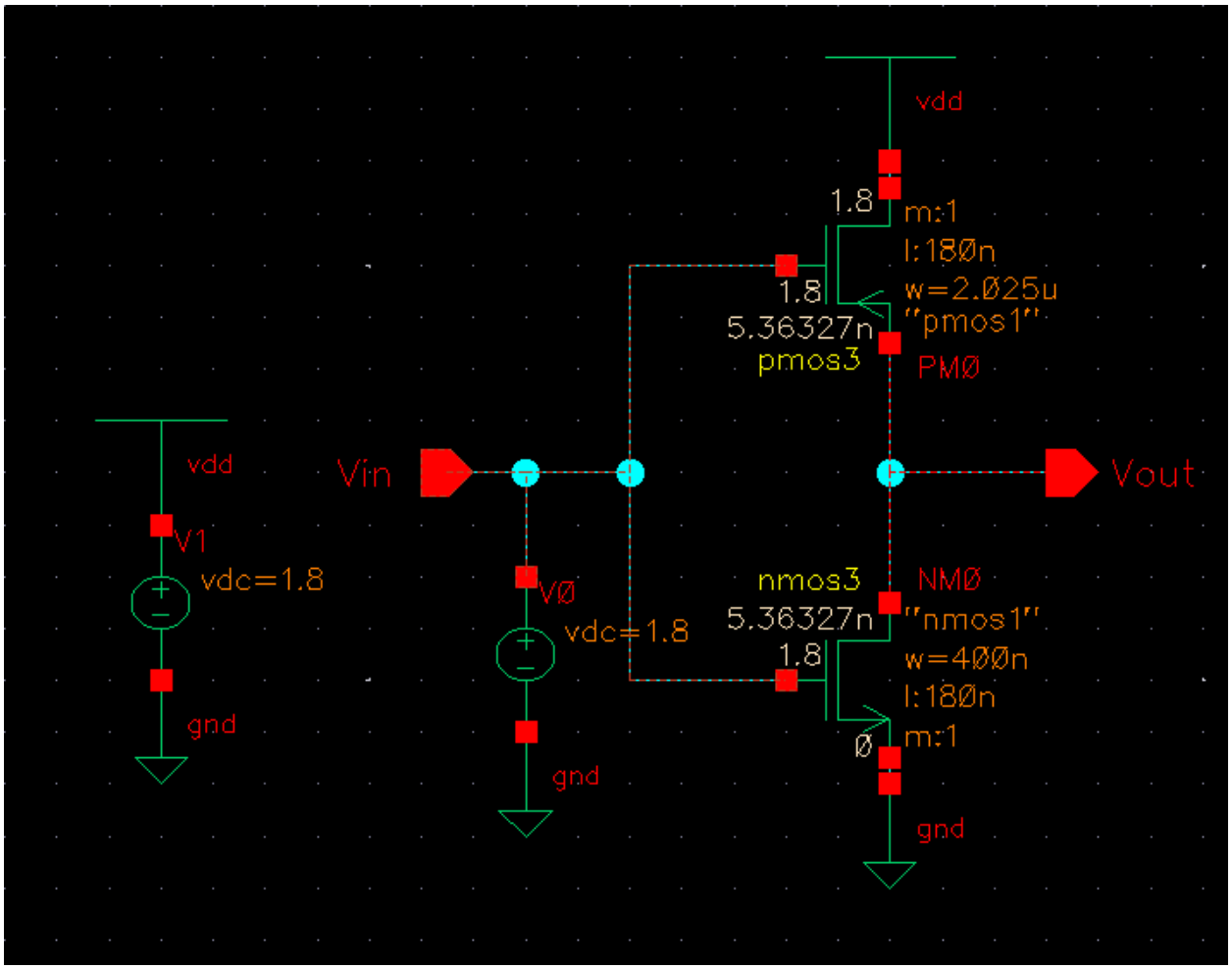
$$\Rightarrow \boxed{W_p = 970\,nm} \rightarrow \text{For } V_M = 0.8V$$

Schematics:

CMOS Inverter with V_M = 0.8 V:

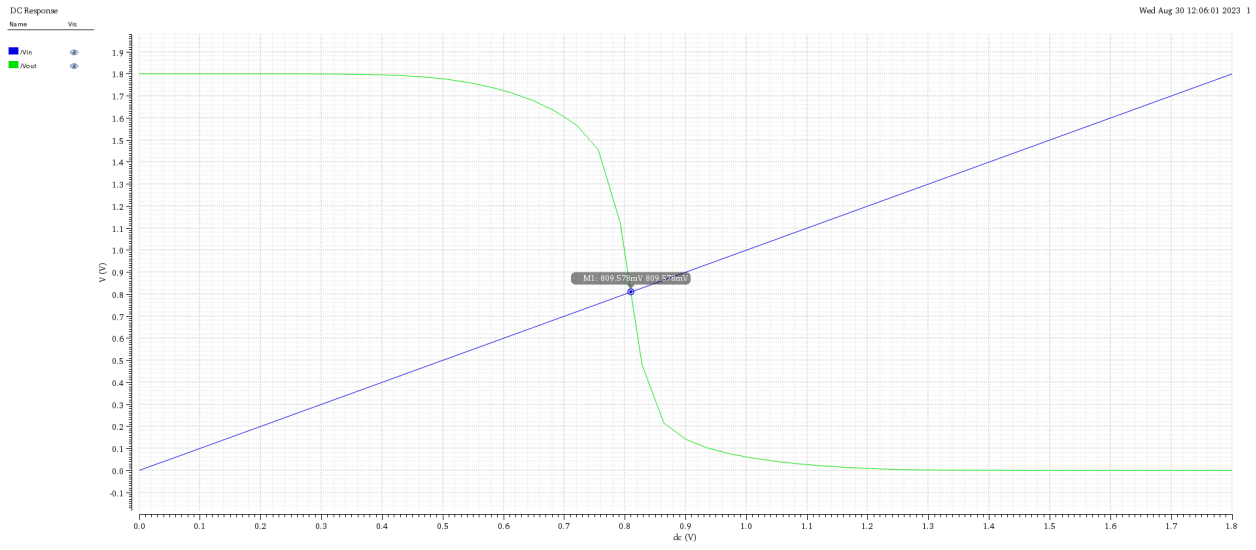


CMOS Inverter with V_M = 0.9 V (Symmetric switching threshold):

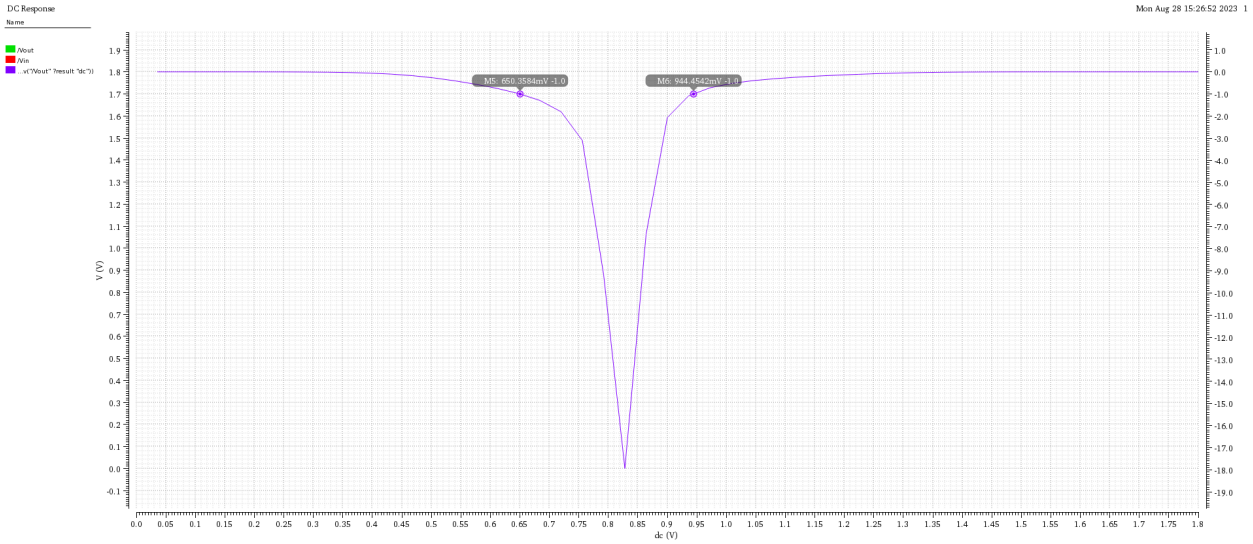


Waveforms:

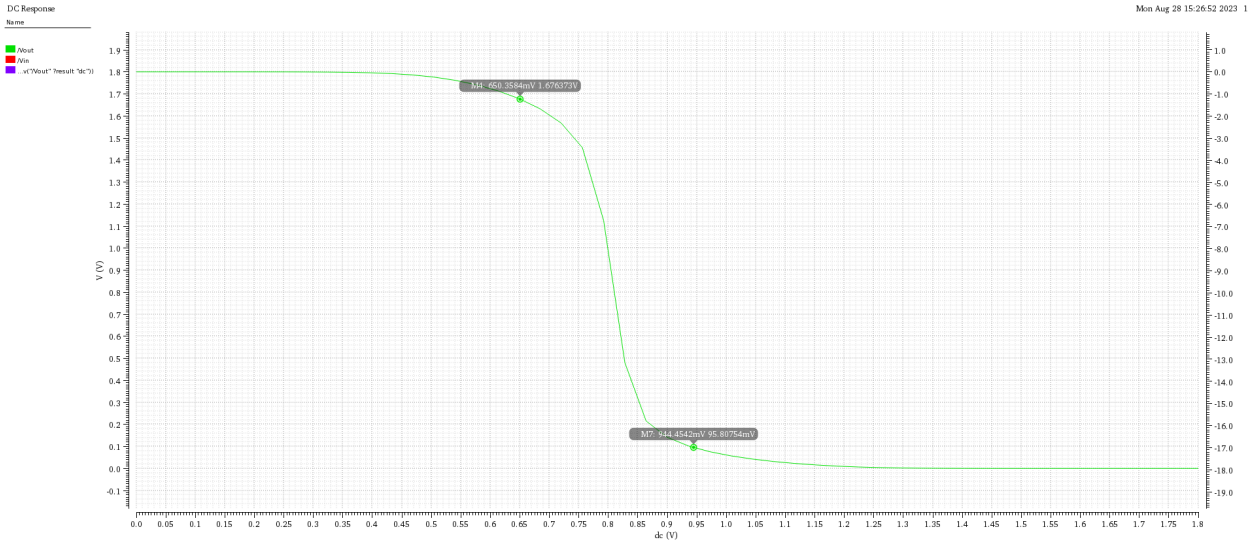
CMOS Inverter with V_M = 0.8 V:



Plot displaying the switching threshold at nearly V_M = 0.81 V.

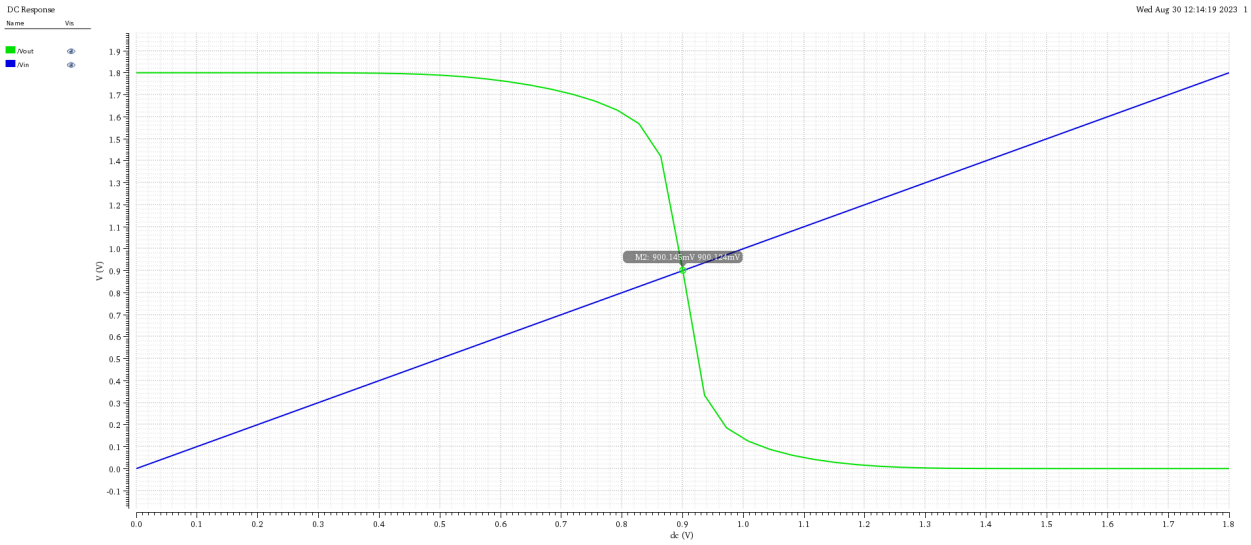


Plot displaying the derivative, dV_{out}/dV_{in}. The points where the ordinate = -1 are also displayed.

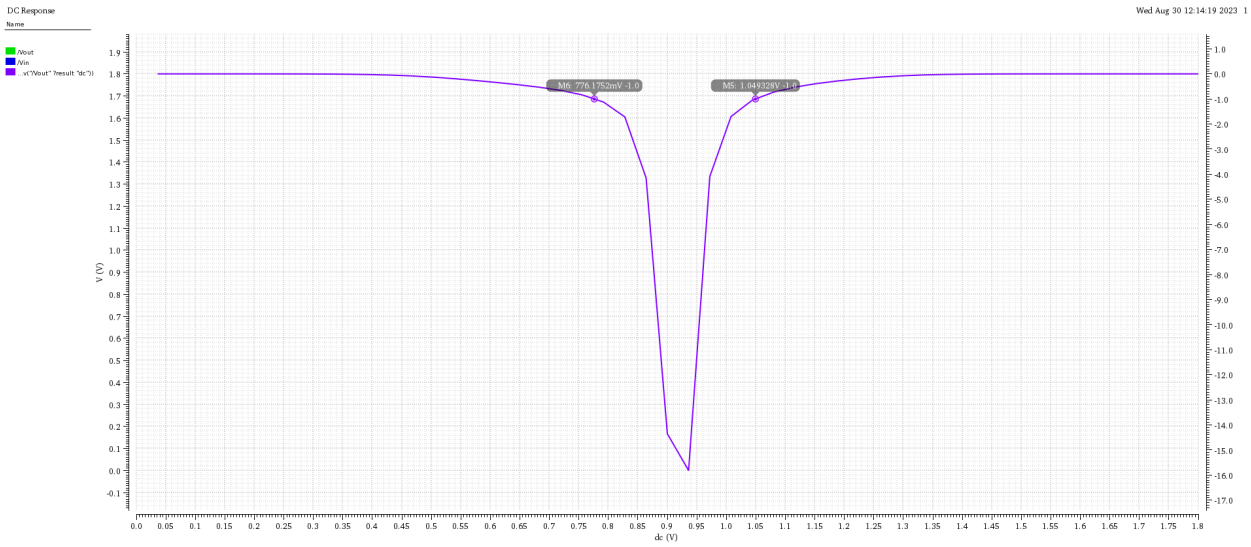


Plot displaying the ordered pairs, (V_{IL}, V_{OH}) & (V_{IH}, V_{OL}).

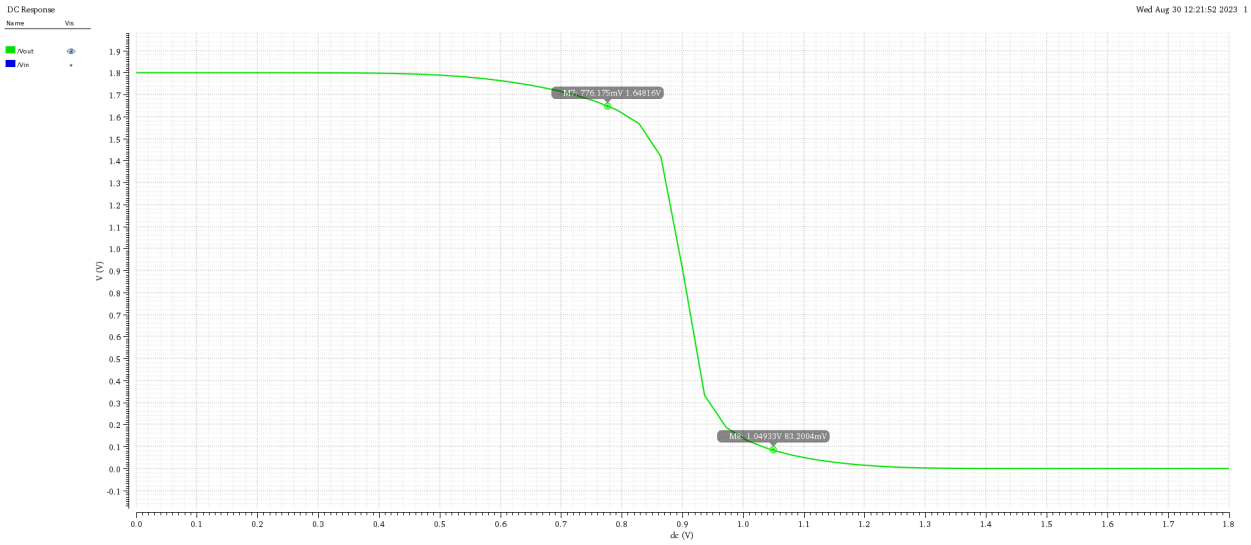
CMOS Inverter with V_M = 0.9 V (Symmetric switching threshold):



Plot displaying the switching threshold at nearly V_M = 0.9 V.



Plot displaying the derivative, dV_{out}/dV_{in}. The points where the ordinate = -1 are also displayed.



Plot displaying the ordered pairs, (V_{IL}, V_{OH}) & (V_{IH}, V_{OL}).

<u>Metrics Measured</u>:

CMOS Inverter with V_M = 0.8 V:

V_M = 809.578 mV (practical)

V_{IL} = 650.3584 mV V_{IH} = 944.4542 mV

V_{OL} = 95.80754 mV V_{OH} = 1.67637 V

NM_H = 0.731916 V NM_L = 0.55455 V

W_p/W_n = 2.432 (For obtaining V_M = 0.8 V)

W_p ~ 970 nm for W_n = 400 nm.

CMOS Inverter with V_M = 0.9 V (Symmetric switching threshold):

V_M = 712.09 mV

V_{IL} = 776.175 mV V_{IH} = 1.04933 V

V_{OL} = 83.2004 mV V_{OH} = 1.64816 V

NM_H = 0.59883 V NM_L = 0.6929746 V

W_p/W_n = 5.0625 (For symmetrical transfer characteristics)

W_p ~ 2.025 μm for W_n = 400 nm.

The noise margin of output = logic-0 increased for V_M =0.9 V as compared to V_M = 0.8 V. This is expected because even when we assume that the transition is abrupt (V_{IL}=V_{IH}=V_M), increasing V_M from 0.8 to 0.9 V would increase the range of voltages where input = logic-0. Similarly, this would decrease the range of voltages where input = logic-1 and hence the noise margin of output = logic-1 is reduced.

For simplicity, assuming V_{IL}=V_{IH}=V_M and V_{OL}=0, V_{OH}=V_{DD}=1.8 V:
V_M = 0.8 V,
$NM_H = V_{OH} - V_{IH} = 1.8 - 0.8 = 1.0$ V
$NM_L = V_{IL} - V_{OL} = 0.8 - 0 = 0.8$ V

V_M = 0.9 V (increased V_M),
$NM_H = V_{OH} - V_{IH} = 1.8 - 0.9 = 0.9$ V (HIGH Noise Margin reduced)
$NM_L = V_{IL} - V_{OL} = 0.9 - 0 = 0.9$ V (LOW Noise Margin increased)

Conclusion:
In this experiment, we designed a CMOS Inverter with a custom switching threshold (V_M = 0.8 V). We have obtained the V_{IL}, V_{IH}, V_{OL}, V_{OH} values, and the noise margins NM_L, & NM_H. Finally, we also obtained the same parameters for a CMOS inverter with a symmetric switching threshold and compared its performance with that of V_M = 0.8 V.