Weiwei Chen

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EDUCATION

- **Doctor of Philosophy, Electrical and Computer Engineering** 2013
  Department of Electrical Engineering and Computer Science
  University of California, Irvine
  Dissertation: Out-of-Order Parallel Discrete Event Simulation for ESL Design
  Committee: Prof. Rainer Dömer, Prof. Daniel D. Gajski, Prof. Brian Demsky
  Outstanding Dissertation Award, European Design and Automation Association

- **Master of Science, Computer Engineering** 2007
  Thesis: A Symbolic Analog Circuit Simulator
  School of Microelectronics
  Shanghai Jiao Tong University, Shanghai, China

- **Bachelor of Engineering, Computer Science and Engineering** 2004
  Thesis: Design and Implementation of a Software Debugger for Digital Signal Processors
  Department of Computer Science and Engineering
  Teaching Reform Class (Advanced Admission)
  Shanghai Jiao Tong University, Shanghai, China

- **International Exchange Student** 2003
  Dean's List and Semester Honor
  School of Electrical and Computer Engineering
  Purdue University, West Lafayette, Indiana

- **High School Graduation** 2000

HONORS AND AWARDS

- Outstanding Dissertation Award, European Design and Automation Association (EDAA) 2014
- Best Paper Award, Design, Automation and Test Conference in Europe (DATE) 2014
- Three Qualstar Diamond Award, Qualcomm Inc. 2014
- Pedagogical Fellowship, UC Irvine 2012-13
- Young Student Support Award, Design Automation Conference (DAC) 2010
- *Henry Samueli* Endowed Fellowship, UC Irvine 2007
- National Scholarship for Academic Excellence, China 2006
- *Infineon, Guanghua, Morgan Stanley* Endowed Scholarship, SJTU 2004-2007
- Exceptional Undergraduate Student, SJTU 2001, 2003
- People's Scholarship for Academic Excellence, SJTU 2001-2004
- Fellowship of Pan Wen-Yuan Foundation 2001

RESEARCH INTERESTS

Parallel computing
Design automation for embedded computer systems
Embedded system-level modeling, validation, and analysis
Embedded hardware and software systems

RESEARCH EXPERIENCE

Qualcomm Research Silicon Valley
Senior Engineer October 2013 – Present

- *Parallel programming patterns for heterogeneous multi-core platforms*
  www.developer.qualcomm.com/mare

University of California, Irvine
Graduate Student Researcher, Department of EECS September 2007 – 2013

- Multi-core parallel simulation for Transaction-Level Models (TLMs)
- Recoding diagnosis for parallel system-level embedded application models
- A SystemC System-level Description Language Frond-end Tool
- System-level modeling and synthesis for parallel embedded standard applications
- Fast simulation for cyclo-static data flow models
- ConcurrenC: a novel Model of Computation (MoC) for effective system-level abstraction of C-based System-Level Description Languages (SLDLs)

Shanghai Jiao Tong University
Graduate Research Assistant, School of Microelectronics December 2004 – January 2007

- Developed a symbolic analog circuit simulation using graph reduction approaches
- Researched on simulation for heterogeneous multiprocessor systems based on the SimpleScalar toolset
- Optimized MP3 decoder algorithm and developed an in-house operating system on the ARM9 platform
- Designed the digital circuit for a reconfigurable cache controller and external memory interface module in VerilogHDL

PUBLICATIONS

Journal Articles (peer reviewed)

J1. **Weiwei Chen**, Xu Han, Rainer Dömer, "Multi-Core Simulation of Transaction Level Models using the System-on-Chip Environment", *IEEE Design & Test of Computers*, vol.28, no.3, pp.20-31, May-June 2011

J2. **Weiwei Chen**, Xu Han, Che-Wei Chang, Rainer Dömer, "Advances in Parallel Discrete Event Simulation for Electronic System-Level Design", *IEEE Design & Test of Computers*, vol.30, no.1, pp.45-54, January-February 2013

J3. **Weiwei Chen**, Xu Han, Che-Wei Chang, Guantao Liu, Rainer Dömer, "Out-of-Order Parallel Discrete Event Simulation for Transaction Level Models", *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD)*, vol.33, no.12, pp.1859-1872, December 2014

Books

B1. **Weiwei Chen**, "Out-of-order Parallel Discrete Event Simulation for Electronic System-level Design", *Springer*, 2014, ISBN 978-3-319-08752-8

Book Chapters

BC1. **Weiwei Chen**, Guoyong Shi, "Symbolic Analysis of Analog Integrated Circuits", *Embedded Systems and Materials Research for Advanced Applications, the 1st Chinese-German Summer School in Shanghai*, September, 2006, ISBN-10: 3-00-019576-9 / ISBN-13: 978-3-00-019576-1

BC2. **Weiwei Chen**, Rainer Dömer, "ConcurrenC: A New Approach towards Effective Abstraction of C-based SLDLs", *Analysis, Architectures and Modeling of Embedded Systems (ed. A. Rettberg, M. Zanella, M. Amann, M. Keckeisen, F. Rammig)*, Springer, 2009, ISBN 978-3-642-04283-6

Conference Papers (peer reviewed)

C1. **Weiwei Chen**, Guoyong Shi, "Implementation of a Symbolic Circuit Simulator for Topological Network Analysis", in Proceedings of *the IEEE Asia Pacific Conference on Circuit and System (APCCAS)*, pp.1368-1372, Singapore, December 2006

C2. Guoyong Shi, **Weiwei Chen**, C.-J. Richard Shi, "A Graph Reduction Approach to Symbolic Circuit Analysis", in Proceedings of *the 12th Asia and South Pacific Design Automation Conference (ASP-DAC)*, pp.197-202, Yokohama, Japan, January 2007

C3. Rongrong Zhong, Yongxin Zhu, **Weiwei Chen**, Mingliang Lin, Weng Fai Wong, "An Inter-core Communication Enabled Multi-core Simulator Based on SimpleScalar", in Proceedings of *the 21st International Conference on Advanced Information Networking and Applications Workshops (AINAW)*, pp.758-763, Niagara Falls, Canada, April 2007

C4. **Weiwei Chen**, Rainer Dömer, "ConcurrenC: A New Approach towards Effective Abstraction of C-based SLDLs", in Proceedings of *the International Embedded Systems Symposium (IESS)*, Langenargen, Germany, September 2009

C5. **Weiwei Chen**, Rainer Dömer, "A Fast Heuristic Scheduling Algorithm for Periodic ConcurrenC Models", in Proceedings of *the 15th Asia and South Pacific Design Automation Conference (ASP-DAC)*, pp.161-166, Taipei, Taiwan, January 2010

C6. **Weiwei Chen**, Xu Han, Rainer Dömer, "ESL Design and Multi-Core Validation using the System-on-Chip Environment", in Proceedings of *the 15th IEEE International High Level Design Validation and Test Workshop (HLDVT)*, pp.142-147, Anaheim, USA, June 2010

C7. Rainer Dömer, **Weiwei Chen**, Xu Han, Andreas Gerstlauer, "Multi-Core Parallel Simulation of System-Level Description Languages", invited paper, in Proceedings of *the 16th Asia and South Pacific Design Automation Conference (ASP-DAC)*, pp.311-316, Yokohama, Japan, January 2011

C8. **Weiwei Chen**, Rainer Dömer, "An Optimizing Compiler for Out-of-Order Parallel ESL Simulation Exploiting Instance Isolation", in Proceedings of *the 17th Asia and South Pacific Design Automation Conference (ASP-DAC)*, pp.461-466, Sydney, Australia, January 2012

C9. Rainer Dömer, **Weiwei Chen**, Xu Han, "Parallel Discrete Event Simulation of Transaction Level Models", invited paper, in Proceedings of *the 17th Asia and South Pacific Design Automation Conference (ASP-DAC)*, pp.227-231, Sydney, Australia, January 2012

C10. **Weiwei Chen**, Xu Han, Rainer Dömer, "Out-of-order Parallel Simulation for ESL design", in Proceedings of *the Design, Automation and Test in Europe Conference (DATE)*, pp.141-146, Dresden, Germany, March 2012

C11. **Weiwei Chen**, Che-Wei Chang, Xu Han, Rainer Dömer, "Eliminating Race Conditions in System-Level Models by using Parallel Simulation Infrastructure", invited paper, in Proceedings of *the IEEE International High Level Design Validation and Test Workshop (HLDVT)*, pp.118-123, Huntington Beach, USA, November 2012

C12. **Weiwei Chen**, Rainer Dömer, "Optimized Out-of-Order Parallel Discrete Event Simulation Using Predictions", in Proceedings of *the Design, Automation and Test in Europe Conference (DATE)*, pp.3-8, Grenoble, France, March 2013

C13. Xu Han, **Weiwei Chen**, Rainer Dömer, "Designer-in-the-Loop Recoding of ESL Models using Static Parallel Access Conflict Analysis", in Proceedings of *the Workshop on Software and Compilers for Embedded Systems (SCOPES)*, Schloss Rheinfels, Germany, June 2013

C14. **Weiwei Chen**, Xu Han, Rainer Dömer, "May-Happen-in-Parallel Analysis based on Segment Graphs for Safe ESL Models", in Proceedings of *the Design, Automation and Test in Europe Conference (DATE)*, Dresden, Germany, March 2014 **(Best Paper Award)**

Technical Reports

TR1. **Weiwei Chen**, Rainer Dömer, "System Specification of a DES Cipher Chip", *TR-08-01*, Center for Embedded Computer System, University of California at Irvine, January 2008

TR2. **Weiwei Chen**, Siwen Sun, Bin Zhang, Rainer Dömer, "System Level Modeling of a H.264 Decoder", *TR-08-10*, Center for Embedded Computer System, University of California at Irvine, August 2008

TR3. **Weiwei Chen**, Rainer Dömer, "A Distributed Parallel Simulator for Transaction Level Models with Relaxed Timing", *TR-11-02*, Center for Embedded Computer Systems, University of California at Irvine, May 2011

TR4. Xu Han, **Weiwei Chen**, Rainer Dömer, "A Parallel Transaction-Level Model of H.264 Video Decoder", *TR-11-03*, Center for Embedded Computer Systems, University of California at Irvine, June 2011

Poster Presentations

P1. **Weiwei Chen**, Rainer Dömer, "Parallel Discrete Event Simulation for ESL Design", in the *SIGDA Ph.D. Forum at the Design Automation Conference (DAC)*, San Francisco, USA, June 2012

P2. **Weiwei Chen**, Rainer Dömer, "Out-of-order Parallel Discrete Event Simulation for ESL Design", *Graduate Student Poster Presentation*, Faculty Retreat, Department of Electrical Engineering and Computer Science, University of California at Irvine, September 2012

P3. **Weiwei Chen**, Rainer Dömer, "Out-of-order Parallel Simulation for Electronic System-Level Design", in the *EDAA/ACM SIGDA PhD Forum at the Design, Automation and Test in Europe Conference (DATE)*, Grenoble, France, March 2013

Number of citations

- **Google Scholar: 153** (http://scholar.google.com/citations?user=pC1k0McAAAAJ&hl=en)

PROFESSIONAL ACTIVITIES AND SERVICES

Conference Reviewer

Expert Reviewer

- Design Automation Conference (DAC) 2013

External Reviewer

- Design Automation Conference (DAC) 2009, 2010
- Design, Automation and Test in Europe Conference (DATE) 2010, 2011, 2013, 2014
- ACM/IEEE International Conference on Formal Methods and Models for Co-design (MEMOCODE) 2010
- International Conference on Hardware/Software Co-design and System Synthesis (CODES+ISSS) 2010, 2012, 2013

Journal Reviewer

- ACM Transaction on Embedded Computing (TECS)
- Springer's Journal of Network and Systems Management

Conference Program Committee

- Artifact Evaluation Committee Member
  International Symposium on Code Generation and Optimization / ACM SIGPLAN Symposium on Principles and Practice of Parallel Programming (CGO/PPoPP) 2015

Professional Association Membership

- ACM, IEEE, IEEE Computer Society

Conference Presentations

- IESS'09, ASP-DAC'10, ASP-DAC'12, DATE'12, DAC'12, HLDVT'12, DATE'13, DATE'14

Invited Talks

T1. Invited Lecture, "Discussion for C-based SLDLs: SpecC and SystemC", *SoC Description and Modeling (EECS 222A)*, UC Irvine, December 4, 2009

T2. Invited Talk, "Multi-Core Parallel Simulation of System-Level Description Languages", School of Microelectronics, Shanghai Jiao Tong University, December 26, 2011

T3. Invited Talk, "Out-of-order Parallel Discrete Event Simulation for Electronic System-Level Design", School of Microelectronics, Shanghai Jiao Tong University, China, December 12, 2012

T4. Invited Talk, "Out-of-order Parallel Simulation for Electronic System-Level Design", Department of Computer Science, The Carl von Ossietzky University of Oldenburg, Germany, March 14, 2013

WORKING EXPERIENCE

Qualcomm Research Silicon Valley

- **Senior Engineer** October 2013 – Present
  Parallel programming research for heterogeneous multi-core platforms

Microsoft, Redmond, WA

- **Software Develop Engineer Intern** June 2011 – September 2011
  Windows Core Security and Identity Public Key Infrastructure Team
  Developed a Windows store application for secure banking with cloud roaming features on the Windows 8 Platform in Javascript (Windows 8 banking app with strong authentication sample)

IBM China System & Technology Lab (CSTL), Shanghai, China

- **R&D Engineer Intern** June 2006– April 2007
  Developed parallel high-performance sorting algorithms on the CELL Broadband Engine platform
  Research and development for system software for storage devices (C++ and Java) based on the OpenPegasus project