Weiwei Chen

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EDUCATION

- **Doctor of Philosophy, Electrical and Computer Engineering** 2013
  Department of Electrical Engineering and Computer Science
  University of California, Irvine
  Dissertation: Out-of-Order Parallel Discrete Event Simulation for ESL Design
  Committee: Prof. Rainer Dömer, Prof. Daniel D. Gajski, Prof. Brian Demsky
  Outstanding Dissertation Award, European Design and Automation Association (EDAA)
- **Master of Science, Computer Engineering** 2007
  Thesis: A Symbolic Analog Circuit Simulator
  School of Microelectronics
  Shanghai Jiao Tong University, Shanghai, China
- **Bachelor of Engineering, Computer Science and Engineering** 2004
  Thesis: Design and Implementation of a Software Debugger for Digital Signal Processors
  Department of Computer Science and Engineering
  Teaching Reform Class (Advanced Admission)
  Shanghai Jiao Tong University, Shanghai, China
- **International Exchange Student** 2003
  Dean's List and Semester Honor
  School of Electrical and Computer Engineering
  Purdue University, West Lafayette, Indiana
- **High School Graduation** 2000

HONORS AND AWARDS

- Outstanding Dissertation Award, European Design and Automation Association (EDAA) 2014
- Best Paper Award, Design, Automation and Test Conference in Europe (DATE) 2014
- Qualstar Diamond Award, Qualcomm Inc. 2014
- Pedagogical Fellowship, UC Irvine 2012-13
- Young Student Support Award, Design Automation Conference (DAC) 2010
- *Henry Samueli* Endowed Fellowship, UC Irvine 2007
- Excellent Teaching Assistant Award, School of Microelectronics, SJTU 2006
- National Scholarship for Academic Excellence, China 2006
- *Infineon, Guanghua, Morgan Stanley* Endowed Scholarship, SJTU 2004-2007
- Exceptional Undergraduate Student, SJTU 2001, 2003
- People's Scholarship for Academic Excellence, SJTU 2001-2004
- Fellowship of Pan Wen-Yuan Foundation 2001

RESEARCH INTERESTS

Parallel computing
Multi-core parallel simulation,
System-level modeling, validation, and analysis
Embedded hardware and software systems
Computer Science education and pedagogy

RESEARCH EXPERIENCE

Qualcomm Research Silicon Valley
Senior Engineer October 2013 – Present

- *Parallel programming model for heterogeneous multi-core platforms*
  Design the parallel pipeline programming model for image processing applications
  Build demo parallel applications on Android platform to showcase the Qualcomm's Multicore Asynchronous Runtime Environment (MARE)
  Task-based parallel modeling for enterprise storage and computational photography applications (achieved 15%-150% speedup compared to well optimized thread-based implementations)

University of California, Irvine
Graduate Student Researcher, Department of EECS September 2007 – 2013

- *Multi-core parallel simulation for Transaction-Level Models (TLMs)* June 2009 - Present
  Design a synchronous parallel simulator for C-based System-level Description Languages
  Propose an out-of-order parallel simulation approach for System-level Description Languages
  Propose an optimized compiler for static code analysis on system-level models

- *Recoding diagnosis for parallel system-level embedded application models* January 2012 - Present
  Design and develop a dynamic race condition diagnosis tool for embedded system-level models
  Design and develop static conflict detection for an Eclipse-based recoding tool

- *A SystemC System-level Description Language Frond-end Tool* February 2013 - Present
  Design the software architecture of a SystemC front-end tool by using the *LLVM+Clang* compiler infrastructure, aiming at model analysis and code transformation for simulation on multi-core/many-core platforms.
  Design and build the compiler metadata for SystemC models, including the structural hierarchy, port binding information, simulation primitives, and so on

- *System-level modeling and synthesis for parallel embedded standard applications* June 2008 - Present
  Designed and developed parallel transaction-level models for a H.264 video decoder, a JPEG image encoder, a video edge detector, and a DES cipher chip

- *Fast simulation for cyclo-static data flow models* June 2009 - January 2010
  Proposed a fast static scheduling strategy for fast simulating cyclo-static data flow models written in SystemC and SpecC SLDLs by using heuristic static scheduling approaches

- *ConcurrenC: a novel Model of Computation (MoC) for effective system-level abstraction of C-based System-Level Description Languages (SLDLs)* June 2008 - June 2009
  Proposed the ConcurrenC MoC with features of communication and computation separation, hierarchy, concurrency, abstract communication, timing, execution semantics, and precisely expressive in both SystemC and SpecC SLDLs

Shanghai Jiao Tong University
Graduate Research Assistant, School of Microelectronics December 2004 – January 2007

- Developed a symbolic analog circuit simulation using graph reduction approaches
- Researched on simulation for heterogeneous multiprocessor systems based on the SimpleScalar toolset
- Optimized MP3 decoder algorithm and developed an in-house operating system on the ARM9 platform
- Designed the digital circuit for a reconfigurable cache controller and external memory interface module in VerilogHDL

PUBLICATIONS

Journal Articles (peer reviewed)

J1. **Weiwei Chen**, Xu Han, Rainer Dömer, "Multi-Core Simulation of Transaction Level Models using the System-on-Chip Environment", *IEEE Design & Test of Computers*, vol.28, no.3, pp.20-31, May-June 2011

J2. **Weiwei Chen**, Xu Han, Che-Wei Chang, Rainer Dömer, "Advances in Parallel Discrete Event Simulation for Electronic System-Level Design", *IEEE Design & Test of Computers*, vol.30, no.1, pp.45-54, January-February 2013

J3. **Weiwei Chen**, Xu Han, Che-Wei Chang, Guantao Liu, Rainer Dömer, "Out-of-Order Parallel Discrete Event Simulation for Transaction Level Models", under revision, *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD)*, April 2014

Books

BC1. **Weiwei Chen**, *Out-of-order Parallel Discrete Event Simulation for Electronic System-level Design,* invited by Springer (in production)

Book Chapters

BC1. **Weiwei Chen**, Guoyong Shi, "Symbolic Analysis of Analog Integrated Circuits", *Embedded Systems and Materials Research for Advanced Applications, the 1st Chinese-German Summer School in Shanghai*, September, 2006, ISBN-10: 3-00-019576-9 / ISBN-13: 978-3-00-019576-1

BC2. **Weiwei Chen**, Rainer Dömer, "ConcurrenC: A New Approach towards Effective Abstraction of C-based SLDLs", *Analysis, Architectures and Modeling of Embedded Systems (ed. A. Rettberg, M. Zanella, M. Amann, M. Keckeisen, F. Rammig)*, Springer, 2009, ISBN 978-3-642-04283-6

Conference Papers (peer reviewed)

C1. **Weiwei Chen**, Guoyong Shi, "Implementation of a Symbolic Circuit Simulator for Topological Network Analysis", in Proceedings of *the IEEE Asia Pacific Conference on Circuit and System (APCCAS)*, pp.1368-1372, Singapore, December 2006

C2. Guoyong Shi, **Weiwei Chen**, C.-J. Richard Shi, "A Graph Reduction Approach to Symbolic Circuit Analysis", in Proceedings of *the 12th Asia and South Pacific Design Automation Conference (ASP-DAC)*, pp.197-202, Yokohama, Japan, January 2007

C3. Rongrong Zhong, Yongxin Zhu, **Weiwei Chen**, Mingliang Lin, Weng Fai Wong, "An Inter-core Communication Enabled Multi-core Simulator Based on SimpleScalar", in Proceedings of *the 21st International Conference on Advanced Information Networking and Applications Workshops (AINAW)*, pp.758-763, Niagara Falls, Canada, April 2007

C4. **Weiwei Chen**, Rainer Dömer, "A Fast Heuristic Scheduling Algorithm for Periodic ConcurrenC Models", in Proceedings of *the 15th Asia and South Pacific Design Automation Conference (ASP-DAC)*, pp.161-166, Taipei, Taiwan, January 2010

C5. **Weiwei Chen**, Xu Han, Rainer Dömer, "ESL Design and Multi-Core Validation using the System-on-Chip Environment", in Proceedings of *the 15th IEEE International High Level Design Validation and Test Workshop (HLDVT)*, pp.142-147, Anaheim, USA, June 2010

C6. Rainer Dömer, **Weiwei Chen**, Xu Han, Andreas Gerstlauer, "Multi-Core Parallel Simulation of System-Level Description Languages", invited paper, in Proceedings of *the 16th Asia and South Pacific Design Automation Conference (ASP-DAC)*, pp.311-316, Yokohama, Japan, January 2011

C7. **Weiwei Chen**, Rainer Dömer, "An Optimizing Compiler for Out-of-Order Parallel ESL Simulation Exploiting Instance Isolation", in Proceedings of *the 17th Asia and South Pacific Design Automation Conference (ASP-DAC)*, pp.461-466, Sydney, Australia, January 2012

C8. Rainer Dömer, **Weiwei Chen**, Xu Han, "Parallel Discrete Event Simulation of Transaction Level Models", invited paper, in Proceedings of *the 17th Asia and South Pacific Design Automation Conference (ASP-DAC)*, pp.227-231, Sydney, Australia, January 2012

C9. **Weiwei Chen**, Xu Han, Rainer Dömer, "Out-of-order Parallel Simulation for ESL design", in Proceedings of *the Design, Automation and Test in Europe Conference (DATE)*, pp.141-146, Dresden, Germany, March 2012

C10. **Weiwei Chen**, Che-Wei Chang, Xu Han, Rainer Dömer, "Eliminating Race Conditions in System-Level Models by using Parallel Simulation Infrastructure", invited paper, in Proceedings of *the IEEE International High Level Design Validation and Test Workshop (HLDVT)*, pp.118-123, Huntington Beach, USA, November 2012

C11. **Weiwei Chen**, Rainer Dömer, "Optimized Out-of-Order Parallel Discrete Event Simulation Using Predictions", in Proceedings of *the Design, Automation and Test in Europe Conference (DATE)*, pp.3-8, Grenoble, France, March 2013

C12. Xu Han, **Weiwei Chen**, Rainer Dömer, "Designer-in-the-Loop Recoding of ESL Models using Static Parallel Access Conflict Analysis", in Proceedings of *the Workshop on Software and Compilers for Embedded Systems (SCOPES)*, Schloss Rheinfels, Germany, June 2013

C13. **Weiwei Chen**, Xu Han, Rainer Dömer, "May-Happen-in-Parallel Analysis based on Segment Graphs for Safe ESL Models", in Proceedings of *the Design, Automation and Test in Europe Conference (DATE)*, Dresden, Germany, March 2014 **(Best Paper Award)**

Technical Reports

TR1. **Weiwei Chen**, Rainer Dömer, "System Specification of a DES Cipher Chip", *TR-08-01*, Center for Embedded Computer System, University of California at Irvine, January 2008

TR2. **Weiwei Chen**, Siwen Sun, Bin Zhang, Rainer Dömer, "System Level Modeling of a H.264 Decoder", *TR-08-10*, Center for Embedded Computer System, University of California at Irvine, August 2008

TR3. **Weiwei Chen**, Rainer Dömer, "ConcurrenC: A Novel Model of Computation for Effective Abstraction of C-based SLDLs", *TR-09-07*, Center for Embedded Computer System, University of California at Irvine, May 2009

TR4. **Weiwei Chen**, Rainer Dömer, "A Distributed Parallel Simulator for Transaction Level Models with Relaxed Timing", *TR-11-02*, Center for Embedded Computer Systems, University of California at Irvine, May 2011

TR5. Xu Han, **Weiwei Chen**, Rainer Dömer, "A Parallel Transaction-Level Model of H.264 Video Decoder", *TR-11-03*, Center for Embedded Computer Systems, University of California at Irvine, June 2011

Poster Presentations

P1. **Weiwei Chen**, Rainer Dömer, "Parallel Discrete Event Simulation for ESL Design", in the *SIGDA Ph.D. Forum at the Design Automation Conference (DAC)*, San Francisco, USA, June 2012

P2. **Weiwei Chen**, Rainer Dömer, "Out-of-order Parallel Discrete Event Simulation for ESL Design", *Graduate Student Poster Presentation*, Faculty Retreat, Department of Electrical Engineering and Computer Science, University of California at Irvine, September 2012

P3. **Weiwei Chen**, Rainer Dömer, "Out-of-order Parallel Simulation for Electronic System-Level Design", in the *EDAA/ACM SIGDA PhD Forum at the Design, Automation and Test in Europe Conference (DATE)*, Grenoble, France, March 2013

Number of citations

- **Google Scholar: 141** (http://scholar.google.com/citations?user=pC1k0McAAAAJ&hl=en)

PROFESSIONAL ACTIVITIES AND SERVICES

Invited Talks

T1. Invited Lecture, "Discussion for C-based SLDLs: SpecC and SystemC", *SoC Description and Modeling (EECS 222A)*, UC Irvine, December 4, 2009

T2. Invited Talk, "Internship in Microsoft", *Group Seminar*, Center for Embedded Computer Systems, UC Irvine, October 14, 2011

T3. Invited Talk, "Multi-Core Parallel Simulation of System-Level Description Languages", School of Microelectronics, Shanghai Jiao Tong University, December 26, 2011

T4. Contributed to Invited Talk, Rainer Dömer, Weiwei Chen, Xu Han, "Advances in Parallel Discrete Event Simulation For Embedded System Design", *EECS Colloquium*, UC Irvine, May 9, 2012

T5. Contributed to Invited Talk, Rainer Dömer, Weiwei Chen, Xu Han, "Advances in Parallel Simulation of System Models", *EECS Colloquium*, UC Irvine, October 17, 2012

T6. Invited Talk, "Out-of-order Parallel Discrete Event Simulation for Electronic System-Level Design", School of Microelectronics, Shanghai Jiao Tong University, China, December 12, 2012

T7. Invited Talk, "Out-of-order Parallel Simulation for Electronic System-Level Design", Department of Computer Science, The Carl von Ossietzky University of Oldenburg, Germany, March 14, 2013

Conference Reviewer

- Design Automation Conference (DAC) 2009, 2010, expert reviewer 2013
- Design, Automation and Test in Europe Conference (DATE) 2010, 2011, 2013, 2014
- ACM/IEEE International Conference on Formal Methods and Models for Co-design (MEMOCODE) 2010
- International Conference on Hardware/Software Co-design and System Synthesis (CODES+ISSS) 2010, 2012, 2013

Journal Reviewer

- ACM Transaction on Embedded Computing (TECS)

Professional Association Membership

- ACM, IEEE, IEEE Computer Society

Conference Presentations

- IESS'09, ASP-DAC'10, ASP-DAC'12, DATE'12, DAC'12, HLDVT'12, DATE'13, DATE'14

TEACHING EXPERIENCE

University of California, Irvine

- **Pedagogical Fellow** Academic year 2012-13
  Teaching, Learning and Technology Center (TLTC) and
  The Henry Samueli School of Engineering
  - *Teaching Assistant Professional Development Program (TAPDP 2012, 2013)*
    Designed and led a day-and-a-half discipline-specific, interactive workshop series to prepare graduate students with their instructional careers in University of California at Irvine. The program included eleven workshops concerning TA responsibilities, learning styles, active learning strategies, problem solving skills, grading, leading discussion sessions, office hours, handling difficult situations, and microteaching
  - *Teaching Consultation*
    Conduct teaching consultations with TAs through reflecting on teaching experience, and identifying effective teaching methods and strategies

- **Teaching Assistant**
  - *Advanced C Programming (EECS22)* Fall 2011, 2012
  - *Computational Methods in Electrical and Computer Engineering (EECS10)*
    Fall 2008, 2009, 2010, Summer 2012
    Led discussion and laboratory sections, designed learning activities, prepared and graded programming homework assignments, held office hours, managed online course message board, prepared the course accreditation (ABET) materials

- **Substitute Lecturer**
  - *Advanced System Software (EECS211)* Winter 2011
    Gave two lectures for memory management in computer systems for graduate students

Shanghai Jiao Tong University

- **Instructor** June 2006
  - *FPGA Training Workshop*
    Gave lectures on embedded system design by using the Embedded Development Kit of Xilinx FPGA, and designed the laboratory exercises

- **Teaching Assistant** Spring 2005 – Fall 2006
  - *Digital Integrated Circuit Design*
  - *Design Automation for Integrated Circuit*
    Prepared exam, homework, and laboratory assignments
  - *Embedded System Design*
    Mentored undergraduate students for embedded system design projects

Future Road College, Shanghai, China

- **Visiting Instructor** July 2006 – July 2007
  Taught high school students Calculus, Linear Algebra and Theory of Probability for preparation for SAT-AP test

WORKING EXPERIENCE

Qualcomm Research Silicon Valley

- **Senior Engineer** October 2013 – Present
  Parallel programming research for heterogeneous multi-core platforms

Microsoft, Redmond, WA

- **Software Develop Engineer Intern** June 2011 – September 2011
  Windows Core Security and Identity Public Key Infrastructure Team
  Developed a Windows store application for secure banking with cloud roaming features on the Windows 8 Platform in Javascript (Windows 8 banking app with strong authentication sample)

IBM China System & Technology Lab (CSTL), Shanghai, China

- **R&D Engineer Intern** June 2006– April 2007
  Developed parallel high-performance sorting algorithms on the CELL Broadband Engine platform
  Research and development for system software for storage devices (C++ and Java) based on the OpenPegasus project

SOFTWARE RELEASES

- *SpecC compiler version 2.2.2, Developer Release*
  Provided the parallel simulation kernel, the out-of-order parallel simulation kernel, the static code analyzer in the compiler, the race condition diagnosis tool, and extended the simulator support for the SoC Environment (SCE) toolset
- *Recoding tool support, System-on-Chip Description and Modeling course (EECS222A), UC Irvine*
  Provide the compiler and simulator infrastructure for the Eclipse IDE tool for the recoding projects of this course
- *Embedded application models in the example repository for the SoC Environment (SCE) toolset*
  Designed an H.264 video decoder model (40k+ lines of code), a JPEG image encoder (2.5k+ lines of code), a video edge detector, and a DES cipher chip model

ONLINE INFORMATION

- Office page: http://www.cecs.uci.edu/∼weiweic
- Pedagogical Fellowship Program, Teaching Learning and Technology Center (TLTC) UC Irvine: http://www.tltc.uci.edu/pfProgram.html, http://www.tltc.uci.edu/teachingAwards2013.html
- TA Professional Development Program (TAPDP) teaching portfolio: http://www.cecs.uci.edu/∼weiweic/teaching.html

RESEARCH ACCOMPLISHMENTS IN MY FIELD

Computers are ubiquitous in our modern society. The rapid growth of application complexities imposes an imperative need on high computational capacities. However, the fundamental physical bottleneck prevents single hardware units from increasing processing frequency indefinitely for high performance. The shift towards multi-core and many-core systems is inevitable to improve the computing capabilities in the future.

In order to exploit the multiple computational resources on the hardware platform, software need to be written in the way that many calculations are carried out concurrently. Parallel programming breaks the program into independent pieces so that they can be executed simultaneously on each processing elements. Parallel programing also makes it possible to save energy consumptions by finishing the work on time without increasing the processor frequency.

Parallel programming is not an easy task since most of the programming languages and existing programs are designed and written in a sequential way. Compiler technologies have been proposed to automatically parallelizing the sequential part of a program to run on multi-core computers. However, existing approaches can only handle some special cases in a program, such as loops. It is still not feasible to parallelize a whole piece of program without any manual work. On the other hand, new programming languages, such as OpenMP, Cilk, CUDA, are proposed so as to write a parallel program from scratch. Parallel programming models, such as shared memory, message passing, and task parallelism, are also developed to provide better abstractions to the programmer so that they can focus more on design their algorithms without worrying to much on the underlying parallelizing details on the hardware platform.

Parallel computing is pervasive in almost all the computational applications, including scientific computations, networking systems, computer vision, machine learning, as well as mobile consumer applications. It is a collaboration work among advanced hardware design, operating system support, compiler technology and parallel algorithms for domain specific applications. Parallel computing is one of the most fundamental and needed technologies for tomorrows computational world.

VALUES OF BENEFITS OF MY PROJECTS

My research work falls into the realm of parallel computing for embedded and mobile computer systems. My Ph.D. dissertation research has been focusing on parallel simulation approaches for system-level

description languages (SLDLs) in which most embedded system models are described. Embedded computing systems have a profound impact on our everyday life with a wide application domain. More than 90% of the computer systems in the world are now embedded. Embedded systems are usually designed for a specific purpose with very strict design requirements. To design an embedded system, engineers start from capturing the critical features of the design in an abstract model, and then refine it step by step to final the implementation. Typically, these models are written in SLDLs and validated through simulation. My Ph.D. work extents the existing sequential discrete event simulation kernel for

SLDLs to support parallel simulation on multicore simulation hosts. In addition to the parallel extension, I also proposed the out-of-order parallel simulation approach to parallelize the simulation more aggressively without loss of accuracy. My work makes it possible for SLDL simulators to exploit the multicore computational capability that are commonly available nowadays in a most efficient way. It has been published in more than 10 peer-reviewed papers and acknowledged by the design automation community with an outstanding dissertation award and one best paper award. A research project has also been funded by Intel to port this technology to industrial usage. Now I am working with the Qualcomm Research

Silicon Valley on the project of Multicore Asynchronous Runtime Environment (MARE). Our work aims at providing a general parallel programming model for programmers to easily design their algorithms and fully exploit the potential computational resources on multicore platforms. We are building the task-based parallel infrastructure and designing parallel programming patterns to capture the high-level essential abstractions of common algorithms, including linear algebra computation, image processing and other parallel patterns. With our runtime library, engineers can focus on designing their parallel algorithms without being distracted by the complexity of the traditional multithreading programming paradigm and be able to optimize their code on hardware platforms with heterogenous computing units including CPUs, graphics processing unit (GPU), digital signal processor (DSP) and other hardware accelerators. Parallel

programming is the cornerstone for the future computation world. It brings the great potential of high execution performance and low energy consumption. The contributions of my research work can help the

engineers to build and validate their designs in an efficient way which lead to lower production prices and shorter time-to-market. The engineers can therefore be freed from dealing with complex low-level implementation details but focus on designing their algorithms to bring more applications with sophisticated functionalities. In other words, my work is promising benefit the national interests with advancing computational technologies, reduced energy usage, and improving economy with more efficient consumer and industrial electronics.

POTENTIAL REFERENCES

Dr. Rainer Dömer (Ph.D. Advisor)
Associate Professor
Electrical Engineering and Computer Science
University of California, Irvine

Dr. Daniel Gajski
Professor, Founding Director
Center for Embedded Computer Systems
University of California, Irvine

Dr. Fadi Kurdahi
Professor, Director
Center for Embedded Computer Systems
University of California, Irvine

Dr. Calin Cascaval
Senior Director, Engineering
Qualcomm Research Silicon Valley

Prof. Dr. Wolfgang Rosenstiel
Dean, Faculty of Science
University of Tübingen, Germany

Prof. Dr.-Ing. Wolfgang Nebel
Professor
Computer Science (Informatik) Department
The Carl von Ossietzky University of Oldenburg, Germany

Prof. Sridevan Parameswaran
Professor, Program Director for Computer Engineering
School of Computer Science and Engineering
University of New South Wales, Australia

Dr. Ajit Dingankar
Principal Engineer at Intel

Dr. Desmond Kirkpatrick
Principal Engineer at Intel

Prof. Petru Eles
Professor of Embedded Computer Systems, Deputy Chairman
Department of Computer and Information Science (IDA)
Linköping University, Sweden

Prof. Soonhoi Ha
Professor
Computer Engineering Department
Seoul National University, South Korea

Prof. Jörg Henkel
Professor, Chair for Embedded Systems
Karlsruhe Institute of Technology, Germany

Prof. Lothar Thiele
Professor
Computer Engineering and Networks Laboratory
Swiss Federal Institute of Technology Zurich, Switzerland

Prof. Dr.-Ing. Dr. h.c. Gerhard Fettweis
Vodafone Chair Mobile Communications Systems
Dresden University of Technology

Prof. Giovanni De Micheli
Professor and Director
The Institute of Electrical Engineering and The Integrated Systems Centre
Swiss Federal Institute of Technology in Lausanne (EPFL), Switzerland

Prof. Dr.-Ing. Jürgen Teich
Professor, Chair for Hardware-Software-Co-Design
Department of Computer Science
University of Erlangen-Nuremberg, Germany

Prof. Dr. Peter Marwedel
Professor
Head of Design Automation for Embedded Systems Group
Technical University of Dortmund

Prof. Dr. Oliver Bringmann
Professor, Chair
Embedded Systems at the Department of Computer Science
The University of Tübingen, Germany
Director
FZI Research Center for Information Technologies in Karlsruhe, Germany