Weiwei Chen

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EDUCATION

Ph.D. Electrical and Computer Engineering 2013
Department of Electrical Engineering and Computer Science
University of California, Irvine
Dissertation: Out-of-Order Parallel Discrete Event Simulation for ESL Design
Committee: Prof. Rainer Dömer, Prof. Daniel D. Gajski, Prof. Brian Demsky
Outstanding Dissertation Award, European Design and Automation Association

M.S. Computer Engineering 2007
Thesis: A Symbolic Analog Circuit Simulator
Shanghai Jiao Tong University, Shanghai, China

B.Eng. Computer Science and Engineering 2004
Thesis: Design and Implementation of a Software Debugger for Digital Signal Processors
Teaching Reform Class (Honor Class with Advanced Admission, National Entrance Exam Waiver)
Shanghai Jiao Tong University, Shanghai, China

International Exchange Student 2003
Dean's List and Semester Honor
School of Electrical and Computer Engineering
Purdue University, West Lafayette, Indiana

HONORS AND AWARDS

- 7 Qualstar Awards, Qualcomm Inc. 2014 - 2016
- Outstanding Dissertation Award, European Design and Automation Association (EDAA) 2014
- Best Paper Award, Design, Automation and Test Conference in Europe (DATE) 2014
- Pedagogical Fellowship, UC Irvine 2012-13
- *Henry Samueli* Endowed Fellowship, UC Irvine 2007
- National Scholarship for Academic Excellence, China 2006
- *Infineon, Guanghua, Morgan Stanley* Endowed merit-based Scholarship, SJTU 2004-2007
- Exceptional Undergraduate Student Awards, SJTU
- People's Scholarship for Academic Excellence, SJTU 2000-2004
- Fellowship of Pan Wen-Yuan Foundation 2001
- Soh Bing (Shu Ping) Scholarship, 9th grade to senior year in college

RESEARCH INTERESTS

- Compiler for ML, HPC, BigData, etc
- Big Data System Architecture and Acceleration
- Heterogeneous Parallel Programming and Compilers
- System-level Modeling, Validation, and Analysis

RESEARCH AND WORKING EXPERIENCE

Modular
Staff Engineer May 2023 – Present

Compiler for the Mojo programming language.

SambaNova Systems
Senior Principal Engineer May 2021 – May 2023
Principal Engineer October 2018 – April 2021

Founding member of the compiler team that builds the compiler stack for the new HW architecture with reconfigurable dataflow units (RDUs): MLIR-based graph compiler, kernel compiler, DSLs for RDU, PyTorch framework integration, other SW infrastructure related work.

BigStream
Founding Software Engineer February 2016 – October 2018

Lead software research and development efforts on compilers, native C++ big data acceleration runtime libraries, tool-chains for hardware acceleration (FPGA) technology, and big data system architecture.

- Native runtime and compiler support for accelerating big data user-defined functions (UDF).
- A dataflow compiler with Spark SQL frontend, query intermediate representations, three backend for native, FPGA, and RISCV code generation, and a planner for optimized SW/HW accelerator partitioning.
- A C++ native acceleration library with templatized SQL operations, cluster data source support (HDFS, amazon S3, Microsoft WASB), various input format support (json, avro, parquet, csv, ...), and tensorflow native integration for data pipelines.
- Spark dataframe and RDD APIs for native and hardware acceleration.
- A Clang-LLVM based high-level synthesis compiler for timing scheduling and code generation of FPGA accelerators.
- On premise Hadoop Cluster setup, and network performance measurement.

Qualcomm Research Silicon Valley
Senior Engineer October 2013 – Feburary 2016

Parallel programming patterns and runtime for heterogeneous multi-core platforms, **Qualcomm Symphony System Manager SDK** http://developer.qualcomm.com/symphony

- Heterogeneous Parallel Pipeline Pattern API and internal scheduling
- Task and dataflow API infrastructures
- Parallelize Android native computational photography and enterprise compression applications using task-based parallel programming patterns
- Power and performance evaluation for native parallel applications

Compiler front-end analysis and back-end code generation for coarse-grain auto-parallelization base on Polyhedral Optimizations in LLVM (llvm-polly).

University of California, Irvine
Graduate Student Researcher, Department of EECS September 2007 – 2013

- Multi-core parallel simulation for Transaction-Level Models (TLMs)
- Recoding diagnosis for parallel system-level embedded application models
- A SystemC frond-end using Clang tooling
- System-level modeling and synthesis for parallel embedded standard applications
- ConcurrenC: a novel Model of Computation (MoC) for effective system-level abstraction of C-based System-Level Description Languages (SLDLs)

Microsoft, Redmond, WA

- **Software Develop Engineer Intern** June 2011 – September 2011
  Windows Core Security and Identity Public Key Infrastructure Team
  Developed a Windows store application for secure banking with cloud roaming features on the Windows 8 Platform in Javascript (Windows 8 banking app with strong authentication sample)

Shanghai Jiao Tong University
Graduate Research Assistant, School of Microelectronics December 2004 – January 2007

- A symbolic analog circuit simulation using graph reduction approaches
- Simulation for heterogeneous multiprocessor systems based on the SimpleScalar toolset
- MP3 decoder algorithm optimization for DSP and an in-house operating system on ARM9 platform
- Digital circuit design for a reconfigurable cache controller and external memory interface module in VerilogHDL

PUBLICATIONS

Journal Articles (peer reviewed)

J1. **Weiwei Chen**, Xu Han, Rainer Dömer, "Multi-Core Simulation of Transaction Level Models using the System-on-Chip Environment", *IEEE Design & Test of Computers*, vol.28, no.3, pp.20-31, May-June 2011

J2. **Weiwei Chen**, Xu Han, Che-Wei Chang, Rainer Dömer, "Advances in Parallel Discrete Event Simulation for Electronic System-Level Design", *IEEE Design & Test of Computers*, vol.30, no.1, pp.45-54, January-February 2013

J3. **Weiwei Chen**, Xu Han, Che-Wei Chang, Guantao Liu, Rainer Dömer, "Out-of-Order Parallel Discrete Event Simulation for Transaction Level Models", *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD)*, vol.33, no.12, pp.1859-1872, December 2014

Books

B1. **Weiwei Chen**, "Out-of-order Parallel Discrete Event Simulation for Electronic System-level Design", *Springer*, 2014, ISBN 978-3-319-08752-8

Book Chapters

BC1. **Weiwei Chen**, Guoyong Shi, "Symbolic Analysis of Analog Integrated Circuits", *Embedded Systems and Materials Research for Advanced Applications, the 1st Chinese-German Summer School in Shanghai*, September, 2006, ISBN-10: 3-00-019576-9 / ISBN-13: 978-3-00-019576-1

BC2. **Weiwei Chen**, Rainer Dömer, "ConcurrenC: A New Approach towards Effective Abstraction of C-based SLDLs", *Analysis, Architectures and Modeling of Embedded Systems (ed. A. Rettberg, M. Zanella, M. Amann, M. Keckeisen, F. Rammig)*, Springer, 2009, ISBN 978-3-642-04283-6

Conference Papers (peer reviewed)

C1. **Weiwei Chen**, Guoyong Shi, "Implementation of a Symbolic Circuit Simulator for Topological Network Analysis", in Proceedings of *the IEEE Asia Pacific Conference on Circuit and System (APCCAS)*, pp.1368-1372, Singapore, December 2006

C2. Guoyong Shi, **Weiwei Chen**, C.-J. Richard Shi, "A Graph Reduction Approach to Symbolic Circuit Analysis", in Proceedings of *the 12th Asia and South Pacific Design Automation Conference (ASP-DAC)*, pp.197-202, Yokohama, Japan, January 2007

C3. Rongrong Zhong, Yongxin Zhu, **Weiwei Chen**, Mingliang Lin, Weng Fai Wong, "An Inter-core Communication Enabled Multi-core Simulator Based on SimpleScalar", in Proceedings of *the 21st International Conference on Advanced Information Networking and Applications Workshops (AINAW)*, pp.758-763, Niagara Falls, Canada, April 2007

C4. **Weiwei Chen**, Rainer Dömer, "ConcurrenC: A New Approach towards Effective Abstraction of C-based SLDLs", in Proceedings of *the International Embedded Systems Symposium (IESS)*, Langenargen, Germany, September 2009

C5. **Weiwei Chen**, Rainer Dömer, "A Fast Heuristic Scheduling Algorithm for Periodic ConcurrenC Models", in Proceedings of *the 15th Asia and South Pacific Design Automation Conference (ASP-DAC)*, pp.161-166, Taipei, Taiwan, January 2010

C6. **Weiwei Chen**, Xu Han, Rainer Dömer, "ESL Design and Multi-Core Validation using the System-on-Chip Environment", in Proceedings of *the 15th IEEE International High Level Design Validation and Test Workshop (HLDVT)*, pp.142-147, Anaheim, USA, June 2010

C7. Rainer Dömer, **Weiwei Chen**, Xu Han, Andreas Gerstlauer, "Multi-Core Parallel Simulation of System-Level Description Languages", invited paper, in Proceedings of *the 16th Asia and South Pacific Design Automation Conference (ASP-DAC)*, pp.311-316, Yokohama, Japan, January 2011

C8. **Weiwei Chen**, Rainer Dömer, "An Optimizing Compiler for Out-of-Order Parallel ESL Simulation Exploiting Instance Isolation", in Proceedings of *the 17th Asia and South Pacific Design Automation Conference (ASP-DAC)*, pp.461-466, Sydney, Australia, January 2012

C9. Rainer Dömer, **Weiwei Chen**, Xu Han, "Parallel Discrete Event Simulation of Transaction Level Models", invited paper, in Proceedings of *the 17th Asia and South Pacific Design Automation Conference (ASP-DAC)*, pp.227-231, Sydney, Australia, January 2012

C10. **Weiwei Chen**, Xu Han, Rainer Dömer, "Out-of-order Parallel Simulation for ESL design", in Proceedings of *the Design, Automation and Test in Europe Conference (DATE)*, pp.141-146, Dresden, Germany, March 2012

C11. **Weiwei Chen**, Che-Wei Chang, Xu Han, Rainer Dömer, "Eliminating Race Conditions in System-Level Models by using Parallel Simulation Infrastructure", invited paper, in Proceedings of *the IEEE International High Level Design Validation and Test Workshop (HLDVT)*, pp.118-123, Huntington Beach, USA, November 2012

C12. **Weiwei Chen**, Rainer Dömer, "Optimized Out-of-Order Parallel Discrete Event Simulation Using Predictions", in Proceedings of *the Design, Automation and Test in Europe Conference (DATE)*, pp.3-8, Grenoble, France, March 2013

C13. Xu Han, **Weiwei Chen**, Rainer Dömer, "Designer-in-the-Loop Recoding of ESL Models using Static Parallel Access Conflict Analysis", in Proceedings of *the Workshop on Software and Compilers for Embedded Systems (SCOPES)*, Schloss Rheinfels, Germany, June 2013

C14. **Weiwei Chen**, Xu Han, Rainer Dömer, "May-Happen-in-Parallel Analysis based on Segment Graphs for Safe ESL Models", in Proceedings of *the Design, Automation and Test in Europe Conference (DATE)*, Dresden, Germany, March 2014 **(Best Paper Award)**

Technical Reports

TR1. **Weiwei Chen**, Rainer Dömer, "System Specification of a DES Cipher Chip", *TR-08-01*, Center for Embedded Computer System, University of California at Irvine, January 2008

TR2. **Weiwei Chen**, Siwen Sun, Bin Zhang, Rainer Dömer, "System Level Modeling of a H.264 Decoder", *TR-08-10*, Center for Embedded Computer System, University of California at Irvine, August 2008

TR3. **Weiwei Chen**, Rainer Dömer, "A Distributed Parallel Simulator for Transaction Level Models with Relaxed Timing", *TR-11-02*, Center for Embedded Computer Systems, University of California at Irvine, May 2011

TR4. Xu Han, **Weiwei Chen**, Rainer Dömer, "A Parallel Transaction-Level Model of H.264 Video Decoder", *TR-11-03*, Center for Embedded Computer Systems, University of California at Irvine, June 2011

Poster Presentations

P1. Balavinayagam Samynathan, Shahrzad Mirkhani, **Weiwei Chen**, John Davis, Maysam Lavasani and Behnam Robatmili , "Accelerating Big Data Workloads with FPGAs", at *Hot Chips: A Symposium on High Performance Chips*, Cupertino, USA, August 2017

P2. **Weiwei Chen**, Rainer Dömer, "Parallel Discrete Event Simulation for ESL Design", in the *SIGDA Ph.D. Forum at the Design Automation Conference (DAC)*, San Francisco, USA, June 2012

P3. **Weiwei Chen**, Rainer Dömer, "Out-of-order Parallel Discrete Event Simulation for ESL Design", *Graduate Student Poster Presentation*, Faculty Retreat, Department of Electrical Engineering and Computer Science, University of California at Irvine, September 2012

P4. **Weiwei Chen**, Rainer Dömer, "Out-of-order Parallel Simulation for Electronic System-Level Design", in the *EDAA/ACM SIGDA PhD Forum at the Design, Automation and Test in Europe Conference (DATE)*, Grenoble, France, March 2013

Patent

PT1. Iteration Synchronization Construct for Parallel Pipelines (filed), US 15/191,266

PROFESSIONAL ACTIVITIES AND SERVICES

Conference Reviewer

Expert Reviewer

- Design Automation Conference (DAC) 2013

External Reviewer

- Design Automation Conference (DAC) 2009, 2010
- Design, Automation and Test in Europe Conference (DATE) 2010, 2011, 2013, 2014
- ACM/IEEE International Conference on Formal Methods and Models for Co-design (MEMOCODE) 2010
- International Conference on Hardware/Software Co-design and System Synthesis (CODES+ISSS) 2010, 2012, 2013
- IEEE Symposium on High Performance Computer Architecture (HPCA) 2016

Book Chapter Reviewer

- Handbook of Hardware/Software Codesign, Springer

Journal Reviewer

- ACM Transaction on Embedded Computing (TECS)
- Springer's Journal of Network and Systems Management
- Elsevier's Journal of Simulation Modelling Practice and Theory
- Journal of Parallel and Distributed Computing
- IEEE Micro
- ACM Transactions on Design Automation of Electronic Systems (TODAES)

Conference Program Committee

- Artifact Evaluation Committee Member
  International Symposium on Code Generation and Optimization (CGO) 2015, 2016
- Area Co-lead
  Qualcomm Innovation Fellowship - Mobile Application and Apps Enablers

Professional Association Membership

- ACM, IEEE, IEEE Computer Society

Conference Presentations

- IESS'09, ASP-DAC'10, ASP-DAC'12, DATE'12, DAC'12, HLDVT'12, DATE'13, DATE'14, PPoPP'15

Invited Talks

T1. Invited Lecture, "Discussion for C-based SLDLs: SpecC and SystemC", *SoC Description and Modeling (EECS 222A)*, UC Irvine, December 4, 2009

T2. Invited Talk, "Multi-Core Parallel Simulation of System-Level Description Languages", School of Microelectronics, Shanghai Jiao Tong University, December 26, 2011

T3. Invited Talk, "Out-of-order Parallel Discrete Event Simulation for Electronic System-Level Design", School of Microelectronics, Shanghai Jiao Tong University, China, December 12, 2012

T4. Invited Talk, "Out-of-order Parallel Simulation for Electronic System-Level Design", Department of Computer Science, The Carl von Ossietzky University of Oldenburg, Germany, March 14, 2013

T5. "Part II, MARE High-level API" MARE Tutorial: Power Programming for Mobile Computing, 20th ACM SIGPLAN Symposium on Principles and Practice of Parallel Programming (PPoPP), San Francisco, February 8, 2015

REFERENCES

Dr. Rainer Dömer (Ph.D. Advisor)
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Barefoot Networks, Palo Alto, CA
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Dr. Brian Demsky (Dissertation Committee)
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