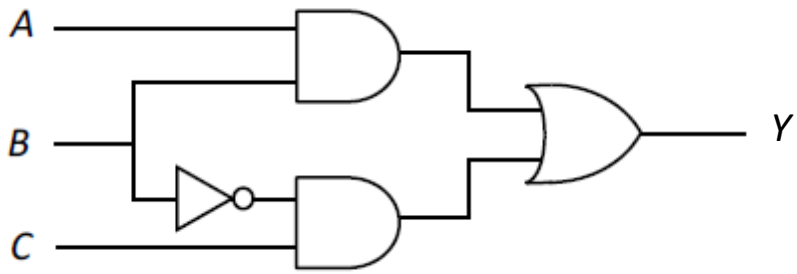
ELEC0010 Digital Design – SystemVerilog coding exercises



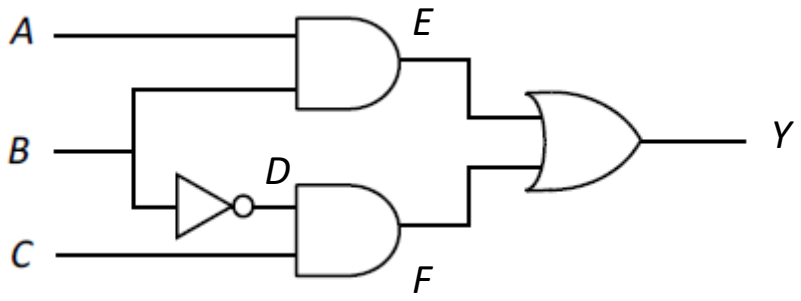
Write SystemVerilog models of the circuit shown above, using:

(i) a netlist of built-in primitives.
(ii) a user-defined primitive (UDP)
(iii) a Boolean expression within a continuous assignment statement

Model solutions are on the next pages.

Solutions

(i) Netlist of built-in primitives. Start by defining internal variables, D, E, and F, as shown in the figure below.




```
module circuit_model1 (input logic a, b, c,
                       output logic y);

logic d, e, f;    // Internal variables

or (y, e, f);
and (e, a, b);
and (f, d, c);
not (d, b);

endmodule
```

(ii) User define primitive (UDP). This method uses the truth table description of the circuit.

```
primitive circuit_model2 (y, a, b, c);
 output y;
 input a, b, c;

 table
 // a  b  c  :  y
    0  0  0 :  0
    0  0  1 :  1
    0  1  0 :  0
    0  1  1 :  0
    1  0  0 :  0
    1  0  1 :  1
    1  1  0 :  1
    1  1  1 :  1
 endtable
 endprimitive
```

(iii) A Boolean expression within a continuous assignment

```
module circuit_model3 (input logic a, b, c,
                       output logic y);

assign y = (a & b) | (~b & c);

endmodule
```