

Digital Design Lab Report

Xiaokun Du

February 2023

1 Arithmetic logic unit (ALU)

Write, as a SystemVerilog module with the name `alu`, a behavioural description of an arithmetic logic unit.

The data inputs, `SrcA` and `SrcB`, and the data output, `ALUResult`, are 8-bit vectors. The `ALUControl` input is a 2-bit vector.

The 1-bit output flag `Zero` = 1 if `ALUResult == 0`, else `Zero` = 0. The ALU carries out bitwise logical operations, and addition and subtraction operations, as specified in the table below.

1.1 Module Code

```
module alu(input logic [7:0] SrcA,
          input logic [7:0] SrcB,
          input logic [1:0] ALUControl,
          output logic [7:0] ALUResult,
          output logic Zero);

always_comb
case (ALUControl)
2'b00 : ALUResult = SrcA & SrcB;
2'b01 : ALUResult = SrcA | SrcB;
2'b10 : ALUResult = SrcA + SrcB;
2'b11 : ALUResult = SrcA - SrcB;
default : ALUResult = 8'bx;
endcase

assign Zero = (ALUResult == 8'b0);
endmodule
```

1.2 Testbench Code

```
`timescale 1ns/1ps
`include "alu.sv"

module alu_tb;
logic [7:0] t_SrcA, t_SrcB;
logic [1:0] t_ALUControl;
logic [7:0] t_ALUResult;
logic t_Zero;

alu uut (t_SrcA, t_SrcB, t_ALUControl, t_ALUResult, t_Zero);

initial begin
    $dumpfile("alu_tb.vcd");
    $dumpvars(0, alu_tb);
    // Stimulus generator
    t_SrcA = 8'h05; t_SrcB = 8'h0A;
    t_ALUControl = 2'b00; #20;
```

```

    t_ALUControl = 2'b01; #20;
    t_ALUControl = 2'b10; #20;
    t_ALUControl = 2'b11; #20;
end

initial begin // Response monitor
    $monitor ("t_ALUControl = %b t_SrcA = %h t_SrcB = %h t_ALUResult = %b t_Zero = %d",t_ALUControl,
        t_SrcA, t_SrcB, t_ALUResult, t_Zero);
end
endmodule

```

1.3 Simulations

The simulation result using Icarus Verilog is as following:

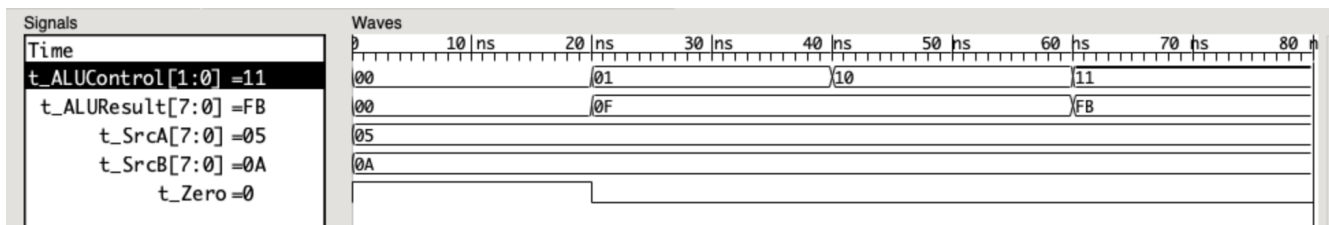
VCD info: dumpfile alu_tb.vcd opened for output.

```

t_ALUControl = 00 t_SrcA = 05 t_SrcB = 0a t_ALUResult = 00000000 t_Zero = 1
t_ALUControl = 01 t_SrcA = 05 t_SrcB = 0a t_ALUResult = 00001111 t_Zero = 0
t_ALUControl = 10 t_SrcA = 05 t_SrcB = 0a t_ALUResult = 00001111 t_Zero = 0
t_ALUControl = 11 t_SrcA = 05 t_SrcB = 0a t_ALUResult = 11111011 t_Zero = 0

```

The simulation results using GTKWave is as following:



2 Register File

The register file has sixteen 8-bit registers. The register with address 0 always contains the value 0. The other 15 registers can have values written into them through the WD3 port.

The contents of any two of the registers (with addresses specified by the 4-bit inputs RA1 and RA2) are continuously output as RD1 and RD2. On the positive edge of the clock, if write_enable is asserted, and A3 \neq 0, the input ALUResult is written into the register at address A3 through the WD3 port. The module includes an output port cpu_out, which continuously outputs the contents of the register at address 15. This will form the main external output of the microprocessor.

2.1 Module Code

```
module reg_file(input logic [3:0] RA1, RA2, WA,
               input logic [7:0] ALUResult,
               input logic clk, write_enable,
               output logic [7:0] RD1, RD2, cpu_out);
logic [7:0] rf [0:15];

assign RD1 = rf[RA1];
assign RD2 = rf[RA2];
assign cpu_out = rf[15];

// register with address 0 always 0
initial begin
rf[4'b0] = 8'b0;
end

always_ff @(posedge clk)
if (write_enable && WA > 0)
rf[WA] <= ALUResult;

endmodule
```

2.2 Testbench Code

```
`timescale 1ps/1ps
`include "reg_file.sv"

module reg_file_tb;
logic [3:0] RA1, RA2, WA;
logic clk, write_enable;
logic [7:0] ALUResult, RD1, RD2, cpu_out;
reg_file dut (RA1, RA2, WA, ALUResult, clk, write_enable, RD1, RD2, cpu_out);

initial begin // Generate clock signal with 20 ns period
    clk = 0;
    forever #10 clk = ~clk;
end

initial begin // Apply stimulus
    $dumpfile("reg_file_tb.vcd");
    $dumpvars(0, reg_file_tb);
    RA1 = 1; RA2 = 2; WA = 0; ALUResult = 5; write_enable = 0;
    #15 write_enable = 1;
    #20 WA = 1; ALUResult = 7;
    #20 WA = 5; ALUResult = 13;
    #20 write_enable = 0;
    #10 RA2 = 5;
```

```

#10;
#10 WA = 15; write_enable = 1;
#10 ALUResult = 15;
#30;
$finish; // This system tasks ends the simulation
end

initial begin // Response monitor
    $monitor ("t = %3d, t_RA1 = %d t_RA2 = %d t_WA = %d ALUResult = %d t_clk = %d t_write_enable = %d
        t_RD1 = %d t_RD2 = %d t_cpu_out = %d",
        $time, RA1, RA2, WA, ALUResult, clk, write_enable, RD1, RD2, cpu_out);
end
endmodule

```

2.3 Simulations

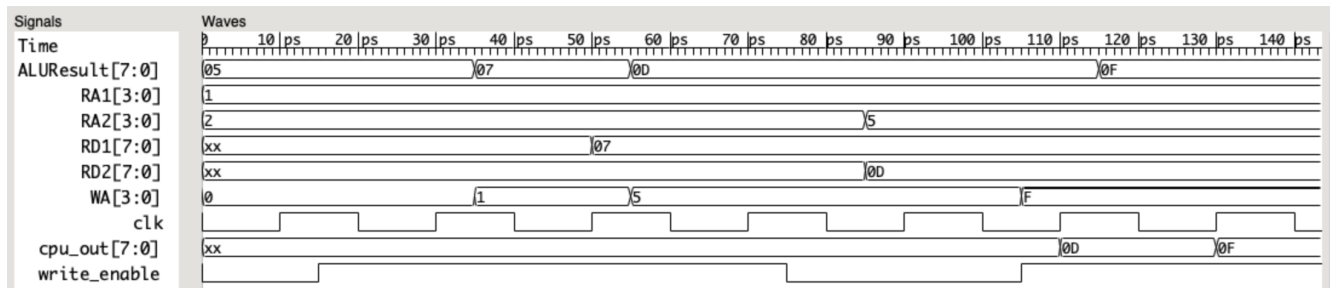
The simulation results using Icarus Verilog is as below:

```

t = 0, RA1 = 1 RA2 = 2 WA = 0 ALUResult = 5 clk = 0 write_enable = 0 RD1 = x RD2 = x cpu_out = x
t = 10, RA1 = 1 RA2 = 2 WA = 0 ALUResult = 5 clk = 1 write_enable = 0 RD1 = x RD2 = x cpu_out = x
t = 15, RA1 = 1 RA2 = 2 WA = 0 ALUResult = 5 clk = 1 write_enable = 1 RD1 = x RD2 = x cpu_out = x
t = 20, RA1 = 1 RA2 = 2 WA = 0 ALUResult = 5 clk = 0 write_enable = 1 RD1 = x RD2 = x cpu_out = x
t = 30, RA1 = 1 RA2 = 2 WA = 0 ALUResult = 5 clk = 1 write_enable = 1 RD1 = x RD2 = x cpu_out = x
t = 35, RA1 = 1 RA2 = 2 WA = 1 ALUResult = 7 clk = 1 write_enable = 1 RD1 = x RD2 = x cpu_out = x
t = 40, RA1 = 1 RA2 = 2 WA = 1 ALUResult = 7 clk = 0 write_enable = 1 RD1 = x RD2 = x cpu_out = x
t = 50, RA1 = 1 RA2 = 2 WA = 1 ALUResult = 7 clk = 1 write_enable = 1 RD1 = 7 RD2 = x cpu_out = x
t = 55, RA1 = 1 RA2 = 2 WA = 5 ALUResult = 13 clk = 1 write_enable = 1 RD1 = 7 RD2 = x cpu_out = x
t = 60, RA1 = 1 RA2 = 2 WA = 5 ALUResult = 13 clk = 0 write_enable = 1 RD1 = 7 RD2 = x cpu_out = x
t = 70, RA1 = 1 RA2 = 2 WA = 5 ALUResult = 13 clk = 1 write_enable = 1 RD1 = 7 RD2 = x cpu_out = x
t = 75, RA1 = 1 RA2 = 2 WA = 5 ALUResult = 13 clk = 1 write_enable = 0 RD1 = 7 RD2 = x cpu_out = x
t = 80, RA1 = 1 RA2 = 2 WA = 5 ALUResult = 13 clk = 0 write_enable = 0 RD1 = 7 RD2 = x cpu_out = x
t = 85, RA1 = 1 RA2 = 5 WA = 5 ALUResult = 13 clk = 0 write_enable = 0 RD1 = 7 RD2 = 13 cpu_out = x
t = 90, RA1 = 1 RA2 = 5 WA = 5 ALUResult = 13 clk = 1 write_enable = 0 RD1 = 7 RD2 = 13 cpu_out = x
t = 100, RA1 = 1 RA2 = 5 WA = 5 ALUResult = 13 clk = 0 write_enable = 0 RD1 = 7 RD2 = 13 cpu_out = x
t = 105, RA1 = 1 RA2 = 5 WA = 15 ALUResult = 13 clk = 0 write_enable = 1 RD1 = 7 RD2 = 13 cpu_out = x
t = 110, RA1 = 1 RA2 = 5 WA = 15 ALUResult = 13 clk = 1 write_enable = 1 RD1 = 7 RD2 = 13 cpu_out = 13
t = 115, RA1 = 1 RA2 = 5 WA = 15 ALUResult = 15 clk = 1 write_enable = 1 RD1 = 7 RD2 = 13 cpu_out = 13
t = 120, RA1 = 1 RA2 = 5 WA = 15 ALUResult = 15 clk = 0 write_enable = 1 RD1 = 7 RD2 = 13 cpu_out = 13
t = 130, RA1 = 1 RA2 = 5 WA = 15 ALUResult = 15 clk = 1 write_enable = 1 RD1 = 7 RD2 = 13 cpu_out = 15
t = 140, RA1 = 1 RA2 = 5 WA = 15 ALUResult = 15 clk = 0 write_enable = 1 RD1 = 7 RD2 = 13 cpu_out = 15

```

The simulation results using GTKWave is as following:



3 Combining the ALU and register file

Write a SystemVerilog module with the name `reg_file_alu`, implementing the combined ALU and register file as shown above. Include a 2-to-1 multiplexer, which selects either the RD2 output from the register file, or an external input (immediate) to be input to the ALU input port `SrcB`.

3.1 Module Code

```
`include "reg_file.sv"
`include "alu.sv"

module reg_file_alu(input logic [3:0] RA1, RA2, WA,
                  input logic [7:0] immediate,
                  input logic [1:0] ALUControl,
                  input logic write_enable, ALUSrc, CLK,
                  output logic [7:0] ALUResult, cpu_out,
                  output logic Zero);
    logic[7:0] x_srcA, x_srcB, x_RD2;

    alu newalu(x_srcA, x_srcB, ALUControl, ALUResult, Zero);
    reg_file newregfile(RA1, RA2, WA, ALUResult, CLK, write_enable, x_srcA, x_RD2, cpu_out);
    // 2 to 1 multiplexer
    assign x_srcB = (ALUSrc) ? immediate : x_RD2;

endmodule
```

3.2 Testbench Code

```
`timescale 1ps/1ps
`include "reg_file_alu.sv"

module reg_file_alu_tb;
    logic [3:0] t_RA1, t_RA2, t_WA;
    logic [7:0] t_immediate, t_ALUResult, t_cpu_out;
    logic [1:0] t_ALUControl;
    logic t_write_enable, t_ALUSrc, clk, t_Zero;

    reg_file_alu dut (t_RA1, t_RA2, t_WA, t_immediate, t_ALUControl, t_write_enable, t_ALUSrc, clk,
                    t_ALUResult, t_cpu_out, t_Zero);

    initial begin
        clk = 0;
        forever #10 clk = ~clk;
    end

    initial begin // Apply stimulus
        $dumpfile("reg_file_alu_tb.vcd");
        $dumpvars(0, reg_file_alu_tb);
        t_RA1 = 4'h0; t_RA2 = 4'h2; t_WA = 4'h0; t_immediate = 8'h0A;
        t_ALUSrc = 1; t_ALUControl = 2'b10; t_write_enable = 1;
        #10 t_RA2 = 4'h1; t_WA = 4'h1;
        #10 t_immediate = 8'h07;
        #20 t_RA1 = 4'h1; t_WA = 4'h1;
        #40 t_ALUControl = 2'b11; t_WA = 4'hF;
        #20 t_immediate = 8'b10111111;
        #20 t_immediate = 8'h0; t_ALUControl = 2'b00;
        #10
    end
```

```

$finish; // This system tasks ends the simulation
end

initial begin // Response monitor
    $monitor ("t = %3d, RA1 = %d RA2 = %d WA = %d Immediate = %d clk = %d write_enable = %d alusRC = %d
        alucontrol = %d aluresult = %d cpu_out = %d zero = %d",
        $time, t_RA1, t_RA2, t_WA, t_immediate, clk, t_write_enable, t_ALUSrc, t_ALUControl,
        t_ALUResult, t_cpu_out, t_Zero);
end
endmodule

```

3.3 Simulations

The simulation result using Icarus Verilog is as following:

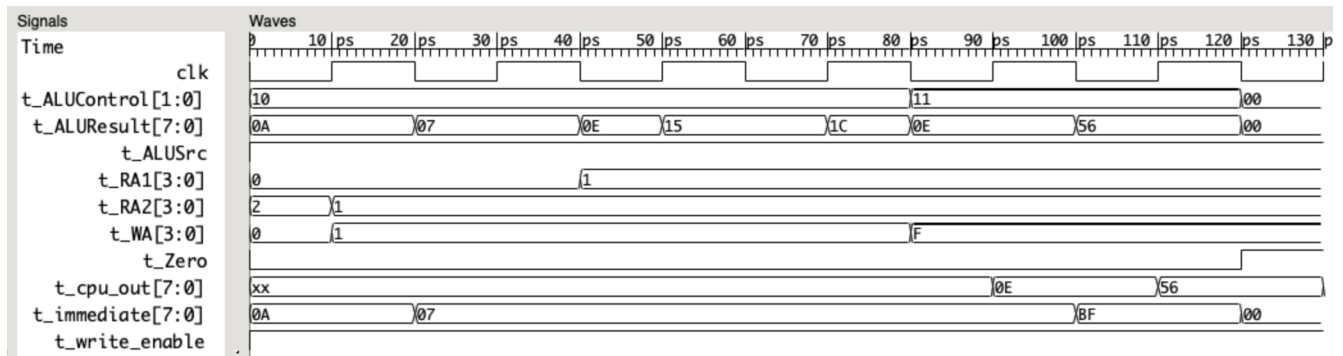
VCD info: dumpfile reg_file_alu_tb.vcd opened for output.

```

t = 0, RA1 = 0 RA2 = 2 WA = 0 Immediate = 10 clk = 0 write_enable = 1 alusRC = 1 alucontrol = 2 aluresult = 10 cpu_out = x zero = 0
t = 10, RA1 = 0 RA2 = 1 WA = 1 Immediate = 10 clk = 1 write_enable = 1 alusRC = 1 alucontrol = 2 aluresult = 10 cpu_out = x zero = 0
t = 20, RA1 = 0 RA2 = 1 WA = 1 Immediate = 7 clk = 0 write_enable = 1 alusRC = 1 alucontrol = 2 aluresult = 7 cpu_out = x zero = 0
t = 30, RA1 = 0 RA2 = 1 WA = 1 Immediate = 7 clk = 1 write_enable = 1 alusRC = 1 alucontrol = 2 aluresult = 7 cpu_out = x zero = 0
t = 40, RA1 = 1 RA2 = 1 WA = 1 Immediate = 7 clk = 0 write_enable = 1 alusRC = 1 alucontrol = 2 aluresult = 14 cpu_out = x zero = 0
t = 50, RA1 = 1 RA2 = 1 WA = 1 Immediate = 7 clk = 1 write_enable = 1 alusRC = 1 alucontrol = 2 aluresult = 21 cpu_out = x zero = 0
t = 60, RA1 = 1 RA2 = 1 WA = 1 Immediate = 7 clk = 0 write_enable = 1 alusRC = 1 alucontrol = 2 aluresult = 21 cpu_out = x zero = 0
t = 70, RA1 = 1 RA2 = 1 WA = 1 Immediate = 7 clk = 1 write_enable = 1 alusRC = 1 alucontrol = 2 aluresult = 28 cpu_out = x zero = 0
t = 80, RA1 = 1 RA2 = 1 WA = 15 Immediate = 7 clk = 0 write_enable = 1 alusRC = 1 alucontrol = 3 aluresult = 14 cpu_out = x zero = 0
t = 90, RA1 = 1 RA2 = 1 WA = 15 Immediate = 7 clk = 1 write_enable = 1 alusRC = 1 alucontrol = 3 aluresult = 14 cpu_out = 14 zero = 0
t = 100, RA1 = 1 RA2 = 1 WA = 15 Immediate = 191 clk = 0 write_enable = 1 alusRC = 1 alucontrol = 3 aluresult = 86 cpu_out = 14 zero = 0
t = 110, RA1 = 1 RA2 = 1 WA = 15 Immediate = 191 clk = 1 write_enable = 1 alusRC = 1 alucontrol = 3 aluresult = 86 cpu_out = 86 zero = 0
t = 120, RA1 = 1 RA2 = 1 WA = 15 Immediate = 0 clk = 0 write_enable = 1 alusRC = 1 alucontrol = 0 aluresult = 0 cpu_out = 86 zero = 1
t = 130, RA1 = 1 RA2 = 1 WA = 15 Immediate = 0 clk = 1 write_enable = 1 alusRC = 1 alucontrol = 0 aluresult = 0 cpu_out = 0 zero = 1

```

The simulation results using GTKWave is as following:



4 Instruction memory

4.1 Module Code

```
module instruction_memory(input logic[7:0] PC,
                        output logic[23:0] Instr);
logic [23:0] data_ROM [0:255];
initial
$readmemh("program.txt", data_ROM);
assign Instr = data_ROM[PC];
endmodule
```

4.2 Text File

This is the content of the text file named “program.txt”:

```
610001
620020
6F0000
701207
211100
6FF001
700003
700007
```

4.3 Testbench Code

```
`timescale 1ns/1ps
`include "instruction_memory.sv"

module instruction_memory_tb;
logic [7:0] t_PC;
logic [23:0] t_Instr;

instruction_memory dut (t_PC, t_Instr);

initial begin
    $dumpfile("instruction_memory_tb.vcd");
    $dumpvars(0, instruction_memory_tb);
    // Stimulus generator
    t_PC = 8'h00;
    #10 t_PC = 8'h01;
    #10 t_PC = 8'h02;
    #10 t_PC = 8'h03;
    #10 t_PC = 8'h04;
    #10 t_PC = 8'h05;
    #10 t_PC = 8'h06;
    #10 t_PC = 8'h07;

end

initial begin // Response monitor
    $monitor ("t_PC = %h t_Instr = %h", t_PC, t_Instr);
end

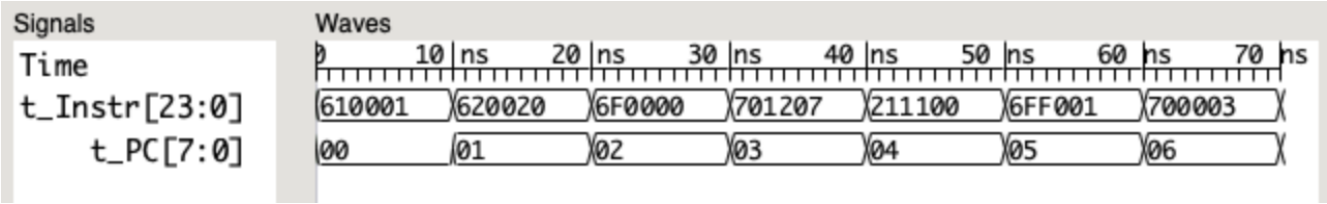
endmodule
```

4.4 Simulations

The simulation result using Icarus Verilog is as following:

```
t_PC = 00 t_Instr = 610001
t_PC = 01 t_Instr = 620020
t_PC = 02 t_Instr = 6f0000
t_PC = 03 t_Instr = 701207
t_PC = 04 t_Instr = 211100
t_PC = 05 t_Instr = 6ff001
t_PC = 06 t_Instr = 700003
t_PC = 07 t_Instr = 700007
```

The simulation results using GTKWave is as following:



5 Program Counter

Implement the 8-bit program counter shown above, as a SystemVerilog module with the name pc. The register should be updated on the positive edges of the clock, and have an active high reset. The 2-to-1 multiplexer selects the next value of PC as either PC+1 (the next instruction in the program will be fetched) or the input immediate (the program branches to an instruction elsewhere).

5.1 Module Code

```
module pc (input logic[7:0] immediate,
           input logic PCSrc, CLK, reset,
           output logic[7:0] PC);
always_ff @ (posedge CLK) begin
    if (reset) PC <= 8'b0;
    else if (PCSrc) PC <= immediate;
    else PC <= PC + 1;
end
endmodule
```

5.2 Testbench Code

```
`timescale 1ns/1ps
`include "pc.sv"

module pc_tb;
logic [7:0] t_PC, t_immediate;
logic t_PCSrc, clk, t_reset;

pc pc(t_immediate, t_PCSrc, clk, t_reset, t_PC);

initial begin
    clk = 0;
    forever #10 clk = ~clk;
end

initial begin
    $dumpfile("pc_tb.vcd");
    $dumpvars(0, pc_tb);
    // Stimulus generator
    t_reset = 1; t_PCSrc = 0; t_immediate = 8'b01;
    #10 t_reset = 0; t_PCSrc = 1;
    #20 t_immediate = 8'b111;
    #20 t_PCSrc = 0;
    #50 t_reset = 1;
    $finish; // This system tasks ends the simulation
end

initial begin // Response monitor
    $monitor ("t = %3d clk = %d, t_immediate = %b t_PCSrc = %b t_reset = %d t_PC = %d", $time, clk,
             t_immediate, t_PCSrc, t_reset, t_PC);
    #120;
end

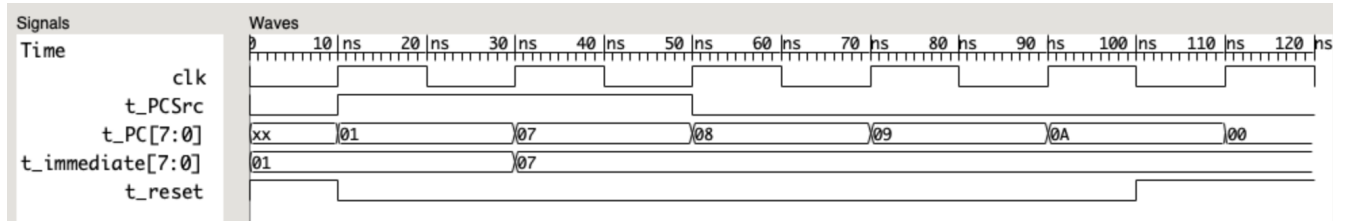
endmodule
```

5.3 Simulations

The simulation result using Icarus Verilog is as following:

```
t = 0  clk = 0, t_immediate = 00000001 t_PCSrc = 0 t_reset = 1 t_PC =  x
t = 10 clk = 1, t_immediate = 00000001 t_PCSrc = 1 t_reset = 0 t_PC =  1
t = 20 clk = 0, t_immediate = 00000001 t_PCSrc = 1 t_reset = 0 t_PC =  1
t = 30 clk = 1, t_immediate = 00000111 t_PCSrc = 1 t_reset = 0 t_PC =  7
t = 40 clk = 0, t_immediate = 00000111 t_PCSrc = 1 t_reset = 0 t_PC =  7
t = 50 clk = 1, t_immediate = 00000111 t_PCSrc = 0 t_reset = 0 t_PC =  8
t = 60 clk = 0, t_immediate = 00000111 t_PCSrc = 0 t_reset = 0 t_PC =  8
t = 70 clk = 1, t_immediate = 00000111 t_PCSrc = 0 t_reset = 0 t_PC =  9
t = 80 clk = 0, t_immediate = 00000111 t_PCSrc = 0 t_reset = 0 t_PC =  9
t = 90 clk = 1, t_immediate = 00000111 t_PCSrc = 0 t_reset = 0 t_PC = 10
t = 100 clk = 0, t_immediate = 00000111 t_PCSrc = 0 t_reset = 1 t_PC = 10
t = 110 clk = 1, t_immediate = 00000111 t_PCSrc = 0 t_reset = 1 t_PC =  0
t = 120 clk = 0, t_immediate = 00000111 t_PCSrc = 0 t_reset = 1 t_PC =  0
```

The simulation results using GTKWave is as following:



6 Combining the ROM with program counter

6.1 Module Code

```
`include "instruction_memory.sv"
`include "pc.sv"

module instruction_memory_pc (input logic[7:0] immediate,
                             input logic PCSrc, CLK, reset,
                             output logic [23:0] Instr);

logic[7:0] x_PC;

pc new_pc (immediate, PCSrc, CLK, reset, x_PC);
instruction_memory new_im(x_PC, Instr);
endmodule
```

6.2 Testbench Code

```
`timescale 1ps/1ps
`include "instruction_memory_pc.sv"

module instruction_memory_pc_tb;
logic [7:0] t_immediate;
logic t_PCSrc, clk, t_reset;
logic [23:0] t_Instr;

instruction_memory_pc dut(t_immediate, t_PCSrc, clk, t_reset, t_Instr);

initial begin
    clk = 0;
    forever #10 clk = ~clk;
end

initial begin
    $dumpfile("instruction_memory_pc_tb.vcd");
    $dumpvars(0, instruction_memory_pc_tb);
    // Stimulus generator
    t_reset = 1; t_PCSrc = 0; t_immediate = 8'b01;
    #10 t_reset = 0; t_PCSrc = 1;
    #20 t_immediate = 8'b101;
    #20 t_PCSrc = 0; t_reset = 1;
    #20 t_reset = 0;
    #20 t_immediate = 8'b111;
    #20 t_PCSrc = 1;
    $finish; // This system tasks ends the simulation
end

initial begin // Response monitor
    $monitor ("t = %3d clk = %d, t_immediate = %b t_PCSrc = %b t_reset = %d t_Instr = %h", $time, clk,
             t_immediate, t_PCSrc, t_reset, t_Instr);
    #120;
end

endmodule
```

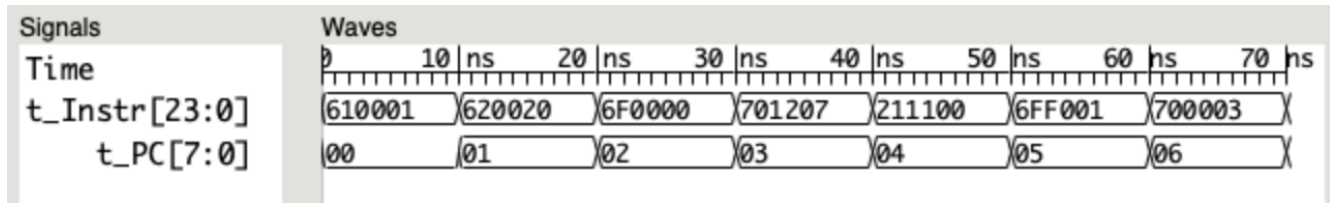
6.3 Simulations

The simulation result using Icarus Verilog is as following:

(t_pc is temporarily outputted as an output to check the working of the system)

```
t = 0 clk = 0, t_immediate = 00000001 t_PCSrc = 0 t_reset = 1 t_Instr = xxxxxx t_pc = xx
t = 10 clk = 1, t_immediate = 00000001 t_PCSrc = 1 t_reset = 0 t_Instr = 620020 t_pc = 01
t = 20 clk = 0, t_immediate = 00000001 t_PCSrc = 1 t_reset = 0 t_Instr = 620020 t_pc = 01
t = 30 clk = 1, t_immediate = 00000101 t_PCSrc = 1 t_reset = 0 t_Instr = 6ff001 t_pc = 05
t = 40 clk = 0, t_immediate = 00000101 t_PCSrc = 1 t_reset = 0 t_Instr = 6ff001 t_pc = 05
t = 50 clk = 1, t_immediate = 00000101 t_PCSrc = 0 t_reset = 1 t_Instr = 610001 t_pc = 00
t = 60 clk = 0, t_immediate = 00000101 t_PCSrc = 0 t_reset = 1 t_Instr = 610001 t_pc = 00
t = 70 clk = 1, t_immediate = 00000101 t_PCSrc = 0 t_reset = 0 t_Instr = 620020 t_pc = 01
t = 80 clk = 0, t_immediate = 00000101 t_PCSrc = 0 t_reset = 0 t_Instr = 620020 t_pc = 01
t = 90 clk = 1, t_immediate = 00000111 t_PCSrc = 0 t_reset = 0 t_Instr = 6f0000 t_pc = 02
t = 100 clk = 0, t_immediate = 00000111 t_PCSrc = 0 t_reset = 0 t_Instr = 6f0000 t_pc = 02
t = 110 clk = 1, t_immediate = 00000111 t_PCSrc = 1 t_reset = 0 t_Instr = 700007 t_pc = 07
t = 120 clk = 0, t_immediate = 00000111 t_PCSrc = 1 t_reset = 0 t_Instr = 700007 t_pc = 07
```

The simulation results using GTKWave is as following:



7 Control Unit

7.1 Module Code

```
module control_unit (input logic[3:0] opcode,
                    output logic Branch, ALUSrc, RegWrite,
                    output logic[1:0]ALUControl);

always_comb
case (opcode)
  4'b0000 : begin
    RegWrite = 1; ALUSrc = 0; ALUControl = 2'b00; Branch = 0;
  end
  4'b0001 : begin
    RegWrite = 1; ALUSrc = 0; ALUControl = 2'b01; Branch = 0;
  end
  4'b0010 : begin
    RegWrite = 1; ALUSrc = 0; ALUControl = 2'b10; Branch = 0;
  end
  4'b0011 : begin
    RegWrite = 1; ALUSrc = 0; ALUControl = 2'b11; Branch = 0;
  end
  4'b0100 : begin
    RegWrite = 1; ALUSrc = 1; ALUControl = 2'b00; Branch = 0;
  end
  4'b0101 : begin
    RegWrite = 1; ALUSrc = 1; ALUControl = 2'b01; Branch = 0;
  end
  4'b0110 : begin
    RegWrite = 1; ALUSrc = 1; ALUControl = 2'b10; Branch = 0;
  end
  4'b0111 : begin
    RegWrite = 0; ALUSrc = 0; ALUControl = 2'b11; Branch = 1;
  end
endcase
endmodule
```

7.2 Testbench Code

```
`timescale 1ps/1ps
`include "control_unit.sv"

module control_unit_tb;
logic[3:0] t_opcode;
logic t_Branch, t_ALUSrc, t_RegWrite;
logic [1:0] t_ALUControl;

control_unit dut (t_opcode, t_Branch, t_ALUSrc, t_RegWrite, t_ALUControl);

initial begin
  $dumpfile("control_unit_tb.vcd");
  $dumpvars(0, control_unit_tb);
  // Stimulus generator
  t_opcode = 4'b0000;
  #20 t_opcode = 4'b0001;
  #20 t_opcode = 4'b0010;
  #20 t_opcode = 4'b0011;
  #20 t_opcode = 4'b0100;
  #20 t_opcode = 4'b0101;
  #20 t_opcode = 4'b0110;
```

```

    #20 t_opcode = 4'b0111;
end

initial begin // Response monitor
    $monitor ("t = %3d t_opcode = %b, t_RegWrite = %d, t_ALUSrc = %d, ALUControl = %b, Branch = %d",
        $time, t_opcode, t_RegWrite, t_ALUSrc, t_ALUControl, t_Branch);
end
endmodule

```

7.3 Simulations

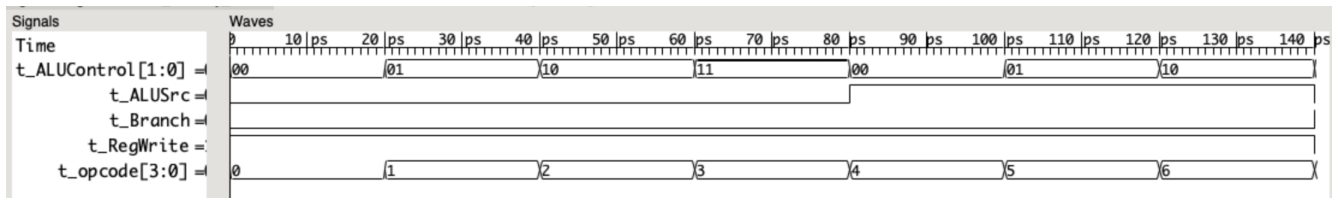
The simulation result using Icarus Verilog is as following:

```

t = 0 t_opcode = 0000, t_RegWrite = 1, t_ALUSrc = 0, ALUControl = 00, Branch = 0
t = 20 t_opcode = 0001, t_RegWrite = 1, t_ALUSrc = 0, ALUControl = 01, Branch = 0
t = 40 t_opcode = 0010, t_RegWrite = 1, t_ALUSrc = 0, ALUControl = 10, Branch = 0
t = 60 t_opcode = 0011, t_RegWrite = 1, t_ALUSrc = 0, ALUControl = 11, Branch = 0
t = 80 t_opcode = 0100, t_RegWrite = 1, t_ALUSrc = 1, ALUControl = 00, Branch = 0
t = 100 t_opcode = 0101, t_RegWrite = 1, t_ALUSrc = 1, ALUControl = 01, Branch = 0
t = 120 t_opcode = 0110, t_RegWrite = 1, t_ALUSrc = 1, ALUControl = 10, Branch = 0
t = 140 t_opcode = 0111, t_RegWrite = 0, t_ALUSrc = 0, ALUControl = 11, Branch = 1

```

The simulation results using GTKWave is as following:



8 Complete CPU design

8.1 Module Code

```
`include "control_unit.sv"
`include "reg_file_alu.sv"
`include "instruction_memory_pc.sv"

module cpu (input logic CLK, reset,
            output logic[7:0] ALUResult, cpu_out);
    logic x_PCsrc;
    logic [23:0] x_Instr;
    logic [1:0] x_ALUControl;
    logic x_ALUSrc, x_RegWrite, x_Branch, x_Zero;

    instruction_memory_pc cpu_instruction_memory_pc(x_Instr[7:0], x_PCsrc, CLK, reset,
        x_Instr);

    reg_file_alu cpu_reg_file_alu (x_Instr[15:12], x_Instr[11:8], x_Instr[19:16], x_Instr[7:0],
        x_ALUControl, x_RegWrite, x_ALUSrc, CLK,
        ALUResult, cpu_out, x_Zero);

    control_unit cpu_control_unit (x_Instr[23:20], x_Branch, x_ALUSrc, x_RegWrite, x_ALUControl);

    assign x_PCsrc = x_Branch & x_Zero;

endmodule
```

8.2 Testbench Code

```
`timescale 1ps/1ps
`include "cpu.sv"

module cpu_tb;
    logic clk, t_reset;
    logic [7:0] t_ALUResult, t_cpu_out;

    cpu dut (clk, t_reset, t_ALUResult, t_cpu_out);

    initial begin
        clk = 0;
        forever #10 clk = ~clk;
    end

    initial begin
        $dumpfile("cpu_tb.vcd");
        $dumpvars(0, cpu_tb);
        // Stimulus generator
        t_reset = 1;
        #20 t_reset = 0;
        #1000 $finish;
    end

    initial begin // Response monitor
        $monitor ("t = %3d clk = %d, t_reset = %d t_ALUResult = %b t_cpu_out = %d", $time, clk, t_reset,
            t_ALUResult, t_cpu_out);
    end

endmodule
```

8.3 Simulations

The simulation result using Icarus Verilog is as following:

[illegible]

The simulation results using GTKWave is as following:

