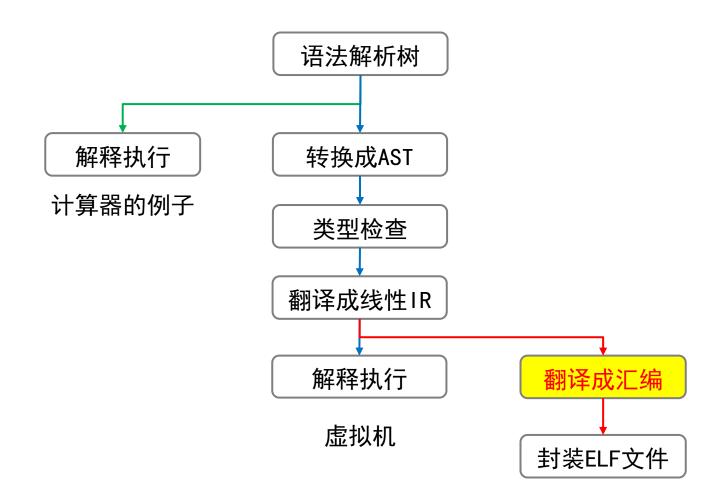
Lecture 12

汇编代码

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编译地图



大纲

- 一、基础arm指令
- 二、调用规约
- 三、更多指令和寄存器

一、基础arm指令

指令集架构: Instruction Set Architecture

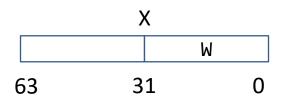
- 精简指令集(RISC)
 - 每条指令只做一件事(主要指内存访问和运算分离)
 - ARM\ RISC-V
- 复杂指令集(CISC)
 - 一条指令可以包含多个底层操作(load-add-store)
 - X86(Intel IA-32)、X86-64架构(AMD64)
- 其它
 - VLIW: Very long instruction word (Intel IA-64)
 - EPIC: Explicitly parallel instruction computing

目标指令集: arm v8a

- 32位版本: ARM Cortex-A32
- 32/64位版本: ARM Cortex-A57/A72/A73等,代表芯片
 - Apple A8/A8x/A9/A9x/A10/A10x (iPhone, iPad)
 - Apple M1/M2 (iPhone, iPad, MacBook)
 - Qualcomm Kryo: 骁龙(Snapdragon 820)
- aarch64 vs arm64 (Apple版本)

arm v8a寄存器:通用寄存器

• 通用寄存器: X0 - X30 (64-bit)



```
mov w1, #5

mov w2, #10

add w0, w1, w2

w1 = 5

w2 = 10

w0 = w1 + w2
```

IR=>Assembly: 数据存取

• 栈(顶)寄存器: SP(16字节对齐)

#: gcc test.o -e main -arch arm64

```
%x = alloca i32
store i32 1, %x
%x0 = load i32, i32* %x

sub sp, sp, #16
mov w0, #1
str w0, [sp]
ldr w0, [sp]
```

#: llc -00 -march=arm64 -filetype=asm foo.ll -o foo.s

```
#: as foo.s -o foo.o
MacOS (M1)

#: ld foo.o -lSystem -syslibroot `xcrun -sdk macosx --show-sdk-path` -e _start -arch arm64
或
```

arm v8a指令: 寻址模式

• 不支持直接寻址,间接寻址

Addressing Made	Offset						
Addressing Mode	Immediate Register		Extended Register				
Base register only (no offset)	[base{, #0}]	-	-				
Base plus offset	[base{, #imm}]	[base, Xm{, LSL #imm}]	[base, Wm, (S U)XT(X W) {#imm}]				
Pre-indexed	[base, #imm]!	-	-				
Post-indexed	[base], #imm	[base], Xm ^a	-				
Literal (PC-relative)	label	-	-				

```
ldr x2, [x1]
ldr x2, [x1, #10]
ldr x2, [x1, x0]
ldr x2, [x1, #10]!
ldr x2, [x1], #10
ldr x2, [x1, x0, ls1 #3]
```

```
x2 = [x1 + 10]

x2 = [x1 + x0]

x1 = x1 + 10, x2 = [x1]

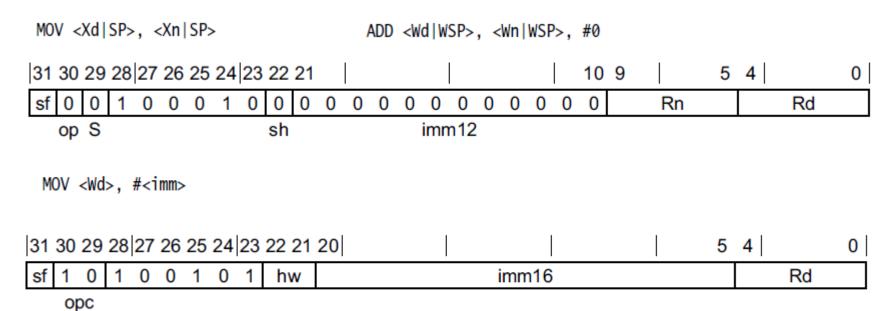
x2 = [x1], x1 = x1 + 10

x2 = [x1 + x0 *3]
```

```
str w0, [x1]
str w0, [x1, #10]
str x2, [x1, x0]
```

arm v8a指令: MOV

• MOV: 任意16位立即数,或左移若干位?



mov x1, #65535 mov x2, #65537 mov x3, #131070

arm v8a指令: LDR(立即数)

LDR <Xt>, [<Xn|SP>], #<simm> 31 30 29 28 27 26 25 24 23 22 21 20 12 11 10 9 5 4 0 1 x 1 1 1 1 0 0 0 0 0 1 0 imm9 0 1 Rn Rt size opc LDR <Xt>, [<Xn|SP>, #<simm>]! 31 30 29 28 27 26 25 24 23 22 21 20 12 11 10 9 5 4 0 1 x 1 1 1 1 0 0 0 0 0 1 0 imm9 Rn Rt size opc LDR <Xt>, [<Xn|SP>{, #<pimm>}] 31 30 29 28 27 26 25 24 23 22 21 10 9 5 4 0 1 0 0 1 0 1 imm₁₂ Rn Rt size opc

```
ldr x2, [x1]
ldr x2, [x1, #10]
ldr x2, [x1, #10]!
```

arm v8a指令: LDR(寄存器/标签)

LDR <Xt>, <label>

31 30 29 28 27 26 25 24 23			5	4	0
0 x 0 1 1 0 0 0	imm19)		Rt	

opc

arm v8a指令: STR

STR <Wt>, [<Xn|SP>], #<simm> 31 30 29 28 27 26 25 24 23 22 21 20 12 11 10 9 5 4 0 1 x 1 1 1 1 0 0 0 0 0 0 0 0 1 Rn Rt imm9 size opc STR <Xt>, [<Xn|SP>, #<simm>]! |31 30 29 28 27 26 25 24 23 22 21 20 | 12 11 10 9 5 4 0 1 x 1 1 1 1 0 0 0 0 0 0 0 imm9 Rn Rt size opc STR <Xt>, [<Xn|SP>{, #<pimm>}] 31 30 29 28 27 26 25 24 23 22 21 10 9 5 4 0 imm₁₂ 1 0 0 1 Rt Rn size opc STR $\langle Xt \rangle$, $[\langle Xn | SP \rangle$, $(\langle Wm \rangle | \langle Xm \rangle) \{$, $\langle extend \rangle \{\langle amount \rangle \} \}]$ 31 30 29 28 27 26 25 24 23 22 21 20 16 15 13 12 11 10 9 5 4 0 1 x 1 1 1 0 0 0 0 0 0 Rm option Rn Rt size opc

复合类型如何翻译?

```
define i32 @main() {
    %1 = alloca [2 x i32]
    %2 = getelementptr [2 x i32], [2 x i32]* %1, i32 0, i32 0
    store i32 99, i32* %2
    %3 = load i32, i32* %2
    ret i32 %3
}
```

```
%mystruct = type { i32, i32 }
define i32 @main() {
   %1 = alloca %mystruct
   %2 = getelementptr %mystruct, %mystruct* %1, i32 0, i32 0
   store i32 1, i32* %2
   ret i32 0
}
```

IR=>Assembly: 算数运算

```
%r1 = add i32 %0, %1
%r2 = sub i32 %r1, 2
%r3 = mul i32 %r2, %1
%r4 = sdiv i32 %r3, %1
add w8, w0, w1
sub w8, w8, #2
mul w8, w8, w1
sdiv w0, w8, w1
```

arm v8a指令: 算数运算: ADD

```
ADD <Xd|SP>, <Xn|SP>, #<imm>{, <shift>} sh == 1, imm左移12位
31 30 29 28 27 26 25 24 23 22 21
                                                           10 9
                                                                          5 4
sf 0 0 1 0 0 0 1 0 sh
                                          imm<sub>12</sub>
                                                                    Rn
                                                                                  Rd
  op S
ADD <Xd>, <Xn>, <Xm>{, <shift> #<amount>}
|31 30 29 28|27 26 25 24|23 22 21 20|
                                          16 15
                                                           10 9
                                                                          5 4
sf | 0 | 0 | 0 | 1 | 0 | 1 | 1 | shift | 0
                                    Rm
                                                   imm6
                                                                    Rn
                                                                                  Rd
  op S
```

```
add x0, x1, #4095
add x0, x1, #4097
add x0, x1, #20480
```

add x0, x1, x2

arm v8a指令: 算数运算: SUB

SUB <Xd|SP>, <Xn|SP>, #<imm>{, <shift>}

31 30	29	28	27	26	25	24	23	22	1		10	9		5	4	0
sf 1	0	1	0	0	0	1	0	sh		imm12			Rn		F	₹d
or	S															

SUB <Xd>, <Xn>, <Xm>{, <shift> #<amount>}

31 30 29 28 27 26 25 2	4 23 22 21	20 16	15 10	9 5	4 0
sf 1 0 0 1 0 1	shift 0	Rm	imm6	Rn	Rd

op S

arm v8a指令: 算数运算: MUL/SDIV

MUL < Xd >, < Xn >, < Xm >

不支持立即数

31	30	29	28	27	26	25	24	23	22	21	20	16	15	14				10	9		5	4		0
sf	0	0	1	1	0	1	1	0	0	0	Rm		0	1	1	1	1	1		Rn			Rd	
													00			Ra								

SDIV <Xd>, <Xn>, <Xm>

31 30 29	28 27 26	25 24 23	3 22 21 2	20 16	15 14 13	12 11 1	0 9 5	4 0
sf 0 0	1 1 0	1 0 1	1 0	Rm	0 0 0	0 1 1	Rn	Rd

arm v8a指令:复合算数运算

MADD < Xd>, < Xn>, < Xm>, < Xa>

31 30 29 28 27 26 25 24 23 22 21 2	0	16 15 14	10	9	5 4	0
sf 0 0 1 1 0 1 1 0 0 0	Rm	0	Ra	Rn	Rd	
		00				
MSUB < Xd>, < Xn>, < Xm>, < Xa>						
31 30 29 28 27 26 25 24 23 22 21 2	0	16 15 14	10	9	5 4	0
sf 0 0 1 1 0 1 1 0 0 0	Rm	1	Ra	Rn	Rd	
		00				

$$x0 = x1 * x2 + x3$$

 $x0 = x1 * x2 - x3$

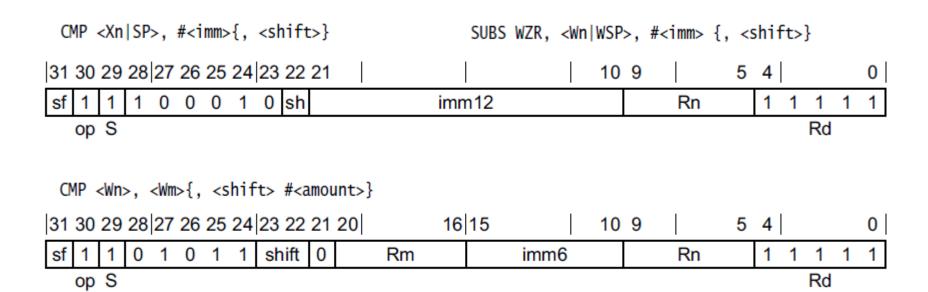
IR=>Assembly: 比较运算和结果获取

条件

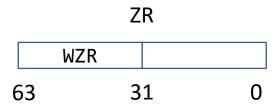
```
cmp w0, w1
%r1 = icmp sgt i32 %0, %1
                                  cset w0, gt
%r2 = zext i1 %r1 to i32
                                  cmp w0, w1
%r1 = icmp sge i32 %0, %1
                                  cset w0, ge
%r2 = zext i1 %r1 to i32
                                       w0, w1
                                  cmp
%r1 = icmp eq i32 %0, %1
                                  cset w0, eq
%r2 = 7ext i1 %r1 to i32
                                       w0, w1
%r1 = icmp ne i32 %0, %1
                                  cmp
                                  cset w0, ne
%r2 = zext i1 %r1 to i32
                                  cmp w0, w1
%r1 = icmp sle i32 %0, %1
                                  cset w0, le
%r2 = 7ext i1 %r1 to i32
                                  cmp w0, w1
%r1 = icmp lt i32 %0, %1
                                  cset w0, It
%r2 = zext i1 %r1 to i32
```

arm v8a指令:比较运算: CMP

• 基于PSR(NZCV)寄存器实现



arm v8a寄存器:零寄存器



mov x1, xzr x1 = 0mov w1, wzr w2 = 0

Arm v8a指令: 读取NZCV

• 基于减法实现,更新CPSR寄存器:

N(31位):符号标志位;如果负,则N=1

▼ Z(30位): 0标志位; 如果0, 则Z=1

C(29位): 进位标志位;

• 无符号数:加法进位,或减法不借位,则C=1

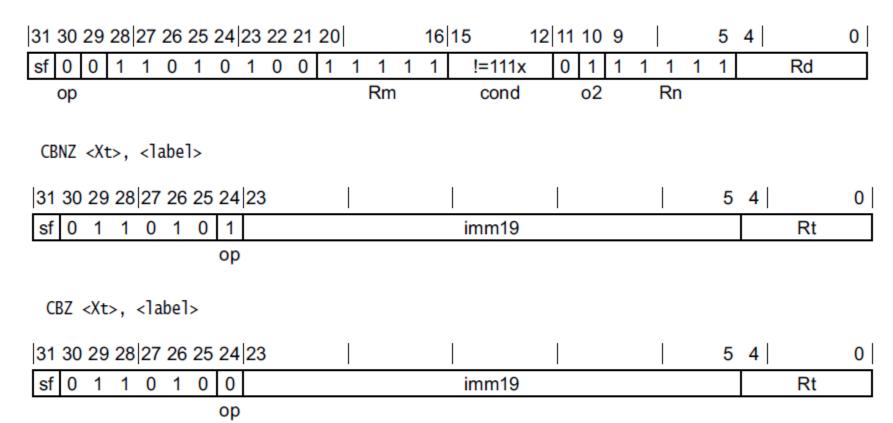
• V(28位):溢出标志位:有符号运算溢出,则V=1

Result	N	Z	C	V
Greater than	0	0	1	0
Less than	1	0	0	0
Equal	0	1	1	0

mrs x0, nzcv

Arm v8a指令:条件指令(举例)

CSET <Xd>, <cond>



IR=>Assembly: 跳转语句

```
bb0:
    %r1 = icmp sgt i32 %0, %1
    br i1 %r1, label %bb1, label %bb2
bb1:
    br label %bb3
bb2:
    br label %bb3
bb3:
```

Arm v8a指令: 跳转指令

B < label>

5 (140-61)				
31 30 29 28 27 26 25				0
0 0 0 1 0 1		imm26		
ор				
B. <cond> <1abe1></cond>				
31 30 29 28 27 26 25 24 23			5 4 3	0
0 1 0 1 0 1 0 0	imm	19	0 cc	ond

Mnemonic	Instruction	Branch offset range from the PC
B.cond	Branch conditionally	±1MB
BC.cond	Branch Consistent conditionally	±1MB
CBNZ	Compare and branch if nonzero	±1MB
CBZ	Compare and branch if zero	±1MB
TBNZ	Test bit and branch if nonzero	±32KB
TBZ	Test bit and branch if zero	±32KB

add w0, w1, w2
cbz zero_set
...
zero_set:

IR=>Assembly: 异或运算(逻辑NOT)

Mnemonic	Instruction
AND	Bitwise AND
ANDS	Bitwise AND and set flags
EOR	Bitwise exclusive OR
ORR	Bitwise inclusive 0R
TST	Test bits

二、函数调用

IR=>Assembly: 函数

```
@g = global i32 10
define i32 @foo(i32 %0) {
   %x = alloca i32
   store i32 %0, %x
   %g0 = load i32, i32* @g
   ret i32 %g0
}
define i32 @main() {
  %r0 = call i32 @foo(i32 1)
  ret i32 %r0;
```

```
foo:
   sub sp, sp, #16
   adrp
          x8, g
   add x8, x8, :lo12:g
   str w0, [sp, #12]
   1dr w0, [x8]
   add
          sp, sp, #16
   ret
main:
          x30, [sp, #-16]!
   str
          w0, #1
   mov
   b1
          foo
   ldr
          x30, [sp], #16
   ret
g:
   .word
          10
```

1 word = 4 byte

调用规约

• 参数传递: X0-X7

• 返回值: X0-X1

• Caller-saved Registers: X9-X15 (临时寄存器)

Callee-saved Registers: X19-X28

• X29: 一般用于栈帧基指针

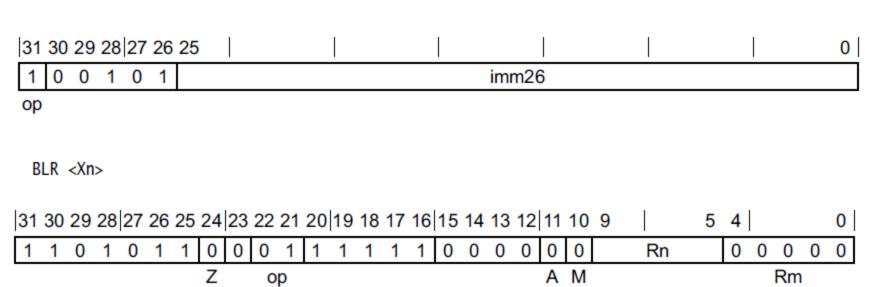
• X30: 一般用于返回地址

• SP: 栈顶指针

arm v8a指令: 函数调用

• 跳转并将X30设置为PC+4

BL < label>



IR=>Assembly: 取址(全局变量)

Mnemonic	Instruction
ADRP	Compute address of 4KB page at a PC-relative offset
ADR	Compute address of label at a PC-relative offset.

4KB对齐: 末尾12位为0

adrp x8, g add x8, x8, :lo12:g

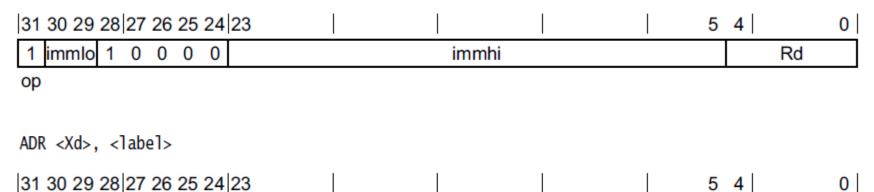
Rd

arm64版本:

adrp x8, g@PAGE add x8, x8, g@PAGEOFF

ADRP <Xd>, <1abe1>

0 immlo 1 0 0 0 0



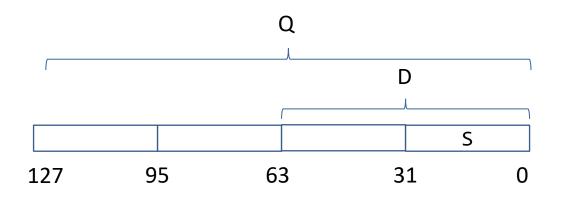
immhi

op

三、更多指令和寄存器

arm v8a寄存器:向量寄存器和SIMD指令

• 向量寄存器: Q0-Q31



```
VLDR S0, [X0]
VLDR S1, [X1]
VADD.F32 S2, S0, S1
```

浮点数运算

VLDR Q0, [X0] VLDR Q1, [X1] VADD.I32 Q2, Q0, Q1

向量运算

参考资料

- Arm® Architecture Reference Manual for A-profile architecture
- 在线模拟器: http://163.238.35.161/~zhangs/arm64simulator/

