

oneAPI Technical Advisory Board Meeting

December 16, 2020

Virtual Meeting

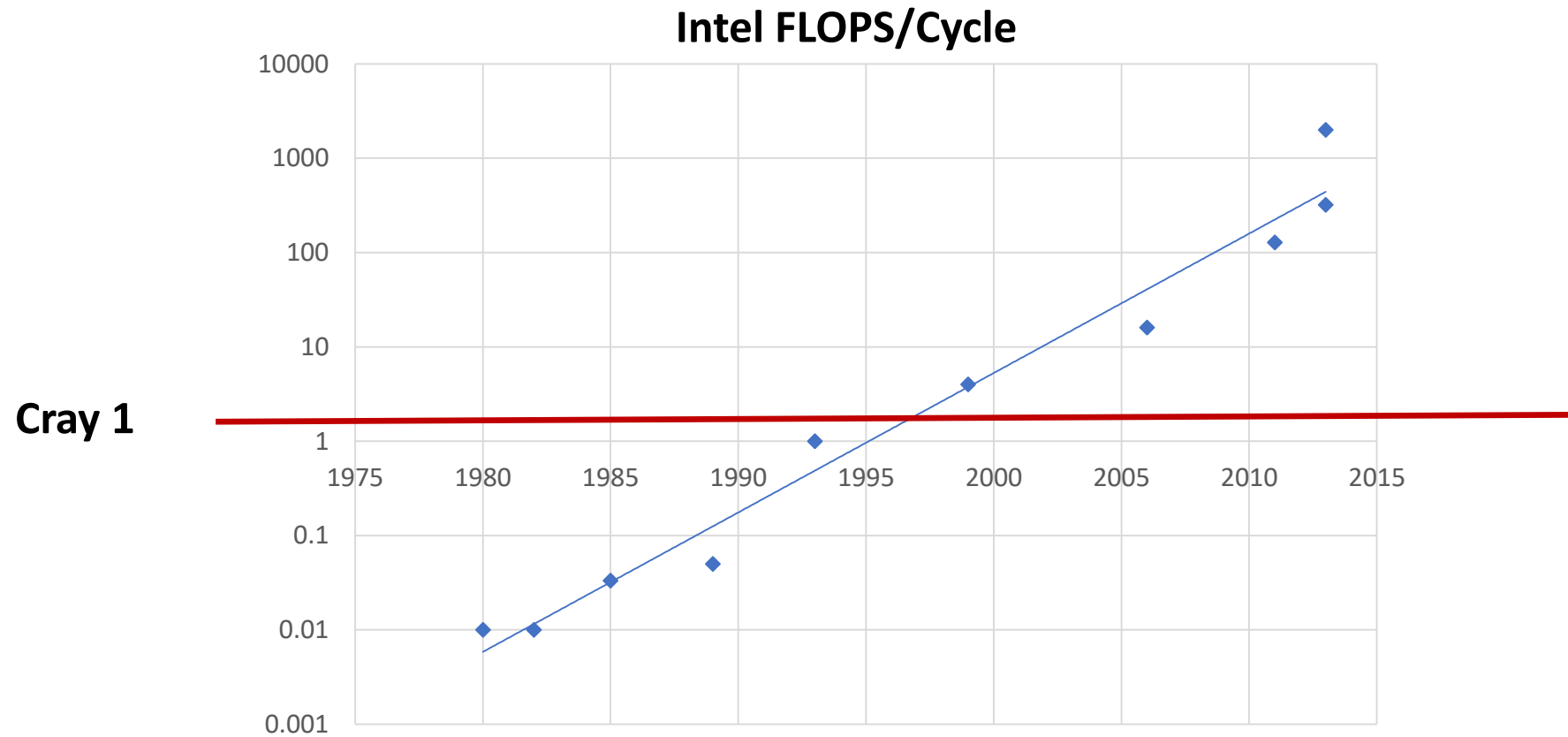
Agenda

Duration	Topics
10 minutes	oneAPI: how we got here, where we are going
40 minutes	Break out sessions
5 minutes	Closing

Welcome and Thanks

- A unique opportunity to steer the parallel programming ecosystem
- A problem worth solving
 - Multi-architecture, avoiding lock-in to 1 specific hardware architecture
 - Direct and library-based programming
 - Extending existing models
 - Performant
- Your leadership, input, and feedback is critical

Moore's Law and compilers



2007: LIBOR loop nest

```
for (path=0; path<npath; path++) {  
    ...  
    for(n=0; n<Nmat; n++) {  
        ...  
        for (i=n+1; i<N; i++) {  
            lam = lambda[i-n-1];  
            con1 = delta*lam;  
            v += (con1*L[i])/(1.0+delta*L[i]);  
            vrat = exp(con1*v + lam*(smez-0.5*con1));  
            L[i] = L[i]*vrat;  
        }  
        ...  
    }  
}
```

Outer loop
parallel

Inner loop
sequential

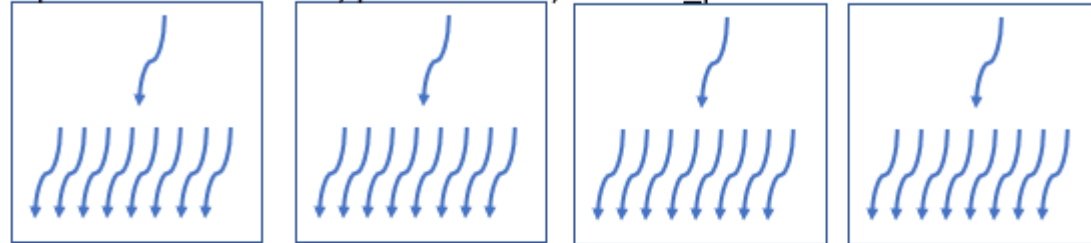
2017: SIMT vs Threads & vectors

CHARMM (Bio) Force-Field from Baseline LAMMPS

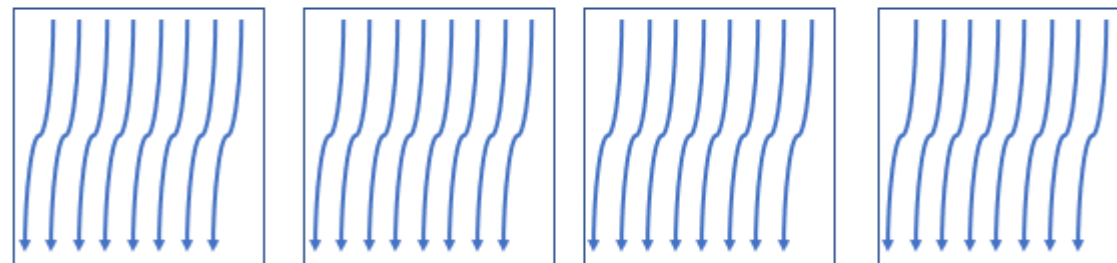
```
for (ii = 0; ii < inum; ii++) {  
  i = ilist[ii];  
  . . .  
  for (jj = 0; jj < jnum; jj++) {  
    j = jlist[jj];  
    . . .  
    if (rsq < cut_bothsq) {  
      . . .  
      if (newton_pair) {  
        f[j][0] -= . . .  
      }  
    }  
  }  
  f[i][0] += . . .  
}
```

	GPU	CPU
1. Inner	92.71%	84.61%
2. Outer	100.00%	84.61%
3. Privatize	66.97%	100.00%
4. Atomic	91.21%	59.14%

Option 1: **Inner** vector, parallel outer, newton_pair == false



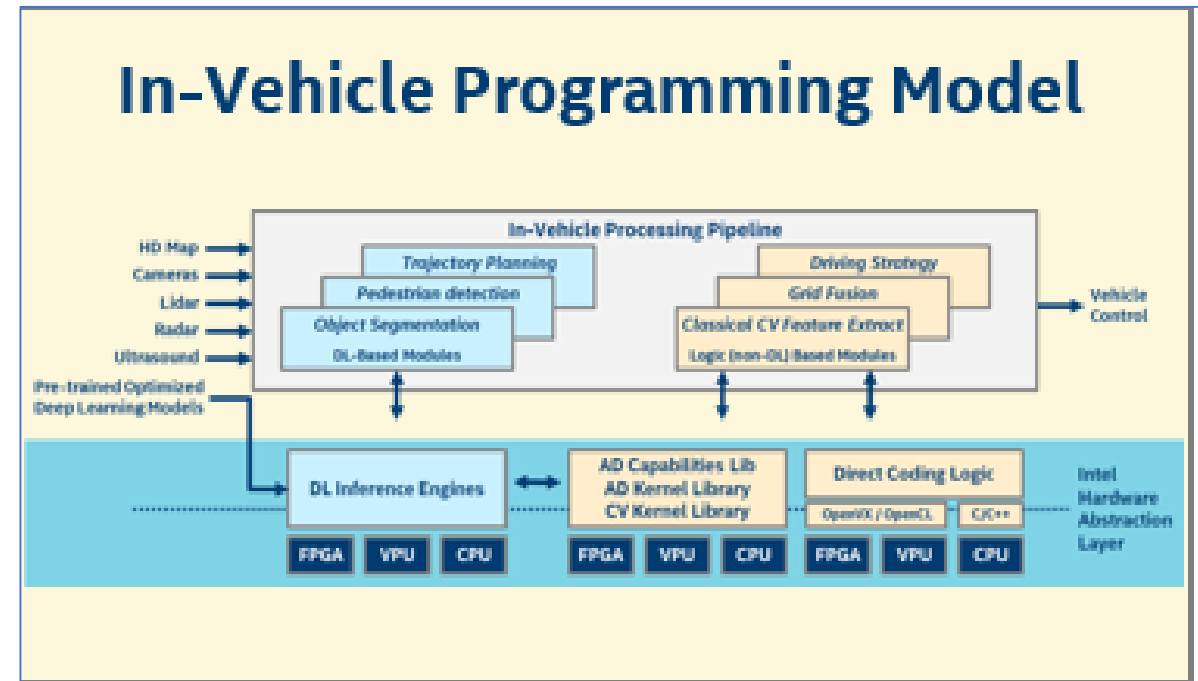
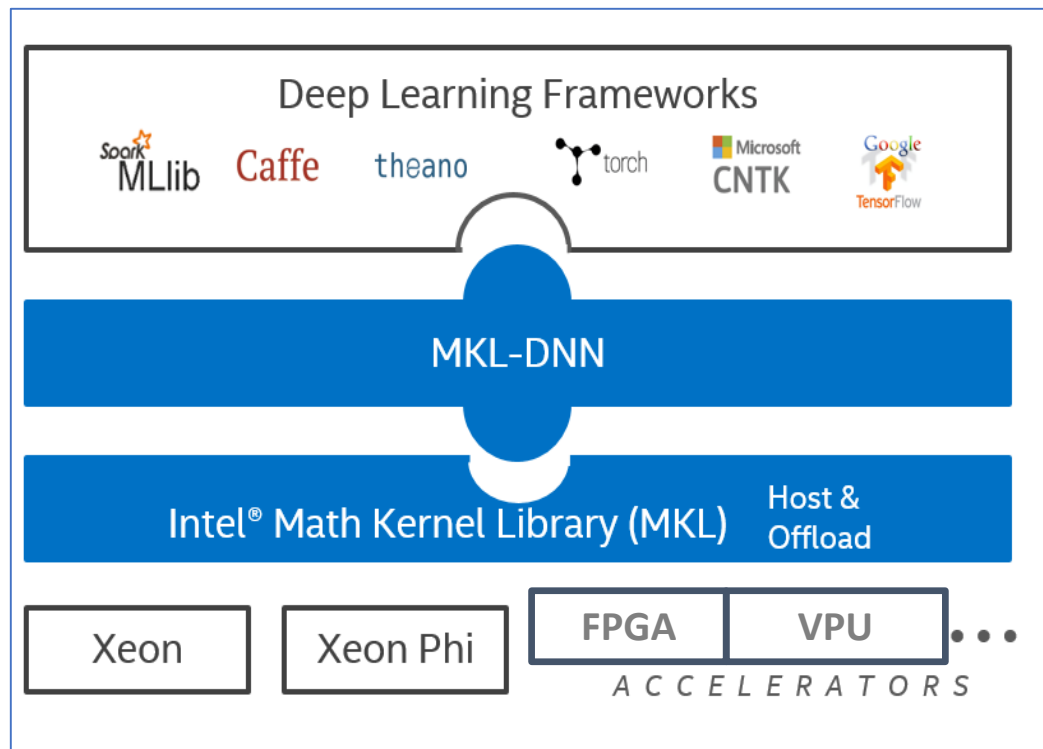
Option 2: **Outer** vector, newton_pair == false



Option 3: **Privatize**, inner vector, parallel outer, newton_pair == true

Option 4: **Atomic**, inner vector, parallel outer, newton_pair == true

2017: API programming and direct programming



2019: oneAPI

ONEAPI INDUSTRY INITIATIVE ALTERNATIVE TO SINGLE-VENDOR SOLUTION

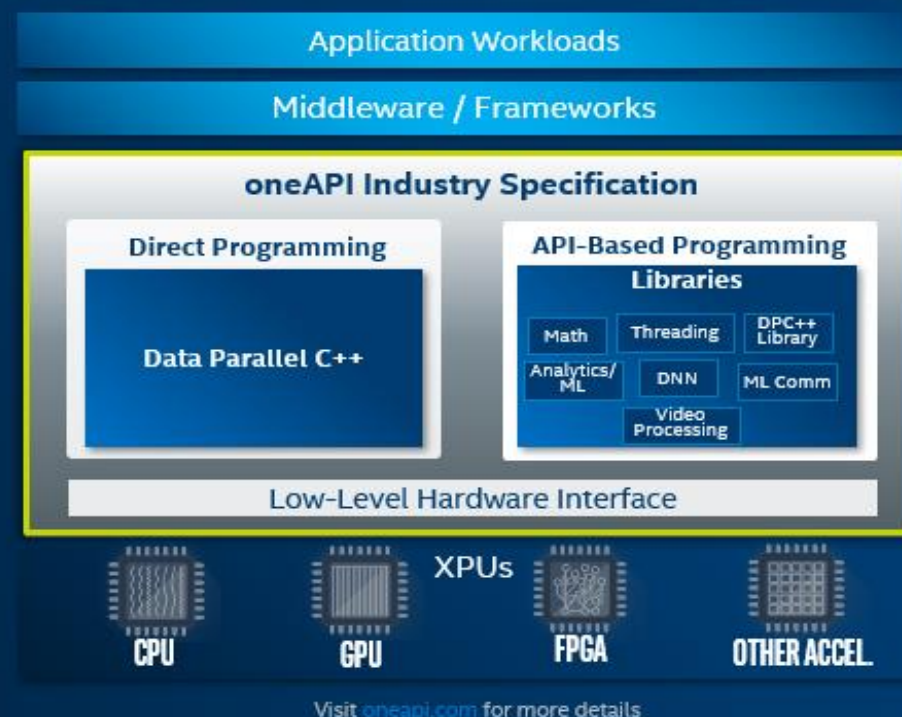
A standards based cross-architecture language, DPC++, based on C++ and SYCL

Powerful APIs designed for acceleration of key domain-specific functions

Low-level hardware interface to provide a hardware abstraction layer to vendors

Open standard to promote community and industry support

Enables code reuse across architectures and vendors



Some capabilities may differ per architecture and custom-tuning will still be required.

Refer to software.intel.com/articles/optimization-notice for more information regarding performance & optimization choices in Intel software products.

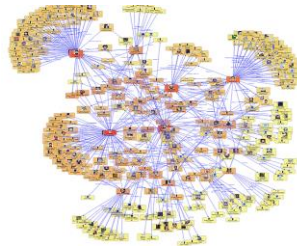
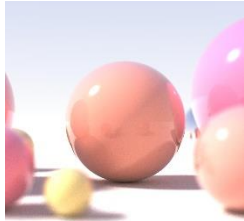
Copyright ©, Intel Corporation. All rights reserved.

*Other names and brands may be claimed as the property of others.



2021: Issues to address

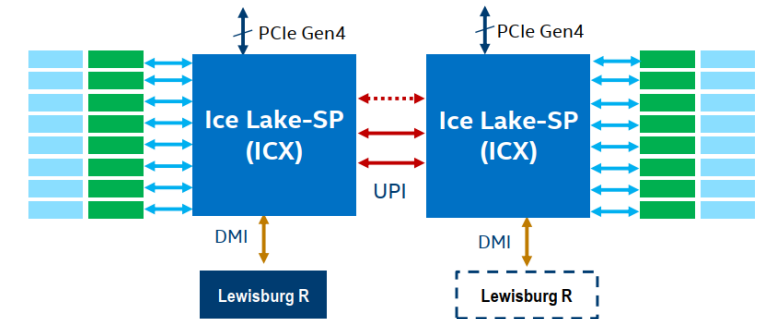
Irregular parallelism



Distributed computing



NUMA



Give the break out information