JoSDC’24 Training

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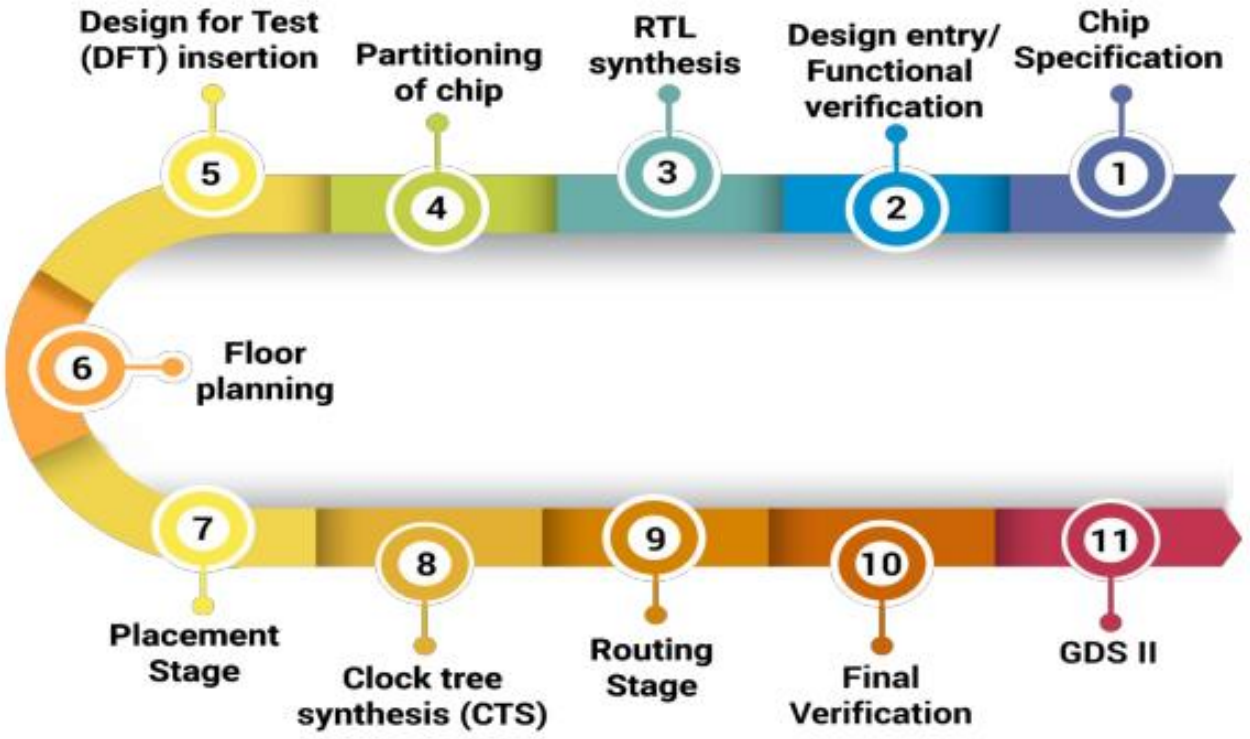
VLSI Design Flow

VLSI Design Flow

- Very-large-scale integration is the process of creating an integrated circuit by combining millions or billions of MOS transistors onto a single chip.



Verilog Hardware Description Language Overview

Background

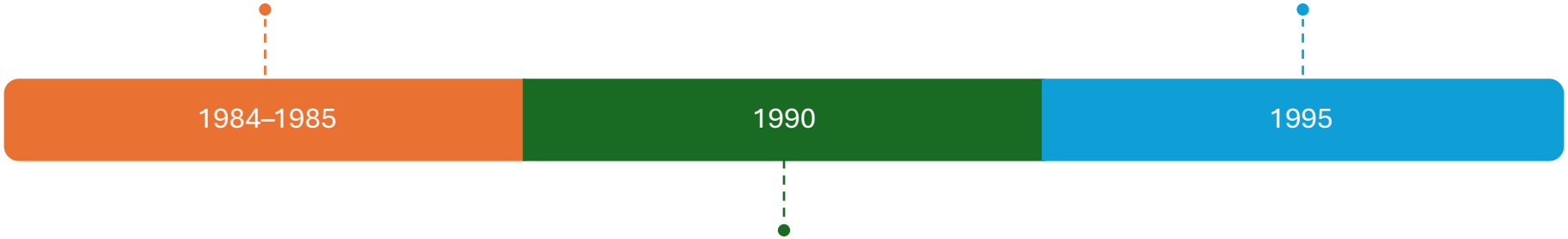
- Modern digital circuits are too complex to be designed using basic logic gates such as AND, OR, NOT gates.

- Hardware Description Languages are languages that had to be developed to use Computer-Aided Design (CAD) tools for the design, implementation, and simulation of complex designs efficiently.

History

Verilog HDL was developed in 1984-1985 as a language for simulation and verification of digital circuits.

In 1995 Verilog became an IEEE standard.



In 1990 Verilog was put into the public domain and became more popular compared with its competitor VHDL.

Describing Digital Circuits in Verilog

Structural:

- Focuses on building blocks using logic gates.

Behavioral:

- Focuses on specifying how the digital circuit should function rather than specifying what the circuit should look like.

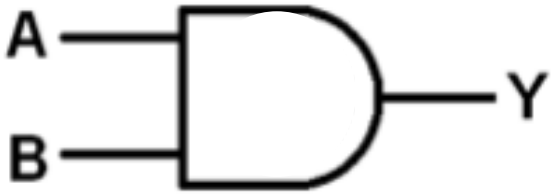
Structural Description

A structural description consists of the interconnection of basic circuit elements such as logic gates.

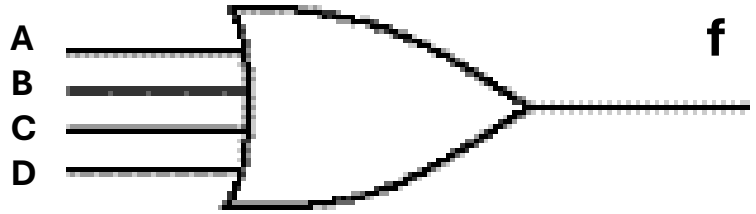
Verilog includes gate-level primitives for AND, NAND, OR, NOR, XOR, XNOR, and NOT.

Structural Description

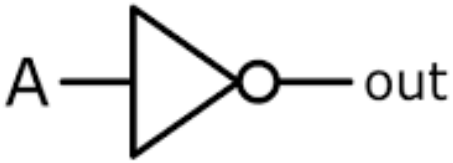
and(Y, A, B);



Or(f, a, b, c, d);

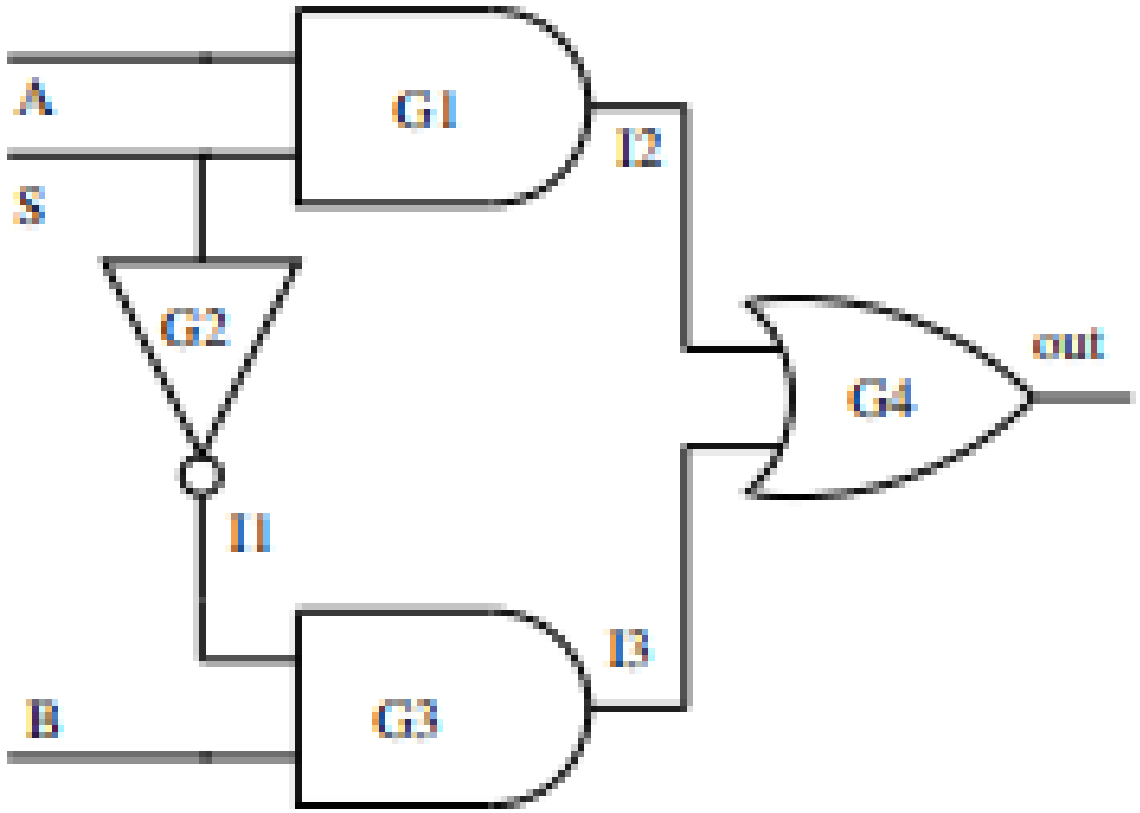


Not(out, A);



Verilog Example- Structural Description

- MUX-Structural form
- EDAPlayground



Solution

```
module MUX(out, A, B, S);
  output out;
  input A, B, S;
  wire I1, I2, I3;

  and G1(I2, A, S);
  and G3(I3, I1, B);
  not G2(I1, S);
  or G4(out, I2, I3);

endmodule
```

Behavioral Description

Instead of describing a circuit using gate-level primitive, it specifies the logic expression that defines the behavior of the circuit.

Uses Continuous or Procedural assignments.

Continuous Assignment

- Adds another level of abstraction in the assignment statement (to a wire or net).

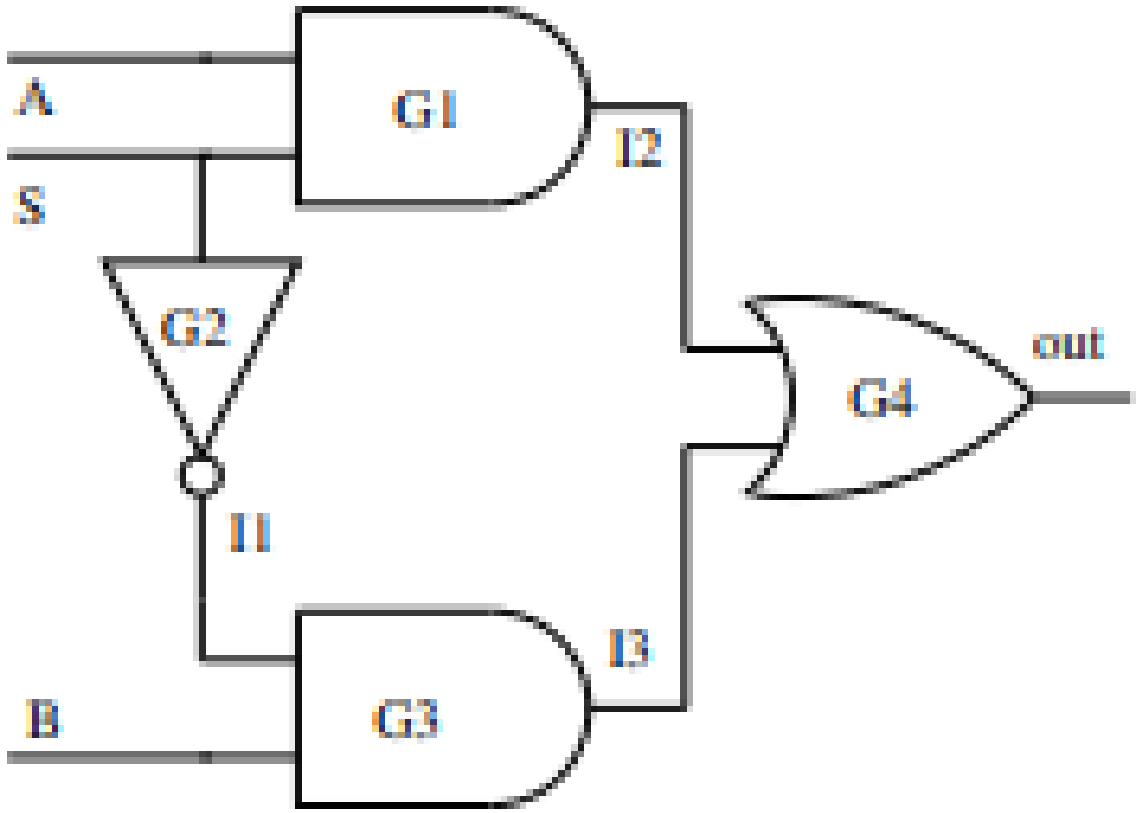
- Whenever the RHS changes, the LHS will be re-evaluated immediately.

- No need to wait for a clock pulse to take effect.

Verilog Example- Structural Description

- MUX-Continuous Assignment form

- EDAPlayground



Solution

```
module MUX(out, A, B, SEL);
  output out;
  input A, B, SEL;

  assign out = SEL ? A : B;

endmodule
```

Procedural Assignment

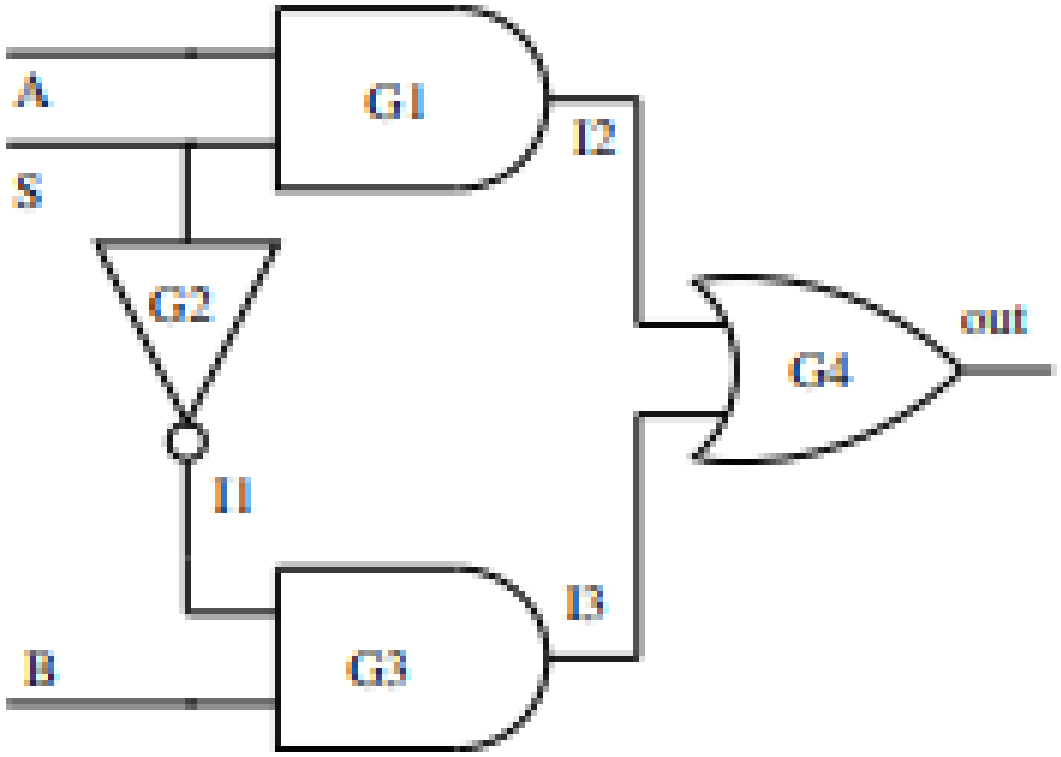
Instead of using Boolean expression use if-else statement (case-statement, while loops, or for loops can be used as well) as a higher level of abstraction.

Procedural assignments are easier when describing large circuits.

Verilog Example- Procedural Assignment

- MUX - Behavioral form

- EDAPlayground



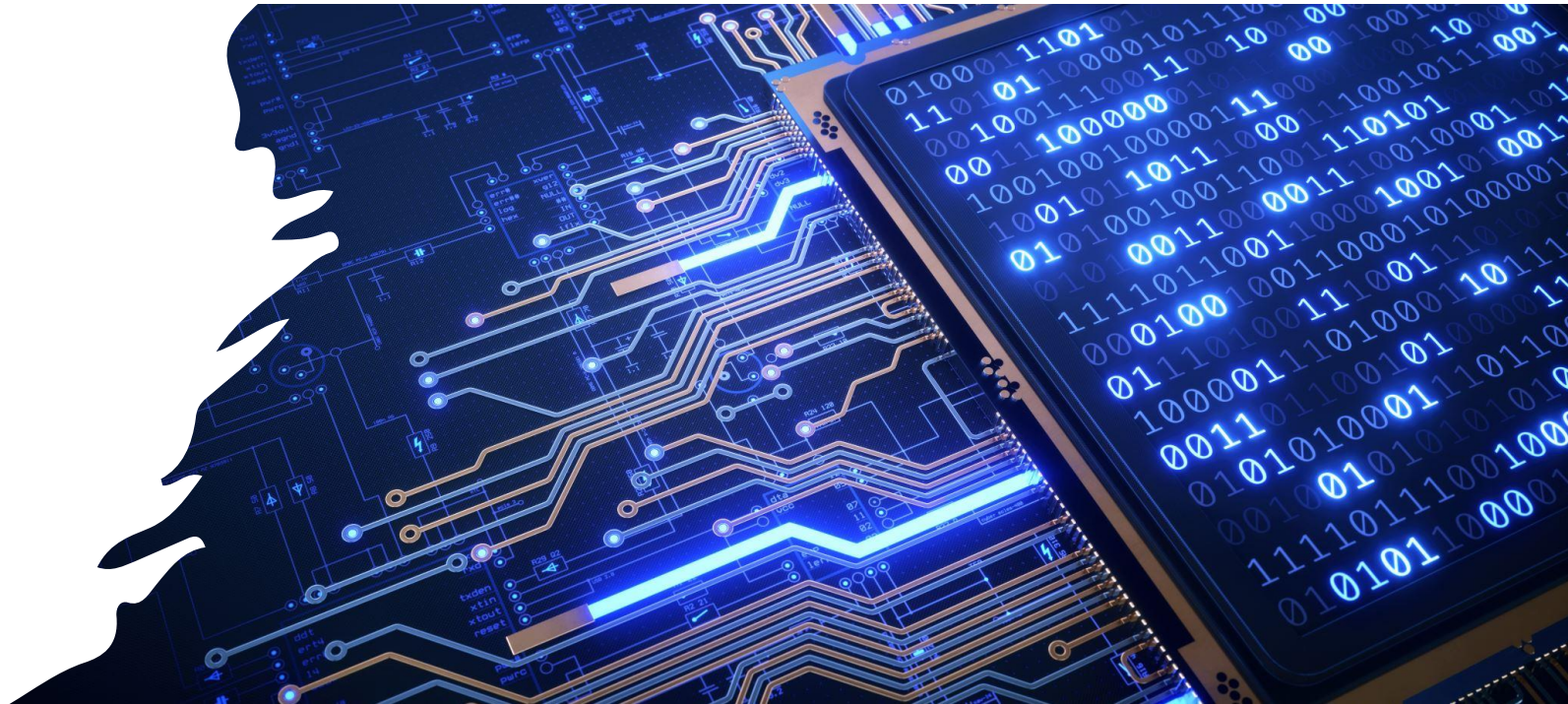
Solution

```
module MUX(out, A, B, SEL);
   output out;
   reg out;
   input A, B, SEL;

   always @(SEL, A, B)
      if(S)
         out=A;
      else
         out=B;

endmodule
```

Introduction to FPGA Design Using Quartus II



What is an FPGA

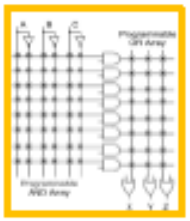
- Field Programmable Gate Array is an Integrated Circuit or chip that allows you to design completely custom digital logic.
- A microcontroller is a purpose-built processor with some peripherals that you can use to connect sensors, motors, lights …etc.
- An FPGA can be used to build your own processor which is called a “soft processor”.
- A soft processor allows you to run code the same as the code you run on a microcontroller or a microprocessor.
- FPGAs are very useful for prototyping. ASICs which stands for Application Specific Integrated Circuits is more cost-effective for mass production.

THE BIRTH OF FPGAs

1970 — First PROM; programmable, but permanent

1971 — First EPROM; erased using UV light

1975 — First PLA; limited to sum of products



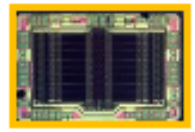
1983 — Altera founded

1983 — EEPROM

1984 — First EPLD; re-programmable CMOS

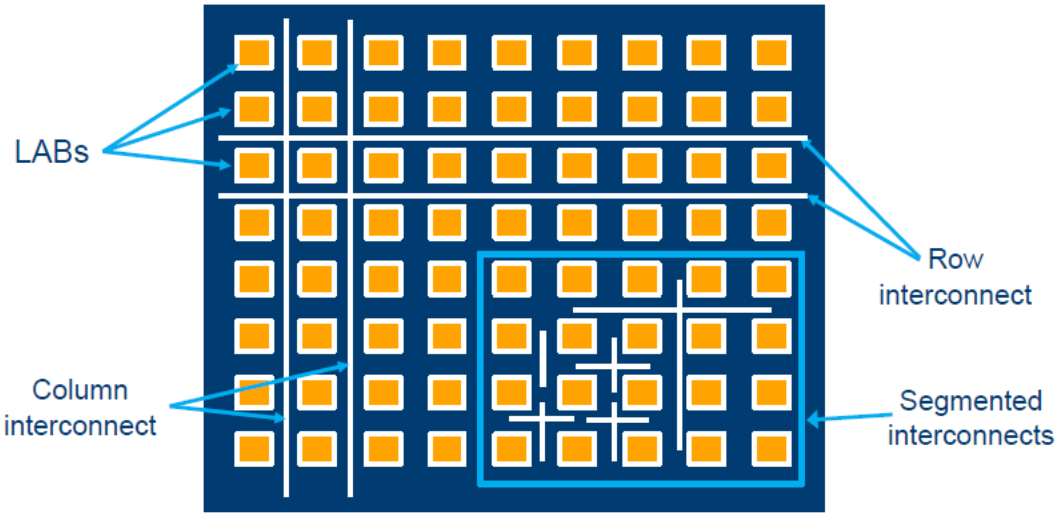
1985 — First FPGA; 64 logic blocks w/ two three-input LUTs

1988 — High-density CPLD; full subsystems



1989 — Altera launches first Integrated graphic design environment

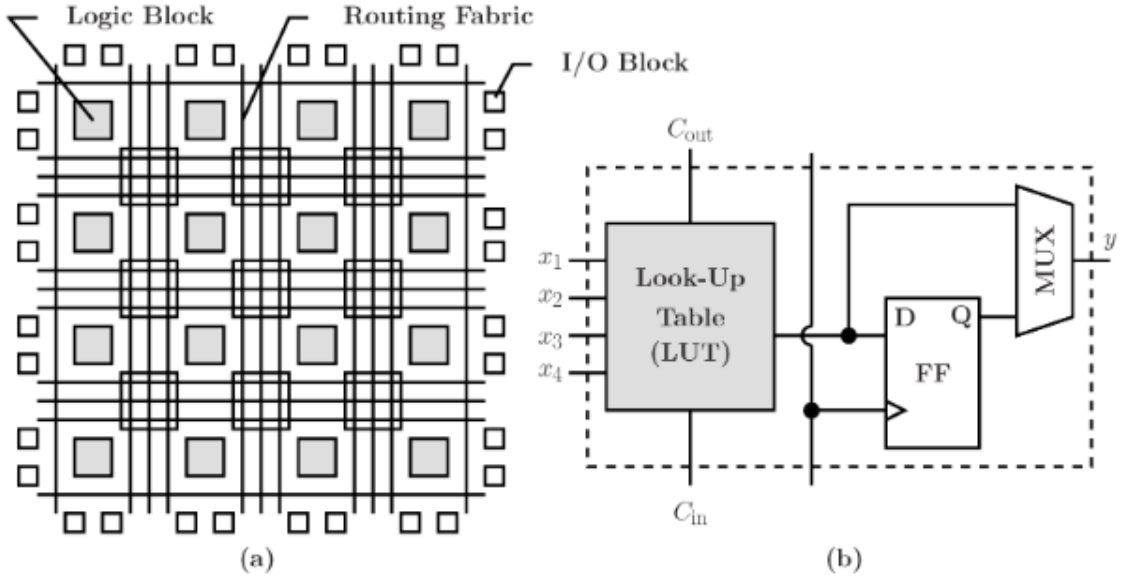
SOURCE: http://www.altera.com/about/company/history.html



FPGA Architecture

- HDL code is synthesized to run on an FPGA.
- Synthesis is the process of mapping this code into a physical hardware block.
- These hardware blocks consist of registers and logic gates.
- FPGA implements logic gates into look-up tables or LUTs.
- So, if you put up a bunch of look-up tables and make them programmable and then you add a switching fabric that can connect them all together, then allow the used to re-program the LUTs to whatever they want, now we have a single device that can run our code called FPGA.

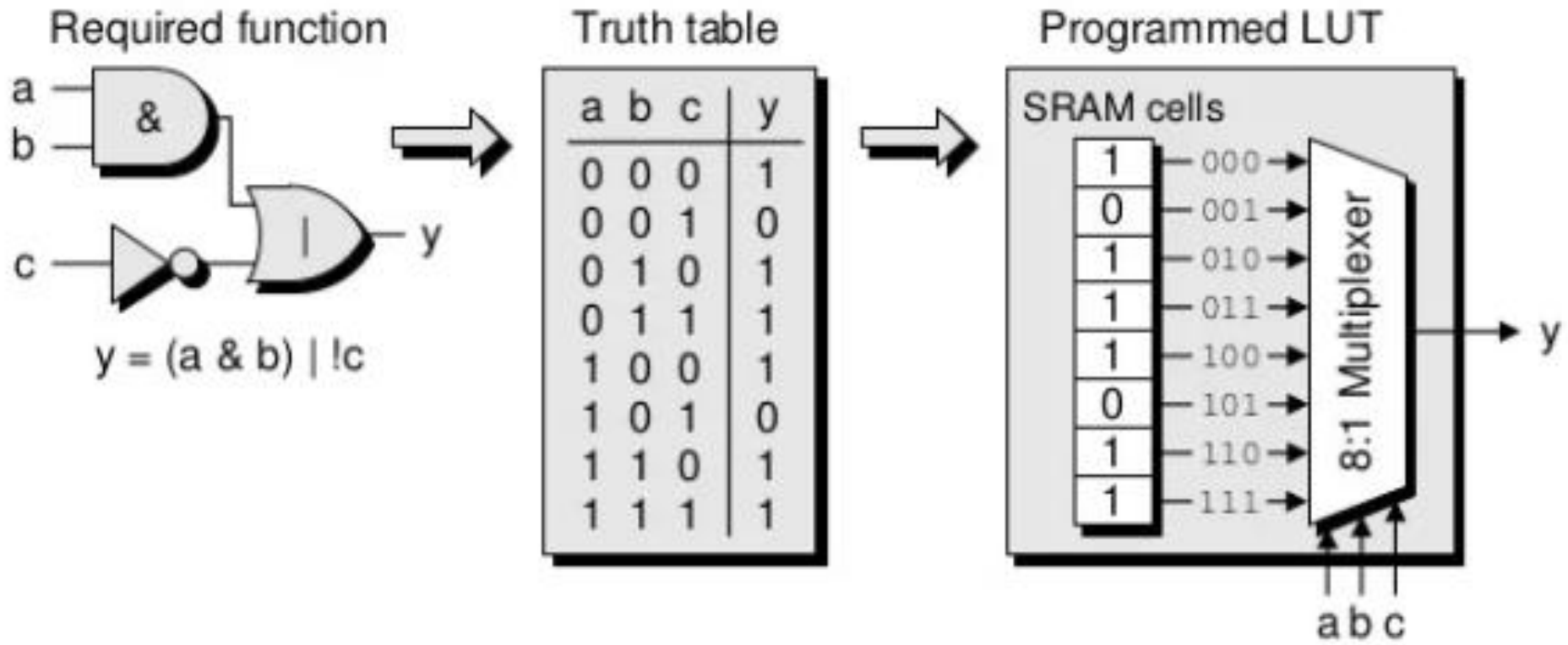
FPGA Architecture



Topology of an FPGA (a), CLB (b)

- The most common FPGA block, called configurable logic block - CLB
- CLB consists of logical cells that can be configured to perform combinatorial functions,
- I/O blocks are also implemented to allow the FPGA to communicate with the outside world.

CLB LUT Programming

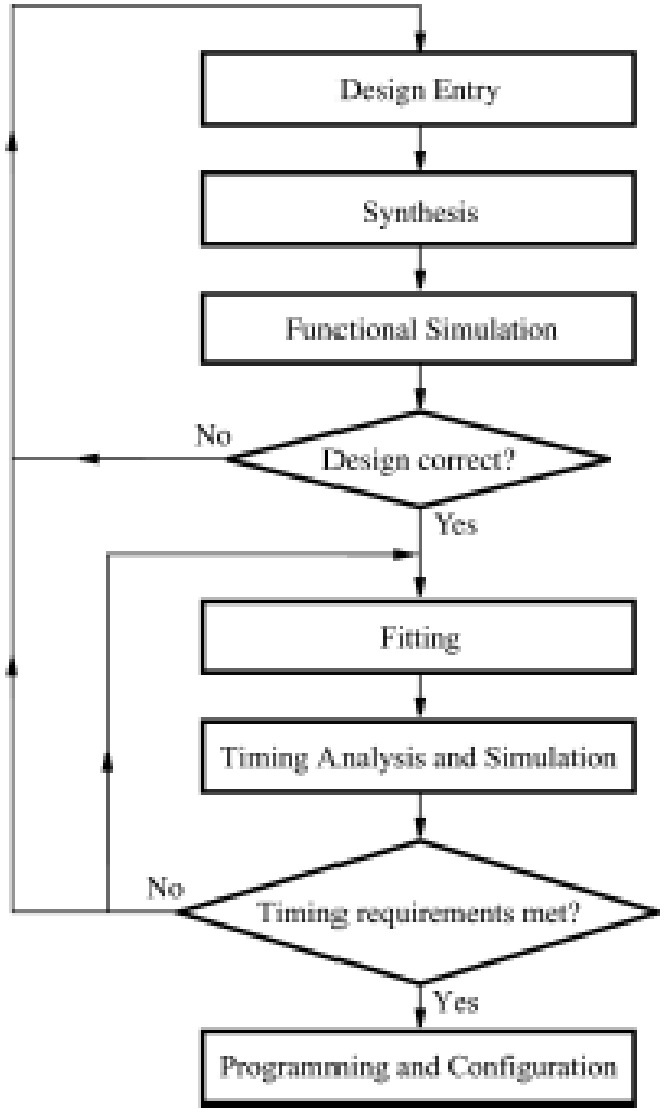


Describing Digital Circuits

- Schematic
- Hardware Description Languages (HDL) – Verilog or VHDL
- High Level Synthesis (HSL):
  - Automatically convert functional design to RTL.
  - C, C++, MATLAB, …etc.
- System Verilog:
  - Extends functionality of Verilog-2005
  - Adds features for testing/verification(testbenches)

FPGA Design Flow

- Design Entry – HDL coding
- Synthesis – the design is mapped into a circuit that consists of the logic elements (LEs) provided in the FPGA.
- Functional Simulation – Test if the design is functionally correct.
- Fitting – Placement & Routing.
- Timing Analysis – propagation delays along the various paths in the fitted circuit are analyzed.
- Timing Simulation – The fitted circuit is tested to verify both its functional correctness and timing.
- Programming and Configuration – The designed circuit is implemented in a physical FPGA chip by programming the configuration switches that configure the LEs and establish the required wiring connections.



DE-Lite Max 10 series