Midterm Exam- Key

Course Title	**Advanced computer architecture**		**Course Code**	**ELE5467**	
Semester	**Second**		**Academic Year**	**2022/2023**	
Exam Date	**10/05/2023**	**Day**	**Monday**	**Time**	**9:00-9:50**

Student Name		**Student ID No.**		**Section**	

GENERAL INSTRUCTIONS

1. Students are not allowed to leave the exam room during the first 30 minutes of the exam.
2. Late students are not permitted to complete their exams after the first 30 minutes unless authorized by the proctor (no students left the exam session), knowing that no additional time will be granted.
3. Students must use a blue or black pen. Pencils are not allowed.
4. Consumption of any food or beverage is prohibited except in medical cases.
5. All electronic devices (e.g., cell phones) are prohibited.
6. All cell phones must be turned off and placed on the invigilator's desk in the exam room.
7. All notes and reading materials must be placed on the invigilator's desk in the exam room.
8. Students are not permitted to speak to or ask questions of their classmates. If a student has a question, he or she must raise his or her hand to be assisted by the proctor.
9. Write the full information required on this page before commencing your exam.
10. Students are not allowed to leave the room once the exam commences for any reason unless it is absolutely necessary.
11. Reported student cheating cases, misbehavior, or other student misconduct on examination sessions will be reported to the Investigations Committee as per internal bylaws.

I have understood and abide with the exam policy. **Student's signature:** _____

Question No.	Question Type	CILOs assessed	Marks Weight	Scored Marks	Marker signature	Student Score
1	Multiple Choice	CLIO 1	10(33.33%)			
2	Essay	CLIO 2, 4, 6	6(20%)			
3-A	Essay	CILO 3, 5	8(26.67%)			
3-B			6(20%)			
Total			30(100%)			

Moderation Review					
Comments					
Marks Reviewed by				**Signature & Date**	

Problem # 1: Multiple choice question. **[10 x 1pt]**

****** Assuming the number of dies per area is 200, wafer yield is 100%, manufacturing complexity is 2, wafer area is 314 cm^2, and defect density is 0.3 per cm^2. Answer questions 1 and 2:

1) The die yield is .....
A. 0.93
B. 0.85
C. 0.66
D. None of the above

Sol:

$$Die\ area = \frac{wafer\ area}{dies\ per\ wafer\ area} = \frac{314}{200} = 1.57$$

$$Die\ yield = Wafer\ yield\ x\ [1 + \frac{Defects\ per\ unit\ area\ \ x\ Die\ area}{\alpha}]^{-\alpha} =$$

$$1\ x\ [1 + \frac{0.3\ per\ cm^2\ \ x\ 1.57}{2}]^{-2} = [1 + \frac{0.471}{2}]^{-2} = [1 + 0.2355]^{-2} = [1.2355]^{-2} = \frac{1}{(1.2355)^2} = 0.66$$

2) The number of defected dies is .....
A. 132
B. 68
C. 200
D. None of the above

Sol:

Number of defected dies = Dies per wafer area x (1- Die yield) = 200 x (1-0.66) = 200 x 0.34 = 68

3) If a computer has a clock rate of 200 MHz, how long does it take to execute a program with 200,000 instructions, if the CPI for the program is 2.5?
A. 2.5 ms
B. 10 ms
C. 5 ms
D. None of the above

Sol: **Cycle time = 1/clock_rate = 1/200MHz = $1/(200*10^6) = 0.5 * 10^{-8} = 5ns$**

CPU time = CP1 * Instruction count * cycle time = $2.5 * 200{,}000 * 5ns = 25 * 10^{-4}$ s
$= 2.5 * 10^{-3}$ second = 2.5ms

4) If a computer has a clock rate of 100 MHz, then the clock cycle time is ……
A. 0.1 ns
B. 0.01 ns
C. 1 ns
D. None of the above

Sol: Clock cycle time = $\frac{1}{clcokc\ rate} = \frac{1}{100\ MHz} = \frac{1}{100\ x\ 10^6} = \frac{1}{10^8} = 1 \times 10^{-8} = 0.1 \times 10^{-9} = 0.1ns$

5) Floating point instructions are improved to run 4 times as fast, but only 35% of the time was spent on these instructions originally. How much faster is the new machine?
A. 35.6%
B. 4.3%
C. 43.7%
D. None of the above

Sol:

$$Speedup = \frac{1}{(1 - Fraction_{enhanced}) + \frac{Fraction\_enhanced}{Speedup\_enhanced}}$$

$$Speedup = \frac{1}{(1-0.35)+\frac{0.35}{4}} = \frac{1}{0.65+0.0875} = \frac{1}{0.7375} = 1.356$$

The new machine is 1.356 times as fast, or 35.6% faster.

6) Million Instructions Per Second (MIPS) and Million Floating Point Operations Per Second (MFLOPS) are accurate indicators of performance.
A. True
B. False

Sol: MIPS and MFLOPS are easy to use, but inaccurate indicators of performance.

7) Throughput is the number of tasks completed per unit of time.
A. True
B. False

******* Consider two different computers A and B, with two different instruction sets, both of which have a clock rate of 200 MHz, the following measurements are recorded on the two computers running a given set of benchmark programs. Answer questions 8, 9, and 10:

	Instruction type	Instruction count (millions)	Cycles per instruction
Computer A	Arithmetic and logic	8	1
	Load and store	4	3
	Branch	2	4
	Others	4	3
Computer B	Arithmetic and logic	10	1
	Load and store	8	2
	Branch	2	4
	Others	4	3

8) The Cycle Per Instruction (CP1) of computer B is ……

A. 2.22
B. 3.4
C. 1.92
D. None of the above

Sol: $CPI_B = \frac{Total\ clock\ cycles\ of\ B}{Instruction\ count\ of\ B} = \frac{10m \times 1cc + 8m \times 2cc + 2m \times 4cc + 4m \times 3cc}{10m+8m+2m+4m} =$

$= \frac{46\ million\ clock\ cycles}{24\ million\ instrcutions} = 1.92$

9) The Millions of Instructions Per Second (MIPS) of computer A is ……

A. 104
B. 90
C. 80
D. None of the above

$CPI_A = \frac{Total\ clock\ cycles\ of\ A}{Instruction\ count\ of\ A} = \frac{8m \times 1cc + 4m \times 3cc + 2m \times 4cc + 4m \times 3cc}{8m+4m+2m+4m} =$

$= \frac{40\ million\ clock\ cycles}{18\ million\ instrcutions} = 2.2222$

$MIPS_A = \frac{Instruction\ count\ of\ A}{Execution\ time\ of\ A\ X\ 10^6} = \frac{Instructio\ count\ of\ A}{(CPI_A\ X\ Instruction\ count\ of\ A\ x\ clock\ cycle\ tim\ of\ A)\ X\ 10^6} =$

$$\frac{1}{CPI_A\ X\ clock\ cycle\ tim\ X\ 10^6} = \frac{1}{2.2222}\ X\ clock\ rate\ x\ 10^{-6}$$

$$= 0.45\ X\ 200MHz\ x\ 10^{-6} = 0.45\ x\ 200\ x\ 10^6\ x\ 10^{-6} = 90$$

10) The execution time of machine B is ……

A. 0.31 second
B. 0.42 second
C. 0.23 second
D. None of the above

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$$Execution\ time\ of\ B = CPI_B\ X\ Instruction\ count\ of\ B\ X\ clock\ cycle\ tim\ of\ B$$
$$= 1.92\ X\ 24\ million\ instructions * \left(\frac{1}{clock\ rate\ of\ B}\right)$$
$$= 1.92\ x\ 24\ x\ 10^6 * \left(\frac{1}{200MHz}\right) = 1.92\ x\ 24\ x\ 10^6\ x\ \left(\frac{1}{200\ x\ 10^6}\right)$$
$$= 0.23\ second$$

*** Write the correct answers to problem # 1 in the table below:

Q1	Q2	Q3	Q4	Q5	Q6	Q7	Q8	Q9	Q10
C	B	A	A	A	B/F/False	A/T/True	C	B	C

Problem # 2: Compare the Reduced Instruction Set Computer (RISC) and the Complex Instruction Set Computer (CISC) processor architectures in terms of the following **[24 x 0.25 pt]**

	RISC	CISC
Number of registers	It requires more registers	It requires less number of registers
Number and complexity of addressing modes	Simple and limited addressing modes	Complex and more addressing modes
Required RAM space	RISC required more RAM	CISC required less RAM
How is the CPU performance or the execution time improved?	It reduces the cycles per instruction and does so at the cost of the total number of instructions per program	It tries to minimize the total number of instructions per program, and it does so at the cost of increasing the total number of cycles per instruction

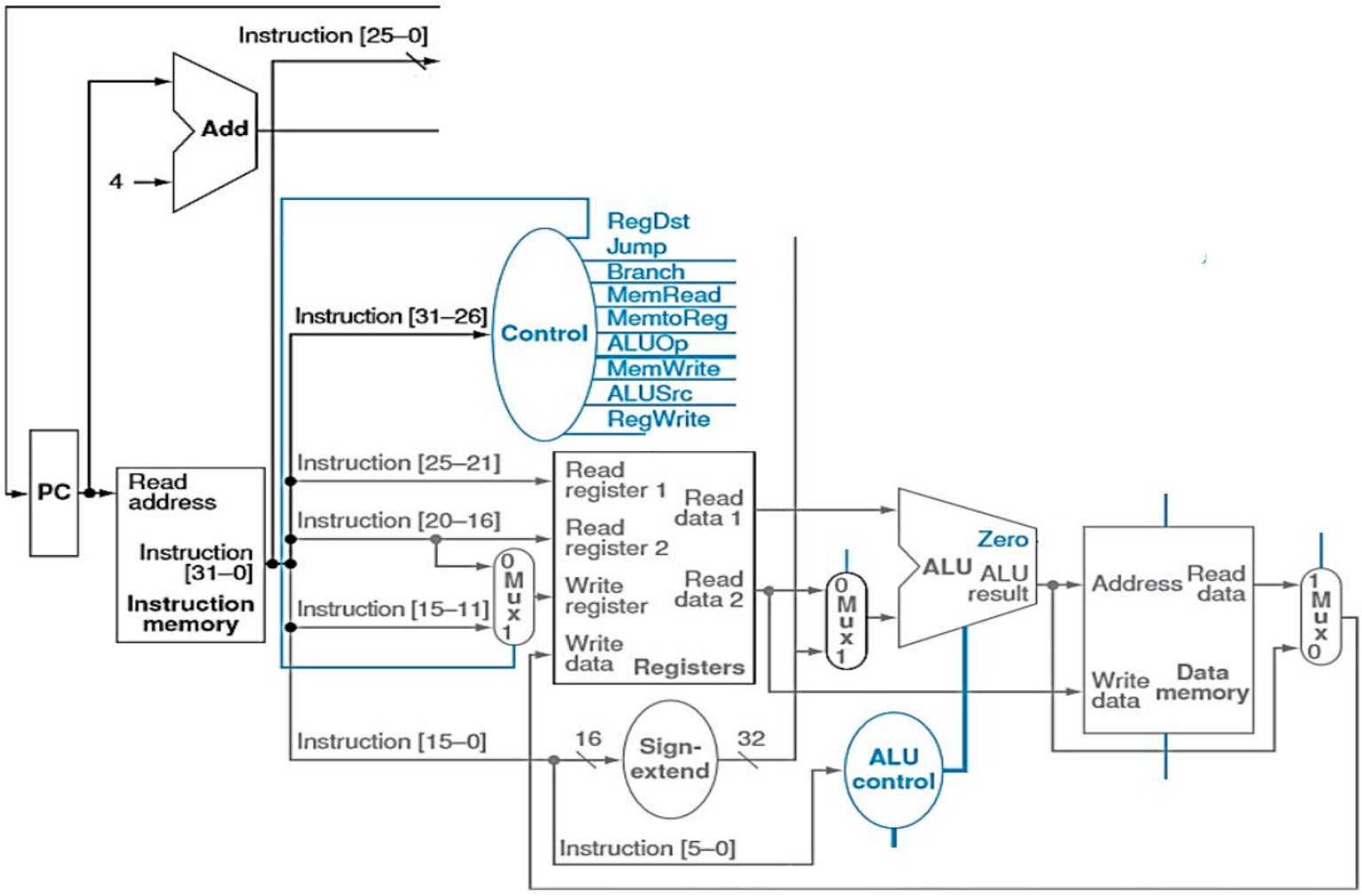
The possibility of Implement Instruction pipelining	The pipeline can be easily achieved	Since CISC devices take more time to execute a single operation, the architecture does not support the parallel processing and pipelining of instructions.
Emphasis on hardware or software	Emphasis/focus on Hardware	Emphasis/focus more on Software
Number of cycles per instruction to get executed	- The instruction takes one clock cycle in order to get executed - Instruction size is mostly varied in size.	- The instruction may take more than one clock cycle in order to get executed - Instruction size is always a set size.
The complexity of instruction decoding	Fast to decode	Difficult to decode
Length of instructions	- An instruction fits in one word - Fixed-length instruction formats	- Instructions are larger than the size of one word - Variable-length instruction formats.
The instructions that are allowed to access memory	- Memory access limited to load and store instructions. - - No memory-to-memory transfers.	- Memory-to-memory: ''Load'' and ''Store'' incorporated in intrusions - The Move operation in CISC has wider scope.

	- Register to register: ''Load'' and ''Store'' are independent instructions.	The CISC instructions can "directly access memory operands".
Power efficiency	It consumes low power.	It consumes more/high power.
Number of transistors	Due to less complex command, it requires fewer transistors of hardware than the complex Instructions.	it requires more transistors of hardware than the reduced Instructions.

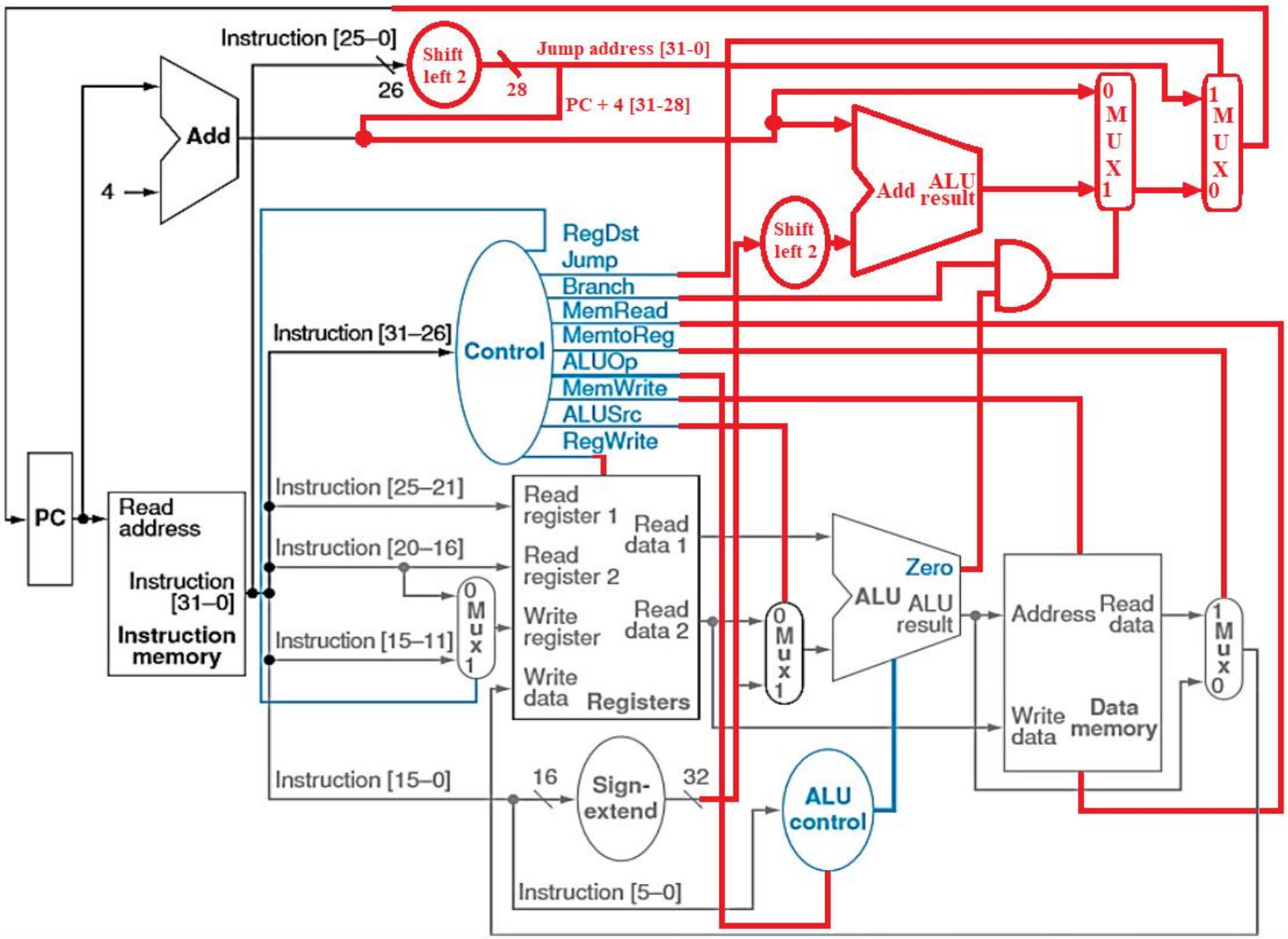
Problem # 3: Answer the following questions:

A- Complete the below single-cycle datapath and control for MIPS processors to work with the following R, I, and J format instructions. **[8pts]**

add $rd, $rs, $rt
lw $rt, immed($rs)
sw $rt, immed($rs)
beq $rs, $rt, immed
J targaddr



Sol: The functional units and the connections in the red color are missing parts to complete the single-cycle MIPS datapath and control



B- Determine the values of the control signals in the table below in case of the load (lw), store (sw), branch (beq), and, set on less than (slt), Jump (J) instructions for the single-cycle MIPS architecture datapath. **[6pts]**

		Instruction					
		lw	sw	beq	and	slt	J
Control signal	RegDst	**0**	**X**	**X**	**1**	**1**	**X**
	ALUSrc	**1**	**1**	**0**	**0**	**0**	**X**
	MemToReg	**1**	**X**	**X**	**0**	**0**	**X**
	RegWrite	**1**	**0**	**0**	**1**	**1**	**0**
	MemRead	**1**	**0**	**0**	**0**	**0**	**0**
	MemWrite	**0**	**1**	**0**	**0**	**0**	**0**
	Branch	**0**	**0**	**1**	**0**	**0**	**X**
	ALUOp1	**0**	**0**	**0**	**1**	**1**	**X**
	ALUOp2	**0**	**0**	**1**	**0**	**0**	**X**
	Jump	0	0	**0**	**0**	**0**	**1**

Note: Both AND and SLT are R-type instructions.

Good Luck