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ASSIGNMENT - 8

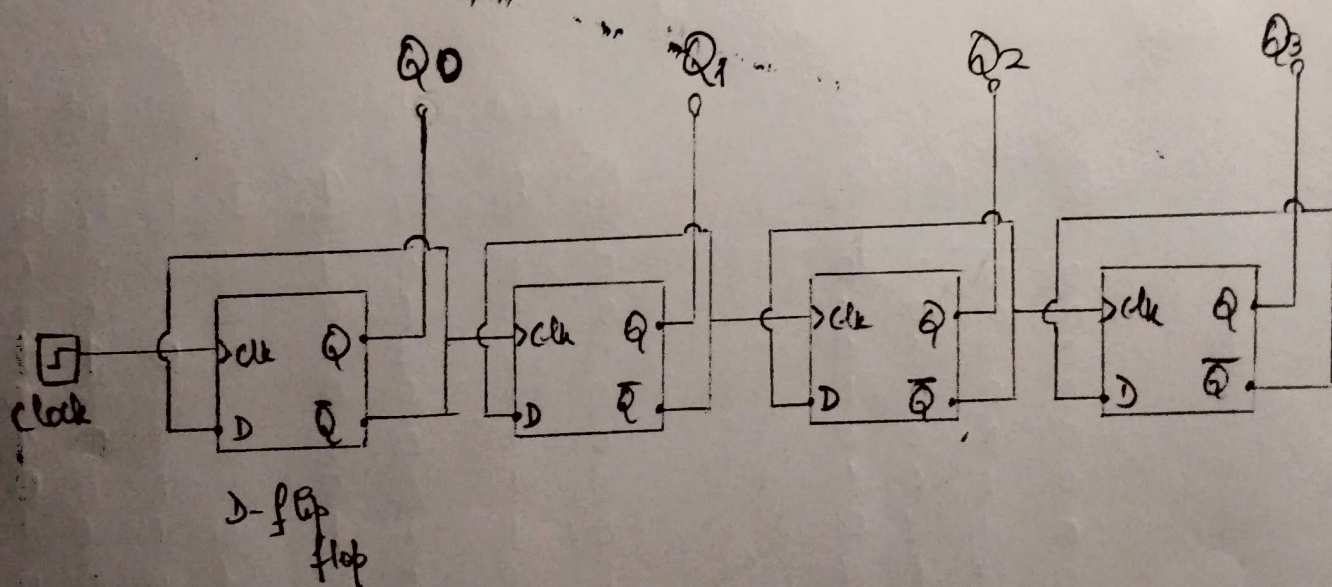
4 bit up and down counters

Submitted by - Sec B
S20210010027
Ameshtan Saxena

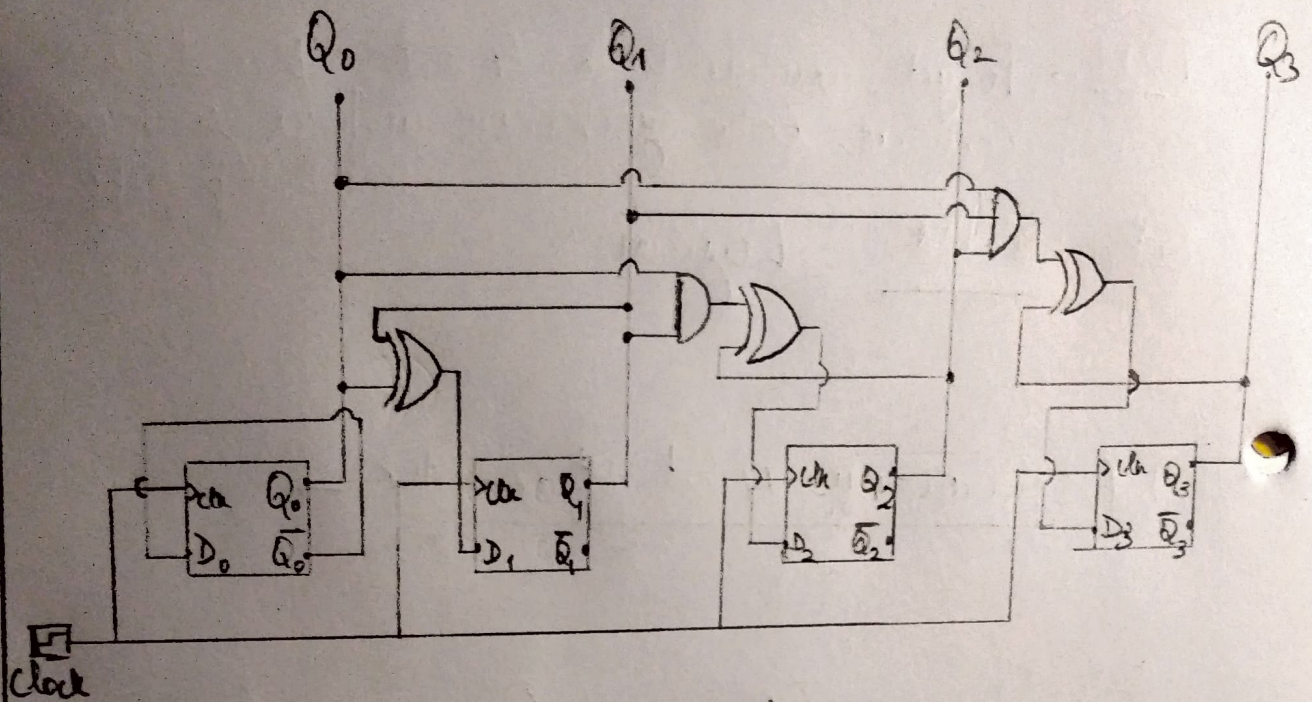
AIM → To get familiar with 4 bit up and down counters, both synchronous and asynchronous, made with D-flip flops

SOFTWARE USED → Logisim.

(I) Asynchronous 4 bit up counter →



II Synchronous 4 bit up Counter →



				Next state				D flip flop input			
Q_3	Q_2	Q_1	Q_0	Q_3^+	Q_2^+	Q_1^+	Q_0^+	D_3	D_2	D_1	D_0
0	0	0	0	0	0	0	1	0	0	0	1
0	0	0	1	0	0	1	0	0	0	1	0
0	0	1	0	0	0	1	1	0	0	1	0
0	0	1	1	0	1	0	0	0	1	0	0
0	1	0	0	0	1	0	1	0	1	0	0
0	1	0	1	0	1	1	0	0	1	1	0
0	1	1	0	0	1	1	1	0	1	1	1
0	1	1	1	1	0	0	0	1	0	0	0
1	0	0	0	1	0	0	1	1	0	0	1
1	0	0	1	1	0	1	0	1	0	1	0
1	0	1	0	1	0	1	1	1	0	1	1
1	0	1	1	1	1	0	0	1	1	0	0
1	1	0	0	1	1	0	1	1	1	0	1
1	1	0	1	1	1	1	0	1	1	1	0
1	1	1	0	1	1	1	1	1	1	1	1
1	1	1	1	0	0	0	0	0	0	0	0
0	0	0	0								

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D₃

$Q_3 Q_2$ \ $Q_1 Q_0$	00	01	11	10
00				
01			1	
11	1	1		1
10	1	1	1	1

$$\begin{aligned}
 D_3 &= Q_3 \bar{Q}_2 + Q_3 \bar{Q}_1 + Q_3 \bar{Q}_0 + \bar{Q}_3 Q_2 Q_1 Q_0 \\
 &= Q_3 [(\bar{Q}_2 + \bar{Q}_1 + \bar{Q}_0)]' + \bar{Q}_3 Q_2 Q_1 Q_0 \\
 &= Q_3 [Q_2 Q_1 Q_0]' + \bar{Q}_3 Q_2 Q_1 Q_0
 \end{aligned}$$

$$\underline{D_3 = Q_3 \oplus Q_2 Q_1 Q_0}$$

D₂

$Q_3 Q_2$ \ $Q_1 Q_0$	00	01	11	10
00			1	
01	1	1		1
11	1	1		1
10			1	

$$\begin{aligned}
 D_2 &= Q_2 \bar{Q}_0 + Q_2 \bar{Q}_1 + \bar{Q}_2 Q_1 Q_0 \\
 &= Q_2 [(\bar{Q}_0 + \bar{Q}_1)]' + \bar{Q}_2 Q_1 Q_0 \\
 &= Q_2 [Q_1 Q_0]' + \bar{Q}_2 Q_1 Q_0
 \end{aligned}$$

$$\underline{D_2 = Q_2 \oplus Q_1 Q_0}$$

D₁

$Q_3 Q_2$ \ $Q_1 Q_0$	00	01	11	10
00		1		1
01		1		1
11		1		1
10		1		1

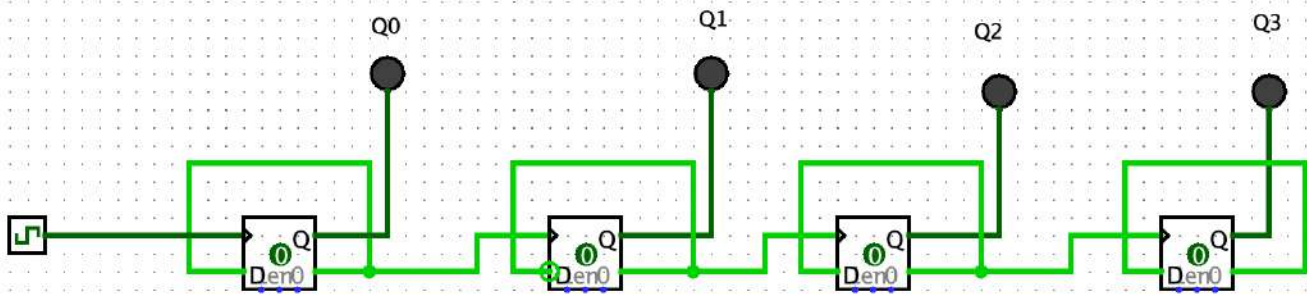
$$D_1 = \bar{Q}_1 Q_0 + Q_1 \bar{Q}_0$$

$$\underline{D_1 = Q_1 \oplus Q_0}$$

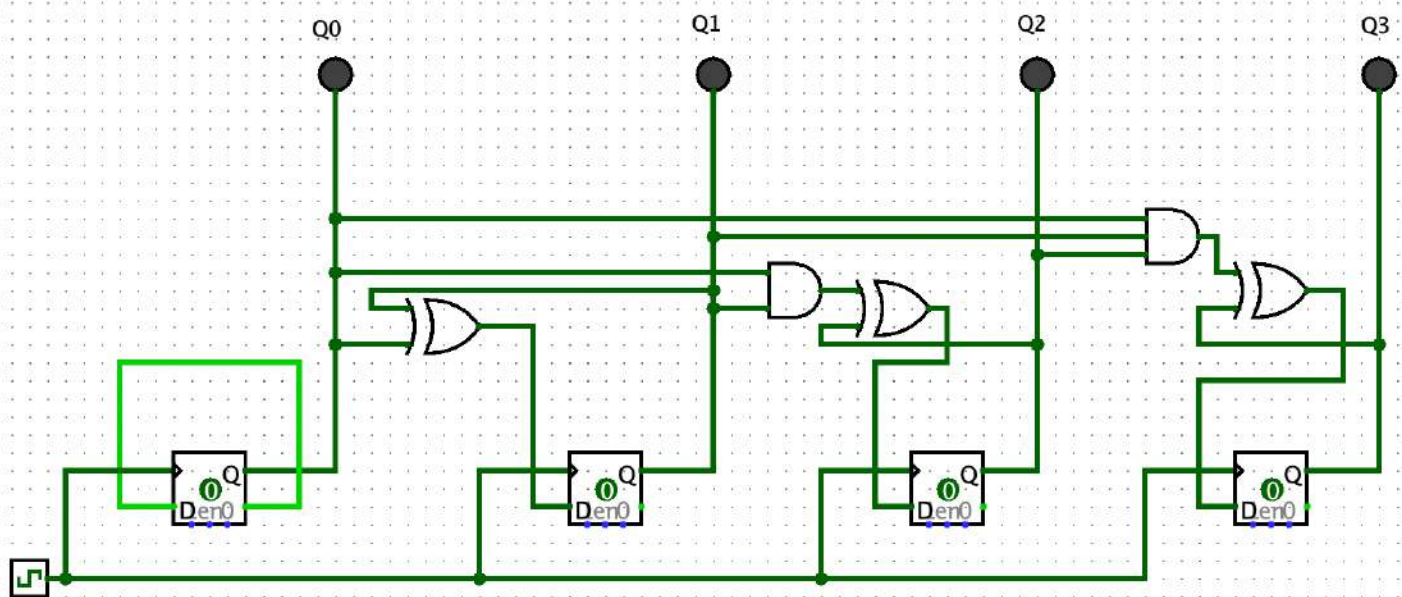
D₀

$Q_3 Q_2$ \ $Q_1 Q_0$	00	01	11	10
00	1			1
01	1			1
11	1			1
10	1			1

$$\underline{D_0 = \bar{Q}_0}$$



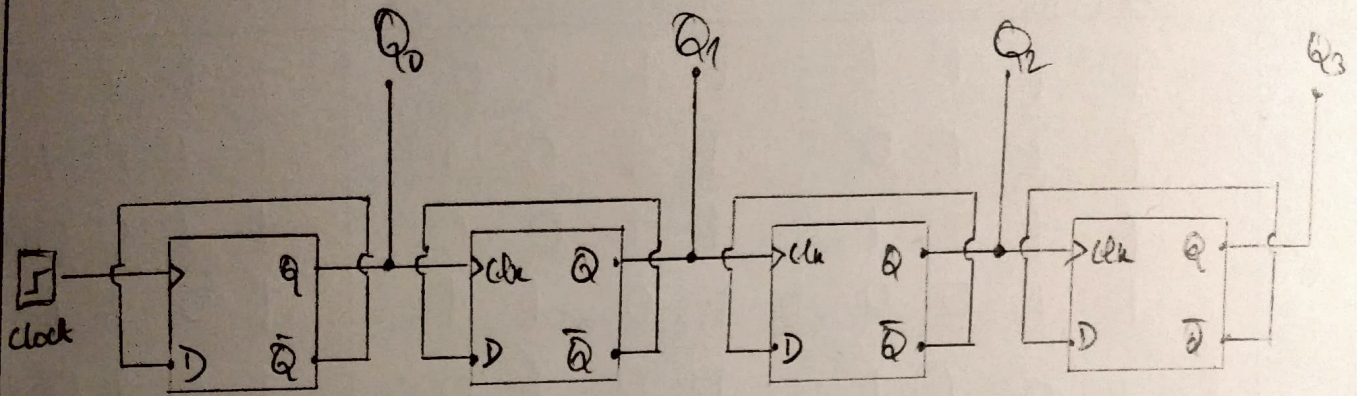
Asynchronous 4 bit up counter



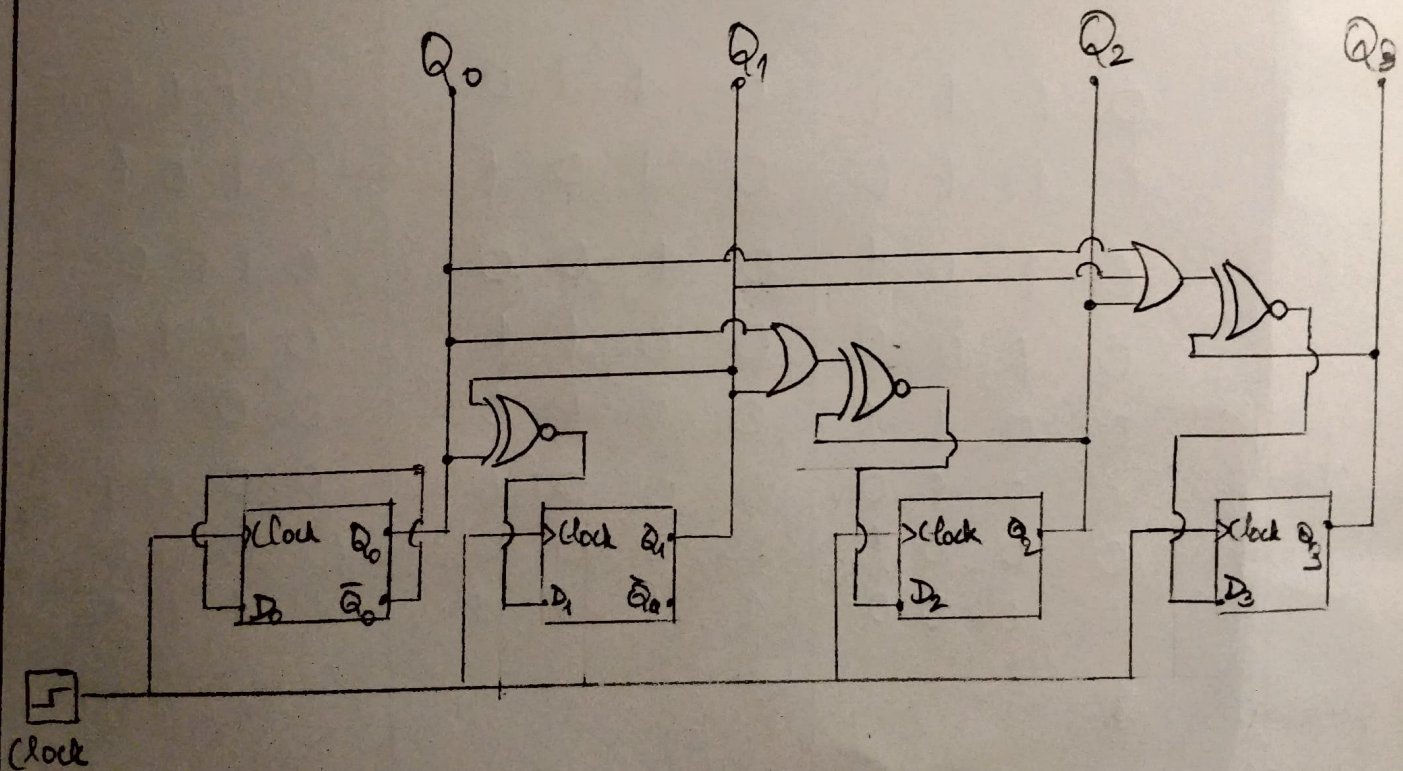
synchronous 4 bit up counter

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(III) Asynchronous 4 bit down counter →



(IV) Synchronous 4 bit down counter →



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$Q_3 Q_2$ $Q_1 Q_0$ D_3

	00	01	11	10
00	1			
01				
11	1	1	1	1
10		1	1	1

$$D_3 = Q_3 Q_2 + Q_3 Q_1 + Q_3 Q_0 + \overline{Q_3} \overline{Q_2} \overline{Q_1} \overline{Q_0}$$

$$= Q_3 (Q_2 + Q_1 + Q_0) + \overline{Q_3} (\overline{Q_2 + Q_1 + Q_0})$$

$$D_3 = Q_3 \odot (Q_2 + Q_1 + Q_0)$$

Q_2 $Q_1 Q_0$ D_2

	00	01	11	10
00	1			
01		1	1	1
11		1	1	1
10	1			

$$D_2 = Q_2 Q_0 + Q_2 Q_1 + \overline{Q_2} \overline{Q_1} \overline{Q_0}$$

$$= Q_2 (Q_1 + Q_0) + \overline{Q_2} (\overline{Q_1 + Q_0})$$

$$D_2 = Q_2 \odot (Q_1 + Q_0)$$

$Q_1 Q_0$ D_1

	00	01	11	10
00	1		1	
01	1		1	
11	1		1	
10	1		1	

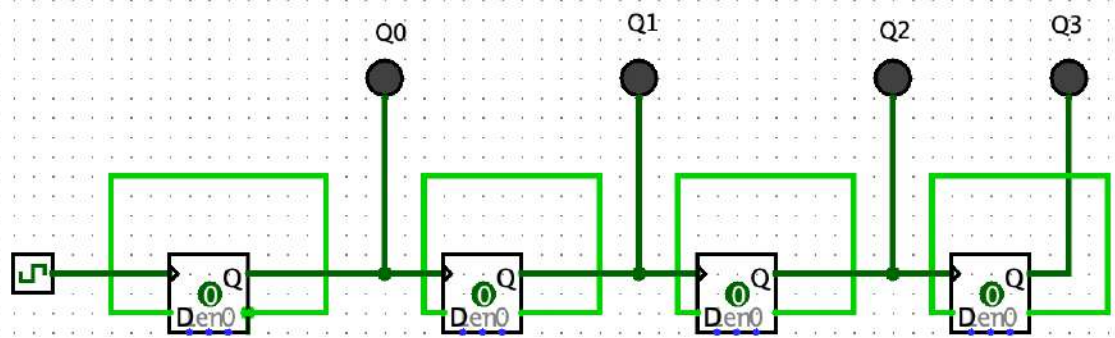
$$D_1 = \overline{Q_1} \overline{Q_0} + Q_1 Q_0$$

$$= Q_1 \odot Q_0$$

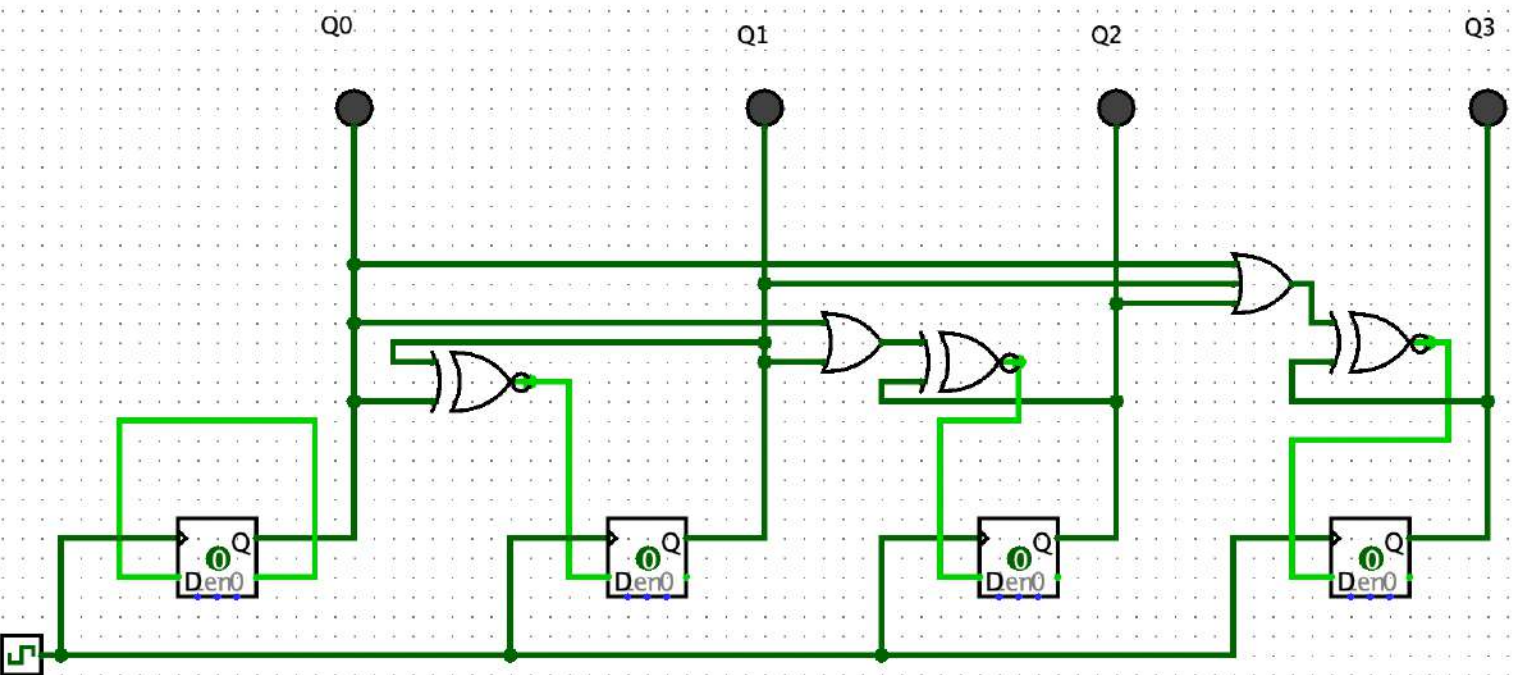
$Q_1 Q_0$

	00	01	11	10
00	1			1
01	1			1
11	1			1
10	1			1

$$D_0 = \overline{Q_0}$$



asynchronous 4 bit down counter



Synchronous 4 bit down counter