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DLD LAB EXAM SARINGI-2022

Q B1

AIH: To implement a synchronous counter using.

JK flip flops for the given sequence:

6, 3, 1, 0, 10, 15, 11

DETAILS:

2) JK flip-flop table: excitation table:

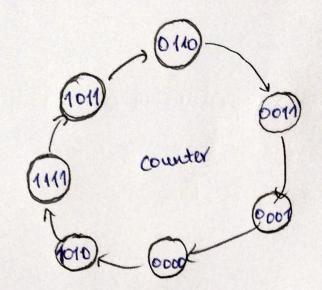
QU)	J	K	Q (+1)
0	0	X	0
0	1	X	1
1	4	1	0
1	*	0	1

1) Ik flip flop truth table:

Qita)	JK	9(4+0)
0	0 0	0
0	01	0
0	10	1
0	11	1
1	00	1
1	01	0
1	10	1
		0

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3) State diagram for:



JK#: 0 (0) X0

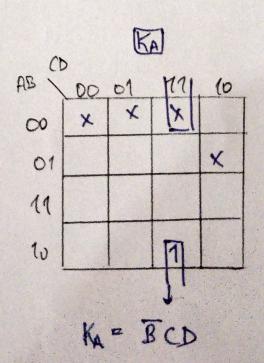
1

4) Circuit excétation table:

Descrit Hate Next state Enput to It					
Acsent Mate A B C D	At Bt Ct Dt	JAKA	JEKB	Jck	Joko
000000000000000000000000000000000000000	000000000000000000000000000000000000000	0 x 0 x 1 x 0 x 1	<pre></pre>	x0 x1 0x 1x x0 x0	1 × × 0 × 1 × × 0 × 1

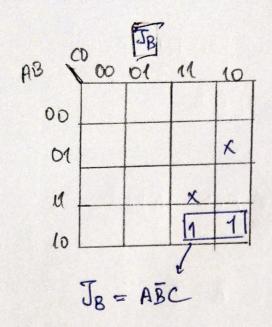
S) KHO	ets:	。压)11	10
00	0			
01				
11			X	
40			×	X

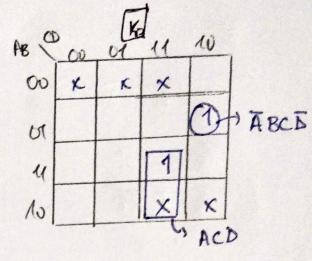
-		-	-
JA=A	R		7
H	'n	-	-



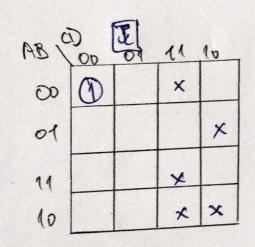
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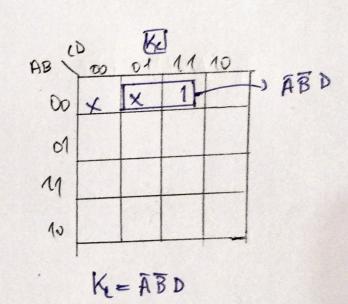
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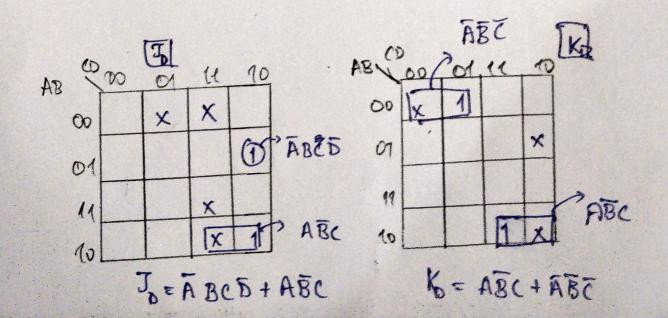




KB = ALD + ABCD







6) Boolean expression:

Obtained from K Maks

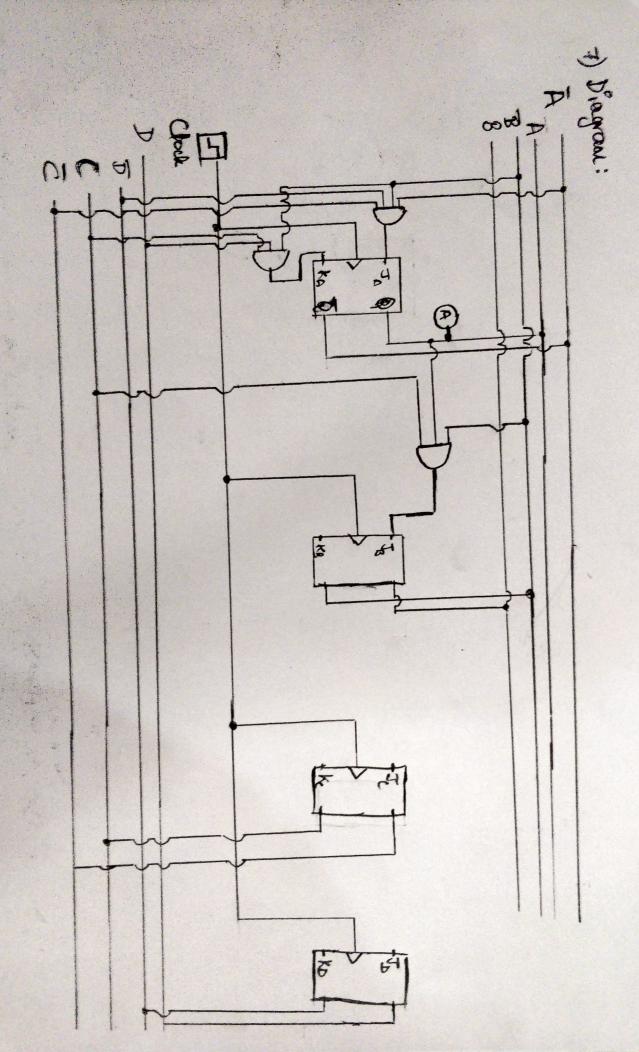
KA=BCD

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KB = ACD + ABCD

Ke ABD

Ro = ABC + ABC



Physistian Sonema