

Mode of Evaluation (DLD)	(%)
1. Mid-sem + Viva	(15+5)
2. End-sem + Viva	(25+5)
3. Surprise Quizzes	10
4. Schedule Quiz	15
5. Assignments	5
6. Lab (Continuous, report, Exam)	20

### Simulation software

**Java**      <https://java.com/en/download/>

**Logisim**    <https://sourceforge.net/projects/circuit/>

# Lab report: Hand written + Simulation (file)

## Consists of following sections:

- Title of the Lab experiment
  - Name, Roll-no, Sec
1. Objective of the experiment
  2. About the experiments (procedure/diagram/programme source code/flowchart etc)
  3. Your observation/what you learned

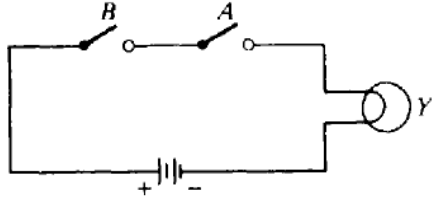
After complementation of the LAB, document has to be uploaded in Google classroom within **given deadline**

**filename:** Rollnumber\_lastname

# Logic gates

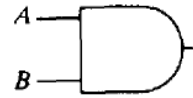
- Logic gates are the basic building blocks of any digital electronic circuits
- Operates on one/more input signals to produce output
- Input elect. signal (0-2.5/3V) could be either High or Low
- High – logic 1, Low- logic 0

# Gates: AND, NAND



Input switches		Output light
B	A	Y
open	open	no
open	closed	no
closed	open	no
closed	closed	yes

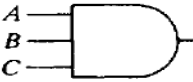
Truth table



Inputs		Output
B	A	Y
0	0	0
0	1	0
1	0	0
1	1	1

AND-gate symbol

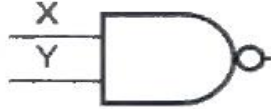
0 = low voltage  
1 = high voltage



Inputs			Output
C	B	A	Y
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	0
1	0	0	0
1	0	1	0
1	1	0	0
1	1	1	1

Truth table with three variables

$A \cdot B \cdot C = Y$

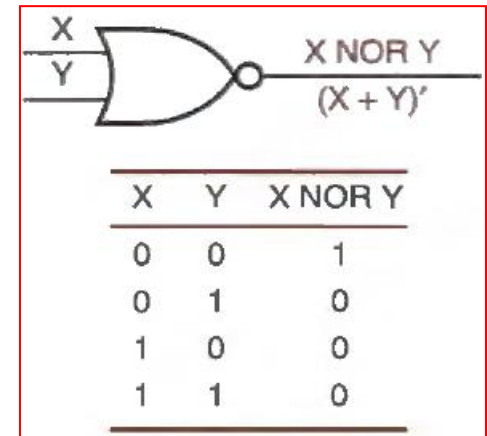
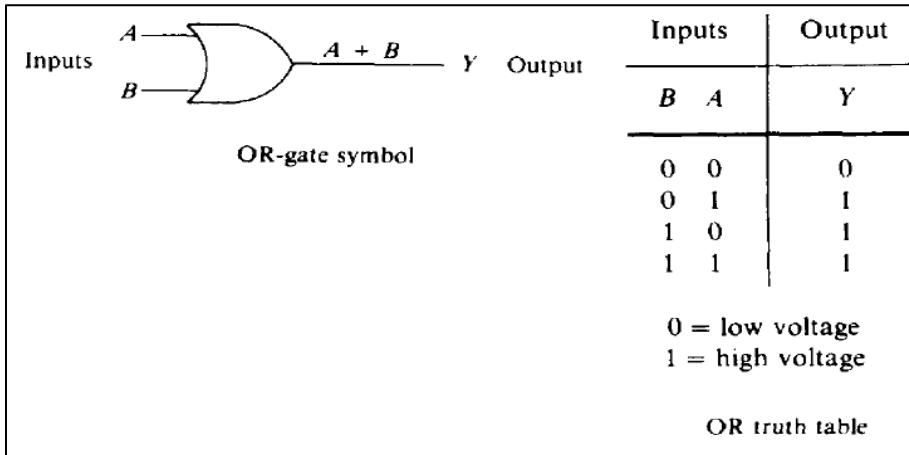
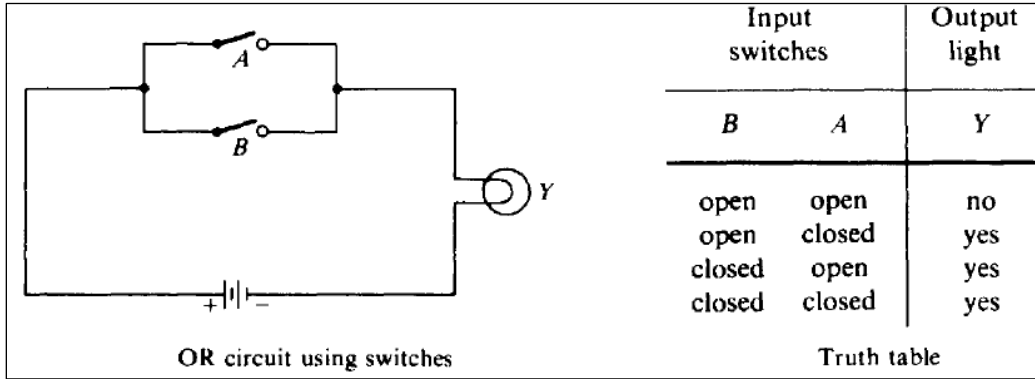


X	Y	X NAND Y
0	0	1
0	1	1
1	0	1
1	1	0

X NAND Y  
 $(X \cdot Y)'$

Complement

# Gates: OR, NOR

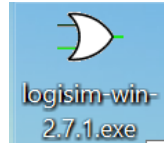


# Lab1: Introduction to Logisim

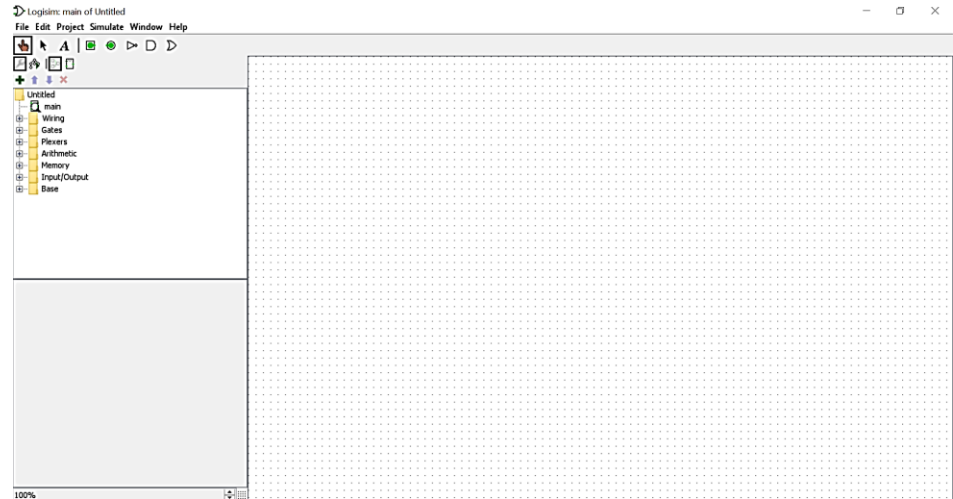
- Logisim is an **software/tool** for **designing and simulating digital logic circuits**
- It has **simple and user friendly toolbar** interface for simulation of circuit
- It is simple **enough to facility learning the most basic concepts** related to logic circuits

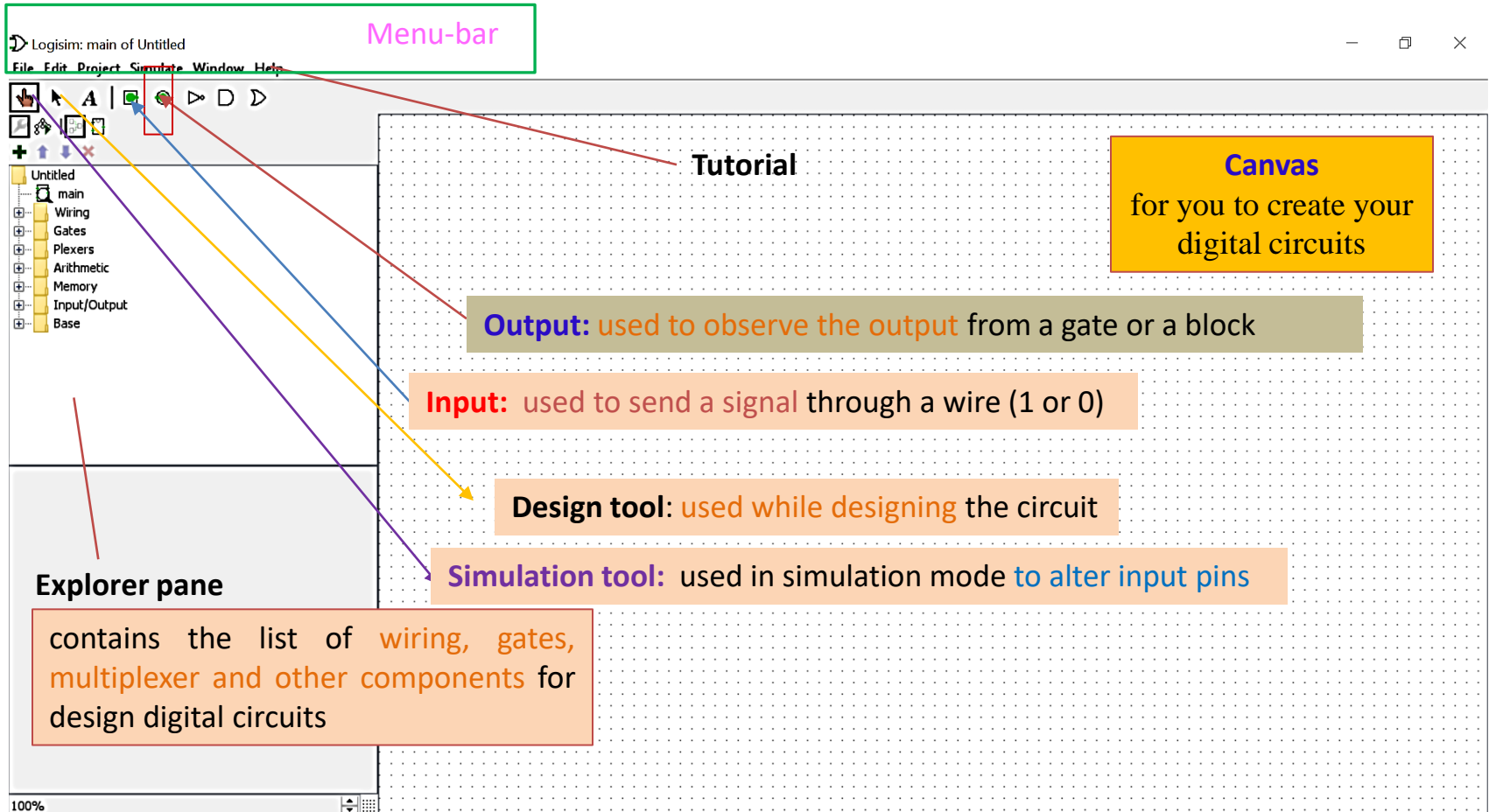
**Step-1: Download and Install** → a) Java <https://java.com/en/download/>  
b) **Logisim** <https://sourceforge.net/projects/circuit/>

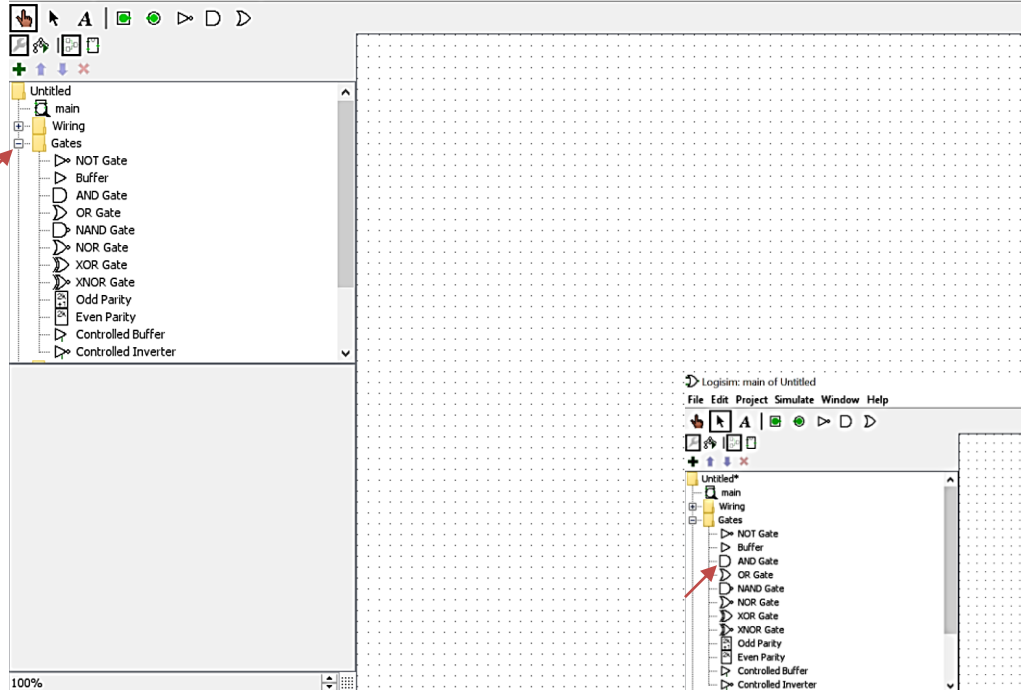
**Step-2: After Install** →



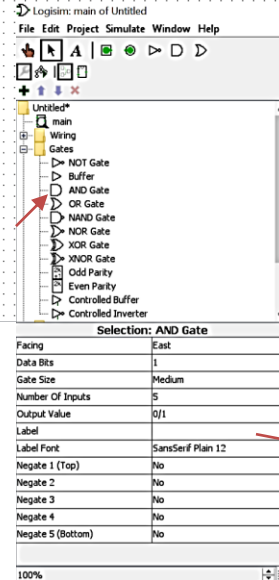
**Step-3: Click on**







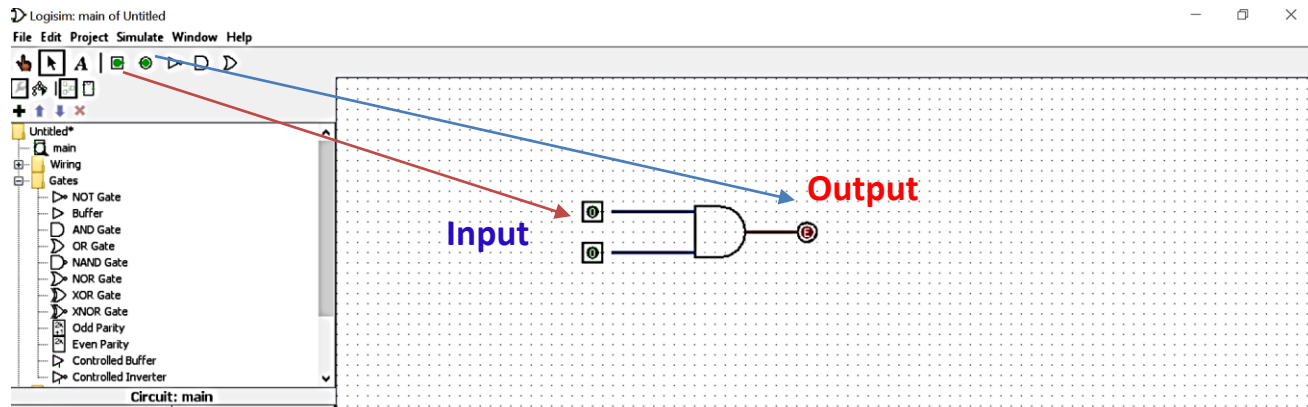
## Verification of AND gate truth table



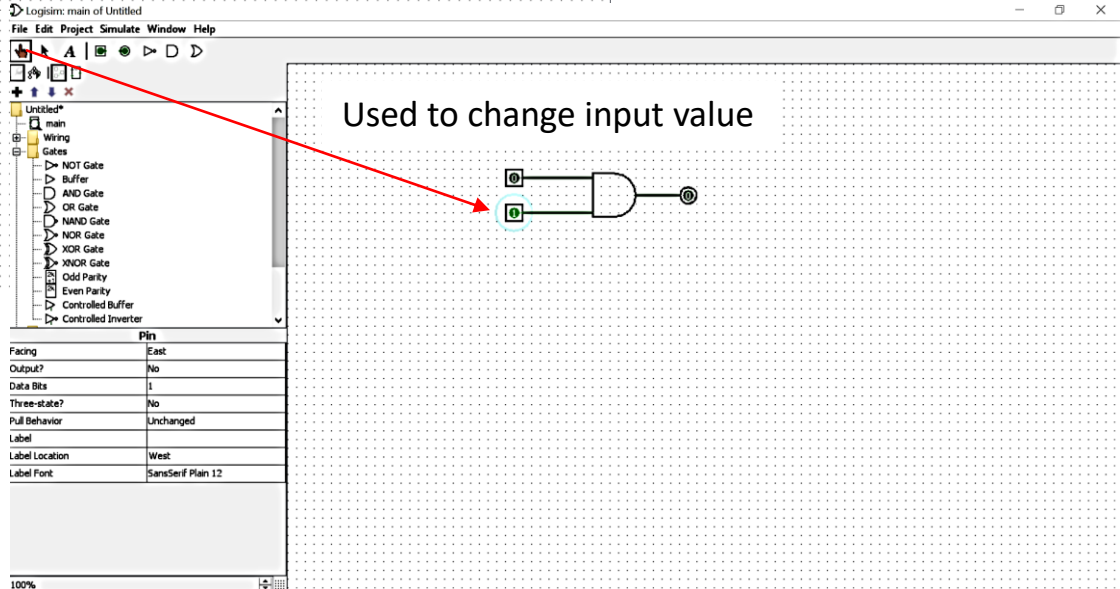
### Attribute table:

Gives detailed **attributes of digital design components** (e.g., AND, OR, XOR gates), e.g. number of inputs

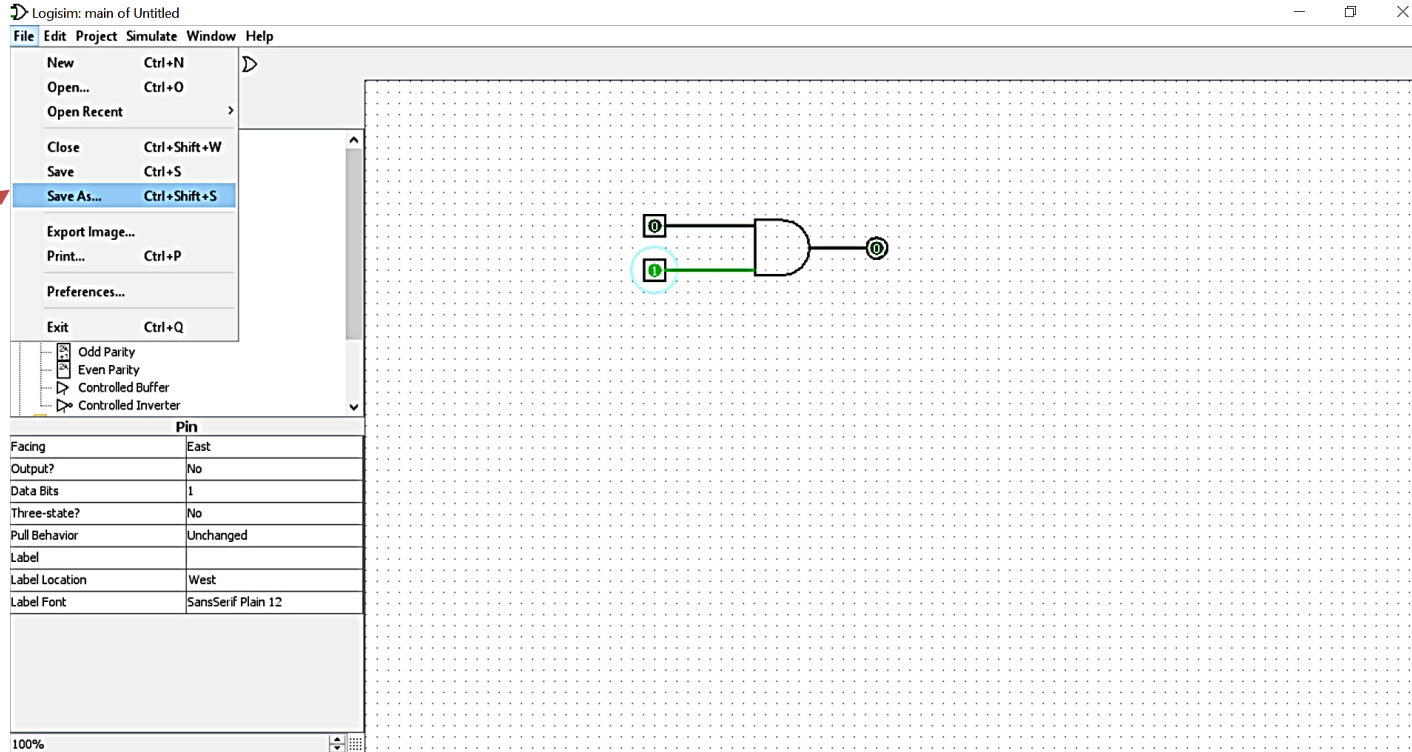




Circuit Name	main
Shared Label Facing	
Shared Label Facing	East
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# To Save the design



**Thank you!**