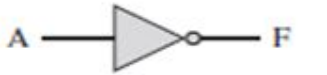
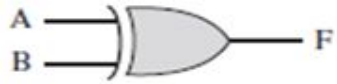
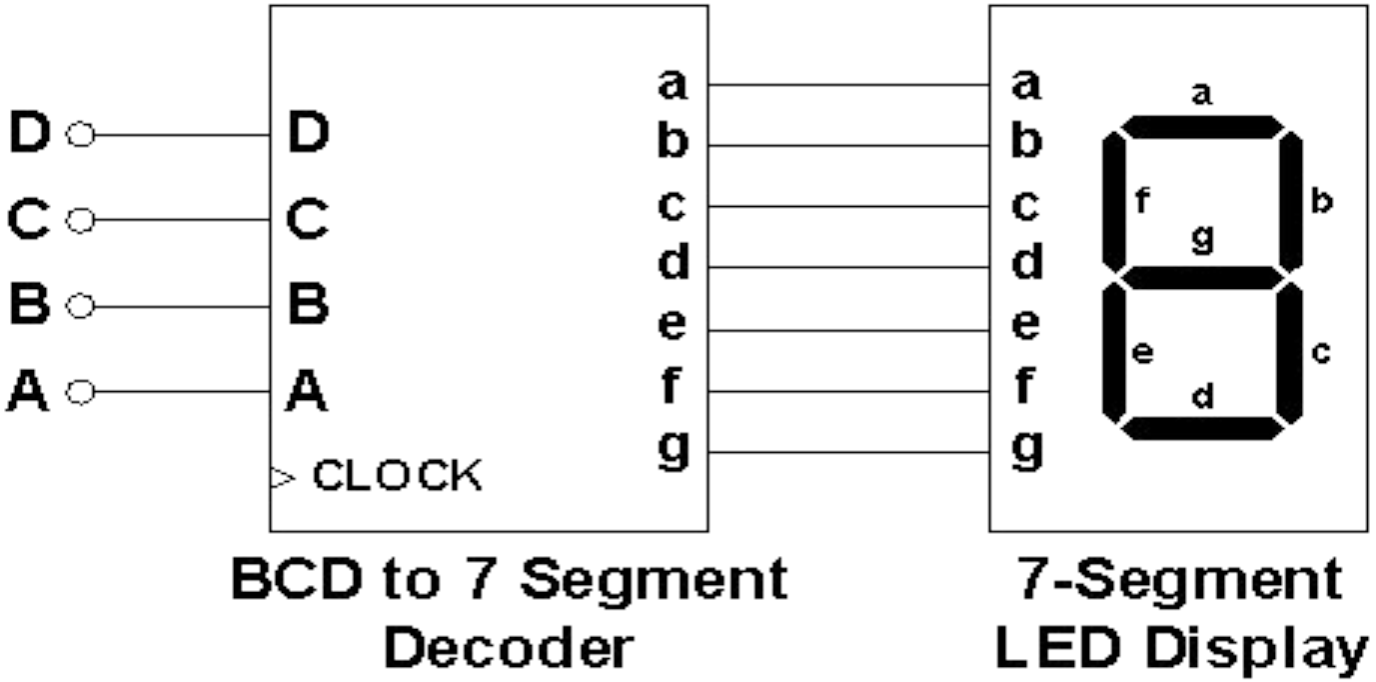
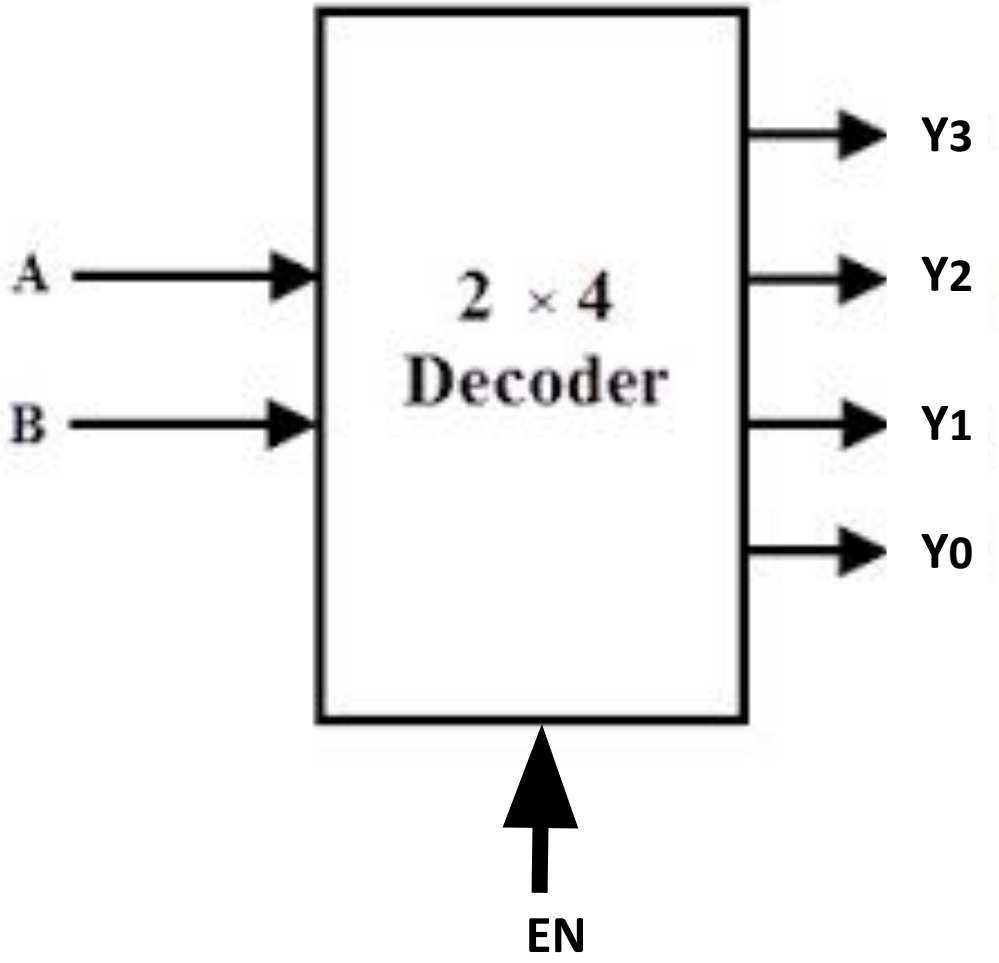
Basic Gates & Universal Gates

IC No	Name	Graphical Symbol	Algebraic Function	Truth Table
7408	AND		$F = A \cdot B$ or $F = AB$	A B | F 0 0 | 0 0 1 | 0 1 0 | 0 1 1 | 1
7432	OR		$F = A + B$	A B | F 0 0 | 0 0 1 | 1 1 0 | 1 1 1 | 1
7404	NOT		$F = \overline{A}$ or $F = A'$	A | F 0 | 1 1 | 0
7400	NAND		$F = \overline{AB}$	A B | F 0 0 | 1 0 1 | 1 1 0 | 1 1 1 | 0
7402	NOR		$F = \overline{A + B}$	A B | F 0 0 | 1 0 1 | 0 1 0 | 0 1 1 | 0
7486	XOR		$F = A \oplus B$	A B | F 0 0 | 0 0 1 | 1 1 0 | 1 1 1 | 0

BCD to 7- Segment Decoder Circuit



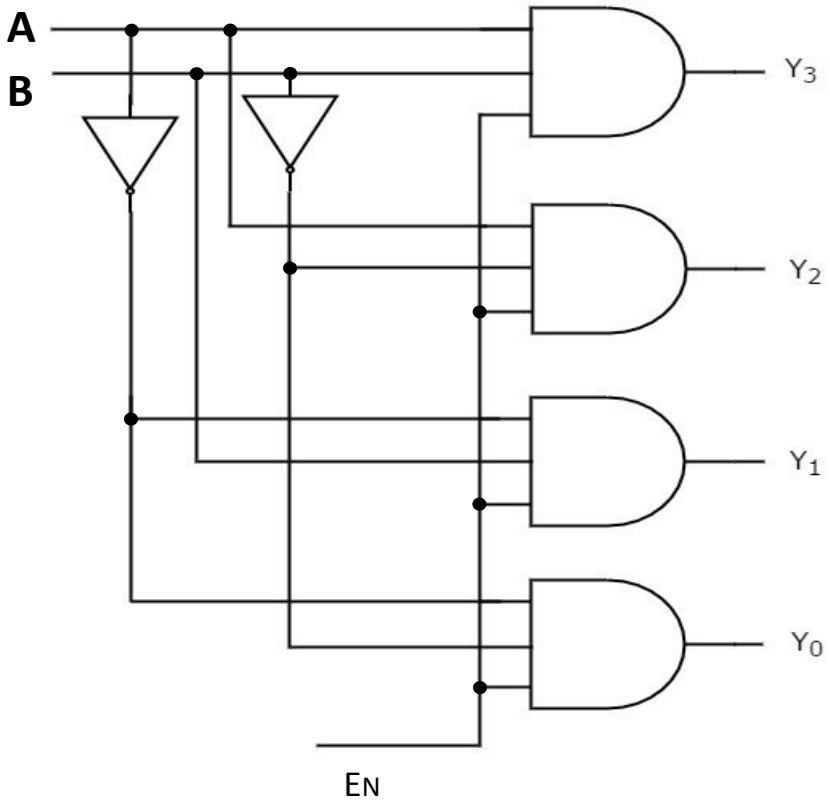
2 - 4 Decoder



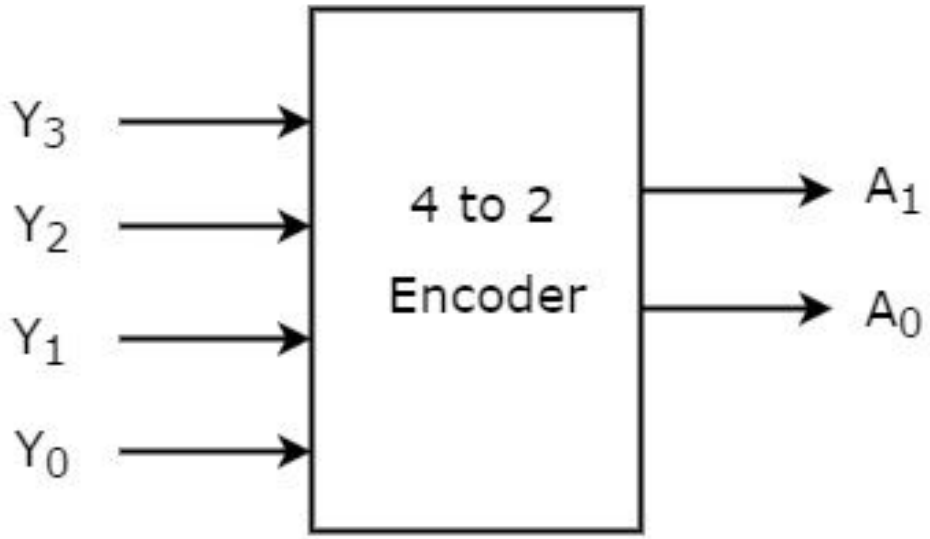
Truth Table

Inputs			Outputs			
EN	A	B	Y_3	Y_2	Y_1	Y_0
0	×	×	0	0	0	0
1	0	0	0	0	0	1
1	0	1	0	0	1	0
1	1	0	0	1	0	0
1	1	1	1	0	0	0

Circuit Diagram



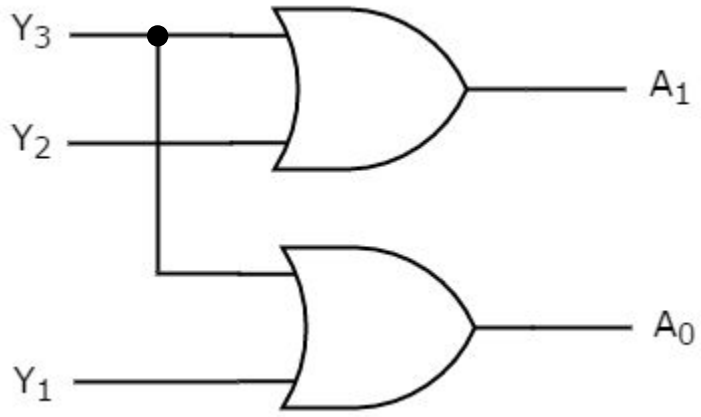
4 - 2 Encoder



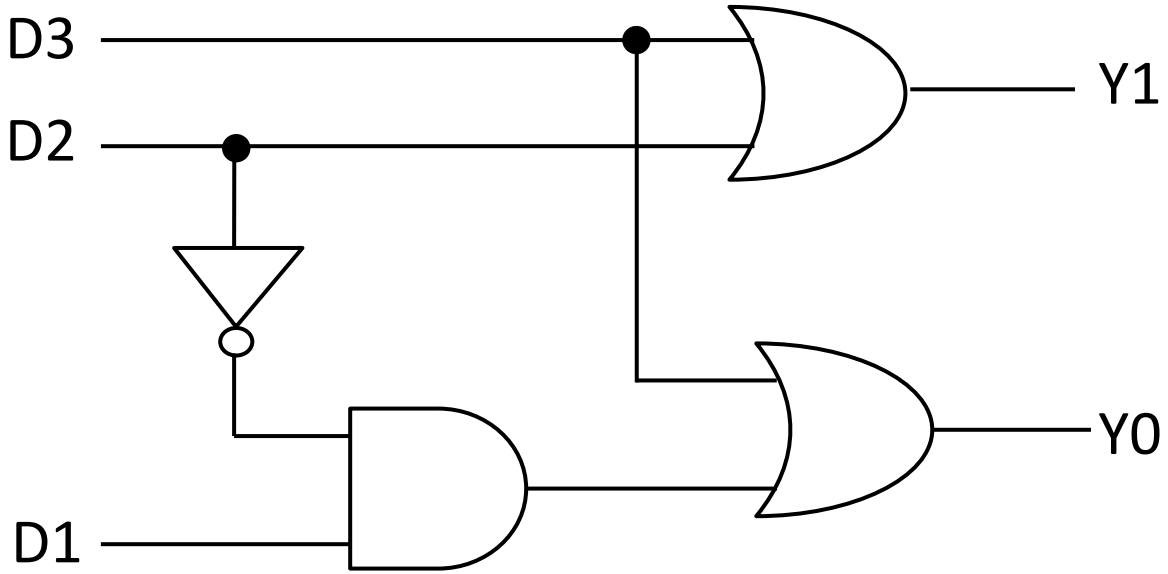
Truth Table

Inputs				Outputs	
Y3	Y2	Y1	Y0	A1	A0
0	0	0	1	0	0
0	0	1	0	0	1
0	1	0	0	1	0
1	0	0	0	1	1

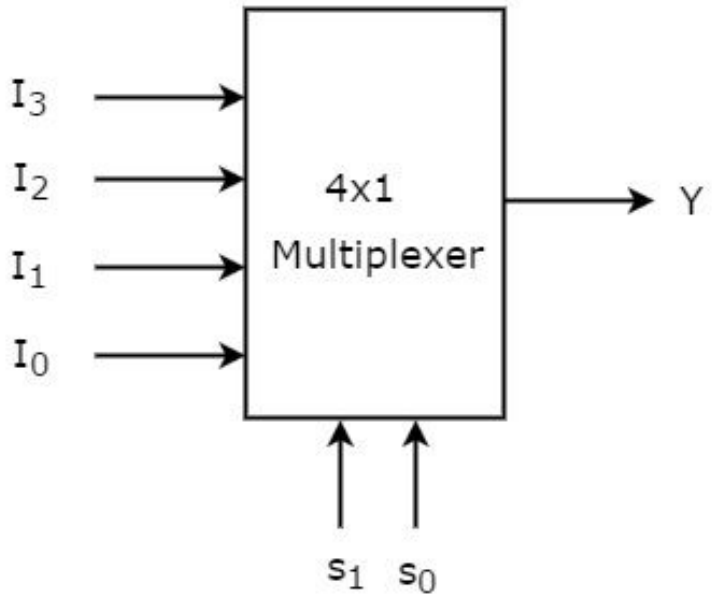
4 - 2 Encoder Circuit



4 - 2 Priority Encoder Circuit



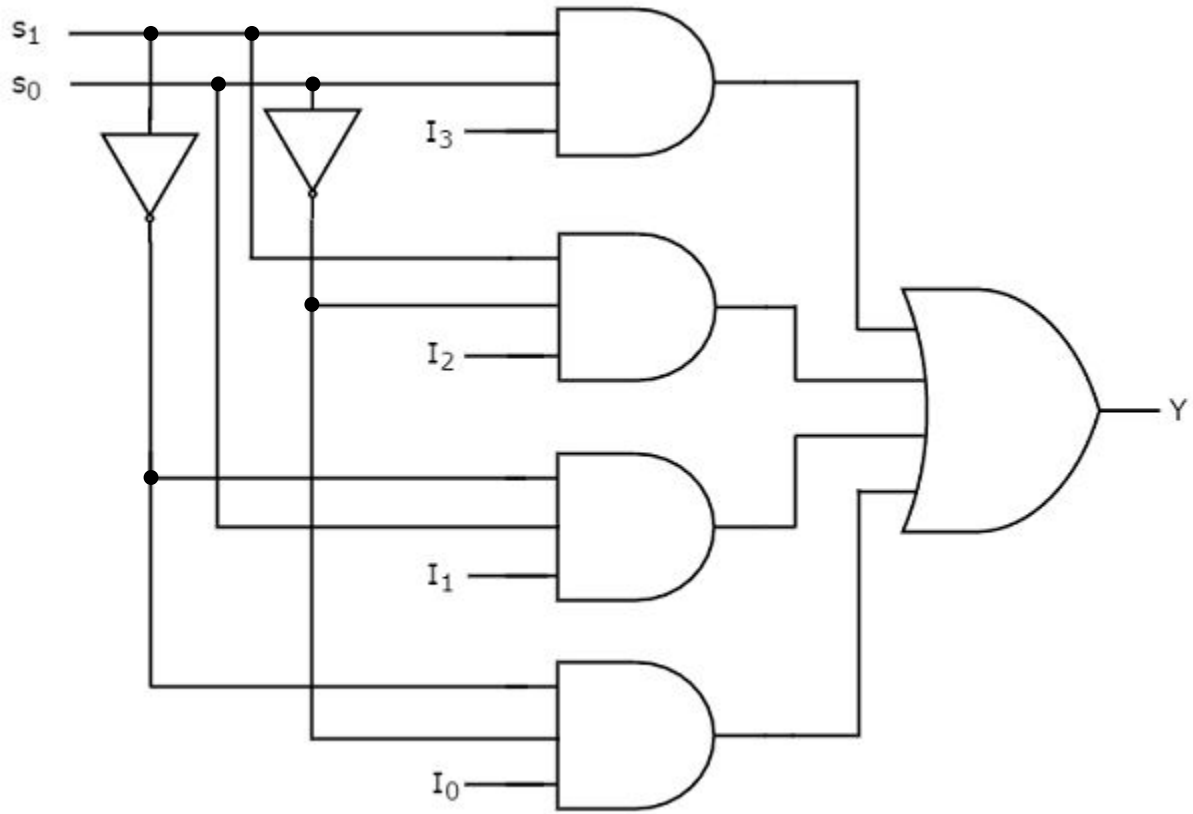
4 x 1 Multiplexer



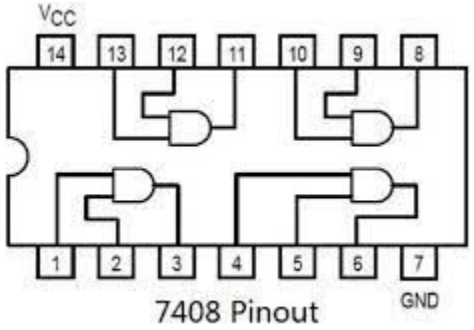
Truth Table

Selection Lines		Output
S_1	S_0	Y
0	0	
0	1	
1	0	
1	1	

4 x 1 Multiplexer Circuit

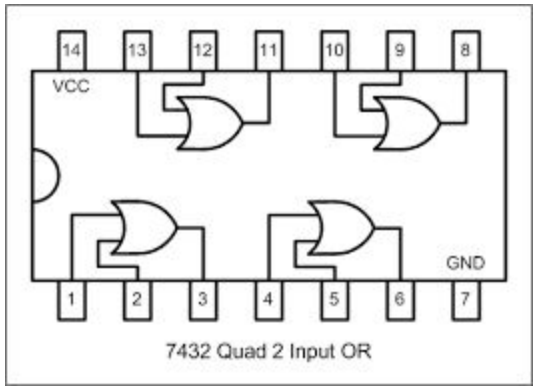


7408



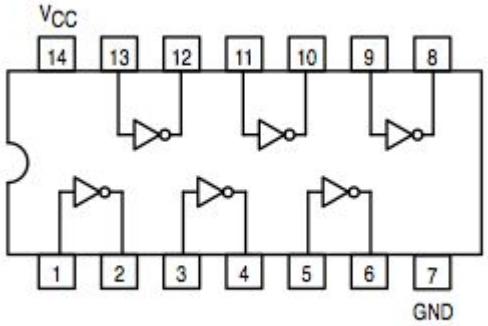
7408 Pinout

7432

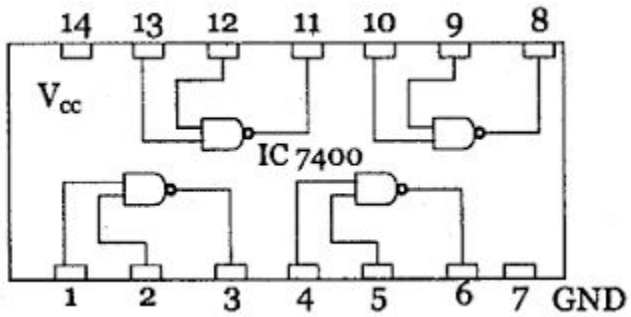


7432 Quad 2 Input OR

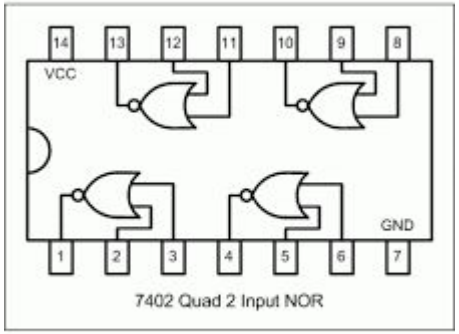
7404



7400

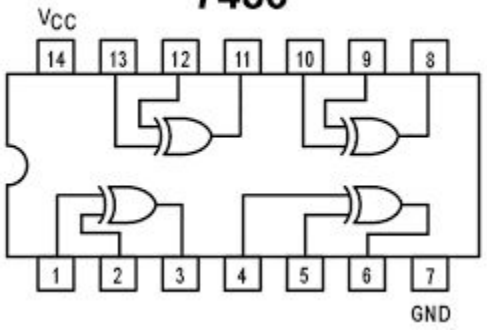


7402

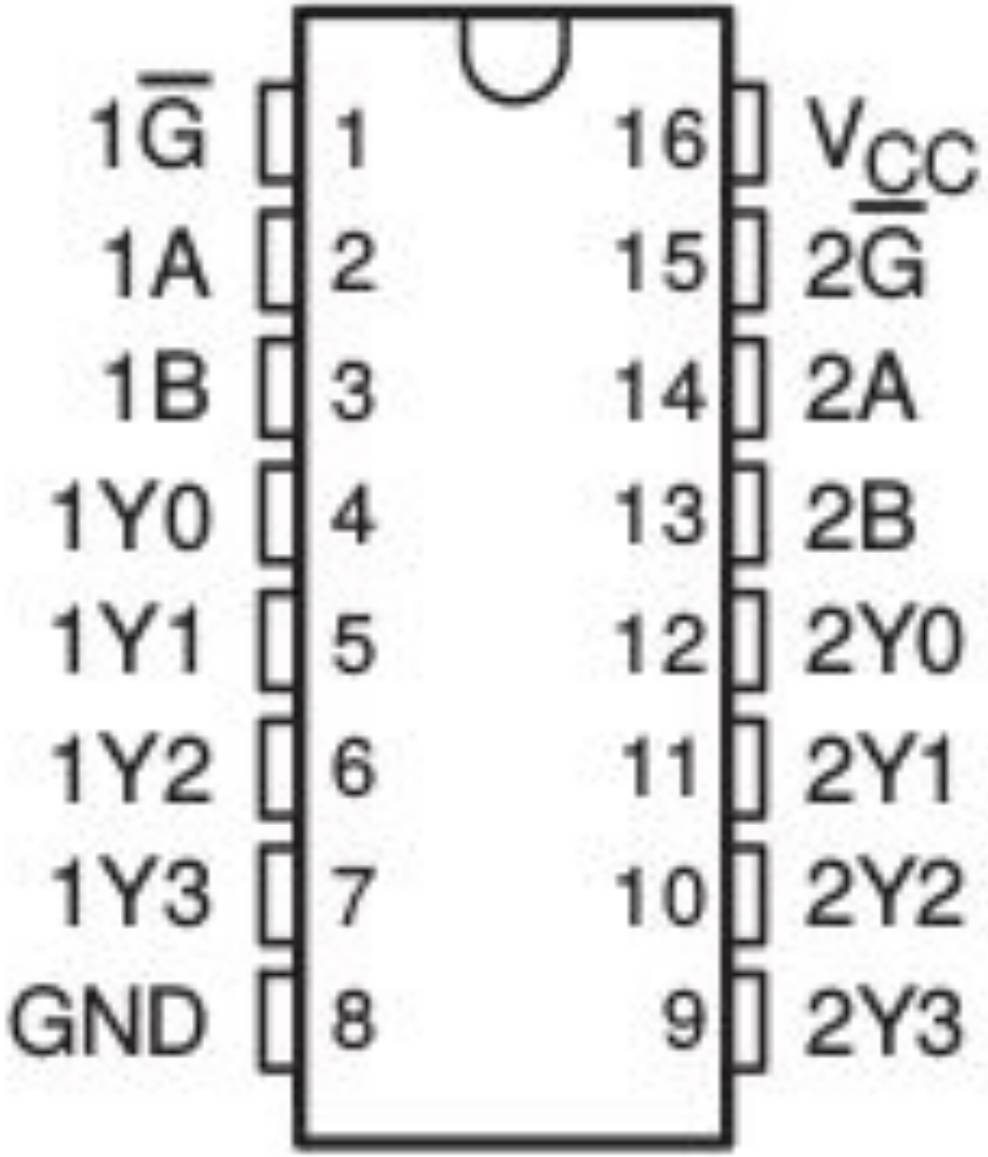


7402 Quad 2 Input NOR

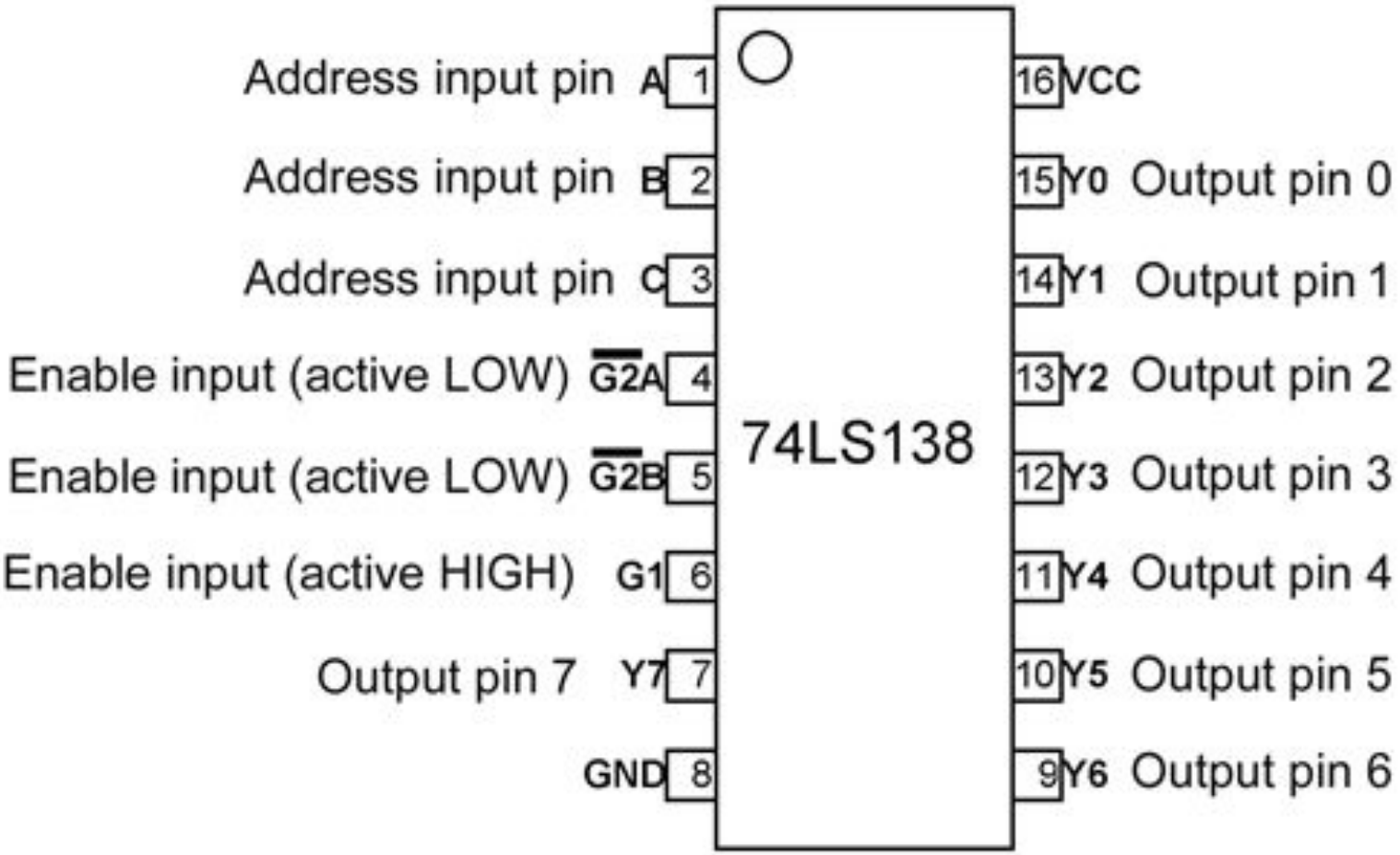
7486



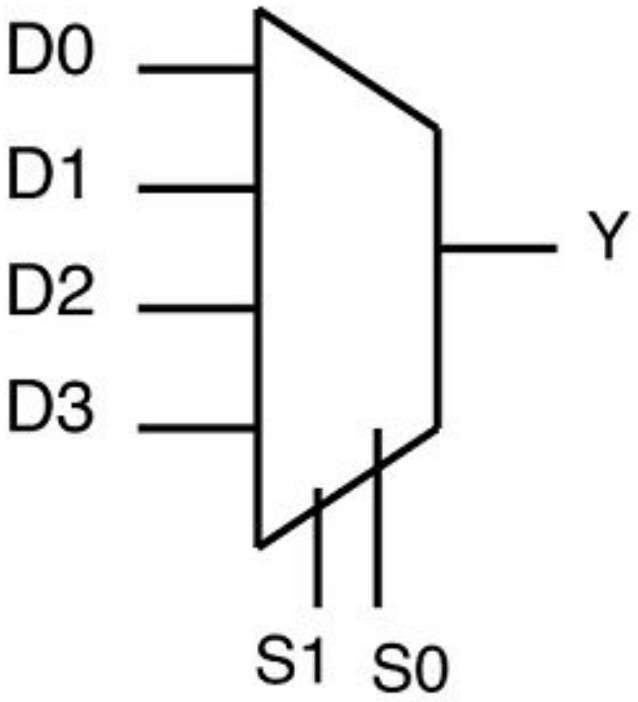
2 - 4 Decoder IC

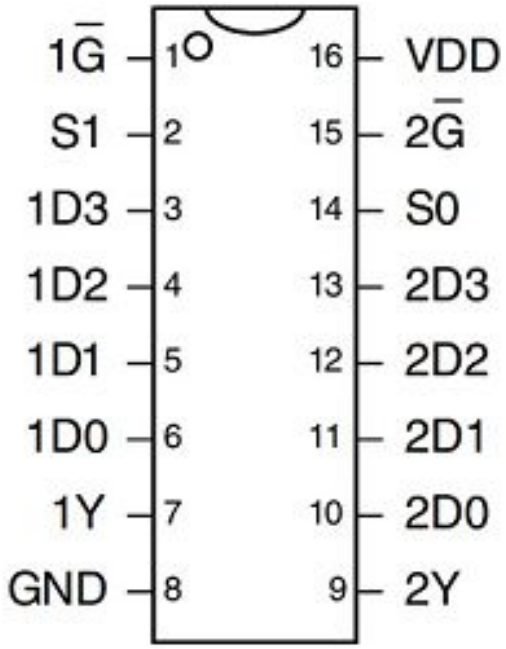


3 - 8 Encoder IC



4 x 1 Multiplexer IC





74153 4 :1 Mux