Introduction to VLSI Design

School of Engineering and Science
Fall 2021

Instructor: Prof. Bryan Ackland
Course Web Address: https://sit.instructure.com/courses/49847
Course Schedule: Monday to Sunday
Contact Info: backland@stevens.edu , cell: (908) 420-2958
Virtual Office Hours: Tuesday 12:00-2:00 pm
Virtual session: Use Zoom from Canvas course home page
Prerequisite(s): None formal, but see below
Corequisite(s): None
Cross-listed with: MT 690-WS, PEP 690-WS

COURSE DESCRIPTION

This course provides a general understanding of digital VLSI design. Emphasis is on transistor-level (full custom) VLSI design. Specific topics discussed in this course include the VLSI manufacturing process, design metrics, physical layout, simulation analysis, stick diagram design, MOS devices, CMOS inverter and logic gate design, static and dynamic logic, power distribution and consumption and timing analysis. Students will complete a design project in which they will use Tanner VLSI design tools to layout, extract and simulate a small digital design of their choosing. This course will also briefly introduce hardware description language (VHDL) based design using Xilinx tools to model and simulate digital circuits.

PREREQUISITES

This course presumes an undergraduate knowledge of simple electronic circuit components (resistors, capacitors, MOS transistors, voltage and current sources) and their interconnection in simple series and parallel circuit configurations. It also presumes a knowledge of Boolean digital logic functions, gates and operators (e.g. multiplexers, latches, flip-flops, adders) and two's complement binary arithmetic.

STUDENT LEARNING OUTCOMES

After successful completion of this course, students will be able to…

- Know how to use a hardware description language (VHDL) to design, model and test complex digital circuits for implementation in FPGA or ASIC standard cell technologies.

- Be able to use commercial CAD tools to simulate and verify the correct operation of digital circuits modeled using a hardware description language (VHDL)
- Be able to develop transistor level circuit diagrams for CMOS digital gates, storage components and arithmetic operators and be able to estimate their performance
- Understand the operation of the MOS transistor and its application to CMOS digital design and understand the tradeoffs between performance, noise margin and power dissipation
- Know how to use CAD tools to layout full custom CMOS circuits obeying process design rules and evaluate the function and performance of these circuits using commercially available circuit simulation tools (SPICE)
- Understand the CMOS fabrication process and the relationship between layout and mask-based fabrication.
- Know how to design transistor-level digital circuits using a number of different circuit techniques including static compound, pseudo-NMOS and dynamic gates and understand the tradeoffs in performance, area and power dissipation.

COURSE FORMAT AND STRUCTURE

This course is fully online. To access the course, please visit stevens.edu/canvas . For more information about course access or support, contact the Technology Resource and Assistance Center (TRAC) by calling 201-216-5500.

Course Logistics

- The course is comprised of one online lecture (100-120 minutes) per week, accompanied by a number of homeworks throughout the semester and a project. There will be a mid-term and a final exam.
- Each lecture consists of a PowerPoint slide presentation accompanied by an audio (MP3) lecture.
- You are encouraged to “mentally enroll” in this course as if it occurred on Mondays. In other words, our weeks will run from Monday to Sunday. I will post any new information (online activities, discussion starters, etc.) for the upcoming week by Sunday evening, so that when you log in on Monday, you can begin the new week.
- When assignments are due, they are due by 12:00 midnight EST on the due date listed in the course schedule.
- Deadlines are an unavoidable part of being a professional and this course is no exception. Course requirements must be completed and posted or submitted on or before specified due date and delivery time deadline. Due dates and delivery time deadlines are defined as Eastern Standard Time (as used in Hoboken, NJ). Please note, students living in distance time zones or overseas must comply with this course time and time and due date deadline policy. Avoid any inclination to procrastinate. To encourage you to stay on schedule, due dates have been established for each assignment; 20% of the total points may be deducted for assignments received 1-6 days late; assignments received more than 1 week late will receive 0 points.

Instructor's Online Hours

- I will be available via email and will respond as soon as I am available (generally within 24 hours).
- I will also have virtual office hours from 1-2 pm on Tuesday afternoons, starting in Week 1 (Tuesday August 31). Please use Zoom tab in Canvas if you wish to meet with me at these times.

TENTATIVE COURSE SCHEDULE

(Go to Canvas Modules page for exact schedule and homework due dates)

Week	Topic(s)	Notes	Homeworks
0	Class organization Introduction to VLSI Design	Lecture 0 Lecture 1	
1	VHDL Design: Entities, Architectures & Signals Dataflow Modeling	Lecture 2	HW1
2	VHDL Design: Behavioral and Structural Modeling Subprograms & Overloading	Lecture 3	HW2
3	VHDL Design: Synthesis and Finite State Machines Test Bench Design	Lecture 4	
4	MOS Transistors and CMOS Logic	Lecture 5	HW3
5	CMOS Fabrication & Layout Computer Aided Design Tools & Flow	Lecture 6 Lecture 6A	HW4 Design Project
6	Transistor Theory and DC Response	Lecture 7	HW5
7	Delay and Transient Response	Lecture 8	
8	SPICE Circuit Simulation	Lecture 9	
9	Midterm Exam		
10	Logical Effort and Multi-Stage Logic Network Design	Lecture 10	HW6
11	Combinational Circuit Families: Pseudo-NMOS and Dynamic Logic	Lecture 11	
12	Design for Low Power	Lecture 12	HW7

13	Design of Arithmetic Circuits	Lecture 13	
14	Complete Design Project		
15	Final Exam		

COURSE MATERIALS

Textbook(s): CMOS VLSI Design: A Circuits and Systems Perspective (4th Edition), Neil Weste and David Harris, Publisher: Addison Wesley, ISBN: 0-321-54774-8, 2010.

Other Ref: (1) Introductory VHDL – From Simulation to Synthesis, Sudhakar Yalamanchili, Prentice Hall, ISBN: 0-13-080982-9, 2001.

(2) CMOS: Circuit Design, Layout and Simulation (2nd Edition), R. Jacob Baker, Wiley-Interscience, ISBN: 0-471-70055-X, 2005.

Materials: Stand-alone scientific calculator

COURSE REQUIREMENTS

Homework There are usually seven (7) homework assignments throughout the course. All assignments count equally towards 20% of the final grade. All assignments should be submitted online (Canvas) by the due date. Homeworks will be graded with online comments within one week of the submission date.

Project Students will complete a project of their own choosing in which they design a small full-custom digital circuit using commercial CAD tools. This includes circuit schematics, physical layout, design rule check, circuit extraction and simulation to verify function and performance over a range of temperatures and voltages using the circuit simulator SPICE. The project is graded according to difficulty of the project, accuracy of the results and quality of the presentation.

Exams There will be two exams in this course: a midterm and a final. The final exam is cumulative. Both exams are taken online. Students have five (5) days to complete the exam.

TECHNOLOGY REQUIREMENTS

Required Equipment

- Computer: PC (Windows 7+) with high-speed internet connection

Required Software

- Microsoft Word
- Microsoft PowerPoint

GRADING PROCEDURES

Grades will be based on:

Homework	20%
Project	25%
Mid-term Exam	25%
Final Exam	30%

Late Policy

Submissions that are a few hours late will not be penalized. More than one day late may incur a penalty of 20%. More than one week late will not be graded.

Academic Integrity

Graduate Student Code of Academic Integrity
All Stevens graduate students promise to be fully truthful and avoid dishonesty, fraud, misrepresentation, and deceit of any type in relation to their academic work. A student's submission of work for academic credit indicates that the work is the student's own. All outside assistance must be acknowledged. Any student who violates this code or who knowingly assists another student in violating this code shall be subject to discipline.

All graduate students are bound to the Graduate Student Code of Academic Integrity by enrollment in graduate coursework at Stevens. It is the responsibility of each graduate student to understand and adhere to the Graduate Student Code of Academic Integrity. More information including types of violations, the process for handling perceived violations, and types of sanctions can be found at www.stevens.edu/provost/graduate-academics.

EXAM CONDITIONS

The following procedures apply to exams for this course. As the instructor, I reserve the right to modify any conditions set forth below by printing revised Exam Conditions on the exam.

1. Students may use the following devices during exams. Any electronic devices that are not mentioned in the list below are not permitted.

Device	**Permitted?**

	Yes	No
Laptops		X
Cell Phones		X
Tablets		X
Smart Watches		X
Stand-alone calculator	X	

2. Students may use the following materials during exams. Any materials that are not mentioned in the list below are not permitted.

Material	**Permitted ?**	
	Yes	No
Handwritten Notes	X	
Typed Notes	X	
Textbooks	X	
Other reference books	X	

3. Students are not allowed to work with or talk to other students during exams.

LEARNING ACCOMODATIONS

Stevens Institute of Technology is dedicated to providing appropriate accommodations to students with documented disabilities. The Office of Disability Services (ODS) works with undergraduate and graduate students with learning disabilities, attention deficit-hyperactivity disorders, physical disabilities, sensory impairments, psychiatric disorders, and other such disabilities in order to help students achieve their academic and personal potential. They facilitate equal access to the educational programs and opportunities offered at Stevens and coordinate reasonable accommodations for eligible students. These services are designed to encourage independence and self-advocacy with support from the ODS staff. The ODS staff will facilitate the provision of accommodations on a case-by-case basis.

For more information about Disability Services and the process to receive accommodations, visit https://www.stevens.edu/office-disability-services. If you have any questions please contact: Phillip Gehman, the Director of Disability Services Coordinator at Stevens Institute of Technology at pgehman@stevens.edu or by phone 201-216-3748.

Disability Services Confidentiality Policy

Student Disability Files are kept separate from academic files and are stored in a secure location within the Office of Disability Services. The Family Educational Rights Privacy Act (FERPA, 20 U.S.C. 1232g; 34CFR, Part 99) regulates disclosure of disability documentation and records maintained by Stevens Disability Services. According to this act, prior written consent by the student is required before our Disability Services office may release disability documentation or records to anyone. An exception is made in unusual circumstances, such as the case of health and safety emergencies.

INCLUSIVITY

Name and Pronoun Usage

As this course includes group work and class discussion, it is vitally important for us to create an educational environment of inclusion and mutual respect. This includes the ability for all students to have their chosen gender pronoun(s) and chosen name affirmed. If the class roster does not align with your name and/or pronouns, please inform the instructor of the necessary changes.

Inclusion Statement

Stevens Institute of Technology believes that diversity and inclusiveness are essential to excellence in academic discourse and innovation. In this class, the perspective of people of all races, ethnicities, gender expressions and gender identities, religions, sexual orientations, disabilities, socioeconomic backgrounds, and nationalities will be respected and viewed as a resource and benefit throughout the semester. Suggestions to further diversify class materials and assignments are encouraged. If any course meetings conflict with your religious events, please do not hesitate to reach out to your instructor to make alternative arrangements.

You are expected to treat your instructor and all other participants in the course with courtesy and respect. Disrespectful conduct and harassing statements will not be tolerated and may result in disciplinary actions.

MENTAL HEALTH RESOURCES

Part of being successful in the classroom involves a focus on your whole self, including your mental health. While you are at Stevens, there are many resources to promote and support mental health. The Office of Counseling and Psychological Services (CAPS) offers free and confidential services to all enrolled students who are struggling to cope with personal issues (e.g., difficulty adjusting to college or trouble managing stress) or psychological difficulties (e.g., anxiety and depression) and who can visit the office in person. CAPS is open from 9:00 am – 5:00 pm Mondays, Wednesdays, Thursdays and Fridays and from 9:00 am – 7:00 pm on Tuesdays during the Fall and Spring semesters; appointments are highly encouraged. For those students who cannot visit the Stevens campus for an in-person appointment, you can contact a local mental health care provider for an in-person appointment, or if you are enrolled in the Stevens Student Health Insurance, you may call Care Connect for 24/7 mental health support at 1-888-857-5462.

For further information please visit the CAPS webpage on Seeking Help Off-Campus.

EMERGENCY INFORMATION

In the event of an urgent or emergent concern about the safety of yourself or someone else in the Stevens community, please immediately call the Stevens Campus Police at 201-216-5105 or on their emergency line at 201-216-3911. These phone lines are staffed 24/7, year round. For students who do not reside near the campus and require emergency support, please contact your local emergency response providers at 911 or via your local police precinct. Other 24/7 national resources for students dealing with mental health crises include the National Suicide Prevention Lifeline (1-800-273-8255) and the Crisis Text Line (text "Home" to 741-741). If you are concerned about the wellbeing of another Stevens student, and

the matter is *not* urgent or time sensitive, please email the CARE Team at care@stevens.edu. A member of the CARE Team will respond to your concern as soon as possible.