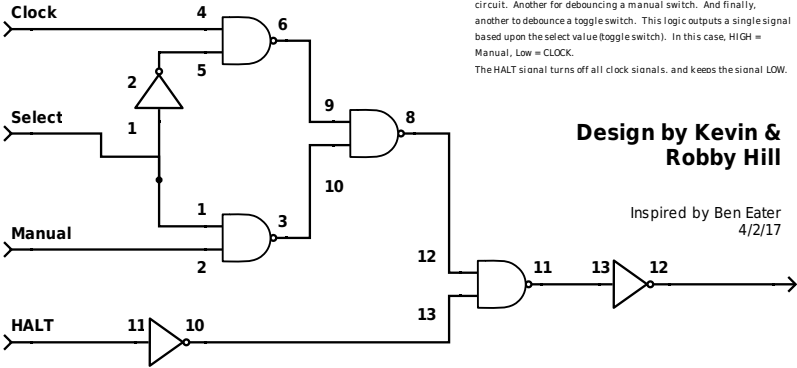# Clock Logic Schematic

Much thanks to Ben Eater who I followed in creating this project. The NAND gates are from a 74LS00 and the inverters are from a 74LS04.

The timer circuit additionally uses 3 555 chips. One for a timing circuit. Another for debouncing a manual switch. And finally, another to debounce a toggle switch. This logic outputs a single signal based upon the select value (toggle switch). In this case, HIGH = Manual, Low = CLOCK.
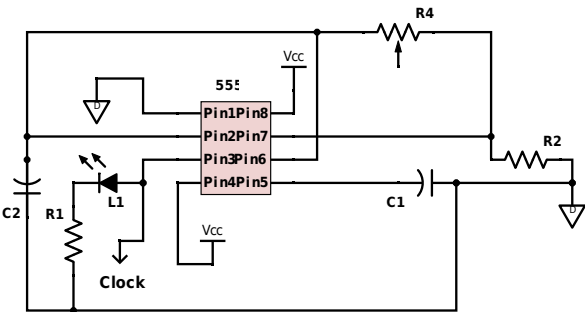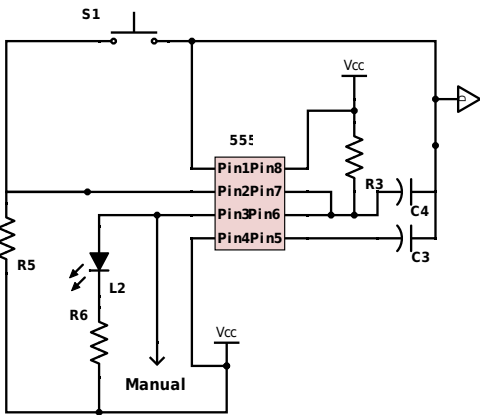The HALT signal turns off all clock signals. and keeps the signal LOW.

Design by Kevin & Robby Hill

Inspired by Ben Eater
4/2/17

Clock
Select
Manual
HALT

ClockTimer Circuit

555
Pin1 Pin8
Pin2 Pin7
Pin3 Pin6
Pin4 Pin5

Vcc
R4
R2
C1
C2
R1
L1
Clock

ClockTimer Circuit

S1
555
Pin1 Pin8
Pin2 Pin7
Pin3 Pin6
Pin4 Pin5

Vcc
R3
C4
C3
R5
L2
R6
Manual
Vcc

Select Switch

S2
Vcc
Pin1 Pin8
Pin2 Pin7
Pin3 Pin6
Pin4 Pin5
C5
R8 R7
L3
Select
Vcc
R9