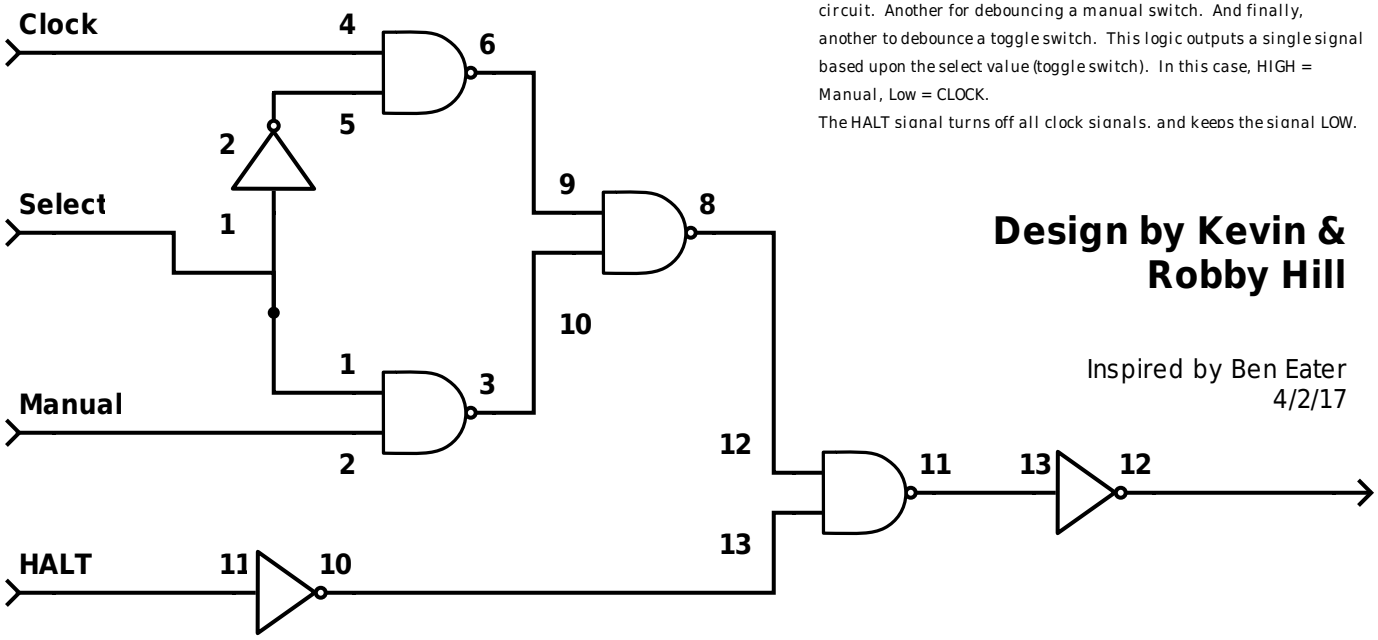
# Clock Logic Schematic

Much thanks to Ben Eater who I followed in creating this project. The NAND gates are from a 74LS00 and the inverters are from a 74LS04.

The timer circuit additionally uses 3 555 chips. One for a timing circuit. Another for debouncing a manual switch. And finally, another to debounce a toggle switch. This logic outputs a single signal based upon the select value (toggle switch). In this case, HIGH = Manual, Low = CLOCK.
The HALT signal turns off all clock signals, and keeps the signal LOW.

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Inspired by Ben Eater
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