LDA	0001	Load Memory > A	0001 xxxx
ADD	0010	Add	0010 xxxx
SUB	0011	Subtract	0011 xxxx
STA	0100	Store A > Memory	0100 xxxx
OUT	0101	Output A > Out	0101
JMP	0110	Jump to Address	0110 xxxx
NOP	0000	No Operation	0000
HLT	1111	Halt execution	1111

CE - Program Counter Enable
CO - Program Counter OUT
JMP - Jump
MI - Memory Address Register IN
RI - RAM IN
RO - RAM OUT
II - Instruction Register IN
IO - Instruction Register OUT

AI - A Register IN
AO- A Register OUT
SU - Subtract
EO - SUM Register(ALU) OUT
BI - B Register IN
OI - Output Register IN
HLT - Halt

Based on https://github.com/space1649/8-bit-SAP-Breadboard-Computer-by-Space-Man
(but heavily modified)

		EEPROM1								EEPROM2								7bits		EEPROM HEX ADDR	DATA ROM1 HEX	DATA ROM2 HEX
																		4 bits	3 bits			
		O7	**O6**	**O5**	**O4**	**O3**	**O2**	**O1**	**O0**	**O7**	**O6**	**O5**	**O4**	**O3**	**O2**	**O1**	**O0**	**Instruction**	Microtick			
		JMP	HLT	MI	RI	RO	II	IO	AI	AO	EO	SU	BI	OI	CE	CO		Opcode	Step			
NOP T0	PC OUT to Memory Address IN			1												1		0000	000	0x0	0x20	0x2
NOP T1	RAM OUT to Inst Reg IN + Increment PC					1	1								1			0000	001	0x1	0xC	0x4
NOP T2																		0000	010	0x2	0x0	0x0
NOP T3																		0000	011	0x3	0x0	0x0
NOP T4																		0000	100	0x4	0x0	0x0
LDA T0	PC OUT to Memory Address IN			1												1		0001	000	0x10	0x20	0x2
LDA T1	RAM OUT to Inst Reg IN + Increment PC					1	1								1			0001	001	0x11	0xC	0x4
LDA T2	Ins Reg OUT to Memory Address IN			1				1										0001	010	0x12	0x22	0x0
LDA T3	RAM OUT, Reg A IN					1			1									0001	011	0x13	0x9	0x0
LDA T4																		0001	100	0x14	0x0	0x0
ADD T0	PC OUT to Memory Address IN			1												1		0010	000	0x20	0x20	0x2
ADD T1	RAM OUT to Inst Reg IN + Increment PC					1	1								1			0010	001	0x21	0xC	0x4
ADD T2	Ins Reg OUT,Memory Address IN			1				1										0010	010	0x22	0x22	0x0
ADD T3	RAM OUT, Reg B IN					1							1					0010	011	0x23	0x8	0x10
ADD T4	ALU OUT, Reg A IN								1		1							0010	100	0x24	0x1	0x40
SUB T0	PC OUT to Memory Address IN			1												1		0000	000	0x30	0x20	0x2
SUB T1	RAM OUT to Inst Reg IN + Increment PC					1	1								1			0000	001	0x31	0xC	0x4
SUB T2	Ins Reg OUT,Memory Address IN			1				1										0011	010	0x32	0x22	0x0
SUB T3	RAM OUT, Reg B IN					1							1					0011	011	0x33	0x8	0x10
SUB T4	ALU OUT, Reg A IN,SUBTRACT								1		1	1						0011	100	0x34	0x1	0x60
STA T0	PC OUT to Memory Address IN			1												1		0100	000	0x40	0x20	0x2
STA T1	RAM OUT to Inst Reg IN + Increment PC					1	1								1			0100	001	0x41	0xC	0x4
STA T2	Ins Reg OUT,Memory Address IN			1				1										0100	010	0x42	0x22	0x0
STA T3	A Reg OUT, RAM IN				1					1								0100	011	0x43	0x10	0x80
STA T4																		0100	100	0x44	0x0	0x0
OUT T0	PC OUT to Memory Address IN			1												1		0101	000	0x50	0x20	0x2
OUT T1	RAM OUT to Inst Reg IN + Increment PC					1	1								1			0101	001	0x51	0xC	0x4
OUT T2	Reg A OUT, Reg Out IN									1				1				0101	010	0x52	0x0	0x88
OUT T3																		0101	011	0x53	0x0	0x0
OUT T4																		0101	100	0x54	0x0	0x0
JMP T0	PC OUT to Memory Address IN			1												1		0110	000	0x60	0x20	0x2
JMP T1	RAM OUT to Inst Reg IN + Increment PC					1	1								1			0110	001	0x61	0xC	0x4
JMP T2	Ins Reg OUT, J	1						1										0110	010	0x62	0x82	0x0
JMP T3																		0110	011	0x63	0x0	0x0
JMP T4																		0110	100	0x64	0x0	0x0
HLT T0	PC OUT to Memory Address IN			1												1		1111	000	0xF0	0x20	0x2
HLT T1	RAM OUT to Inst Reg IN + Increment PC					1	1								1			1111	001	0xF1	0xC	0x4
HLT T2	Halt OUT		1															1111	010	0xF2	0x40	0x0
HLT T3																		1111	011	0xF3	0x0	0x0
HLT T4																		1111	100	0xF4	0x0	0x0