LLM4ChipDesign

Comprehensive Research Framework for LLM-based Hardware Design

Three Main Research Areas: LLM4Verilog Generation • LLM4Security • LLM4C2HLS

LLM4Verilog Generation

- AutoChip: Functional Verilog from prompts
- VeriThoughts: Reasoning-based generation
- ROME: Hierarchical prompting
- Veritas: CNF-based synthesis
- PrefixLLM: Prefix circuit design

LLM4Security

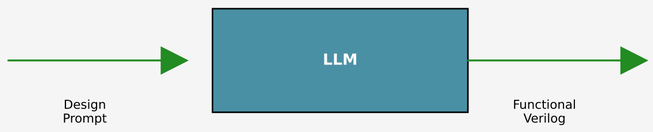
- LLMPirate: IP piracy detection
- Security Assertions: LLM-generated SVA
- Hybrid-NL2SVA: Enhanced NL2SVA
- OpenTitan RAG: SVA for IP blocks

LLM4C2HLS

- C2HLSC: Software-to-hardware gap
- Automated C code refactoring
- HLS-compatible transformation
- Iterative LLM feedback

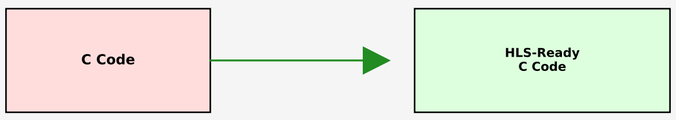
Featured Submodules

AutoChip



Generates functional Verilog modules with iterative error feedback

C2HLS



Bridges software-to-hardware design gap with LLM guidance

Security Assertions

Generates SystemVerilog assertions for security verification

Key Framework Features

- End-to-end automated pipelines for hardware design
- Iterative feedback mechanisms with EDA tools
- Security-focused verification and assertion generation
- Multi-modal LLM integration (text, code, schematics)
- Comprehensive evaluation frameworks and benchmarks
- Hierarchical design methodologies for complex systems

Repository: github.com/FCHXWH823/LLM4Hardware

Papers • Code • Tutorials • Collaborative Research Framework