Generative AI for Chip Design

A Comprehensive Learning Resource Collection

■ Target Audience

This resource collection targets professionals and learners at the intersection of AI and hardware design:

• **Hardware Engineers** leveraging AI for Verilog generation and verification

• **Researchers** exploring LLM applications in Electronic Design Automation

• **Students** studying computer architecture, VLSI design, or AI/ML

• **EDA Developers** integrating LLM capabilities into design workflows

• **Industry Professionals** accelerating chip design with AI tools

■■ Expected Learning Time

Flexible learning paths with varying time commitments:

Component	Time	Description
Quick Overview	2-3 hrs	Browse README, intro videos
Single Tutorial	1-2 hrs	One Colab notebook
Project Deep-dive	8-12 hrs	Study one research area
Full Study	30-40 hrs	All tutorials and materials
Implementation	50+ hrs	Adapt for your projects

■ Material Description

A comprehensive educational hub for applying LLMs to chip design challenges, encompassing research, tutorials, and tools:

• **Verilog Generation:** AutoChip, VeriThoughts, ROME for functional hardware descriptions

• **Verification:** LLM-aided testbench generation and SystemVerilog assertion creation

• **HLS Bridge:** C2HLSC framework transforming C code to HLS-synthesizable formats

• **Specialized Tools:** Prefix circuits, analog netlists, security assertions

• **Hands-on Learning:** 13 Jupyter tutorials with real-world examples

■ Key Features

Practical Implementation: Each project includes working code, detailed tutorials, and integration examples.
Research Foundation: All tools are backed by peer-reviewed publications and conference presentations.
Hands-on Learning: Google Colab notebooks enable immediate experimentation without local setup.
Industry Relevance: Tools address real challenges in modern chip design workflows and EDA processes.