



LLM4ChipDesign

Generative AI for Chip Design: Stackable Modules

Three main topics: LLM4Verilog | LLM4Validation | LLM4Security



Github: <https://github.com/FCHXWH823/LLM4Hardware>



Introduction



This project explores the application of large language models (LLMs) in the field of chip design with three main topics:

- **LLM4Verilog:** Generate functional Verilog modules from design prompts using LLMs.
- **LLM4Validation:** LLM-generated SystemVerilog assertions, testbench files for hardware validation.
- **LLM4Security:** LLM-aided detection of hardware security risks.

The teaching duration for each **topic** is approximately 4 hours.

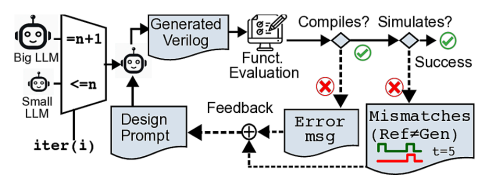


Featured Modules



LLM4Verilog

AutoChip: Generate functional Verilog modules from design prompts using LLMs with iterative error feedback

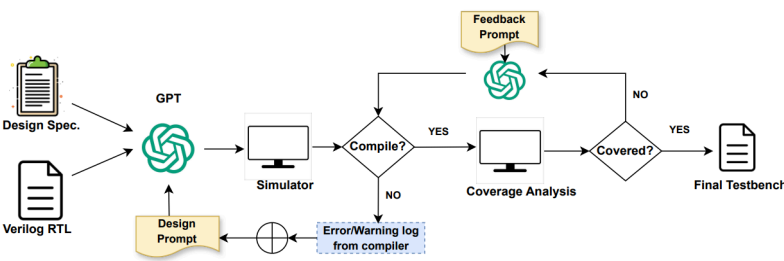


[Paper](#)



LLM4Validation

FSM Testbench Generation: LLM-generated testbench files for hardware validation

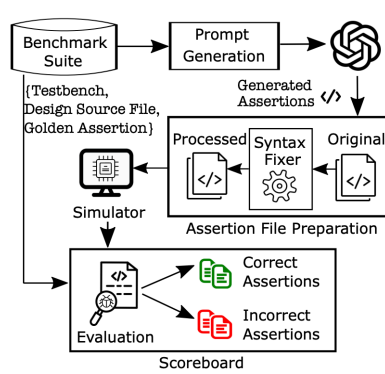


[Paper](#)



LLM4Security

Security Assertions: LLM-generated security assertions for detecting security risks



[Paper](#)



LLM4Verilog

Functional Verilog generation with LLM feedback (AutoChip)

[Paper](#) [Code](#) [Slides](#)

LLM Reasoning-based Verilog code generation (VeriThoughts)

[Paper](#) [Code](#)

Hierarchical LLM prompting for complex chip design (ROME)

[Paper](#) [Code](#) [Slides](#)

Deterministic LLM-based Verilog synthesis from Conjunctive Normal Form (Veritas)

[Paper](#) [Code](#) [Slides](#)

LLM-aided prefix adder circuit design (PrefixLLM)

[Paper](#) [Code](#)



LLM4Validation

LLM-based Natural Language to SystemVerilog Assertion (Hybrid-NL2SVA)

[Paper](#) [Code](#) [Slides](#)

LLM-based testbench generation and bug detection (FSM Testbench Generation)

[Paper](#) [Code](#)

Retrieval-Augmented Generation (RAG)-based SystemVerilog assertion using LLM

[Code](#)

LLM-based hardware assertion generation for security (Security Assertions)

[Paper](#) [Slides](#)



LLM4Security

LLM-based testbench generation and bug detection (FSM Testbench Generation)

[Paper](#) [Code](#)

LLM-based hardware assertion generation for security (Security Assertions)

[Paper](#) [Slides](#)

LLMs for black-box hardware IP piracy (LLMPirate)

[Paper](#) [Slides](#)



LLM4HLS

Bridge software-to-hardware design gap using LLMs to refactor C code for High-Level Synthesis (C2HLS)

[Paper](#) [Code](#) [Slides](#)



LLM4Analog

LLM-generated analog circuit netlists for circuit schematic images (Masala-CHAI)

[Paper](#) [Code](#)



Repository Statistics

12+

Research Projects

9

Git Submodules

10+

Research Papers

5

Main Focus Areas



Mission: Advancing the intersection of Large Language Models and Chip Design



Research Areas: Verilog Generation • Validation • Security • High-Level Synthesis • Analog Circuit Generation



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