Generative AI for Chip Design

A Comprehensive Learning Resource Collection

■ Who This Is For

This collection of training modules is designed for those from relevant backgrounds who want to understand how artificial intelligence is revolutionizing computer chip design. Whether you are a high school student exploring STEM fields, an undergraduate student in EE/CS/CE or any other STEM field, an educator in the relevant fields, a professional chip designer interested in AI applications, these materials will guide you.

■ What You'll Discover

Explore how Large Language Models (LLMs) are being used to automatically design computer chips. You will learn about how to convert software code to hardware designs, generating computer circuits from natural language descriptions, creating tests for chip validation, and much more.

■■ Time Investment Guide

Material Type	Time Commitment	Best For
Quick Overview (This Document)	5 minutes	Getting oriented
Interactive Tutorials (Colab Scripts)	30-90 minutes each	Hands-on learning
Research Papers	20-45 minutes each	Deep understanding
Presentation Slides	15-30 minutes each	Visual learners
Video Presentations	45-60 minutes each	Comprehensive overview
Complete Collection	40-45 hours total	Thorough exploration

■ Featured Research Areas

- LLM4Verilog: Automatic generation of Verilog using LLM
- LLM4Validation: Automatic generation of SystemVerilog assertions & testbench files using LLM
- LLM4Security: Automatic detection of hardware security risks using LLM
- LLM4HLS: Automatic High-level Synthesis for C codes using LLM
- LLM4Analog: Automatic generation of analog circuit netlists from schematics.

■ Getting Started

Begin with the interactive tutorials in the 'colab-scripts' folder - these are designed to run in your web browser without any software installation. Each tutorial includes step-by-step explanations and real examples. The README.md file provides links to all papers, code repositories, and additional resources. Don't worry if some technical terms are unfamiliar at first - the materials are designed to build your understanding progressively.

LLM4ChipDesign Course Syllabus

14-Week Timeline Overview

Course Structure: Each module is taught over 2 weeks following a consistent pattern:

- **Week 1:** Introduce basic concepts and theory, assign homework/projects
- **Week 2:** Hands-on practice solving assignments and implementing tools

Week	Module	Focus	Activities
1	**AutoChip: Automated Verilog Generation**	Theory & Introduction	Introduction to LLM-based Verilog Generation
2		Hands-on Practice	Hands-on AutoChip Implementation
3	**VeriThoughts: Reasoning-based Code Generation**	Theory & Introduction	Formal Verification in Hardware Design
4		Hands-on Practice	Building VeriThoughts Models
5	**ROME: Hierarchical Prompting for Complex Designs**	Theory & Introduction	Hierarchical Design Methodologies
6		Hands-on Practice	Implementing Hierarchical Verilog Generation
7	**Veritas: CNF-guided Verilog Synthesis**	Theory & Introduction	Conjunctive Normal Form in Hardware Design
8		Hands-on Practice	CNF to Verilog Translation Projects
9	**Testbench Generation & Bug Detection**	Theory & Introduction	LLM-aided Testing Methodologies
10		Hands-on Practice	FSM Testbench Generation Workshop
11	**Hybrid-NL2SVA: Natural Language to Assertions**	Theory & Introduction	SystemVerilog Assertions and Security
12		Hands-on Practice	Building NL2SVA Tools
13	**C2HLSC: Software-to-Hardware Design Bridge**	Theory & Introduction	High-Level Synthesis with LLMs
14		Hands-on Practice	C to HLS Translation Projects