Product Brief

AWGN Channel Emulator

Product Name: **AWGN_ELTR**

The **AWGN Channel Emulator** Soft IP Core emulates the AWGN channel used in the analysis of communications systems. With features such as large pseudorandom period, simple interfacing and small FPGA area, the **AWGN Channel** is ideal for statistical testing of communications system components, for target BER as low as $\mathbf{10^{-12}}$.

Technical description

The **AWGN Channel Emulator** has been designed for easy integration with any set of communications system blocks that need statistical testing over noisy channel conditions. The block diagram of the **AWGN Channel Emulator** is shown in Figure 1. The channel input is n bits wide, and easily reconfigurable, enabling the transmission of virtually any kind of signal representation. The variance input is **13 bits wide**, represented as an unsigned integer, whose value is determined by the desired variance scaled by 2^{12}. In this way, variance values in the range $\sigma\in(1,2^{-12}]$ can be represented. A random variable (RV) generator generates RVs belonging to N(0,1) and these are multiplied with σ to produce a RV belonging to N(0,σ). The result of the multiplication is scaled to n bits, for enabling addition with the n bit input symbol value. For each n bit input, an n+1 bits noisy output is produced.

The realization of the RV generator is accomplished by using an extremely efficient Box-Muller implementation. An example of the RV PDF for σ=1 and 600k samples is shown in Figure 2 (results from Virtex-6 XC6VLX240T-1), in comparison with the results produced by MATLAB. Figure 3 also shows the random variable PSD, which corresponds to white noise. This extremely accurate implementation of the noise samples leads to extremely accurate results, as shown in Figure 4, where the theoretical uncoded BER performance of BPSK is compared with the BER resulting from measurements on the channel emulator. The period of the random number generator is 2^{51}-1 enabling efficient measurement of BER values even lower than $\mathbf{10^{-12}}$.

Maximum channel throughput has been measured at **166 MBd** at clock frequency **166 MHz,** achieving **latency** below **5μs** (measurements taken on aVirtex-6 XC6VLX240T-1 FPGA). For BPSK and n=7, this leads to 1.328 Gbps throughput. Flexibility is offered by avoiding to internally store data and employing a simple handshaking protocol to communicate with neighboring blocks. This transparent operation allows for the use of the AWGN channel emulator in a variety of communication system configurations.

The **AWGN Channel Emulator** IP core has been tested on Virtex-6 XC6VLX240T-1 FPGA device and can be readily delivered as a soft-IP core targeted for any Virtex-6 device. Matlab models and RMM synthesizable VHDL code with the corresponding test benches are also available.

Applications

- Communications system testing

Features

- Random number with period of 2^{51}-1
- Extremely accurate implementation of N(0,1)
- Variance range $\sigma\in(1,2^{-12}]$
- Arbitrary representation of input/output symbols
- Transparent operation
- Gbit throughput support

Deliverables

- Soft-IP core
  - Double-precision Matlab models
  - .edf files targeted on Virtex-6 FPGA devices
  - RMM synthesizable VHDL code
  - Full specification documentation
  - Complete test plan and test bench

Support

- Technical support by phone or email is included. First year of maintenance is also included. Additional support and annual maintenance options are available.

Product Brief

Resources Utilization on Virtex-6 XC6VLX240T-1 FPGA device (place and route)

AWGN Channel - ANL-AWGNEMLTR:	
Max. Freq	**180 MHz**
# of Slice LUTs	**8000 out of 150,720 (5%)**
# DSP48E1	**50 uses**

Throughput and Latency

The AWGN Channel supports a throughput rate of 1.328 Gbps on Virtex-6 XC6VLX240T-1 FPGA, when clocked at 166 MHz for BPSK modulation and n=7 bit representation of each transmitted symbol. Latency is below 5μs

Soft IP Core Block Diagram and Channel Characteristics

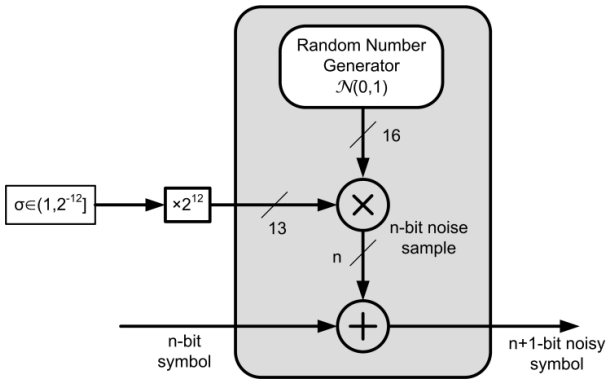

Figure 1 AWGN Channel block diagram.

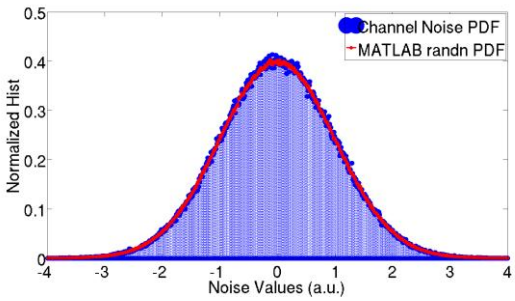

Figure 2 Random variable histogram at the output of the random number generator.

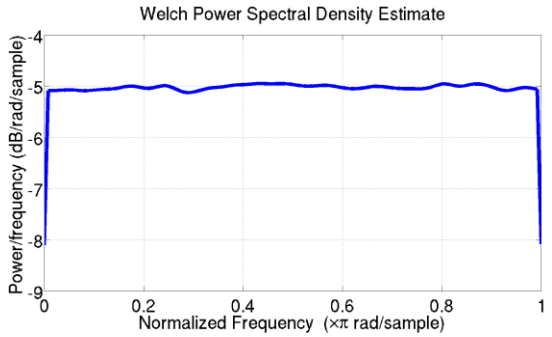

Figure 3 Random variable power spectral density.

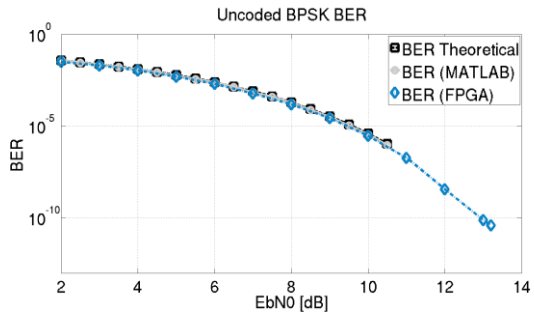

Figure 4 Comparison of theoretical uncoded BPSK BER with BER when the channel emulator is used.

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